

# Fault Arc Suppression Method with Elimination of Line Voltage Drop Influence for Flexible Distribution Networks Connected via Power Electronics

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**Abstract**—Single phase-to-ground (SPG) faults constitute the prevalent type of electrical failure in live distribution networks, posing critical threats including electrocution hazards, electrical fires, and widespread power supply disruptions. Power electronic converter can suppress the fault current and voltage, sustaining this suppression effect throughout the fault arc persistence period until arc extinction. However, not only does it consume additional resources, but the effect is also significantly affected by the line impedance voltage drop. This paper analyzes the causes of line voltage drop and proposes an SPG fault arc suppression method for flexible distribution networks. The line voltage drop caused by the load currents of faulty feeder is eliminated by transferring the load currents via the employed flexible interconnection device during simultaneous fault arc suppression. The line voltage drop caused by the zero-sequence currents output from the device for fault arc suppression during simultaneous load current transfer is also eliminated, by only adopting the device arms connected to non-faulty phase of the faulty feeder to output the zero-sequence currents. Extensive simulation study and experimental validation demonstrate that the fault current and voltage can be suppressed efficiently with a suppression rate of more than 98% in the case of different operating conditions.

**Index Terms**—single phase-to-ground (SPG) fault, active fault arc suppression, power electronic transformer, flexible distribution networks, soft open points, flexible interconnection devices, line impedance voltage drop

This work was supported in part by the National Natural Science Foundation of China under Project 51677030, and in part by the Natural Science Foundation of Fujian Province of China under Award 2023J05106. (Corresponding author: Mou-Fa Guo).

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## I. INTRODUCTION

With the ongoing advancement of smart power grid technologies, the distribution network architectures demonstrate continuously growing complexity and expanding operational scales [1]. The integration of increasing renewable energy into distribution networks via power converters has transformed conventional networks into active distribution networks [2]. This transition has led to a higher incidence for single phase-to-ground (SPG) faults and greater technical challenges concurrently in addressing them [3]. The statistical analyses reveal that SPG faults remain the predominant fault mode in distribution networks, representing over 70% of all recorded electrical faults [4]. Under SPG fault conditions, substantial fault currents originating from phase-to-ground impedance pass through the affected SPG branch, often generating arcing phenomena capable of triggering fire hazards, equipment degradation, and large-scale power supply interruptions [5]. Moreover, hazardous step voltage potentials manifest radially from SPG fault location, posing significant electrocution risks to nearby personnel or bystanders [6]. The distribution networks are particularly susceptible to transient overvoltage phenomena during such events, with the potential to escalate into catastrophic multi-phase short-circuit faults [7]. This operational reality necessitates the development of advanced mitigation techniques for simultaneous fault current and voltage control to effectively eliminate arcing hazards [8].

Available fault arc suppression methodologies leverage the inherent current and voltage regulation capabilities of power converters to attempt to mitigate fault arcing phenomena [9]. The operational paradigm can involve strategic deployment of the power converters at the neutral point locations, mandating the adequate voltage withstand specifications to accommodate potential of neutral points [10]. Such systems predominantly incorporate modular configurations employing either H-bridge or T-type multilevel converters synergistically integrated with voltage amplification transformers [11]. Such configurations interface the power converter with the transformer's secondary winding, thereby relaxing the power converter's voltage stress requirements while maintaining operational efficacy [12]. An alternative advanced implementation employs a cascaded H-bridge converter, demonstrating voltage-handling capabilities through the distributed semiconductor stress and the enhanced harmonic suppression characteristics in output waveforms [13]. These systems adhere to the fundamental neutral point current

injection mechanisms, i.e., precisely controlled counter-phase quantities are superimposed on the neutral path of distribution networks to realize the fault current and voltage neutralization [14], [15]. Noteworthy that such architectures permit flexible connection configurations, i.e., either through direct busbar or power line connections [16], [17]. Simultaneously, such power converters exhibit multipurpose operational modes, delivering coordinated active/reactive power regulation alongside fault arc suppression functionalities, thus enhancing overall power quality during SPG fault suppression conditions [18].

These power converters for fault arc suppression typically are fixed to a node in distribution networks, thereby they can only achieve the fault current and voltage neutralization based on information obtained locally [19]. Because the SPG fault location is random and unknown and will not be completely at the power converter grid-connected node [20]. Therefore, no matter whether the fault current or fault voltage is regulated, the final result is that the faulty phase voltage at the power converter grid-connected node is zero [21]. Accordingly, the voltage across the fault resistance is suppressed, and the fault current is also suppressed [22]. However, due to the distance between the SPG fault node and the power converter grid-connected node, there must be line impedance between the two [23]. Therefore, the line impedance voltage drop will be generated due to the line currents, resulting in the voltage at the fault node not being zero, and there being a residual fault voltage and current, causing the fault arc to fail to suppress or to reignite repeatedly [24]. Therefore, these existing problems are summarized as follows.

1) The line impedance voltage drop caused by the positive sequence currents passing through the faulty feeder makes the residual fault current and voltage exist.

2) The zero-sequence currents provided by power electronic converters for fault arc suppression pass through faulty feeder, which increases the line impedance voltage drop, causing the residual fault current and voltage to further increase.

3) The additional power electronic converter devices fixed to a node in distribution networks, and poor fault current and voltage suppression cause a low cost-effectiveness.

In this paper, a fault arc suppression method is proposed for flexible distribution networks through flexible interconnection device to address these existing problems summarized above. The main contributions of this article can be summarized as follows.

- 1) The dynamically changing line impedance voltage drop between the fault node and flexible connection node in faulty feeder, caused by the positive-sequence currents at the end of the faulty feeder, is eliminated. Thus, the residual SPG fault voltage and current is significantly reduced during fault arc suppression.
- 2) The line impedance voltage drop in the faulty phase of faulty feeder between the SPG fault node and flexible connection node at the end of faulty feeder, caused by the zero-sequence currents supplied from the flexible interconnection device port in faulty feeder for fault arc suppression, is eliminated. Therefore, the residual fault voltage and current is further reduced during fault arc suppression.
- 3) The additional stand-alone power electronic converters

fixed to a node of distribution networks for SPG fault arc suppression can be saved, and the line impedance voltage drop caused by the positive- and zero-sequence currents can be eliminated simultaneously by flexible interconnection device in flexible distribution networks. Thus, the cost-effectiveness of fault arc suppression is improved.

The remainder of this article is organized as follows: The proposed SPG fault arc suppression for flexible distribution networks is presented in Section II. The proposed method for eliminating the influence of line impedance voltage drop is represented in Section III. Simulation study and experimental validation are presented in Sections IV and V, respectively. Conclusions are elaborated in Section VI.

## II. PROPOSED SPG FAULT ARC SUPPRESSION FOR FLEXIBLE DISTRIBUTION NETWORKS

In this section, a topology of flexible distribution networks with flexible interconnection device is presented, and the SPG fault arc suppression principle and method are derived.

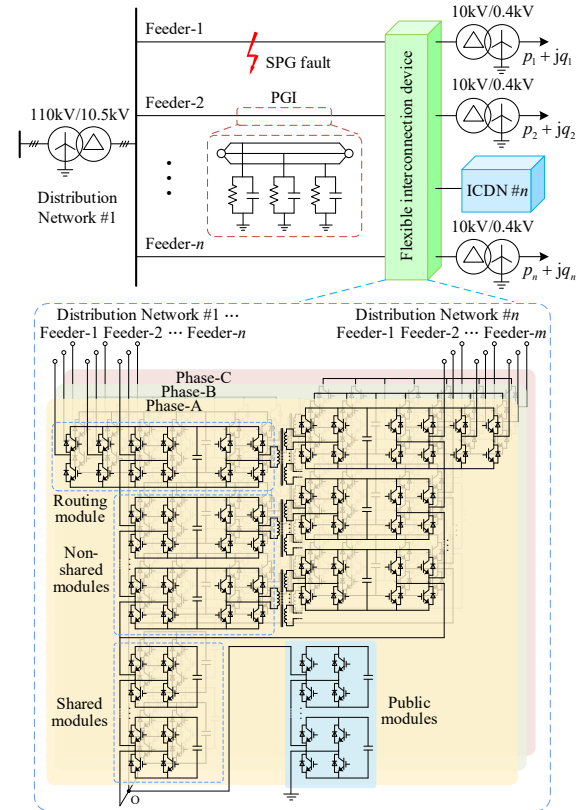


Fig. 1. Schematic diagram of flexible distribution network.

### A. Distribution Networks with Flexible Interconnection Device

The schematic diagram of flexible distribution networks is shown in Fig. 1. It has  $n$  feeders and a SPG fault on feeder-1. The ends of all feeders are connected to each other by flexible interconnection device and also connected to other distribution networks (ICDN). The phase-to-ground impedance (PGI) is between each feeder and the ground, including the phase-to-ground resistances and capacitances. The topology of flexible interconnection device in [25] is employed to suppress SPG fault arc. It consists of public, routing, non-shared, and shared

modules. Because the phase differences of the same phase at different feeder ends of the same distribution network are not large, they can be compensated by the routing module [26]. Moreover, since the phases of different distribution networks are typically not completely reversed, the remaining modules are divided into shared modules and non-shared modules. The non-shared modules can be utilized to compensate the phase difference of different distribution networks, thus the dc-links for interconnection have isolations [27]. The shared modules are applied to share the remaining components with the same phase. The public point O is connected to the ground through the public modules. It is utilized to regulate the zero-sequence components to suppress the SPG fault current and voltage in interconnected distribution networks.

### B. Principle of SPG Fault Arc Suppression

When an SPG fault occurs on phase-A of the feeder-1, the topology of distribution network with flexible interconnection device is shown in Fig. 3. Where  $u_{SA}$ ,  $u_{SB}$ , and  $u_{SC}$  are three phase-to-ground voltages at the busbar node.  $i_{dA}$ ,  $i_{dB}$ , and  $i_{dC}$  are the currents passing through the line impedance of feeder-1.  $u_{eA}$ ,  $u_{eB}$ ,  $u_{eC}$  are three phase-to ground voltages at the end of feeder-1.  $u_f$  is the SPG fault node voltage.  $i_{LA}$ ,  $i_{LB}$ , and  $i_{LC}$  are the positive sequence currents of feeder-1.  $i_{iA}$ ,  $i_{iB}$ , and  $i_{iC}$  are the currents output to the end of feeder-1 by the arms with the routing, non-shared, and shared modules of the flexible interconnection device port side connected to the three phase at the end of feeder-1.

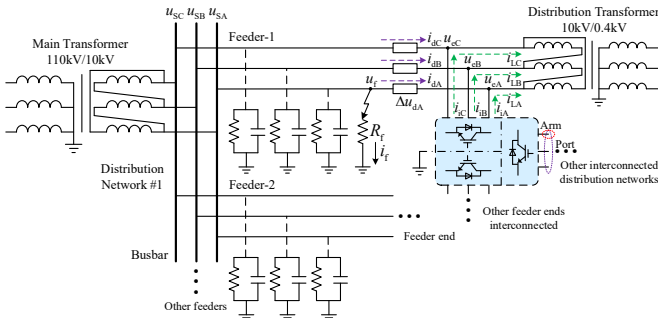


Fig. 2. Topology of distribution network with flexible interconnection device.

The equivalent circuit of distribution network can be shown in Fig. 3.  $u_{S0}$  is the zero-sequence voltage at the busbar, and  $e_{SA}$ ,  $e_{SB}$ , and  $e_{SC}$  are the equivalent three-phase power supply voltages at the busbar.  $Z_{LA}$ ,  $Z_{LB}$ , and  $Z_{LC}$  are the equivalent load impedance of feeder-1.  $u_{iA}$ ,  $u_{iB}$ , and  $u_{iC}$  are the voltages output by the three-phase arms consisting of the routing, non-shared, and shared modules of flexible interconnection device port side connected to the end of feeder-1.  $i_p$  and  $u_p$  are the current and voltage output by the public arm consisting of public modules.  $R_A$ ,  $R_B$ , and  $R_C$  are the total phase-to-ground resistances, and  $C_A$ ,  $C_B$ , and  $C_C$  are the total phase-to-ground capacitances, which can be measured individually by [28].  $i_A$ ,  $i_B$ , and  $i_C$  are the currents passing through the total phase-to-ground impedance.  $\Delta u_{dA}$ ,  $\Delta u_{dB}$ , and  $\Delta u_{dC}$  are the line impedance voltage drop between the SPG fault node and the flexible connection node at the end of feeder-1.

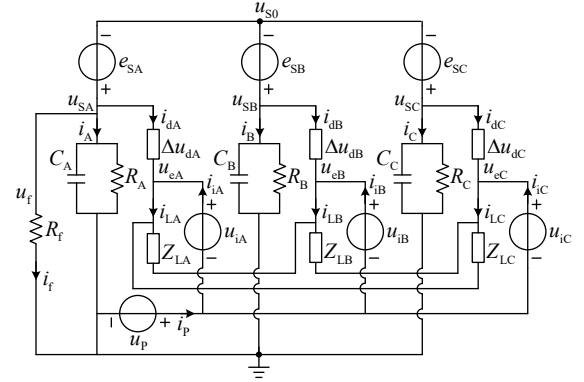


Fig. 3. Equivalent circuit of flexible distribution network.

According to Kirchhoff's current law, the currents passing through the ground node can be expressed as

$$i_A + i_B + i_C + i_f = i_p \quad (1)$$

Therefore, the SPG fault current can be expressed as

$$\begin{aligned} i_f &= \frac{u_f}{R_f} = \frac{u_{SA}}{R_f} = \frac{e_{SA} + u_{S0}}{R_f} \\ &= i_p - i_A - i_B - i_C = i_p - u_{SA} \left( \frac{1}{R_A} + j\omega C_A \right) \\ &\quad - u_{SB} \left( \frac{1}{R_B} + j\omega C_B \right) - u_{SC} \left( \frac{1}{R_C} + j\omega C_C \right) \end{aligned} \quad (2)$$

According to (2), the current  $i_p$  should be regulated as

$$\begin{aligned} i_p &= i_A + i_B + i_C \\ &= u_{SA} \left( \frac{1}{R_A} + j\omega C_A \right) + u_{SB} \left( \frac{1}{R_B} + j\omega C_B \right) + u_{SC} \left( \frac{1}{R_C} + j\omega C_C \right) \end{aligned} \quad (3)$$

In this way, the SPG fault current  $i_f$  will be zero, and the fault voltage  $u_f$  will be zero as well, so that the SPG fault arc can be suppressed without reignition. At this time,  $u_{S0} = -e_{SA}$ . However,  $u_{SA}$ ,  $u_{SB}$ , and  $u_{SC}$  at the busbar cannot be sampled for the flexible interconnection device ports connected at the end of feeders. Accordingly, (3) is invalid for calculating the reference current of the flexible interconnection device.

### C. SPG Fault Arc Suppression Method for Flexible Interconnection Distribution Networks

Temporarily, assuming that the line impedance voltage drop is not considered, i.e.,  $\Delta u_d = 0$ , therefore,

$$\begin{cases} u_{SA} = u_{eA} \\ u_{SB} = u_{eB} \\ u_{SC} = u_{eC} \end{cases} \quad (4)$$

In this case, according to (3), the reference current  $i_{pref}$  can be calculated as

$$i_{pref} = u_{eA} \left( \frac{1}{R_A} + j\omega C_A \right) + u_{eB} \left( \frac{1}{R_B} + j\omega C_B \right) + u_{eC} \left( \frac{1}{R_C} + j\omega C_C \right) \quad (5)$$

where  $u_{eA}$ ,  $u_{eB}$ ,  $u_{eC}$  at the end of feeder-1 can be sampled for the flexible interconnection device port at the end of feeder-1. Based on Kirchhoff's current law, the zero-sequence reference currents  $i_{iA0ref}$ ,  $i_{iB0ref}$ , and  $i_{iC0ref}$  should meet the following

$$\begin{aligned} i_{pref} &= i_{iA0ref} + i_{iB0ref} + i_{iC0ref} \\ &= u_{eA} \left( \frac{1}{R_A} + j\omega C_A \right) + u_{eB} \left( \frac{1}{R_B} + j\omega C_B \right) + u_{eC} \left( \frac{1}{R_C} + j\omega C_C \right) \end{aligned} \quad (6)$$

Furthermore, the total current passing through the phase-to-ground impedance to the ground node is also represented as

$$i_A + i_B + i_C = u_{s0} \left( \frac{1}{R_0} + j\omega C_0 \right) = u_{e0} \left( \frac{1}{R_0} + j\omega C_0 \right) \quad (7)$$

where  $u_{e0}$  is the zero-sequence voltage at the end of feeder-1, which can be expressed as  $u_{e0} = (u_{eA} + u_{eB} + u_{eC})/3$ .  $R_0$  and  $C_0$  are the total phase-to-ground resistance and capacitance, and they can be measured as a whole by [29].

Accordingly, (3) can be represented as

$$i_p = i_A + i_B + i_C = u_{e0} \left( \frac{1}{R_0} + j\omega C_0 \right) \quad (8)$$

In this way, the faulty phase voltage at the end of feeder-1 will be zero, i.e.,  $u_{eA} = 0$ . Since  $u_f = u_{eA} = 0$ , the fault current  $i_f$  and the fault voltage  $u_f$  will be zero as well. At this time,  $u_{e0ref} = -e_{eA}$ , the reference current  $i_{pref}$  can also be presented as

$$i_{pref} = -e_{eA} \left( \frac{1}{R_0} + j\omega C_0 \right) \quad (9)$$

where  $e_{eA}$  is the equivalent power supply voltage of phase-A at the end of feeder-1.  $e_{eB}$  and  $e_{eC}$  are the equivalent power supply voltage of phase-B and phase-C at the end of feeder-1.

### III. PROPOSED METHOD FOR ELIMINATING INFLUENCE OF LINE IMPEDANCE VOLTAGE DROP

In this section, the above SPG fault arc suppression for the flexible distribution networks will be analyzed and evaluated, and a solution will be proposed to eliminate the influence of line impedance voltage drop to improve fault arc suppression.

#### A. Analysis and Evaluation of SPG Fault Arc Suppression Performance for Flexible Distribution Networks

It can be witnessed that the flexible interconnection device port connected at the end of feeder-1 can suppress the faulty phase voltage at the end of feeder-1 by regulating its output zero-sequence current, thereby indirectly suppressing the fault voltage and fault current at the SPG fault node when the line impedance voltage drop between the fault node and flexible connection node at the end of feeder-1 is not considered.

However, the line impedance voltage drop between the fault node and the flexible connection node in phase-A of feeder-1 has non-negligible impacts on fault arc suppression in actual situations. There are two main factors that can be summarized as follows:

- 1) The positive sequence currents of flexible distribution network pass through the line impedance of feeder-1, and it changes in real-time, resulting in the dynamically changing line impedance voltage drop.
- 2) The zero-sequence currents supplied from the flexible interconnection device port at the end of feeder-1 for fault arc suppression pass through the line impedance, which will cause the line impedance voltage drop to further change.

According to Fig. 3 and Kirchhoff's current law, the line impedance voltage drop can be represented as

$$\begin{cases} \Delta u_{dA} = i_{dA} \cdot Z_{dA} = (i_{LA} - i_{IA}) \cdot Z_{dA} \\ \Delta u_{dB} = i_{dB} \cdot Z_{dB} = (i_{LB} - i_{IB}) \cdot Z_{dB} \\ \Delta u_{dC} = i_{dC} \cdot Z_{dC} = (i_{LC} - i_{IC}) \cdot Z_{dC} \end{cases} \quad (10)$$

where  $Z_{dA}$ ,  $Z_{dB}$ , and  $Z_{dC}$  is the line impedance between the fault node and the flexible connection node of feeder-1.

For (10), since  $Z_{dA}$  is an unknown parameter,  $\Delta u_{dA}$  cannot be quantified to be compensated. Accordingly, only the faulty phase voltage at the end of feeder-1 is suppressed to zero by the flexible interconnection device port at the end of feeder-1, the fault voltage at the SPG fault node will be  $\Delta u_{dA}$  but not zero. Thereby, the fault arc will not be able to be suppressed or will repeatedly reignite.

#### B. Proposed Method for Eliminating Line Impedance Voltage Drop Influence

According to (10),  $Z_{dk}$  and  $i_{Lk}$  cannot be regulated, so only the currents  $i_{Lk}$  output by the flexible interconnection device port at the end of feeder-1 can be regulated to make  $\Delta u_{dk}$  zero, where  $k = A, B, \text{ and } C$ .

*Addressing the factor 1*): the line impedance voltage drop between the SPG fault node and flexible connection node at the end of feeder-1 caused by the positive sequence currents of feeder-1.

The positive sequence currents for loads can be provided by the flexible interconnection device port at the end of feeder-1. Consequently, the three-phase reference currents output from the flexible interconnection device port connected to the end of feeder-1 are

$$\begin{cases} i_{IAref} = i_{LA} \\ i_{IBref} = i_{LB} \\ i_{ICref} = i_{LC} \end{cases} \quad (11)$$

In this way, the positive sequence currents will be supplied at the end of feeder-1 via the flexible interconnection device that interconnects the feeder ends, i.e., the positive sequence currents can be transferred from feeder-1 to non-feeder-1 by the flexible interconnection device. Thus, no positive sequence currents pass through the line impedance  $Z_{dA}$ ,  $Z_{dB}$ , and  $Z_{dC}$  between the SPG fault node and the flexible connection node at the end of feeder-1.

*Addressing the factor 2*): the line impedance voltage drop between the SPG fault node and the flexible connection node at the end of feeder-1 caused by the zero-sequence currents output by the flexible interconnection device port at the end of feeder-1 for fault arc suppression.

The zero-sequence currents can be provided to the flexible distribution networks via the flexible interconnection device arms connected to the non-faulty phase at the end of feeder-1. From section II-B,  $u_{eA} = 0$ ,  $u_{eB} = e_{eB} - e_{eA}$ , and  $u_{eC} = e_{eC} - e_{eA}$  during the fault arc suppression, thus, (6) can be represented as

$$\begin{aligned} i_{pref} &= i_{IA0ref} + i_{IB0ref} + i_{IC0ref} \\ &= u_{eA} \left( \frac{1}{R_A} + j\omega C_A \right) + u_{eB} \left( \frac{1}{R_B} + j\omega C_B \right) + u_{eC} \left( \frac{1}{R_C} + j\omega C_C \right) \\ &= 0 + (e_{eB} - e_{eA}) \left( \frac{1}{R_B} + j\omega C_B \right) + (e_{eC} - e_{eA}) \left( \frac{1}{R_C} + j\omega C_C \right) \end{aligned} \quad (12)$$

Consequently, the zero-sequence reference currents  $i_{IA0ref}$ ,  $i_{IB0ref}$ , and  $i_{IC0ref}$  output by the flexible interconnection device port connected to the end of feeder-1 can be

$$\begin{cases} i_{iA0ref} = 0 \\ i_{iB0ref} = (e_{eB} - e_{eA}) \left( \frac{1}{R_B} + j\omega C_B \right) \\ i_{iC0ref} = (e_{eC} - e_{eA}) \left( \frac{1}{R_C} + j\omega C_C \right) \end{cases} \quad (13)$$

From (13), it can be seen that the zero-sequence currents output by the arms connected to the non-faulty phase-B and phase-C at the end of feeder-1 will only pass through the non-faulty phase-B and phase-C of feeders, respectively. The zero-sequence current output by the arm connected to the phase-A is zero. Therefore, no zero-sequence current flows through the line impedance  $Z_{dA}$  between the SPG fault node and flexible connection node in phase-A of feeder-1.

Therefore, the total reference currents output by the flexible interconnection device port connected to the end of feeder-1 can be presented as

$$\begin{cases} i_{iAref} = i_{iA1ref} + i_{iA0ref} = i_{LA} \\ i_{iBref} = i_{iB1ref} + i_{iB0ref} = i_{LB} + (e_{eB} - e_{eA}) \left( \frac{1}{R_B} + j\omega C_B \right) \\ i_{iCref} = i_{iC1ref} + i_{iC0ref} = i_{LC} + (e_{eC} - e_{eA}) \left( \frac{1}{R_C} + j\omega C_C \right) \end{cases} \quad (14)$$

In this case, substituting (14) into (10), it can be represented as

$$\begin{cases} \Delta u_{dA} = (i_{LA} - i_{iAref}) \cdot Z_{dA} = 0 \\ \Delta u_{dB} = (i_{LB} - i_{iBref}) \cdot Z_{dB} = (e_{eB} - e_{eA}) \left( \frac{1}{R_B} + j\omega C_B \right) \cdot Z_{dB} \\ \Delta u_{dC} = (i_{LC} - i_{iCref}) \cdot Z_{dC} = (e_{eC} - e_{eA}) \left( \frac{1}{R_C} + j\omega C_C \right) \cdot Z_{dC} \end{cases} \quad (15)$$

Therefore,  $\Delta u_{dA} = 0$ , i.e., when the flexible interconnection device port connected at the end of feeder-1 can suppress the faulty phase voltage at the end of feeder-1 to zero, the fault voltage at the SPG fault node can be also suppressed to zero. Simultaneously, the fault current will also be zero. Thus, the influence of line impedance voltage drop is eliminated so that the fault arc will be suppressed reliably without reignition. The schematic diagram of the distribution network operation with flexible interconnection device according to the proposed method is shown in Fig. 4.

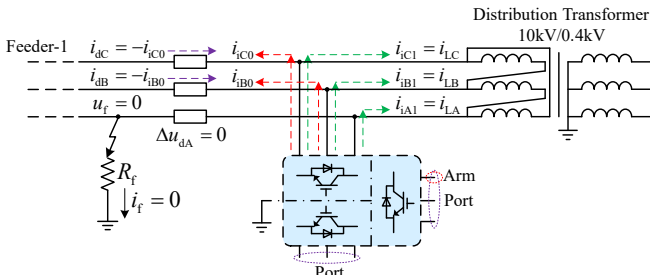


Fig. 4. Schematic diagram of operation based on proposed method.

Obviously, the proposal inherently can possess adaptive arc suppression capability due to the current reference calculation mechanism, where this adaptive process allows the device to automatically adjust its current output according to variations in fault resistances, fault distances, and line impedance voltage drops. Thus, the suppression performance remains consistent under different operating conditions.

For the flexible interconnection device's ports, each port is with three-phase arms. Only one port connected to the faulty feeder operates in the flexible arc suppression mode that can eliminate the influence of the line impedance voltage drop, the other ports operate in the power balancing mode to maintain voltages stability on the DC side shared by all ports of device. For the public modules of the flexible interconnection device, it provides all the compensation current required for fault arc suppression, but it primarily provide reactive power, thereby the required active power is small [13].

### C. Implementation Process Based on Proposed Method

The implementation process based on the proposed method is shown in Fig. 5. The three phase-to-ground voltages and the zero-sequence voltage are monitored to detect if a SPG fault occurs [30]. After a SPG fault is identified, the fault feeder and faulty phase are further identified [31]. Then, the zero-sequence reference currents output by flexible interconnection device arms connected to non-faulty phase of faulty feeder are calculated by (13). Moreover, the positive sequence currents upstream of the flexible interconnection device and the faulty feeder connection node can be measured to obtain the positive sequence reference currents demand. Furthermore, the total reference currents supplied by flexible interconnection device port connected to faulty feeder are calculated by (14). Hence, the fault arcs at the SPG fault node can be suppressed, and the influence of the line impedance voltage drop can be eliminated simultaneously. During this period, the SPG fault is cyclically determined to see if it disappears [32]. When the SPG fault is judged to have disappeared, the flexible distribution network will resume to operate normally.

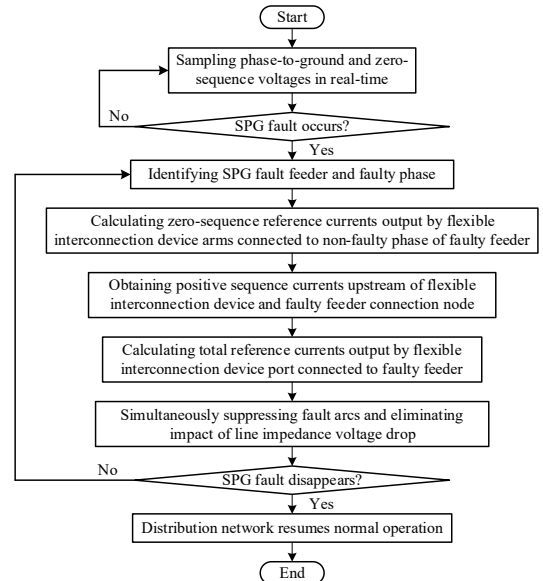


Fig. 5. Implementation flowchart based on proposed method.

The flexible interconnection device is based on cascaded H-

bridge configurations, which can inherently provide redundant switching paths and independent arm power control. Thus, it provides intrinsic fault-tolerant capability, minimizing the risk of commutation failure and control strategy disruption. In the case of SPG faults, the power electronic device operates with circulating current suppression and voltage balancing control to prevent the overvoltage and loss of current transfer between arms, avoiding commutation failure. Even assuming control is interrupted, the power electronic device arms can be switched into a fault ride-through mode. In the mode, the inner current control loops maintain stable operation of the power electronic, while the outer control loops are temporarily suspended until fault disappears and system voltage recovers. In fact, based on (14), the proposed method is based on current control loops.

In addition, following (10), the impacts of line impedance voltage drops depend only on the value of line impedance and load currents. Besides, when the input power of the fault arc is lower than the cooling power and the arc voltage is lower than the recovery voltage, the fault arc can be extinguished. I.e., the fault current and voltage only need to be suppressed below the threshold. Thus, only when the line impedance is too large or the load currents are too large, is it necessary to eliminate the line impedance voltage drops via the flexible interconnection device. I.e., only the device ports installed on longer feeders or feeders with heavy-loads have a relatively higher probability of being used, thence they do not need to be installed on every feeder. Coincidentally, the flexible interconnection devices are usually connected at key nodes where the power flow gathers or at distant end nodes. Therefore, the proposed method fully follows this characteristic and fully utilizes the advantages and utilization of the device. Furthermore, due to the fact that the flexible interconnection device exists in flexible distribution networks, the proposal only utilizes the device to achieve fault arc suppression, which only involves adding public modules at the neutral point of the original device. Thence, the additional costs and space are only related to the added public modules.

#### IV. SIMULATION STUDY

The proposed method is implemented through simulation on MATLAB/Simulink. The flexible distribution network with an SPG fault and flexible interconnection device is built based on Fig. 2. The main parameters are shown in Table I [28].

Table I  
Main Simulation Parameters

Symbol	Parameters	Value
$E$	Amp. of power supply voltage	8.165 [kV]
$f$	Fundamental frequency	50 [Hz]
$C_0$	phase-to-ground capacitance	6.98 [ $\mu$ F]
$R_0$	Phase-to-ground resistance	5684 [ $\Omega$ ]
$L_{d1}$	Positive sequence line reactance	1.21 [ $\Omega$ /km]
$R_{d1}$	Positive sequence line resistance	0.17 [ $\Omega$ /km]
$L_{d0}$	Zero-sequence line reactance	5.48 [ $\Omega$ /km]
$R_{d0}$	Zero-sequence line resistance	0.23 [ $\Omega$ /km]
$T_s$	Sampling cycle	$1e^{-5}$

##### A. Results of SPG Fault Current and Voltage Suppression under Different Fault Distances (Line Impedance)

Fig. 6 (a) and (b) show the SPG fault current and voltage suppression results under fault distances of 5 km and 10 km,

respectively. A SPG fault occurs at  $t = 0.03s$ . The fault current and voltage start to be suppressed at  $t = 0.1s$ . Originally, the fault current and voltage can be suppressed to a great extent, but they are still not small enough. Further, the residual fault current and voltage increase as the fault distance goes up from 5 km to 10 km, which will cause the fault arc to not suppress or to reignite repeatedly. When the proposed method starts to work at  $t = 0.2s$ , the residual current and voltage are further reduced, i.e., the influence of line impedance voltage drop on residual fault current and voltage are significantly eliminated whether the fault distance is 5 km or 10 km, ensuring that the fault arc can be reliably suppressed without reignition.

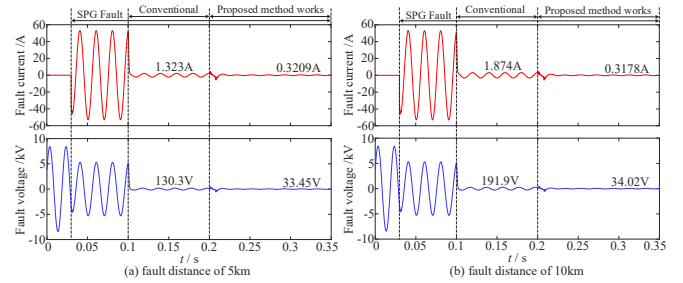


Fig. 6. SPG fault current and voltage suppression results under different fault distances of (a) 5 km and (b) 10km.

Fig. 7 (a) and (b) show the SPG fault current and voltage suppression results under fault distances of 15 km and 20 km, respectively. Likewise, the SPG fault occurs at  $t = 0.03s$ . The fault current and voltage start to be suppressed at  $t = 0.1s$ . The residual fault current and voltage continue to go up as the fault distance increases before the proposed method works, causing the fault arc to not suppress. However, when the proposed method starts to work at  $t = 0.2s$ , they can still be suppressed to a smaller enough level, i.e., the influence of line impedance voltage drop on the residual fault current and voltage can be significantly eliminated regardless of fault distances, ensuring reliable fault arc suppression.

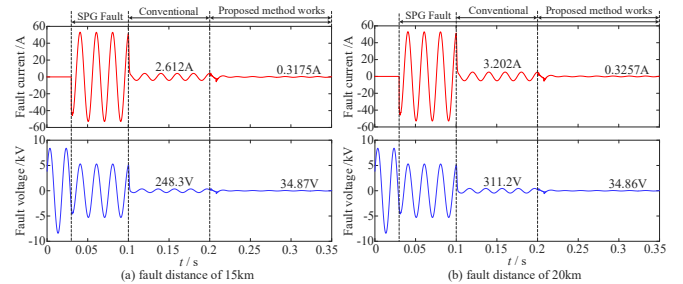
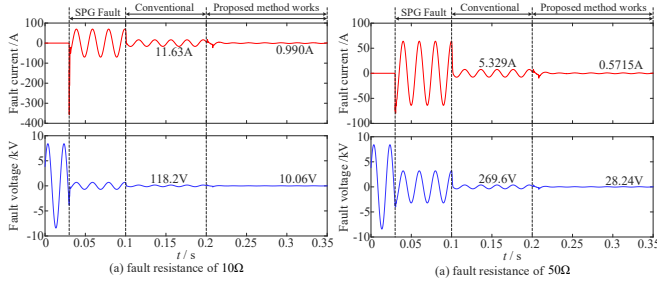


Fig. 7. SPG fault current and voltage suppression results under different fault distances of (a) 15 km and (b) 20 km.

##### B. Results of SPG Fault Current and Voltage Suppression under Different Fault Resistances

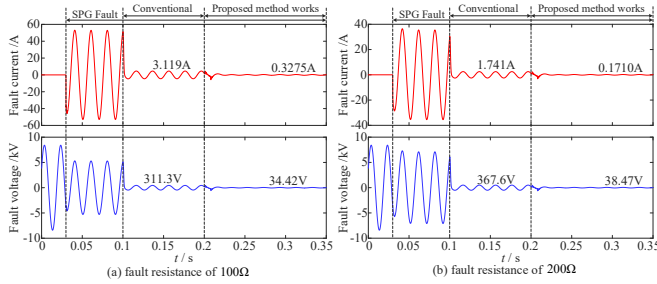
Fig. 8 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of 10  $\Omega$  and 50  $\Omega$ , respectively. The SPG fault occurs at  $t = 0.03s$ , and the fault currents have impulse at the initial moment. The fault current and voltage start to be suppressed at  $t = 0.1s$ . It can be seen that the residual fault current is still significantly large before the proposed method works. When the proposed method starts to work at  $t = 0.2s$ , the residual fault current and voltage can be suppressed to be small enough. Thus, the serious influence of line impedance voltage drop on residual fault current under

low-resistance ground fault can be significantly eliminated.



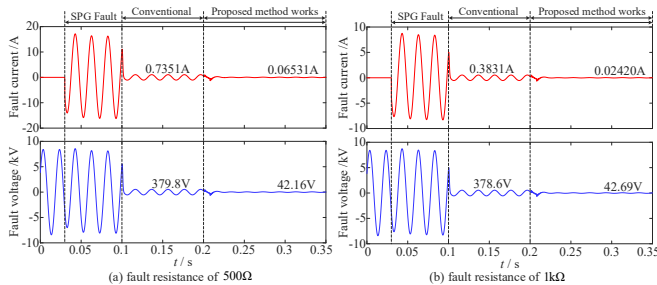
**Fig. 8.** SPG fault current and voltage suppression results under different fault resistances of (a)  $R_f = 10\Omega$  and (b)  $R_f = 50\Omega$ .

Fig. 9 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of  $100\Omega$  and  $200\Omega$ , respectively. Likewise, the SPG fault occurs at  $t = 0.03s$ . The fault current and voltage start to be suppressed at  $t = 0.1s$ . It can be witnessed that the residual fault current and voltage are both large before the proposed method works. However, after the proposed method starts to work at  $t = 0.2s$ , the fault current and voltage have less residual, which proves that the influence of line impedance voltage drop on fault current and voltage under medium-resistance ground fault can be largely eliminated.



**Fig. 9.** SPG fault current and voltage suppression results under different fault resistances of (a)  $R_f = 100\Omega$  and (b)  $R_f = 200\Omega$ .

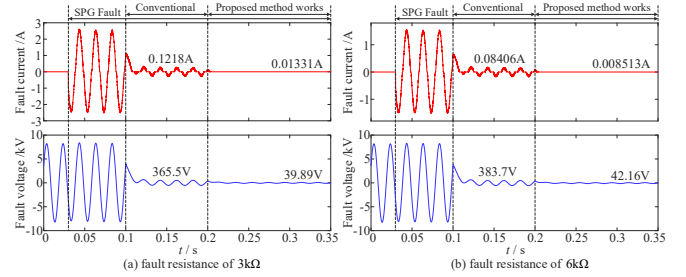
Fig. 10 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of  $500\Omega$  and  $1k\Omega$ , respectively. Originally, the fault current and voltage start to be suppressed at  $t = 0.1s$ , the residual fault current is small but the residual fault voltage is large before the proposed method works. After the proposed method starts to work, the residual fault voltage is significantly suppressed, and the residual fault current is also suppressed to be smaller. Thus, the influence of line impedance voltage drop on fault current and voltage can be eliminated whether the fault resistance is low, medium or high. The fault arc can be reliably suppressed under different fault resistance conditions.



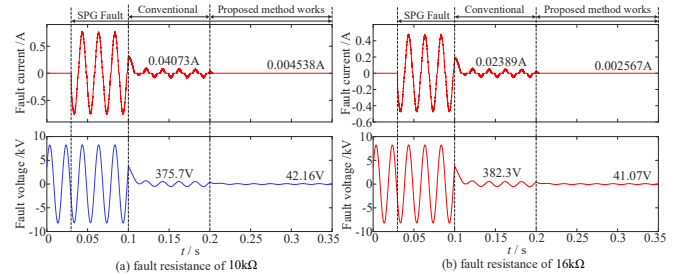
**Fig. 10.** SPG fault current and voltage suppression results under different fault resistances of (a)  $R_f = 500\Omega$  and (b)  $R_f = 1k\Omega$ .

### C. Results of SPG Fault Current and Voltage Suppression under Intermittent Fault Arcs

Fig. 11 and Fig. 12 show the SPG fault current and voltage suppression results under extremely fault resistances of  $3k\Omega$ ,  $6k\Omega$ ,  $10k\Omega$ , and  $16k\Omega$  with intermittent fault arc. When the SPG fault occurs at  $t = 0.03s$ , the fault current exhibits slight intermittent arc characteristics with discontinuity, distortion, and spike pulses, but is more inclined towards stable resistive characteristics. After the fault current and voltage start to be suppressed at  $t = 0.1s$ , they decrease but not small enough, so the fault current exhibits common details of intermittent arcs, such as distinct discontinuity, distortion, and spike pulse. The residual fault voltage is also large before the proposed method works. After the proposed method starts to work, the residual fault voltage is significantly suppressed, and the residual fault current is also suppressed to be smaller. Thus, the influence of line impedance voltage drop on fault current and voltage can be eliminated under extremely high fault resistances, and the intermittent fault arcs can be reliably suppressed.



**Fig. 11.** SPG fault current and voltage suppression results under different fault resistances of (a)  $R_f = 3k\Omega$  and (b)  $R_f = 6k\Omega$  with intermittent fault arcs.



**Fig. 12.** SPG fault current and voltage suppression results under different fault resistances of (a)  $R_f = 10k\Omega$  and (b)  $R_f = 16k\Omega$  with intermittent fault arcs.

## V. EXPERIMENTAL VALIDATION

The results of the proposed method are further validated on the physical experimental platform consistent with Fig. 2, as shown in Fig. 13, and its specifications are shown in Table II.

TABLE II  
Specifications of Experimental Platform

Symbol	Parameters	Value
$E_m$	Amp. of power supply voltage	311 [V]
$f$	Fundamental frequency	50 [Hz]
$C_0$	Phase to ground capacitance	8.8 [ $\mu$ F]
$R_0$	Phase to ground resistance	800 [ $\Omega$ ]
$L_{d1}$	Positive sequence line reactance	0.3 [ $\Omega$ /km]
$R_{d1}$	Positive sequence line resistance	0.1 [ $\Omega$ /km]
$L_{d0}$	Zero-sequence line reactance	1.2 [ $\Omega$ /km]
$R_{d0}$	Zero-sequence line resistance	0.1 [ $\Omega$ /km]

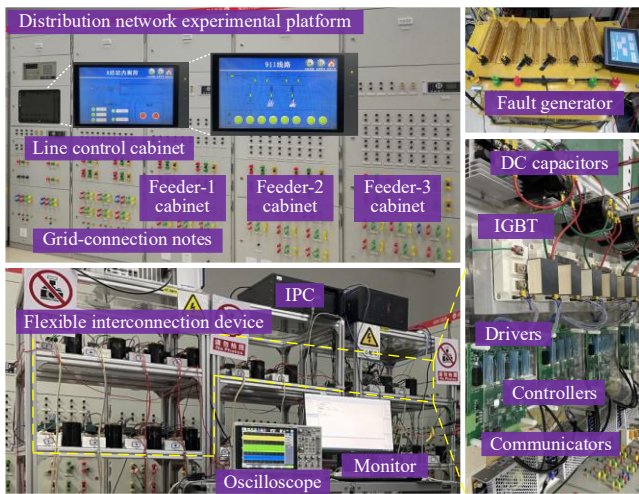


Fig. 13. Physical experimental platform and prototype.

Moreover, the configuration of prototype is shown in Table III, and the overall experimental operation process diagram is exhibited in Fig. 14. Specifically, the electrical signals of the distribution networks and prototype are acquired in real time and fed into the industrial PC. The fault generator is set to be activated at random times. When the industrial PC detects the SPG fault based on the electrical signals, it controls the switch to close, connecting the prototype to the distribution networks. Meanwhile, the industrial PC calculates the reference currents based on the electrical signals and controls the output currents of the prototype. Then, the signals obtained from controller are sent to the units of each arm for modulation by MPU. Finally, the MPU generates drive signals to control the IGBT turn-on or turn-off of the arms for SPG fault arc suppression. During this period, the oscilloscopes record waveforms in real time.

TABLE III  
CONFIGURATION OF PROTOTYPE

Parameters	Value
Sample frequency	6 [kHz]
Voltage acquisition range	0-±480 [V]
Current acquisition range	0-±48 [A]
Communication frequency	2 [MHz]
DC-link voltage of each unit	60 [V]
DC-link capacitor of each unit	600 [μF]
Filter inductance of each arm	100 [mH]
Rated insulation voltage of contactor	690 [V]
Number of units per arm	6

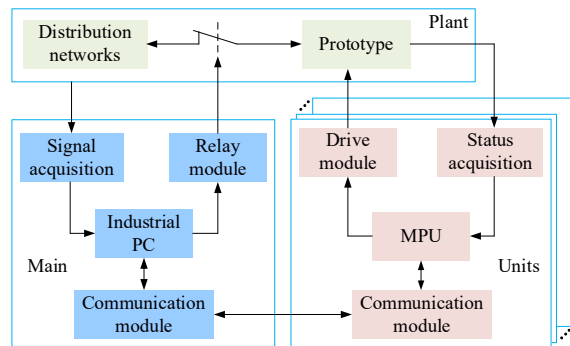


Fig. 14. Overall experimental operation process diagram.

### A. Experimental Results under Difference Fault Distances (Line Impedance)

Fig. 15 (a) and (b) show the SPG fault current and voltage suppression results under fault distances of 5 km and 10 km, respectively. When the SPG fault current and voltage start to be suppressed, it can be witnessed that they can be suppressed to a great extent, but the residual fault current and voltage is originally large before the proposed method works. Moreover, the residual fault current and voltage grow as the fault distance increases from 5 km to 10 km, which will cause the fault arc to not suppress or to reignite repeatedly. After the proposed method starts to work, the residual fault current and voltage can be further suppressed to be smaller. Therefore, influence of line impedance voltage drop on residual fault current and voltage are significantly eliminated whether the fault distance is 5 km or 10 km, ensuring that the fault arc can be reliably suppressed without reignition.

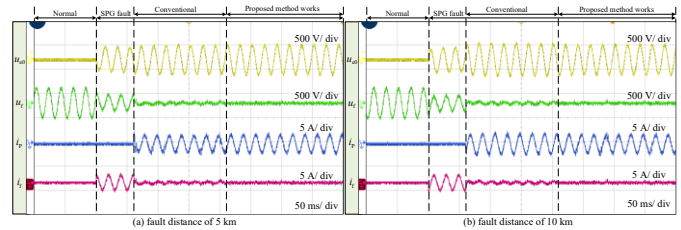


Fig. 15. Experimental results under different fault distances of (a) 5 km and (b) 10 km.

Fig. 16 (a) and (b) show the SPG fault current and voltage suppression results under fault distances of 15 km and 20 km, respectively. Likewise, after the fault current and voltage start to be suppressed, they can be suppressed to a great extent, but the residual fault current and voltage grow as the fault distance increases before the proposed method works, resulting in the fault arc to not suppress. When the proposed method starts to work, they can still be suppressed to a smaller enough level. Therefore, the influence of line impedance voltage drop on the residual fault current and voltage are significantly eliminated regardless of fault distances, which ensures reliable fault arc suppression.

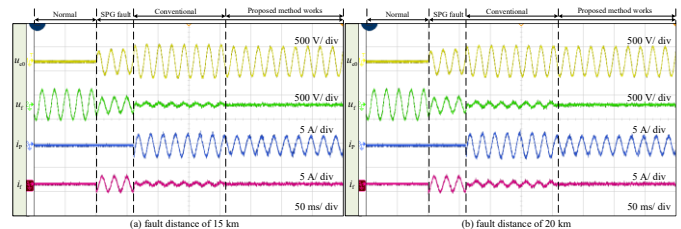


Fig. 16. Experimental results under different fault distances of (a) 15 km and (b) 20 km.

### B. Experimental Results under Difference Fault Resistances

Fig. 17 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of 10 Ω and 50 Ω, respectively. When a SPG fault occurs, the fault current has a large impulse at the initial moment in the case of  $R_f = 10\Omega$ . The amplitude of the impulse decreases when  $R_f$  increases to 50 Ω. In both cases, after the fault current and voltage start to be suppressed, it can be seen that the residual fault current is still significantly large before the proposed method works due to the line impedance voltage drop. After the proposed method

starts to work, the fault current and voltage can be suppressed to be smaller enough, which means that the serious influence of line impedance voltage drop on residual fault current under low fault resistances can be significantly eliminated.

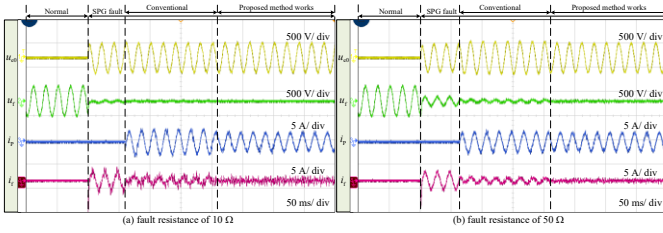


Fig. 17. Experimental results under different fault resistances of (a)  $R_f = 10\Omega$  and (b)  $R_f = 50\Omega$ .

Fig. 18 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of  $100\Omega$  and  $200\Omega$ , respectively. There is no fault current impulse at the initial moment of fault. It can be seen that the residual fault current and voltage are both large before the proposed method works. However, after the proposed method starts to work, the fault current and voltage have less residual component. Therefore, the influence of line impedance voltage drop on residual fault current and voltage under medium fault resistance is largely eliminated.

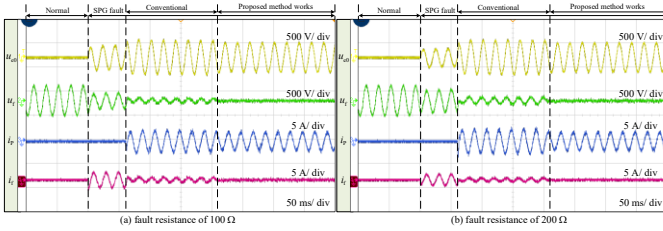


Fig. 18. Experimental results in the case of different fault resistances of (a)  $R_f = 100\Omega$  and (b)  $R_f = 200\Omega$ .

Fig. 19 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of  $500\Omega$  and  $1\text{ k}\Omega$ , respectively. When the fault current and voltage start to be suppressed, the residual fault current is originally small but the residual fault voltage is not small before the proposed method works. After the proposed method starts to work, the residual fault voltage is significantly suppressed, and the residual fault current is also suppressed to be smaller. Thus, the influence of line impedance voltage drop on fault current and voltage can be eliminated.

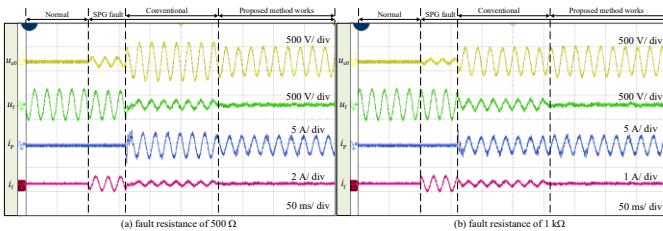


Fig. 19. Experimental results in the case of different fault resistances of (a)  $R_f = 500\Omega$  and (b)  $R_f = 1\text{ k}\Omega$ .

Fig. 20 (a) and (b) show the SPG fault current and voltage suppression results under fault resistances of  $5\text{ k}\Omega$  and  $10\text{ k}\Omega$ , respectively. In the initial stage when fault current and voltage start to be suppressed, spikes can be observed, and the residual fault current is originally small but the residual fault voltage is

not small before the proposed method works. However, after the proposed method starts to work, the residual fault voltage is suppressed, and the residual fault current is also suppressed to be smaller. Thus, the impact of line impedance voltage drop on fault current and voltage still can be eliminated whether the fault resistance is low, medium, or high, and the residual fault current and voltage are small enough to suppress the fault arc under different fault resistances.

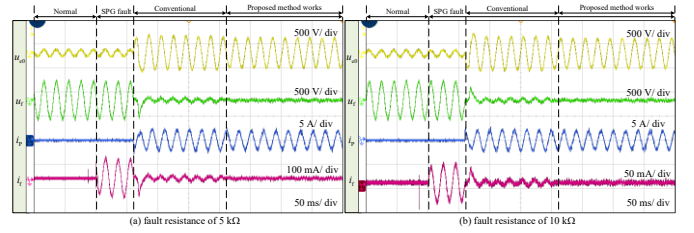


Fig. 20. Experimental results in the case of different fault resistances of (a)  $R_f = 5\text{ k}\Omega$  and (b)  $R_f = 10\text{ k}\Omega$ .

### C. Results Analysis and Discussions

Generally speaking, a desirable SPG fault arc suppression method for distribution networks should have sufficiently high adaptability, convenient implementation, and smaller residual fault current and voltage. In this way, it can reliably suppress SPG fault arcs under different conditions, preventing repeated reignition of the arcs. This part analyzes the implementation results to clarify the performance of the proposed enhancing SPG fault arc suppression method following the above-desired needs. Table IV summarizes the implementation results before and after the proposed method works. Originally, the residual fault current and voltage obviously go up as the fault distance increases, and the residual fault current is large under low fault resistances and the residual fault voltage is large under high fault resistances. The line impedance voltage drop is the main cause of them. The proposed method can greatly eliminate the influence of line impedance voltage drop, caused by positive currents in the faulty feeder and the zero-sequence currents for fault arc suppression, under different fault distances and fault resistances, achieving high suppression rates (SR). The SR of fault current  $s_c$  and fault voltage  $s_v$  can be presented as

$$\begin{cases} s_c = \frac{i_{\text{RMS}}^- - i_{\text{RMS}}^+}{i_{\text{RMS}}^-} \\ s_v = \frac{u_{\text{RMS}}^- - u_{\text{RMS}}^+}{u_{\text{RMS}}^-} \end{cases} \quad (16)$$

where  $i_{\text{RMS}}^-$  is the root mean square (RMS) value of the fault current before fault arc suppression starts;  $i_{\text{RMS}}^+$  is the RMS value of the residual fault current after fault arc suppression starts.  $u_{\text{RMS}}^-$  is the RMS value of the rated fault phase voltage before fault occurs;  $u_{\text{RMS}}^+$  is the RMS value of fault voltage after fault arc suppression starts.

Moreover, Table V provides a comparison of average fault current suppression rates. Thus, not only the proposed method improves adaptability to different fault distances and different fault resistances, but it can also effectively improve the effect of residual SPG fault current and voltage suppression rates in steady-state.

TABLE IV

Summary of Implementation Results for Proposed and Typical Methods			
Fault	Items	Before proposed	After proposed

resistance		method	method
Low	Fault current SR	82.22%	98.37%
	Fault voltage SR	81.95%	98.39%
Medium	Fault current SR	92.20%	98.78%
	Fault voltage SR	95.09%	98.74%
High	Fault current SR	93.39%	98.14%
	Fault voltage SR	93.19%	98.13%
Fault distance	Items	Before proposed method	After proposed method
5 km	Fault current SR	96.40%	98.95%
	Fault voltage SR	96.42%	98.97%
10 km	Fault current SR	94.93%	98.74%
	Fault voltage SR	94.91%	98.71%
15 km	Fault current SR	92.97%	98.39%
	Fault voltage SR	93.17%	98.40%
20 km	Fault current SR	91.12%	98.13%
	Fault voltage SR	91.49%	98.06%

TABLE V  
Comparison of Average Fault Current Suppression Rate

Fault resistance	[13]	[20]	[33]	Proposed
Low	93.40%	92.9%	94.6%	98.37%
Medium	94.65%	91.7%	93.3%	98.77%
High	95.57%	85.9%	88.4%	98.13%

## VI. CONCLUSION

This paper proposes a SPG fault arc suppression method for flexible distribution networks to eliminate the line impedance voltage drop influence using flexible interconnection device. The line impedance voltage drop caused by positive sequence currents of faulty feeder can be eliminated by transferring the positive sequence currents via flexible interconnection device during simultaneous fault arc suppression. The line impedance voltage drop caused by the zero-sequence currents output from flexible interconnection device for fault arc suppression during simultaneous positive sequence currents transfer can also be eliminated, through returning the output current of the flexible interconnection device arm connected to the faulty phase of the faulty feeder to zero. Simulation study and experimental results in the case of different fault distances and resistances demonstrate that the residual fault current and voltage after the proposed method works can be significantly suppressed to be smaller than that before the proposed method works, and the fault current and fault voltage suppression rates are increased to more than 98%, less affected by the line impedance voltage drop.

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