Minimizing Required DC Sources of Cascaded H-bridge Multilevel Converter for Fault Suppression in Active Distribution Networks

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***Abstract*—Single-line ground (SLG) faults are the most common faults in distribution networks. Cascaded H-bridge multilevel converters (CHMC) can be employed to suppress fault current and potential and prevent hazards promptly. However, their application is limited by their high cost and large size. This paper proposes a cost- and size-efficient implementation method of single-phase CHMC for fault suppression, performed by minimizing the required DC sources. In this method, the output voltage vector of CHMC is reconstructed during fault elimination by two mutually perpendicular sub-voltage vectors, one perpendicular and the other parallel to the target output current vector of CHMC. The sub-voltage parallel to the target output current, which provides all required active power output, is generated using an H-bridge cell supplied by a DC source with minimized capacity. The remaining H-bridge cells generate the sub-voltage perpendicular to the target output current without any DC source employment since they are solely responsible for reactive power output, thus maintaining their DC capacitor voltages. The simulation study and experimental validation have been conducted, and the results demonstrate that not only is the proposed method cost- and size-effective but also effectively ensures SLG fault elimination.**

***Index Terms*—cascaded H-bridge multilevel converter (CHMC), minimizing DC sources, active arc suppression, active distribution networks, single-line ground (SLG) fault, fault elimination**

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I. Introduction

With the development of power electronic technology, large amounts of high-capacity distributed resources are connected to distribution networks, forming an AC-DC hybrid system [1]. The penetration of the distributed resources causes randomness in the magnitude and direction of the power flow, resulting in the conventional protection to make mistakes [2], [3]. When a single-line ground (SLG) fault occurs in the distribution network, a large fault current will be generated, seriously affecting its safe operation. [4]-[6].

Limiting fault current is a typical effective protection means, such as the use of inductive elements, superconductors, and power electronics. However, the inductive elements are less flexible than superconductors [7]-[9]. The fault current limiter based on the superconductor operates with intrinsic high resistance at high fault current and low or zero resistance at non-fault [10]. However, it still has some problems that need to be addressed: 1) a required low-temperature operating condition; 2) high cost with design, manufacture, and application [11].

Power electronics offer high flexibility and relatively low cost. In a DC system, a rectifier dc-link is connected in series to the DC line, providing a series virtual inductor with set-slope linear current and regulating the voltage drop of the inductor during a single pole grounding fault [12]. Furthermore, a bridge-type multiport fault current limiter that can be installed at the DC bus is proposed [13]. It works for all DC lines connected to the DC bus and can cooperate with the existing DC circuit breakers, so that the fault current can be limited without time delay and its internal energy dissipation circuit can suppress the negative impacts of the inductor. The same research term further proposes a hybrid DC current-limiting circuit breaker, which can limit the rising speed of current by embedded inductors and suppress their negative impacts on fault current interruption [14].

Compared with DC systems, the difference is that only the SLG fault branch current needs to be limited in AC systems [15]-[17]. Thus, power electronics need to be connected in parallel in distribution networks, which requires a higher voltage level and sine output capability [18]. One of the most typical topologies currently used is H-bridges [19], [20]. A

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single-phase single-cascade H-bridge converter is connected to the distribution network via a step-up transformer to limit the fault current [21], [22]. It can meet high voltage level access requirements, but the sinusoidal output capability needs improvement. A single-phase cascaded H-bridge multilevel converter (CHMC) can be connected directly between the neutral point and the ground. It provides a high sinusoidal zero-sequence current to compensate for the SLG fault current, and the fault potential is suppressed and clamped to zero [23]. Further, an active disturbance rejection control and a soft grid-connection scheme can be designed for the CHMC [24]. However, each H-bridge of the CHMC needs to provide a separate DC source to maintain its DC voltage, and the DC sources are inconvenient to access in the medium-voltage distribution networks. I.e., a series of step-down, rectifiers, and dc/dc conversion devices are required, resulting in large size, high cost, and heavyweight [25].

Two arms of a revised static synchronous compensator based on CHMC can be used to inject the compensation current cooperatively, allowing the DC voltages of the CHMC to be self-maintaining [26]. In addition, two-phase arms of a three-phase CHMC without DC sources are connected to the two non-faulty lines to limit fault current and suppress fault potential by working and charging in turns [27]. That could be a very novel idea, but the cost and size may increase further instead of decreasing due to the additional CHMC components and higher voltage level requirements than single-phase CHMC. Besides, all arms of a three-phase CHMC are used to optimize the performances of fault current limitation and fault potential suppression [28], [29]. However, the DC sources are still indispensable, and the additional CHMC components and higher voltage levels are still required. Despite its versatility, its cost-effectiveness in practice needs to be further evaluated [30]. Therefore, at present, the single-phase CHMC has a higher cost performance, but it is still limited by its high cost and large size caused by its DC power supply systems.

This paper presents a novel implementation approach that minimizes the number and capacity of DC sources required in the fault suppression method based on separate control of main and auxiliary modules of single-phase CHMC. The main contributions of the article are summarized as follows.

1) The output characteristics of CHMC during SLG fault suppression are comprehensively analyzed. The analysis indicates that the CHMC should deliver only a small amount of active power during fault suppression, and a single DC source with low capacity can effectively supply this active power. Accordingly, the necessary conditions for minimizing the required number and capacity of DC sources exist in SLG fault suppression through the utilization of CHMC.

2) To separate the H-bridge cells responsible for delivering active and reactive power, the output voltage vector of CHMC is restructured using two mutually perpendicular sub-voltage vectors. One sub-voltage vector is perpendicular to the target output current vector of the CHMC, while the other sub-voltage vector is parallel to it. The active power output is generated by the product of the parallel sub-voltage and the target output current, while the reactive power output is generated by the product of the perpendicular sub-voltage and the target output current. This allows for allocating distinct H-bridge cells to solely output active power (the parallel sub-voltage) or reactive power (perpendicular sub-voltage).

3) An H-bridge supplied by a DC source is controlled as a main module to generate the sub-voltage parallel to the target output current and is solely responsible for active power output. The capacity of this DC source is low since CHMC should deliver only a small amount of active power during fault suppression. The other H-bridge cells are controlled as auxiliary modules to generate the sub-voltage perpendicular to the target output current without any DC source employment since they are solely responsible for reactive power output, thus maintaining their DC capacitor voltages. In this way, the proposed implementation method effectively minimizes the capacity and number of required DC sources, reducing cost and size.

The remainder of this paper is organized as follows: the analysis of CHMC output characteristics under SLG fault is introduced in Section II. The proposed method is presented in Section III. The simulation study and experimental validation are presented in Section IV and Section V, respectively. The conclusions are elaborated in Section VI.

II. Analysis of CHMC Output Characteristics under SLG Fault

A schematic diagram of a distribution network with an SLG fault and a CHMC is shown in Fig. 1. The distribution network contains n feeder lines with hybrid overhead lines and cable lines, and they have parallel impedances induced with ground, i.e., line-to-ground impedance (LGI). The scaled-up distributed resources are connected, including photovoltaic (PV) plant and energy storage (ES) plant, forming active distribution networks. CHMC is connected between the neutral point constructed by a zigzag transformer and the earth, and the zigzag transformer is connected to the busbar of the active distribution network.

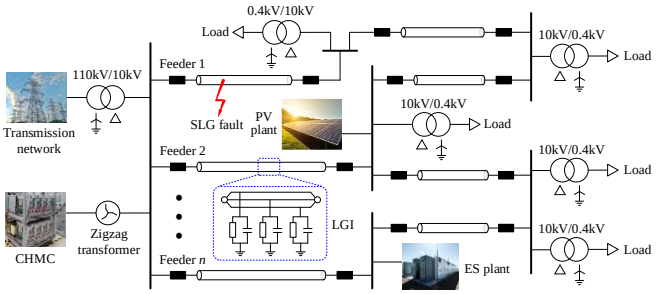


Fig. 1. Schematic diagram of active distribution network.

The topological structure of a distribution network with an SLG fault and a CHMC is shown in Fig. 2. Assuming that the SLG fault occurs in phase A, based on the analysis method of asymmetric faults in power systems [31], [32], [33], the zero-sequence equivalent circuit of the distribution network is drawn in Fig. 3. Where R_0 and C_0 are the induced zero-sequence line-to-ground resistance and capacitance, respectively. i_f is the fault current, and R_f is the fault resistance. e_A is the line-to-neutral voltage of the faulty phase. u_M is the modulated CHMC output voltage. L and R are the filter inductor and the equivalent resistance of the CHMC branch circuit. u_L, u_R, and u_f are the voltages of L, R, and R_f, respectively. u_N is the neutral point voltage, and i_N is the

current from the CHMC output to the neutral point.

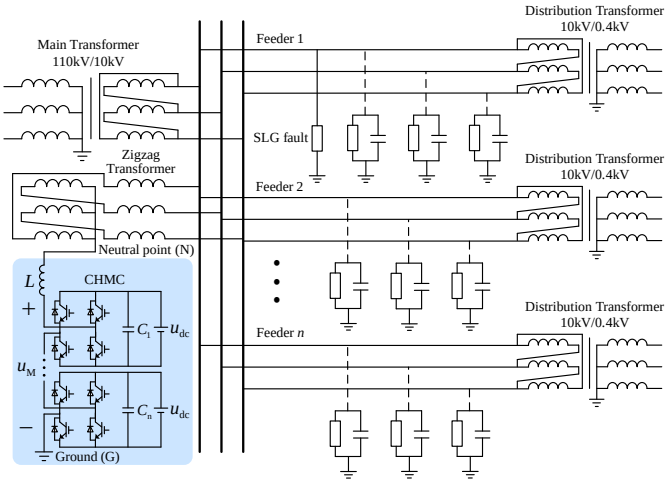


Fig. 2. Topological structure of distribution network with CHMC and SLG fault.

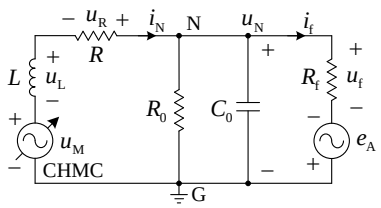


Fig. 3. Zero-sequence equivalent circuit of active distribution network.

According to Fig. 3 and Kirchhoff's current law (KCL), it can be expressed as

$$i_{\mathrm{N}} - i_{\mathrm{f}} = u_{\mathrm{N}}\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right) \tag{1}$$

where

$$i_{\mathrm{f}} = \frac{u_{\mathrm{N}} + e_{\mathrm{A}}}{R_{\mathrm{f}}} \tag{2}$$

$$i_{\mathrm{N}} = \frac{u_{\mathrm{M}} - u_{\mathrm{N}}}{R + \mathrm{j}\omega L} \tag{3}$$

By controlling u_{M}, when i_{N} is regulated as

$$i_{\mathrm{N}} = u_{\mathrm{N}}\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right) \tag{4}$$

The SLG fault current is regulated as $i_{\mathrm{f}} = 0$, and $u_{\mathrm{N}} = -e_{\mathrm{A}}$, the fault potential is $u_{\mathrm{f}} = 0$, so that the fault factors can be removed in time to avoid the negative impacts of SLG fault. At this time, the modulation voltage of the CHMC u_{M} can be calculated by

$$\begin{aligned} u_{\mathrm{M}} &= u_{\mathrm{N}}\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right)\left(R + \mathrm{j}\omega L\right) + u_{\mathrm{N}} \\ &= -e_{\mathrm{A}}\left(\frac{1}{R_0} + \mathrm{j}\omega C_0\right)\left(R + \mathrm{j}\omega L\right) - e_{\mathrm{A}} \end{aligned} \tag{5}$$

Typically, the three line-to-neutral voltages are expressed as

$$\begin{aligned} e_{\mathrm{A}} &= E_{\mathrm{m}} \sin\left(\omega t + \theta_0\right) \\ e_{\mathrm{B}} &= E_{\mathrm{m}} \sin\left(\omega t + \theta_0 - \frac{2}{3}\pi\right) \\ e_{\mathrm{C}} &= E_{\mathrm{m}} \sin\left(\omega t + \theta_0 + \frac{2}{3}\pi\right) \end{aligned} \tag{6}$$

where E_m and θ_0 are the amplitude and initial angle of the line-to-neutral voltage. Since R_0 and C_0 are constants and can be measured [25], the reference current i_{N} is determined based on (4), and can be written as

$$i_{\mathrm{N}} = I_{\mathrm{N}} \sin\left(\omega t + \theta_0 - \alpha_0 - \frac{\pi}{2}\right) \tag{7}$$

where

$$\begin{aligned} I_{\mathrm{N}} &= E_{\mathrm{m}} \sqrt{\frac{1}{R_0^2} + \omega^2 C_0^2} \\ \alpha_0 &= \arctan\frac{1}{\omega R_0 C_0} \end{aligned} \tag{8}$$

Correspondingly, u_{L} and u_{R} can be expressed as

$$\begin{aligned} u_{\mathrm{L}} &= I_{\mathrm{N}} \omega L \sin\left(\omega t + \theta_0 - \alpha_0 + \pi\right) \\ u_{\mathrm{R}} &= I_{\mathrm{N}} R \sin\left(\omega t + \theta_0 - \alpha_0 + \frac{\pi}{2}\right) \end{aligned} \tag{9}$$

Therefore, the active power p_{M} and reactive power q_{M} output by the CHMC can be presented as

$$\begin{aligned} p_{\mathrm{M}} &= \mathrm{Re}\left(u_{\mathrm{M}} i_{\mathrm{N}}\right) = \frac{I_{\mathrm{N}}^2 R}{2} + \frac{I_{\mathrm{N}} E_{\mathrm{m}}}{2} \cos\left(-\alpha_0 + \frac{\pi}{2}\right) \\ q_{\mathrm{M}} &= \mathrm{Im}\left(u_{\mathrm{M}} i_{\mathrm{N}}\right) = -\frac{I_{\mathrm{N}}^2 \omega L}{2} + \frac{I_{\mathrm{N}} E_{\mathrm{m}}}{2} \sin\left(-\alpha_0 + \frac{\pi}{2}\right) \end{aligned} \tag{10}$$

Since the damping rate d of the distribution network typically does not exceed 5% [34], [35], i.e. $R_0 \gg 1/\omega C_0$, α_0 is small according to (8), and the active power consumed by R is sufficiently small. Consequently, the CHMC provides a large amount of reactive power q_{M} and a small amount of active power p_{M}.

III. Proposed Method

Considering the analysis in section II, the CHMC's active power output generally does not exceed 5% of the total output capacity during fault suppression. Accordingly, this section proposes an implementation method to minimize the number and capacity of DC sources equipped with the CHMC. In this regard, the following voltage vector group is constructed.

Since the neutral point voltage of the distribution network is regulated as $u_{\mathrm{N}} = -e_{\mathrm{A}}$ during SLG fault suppression, the zero-sequence equivalent circuit in Fig.3 can be further equivalent, as shown in Fig. 4.

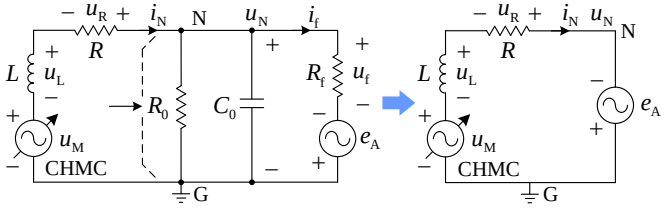


Fig. 4. Zero-sequence equivalent circuit of active distribution network during SLG fault suppression.

In order to minimize the number and capacity of DC sources equipped with the CHMC, the following voltage vector group is constructed.

$$\begin{aligned} u_1 &= U_1 \sin\left(\omega t + \theta_0 - \alpha_0 - \frac{\pi}{2}\right) \\ u_2 &= U_2 \sin\left(\omega t + \theta_0 - \alpha_0 + \pi\right) \\ u_1 + u_2 + u_{\mathrm{L}} + u_{\mathrm{R}} &= u_{\mathrm{N}} = -e_{\mathrm{A}} \end{aligned} \tag{11}$$

where U_1 and U_2 are the amplitude of u_1 and u_2. Thus, the voltage and current vectors can be drawn in Fig. 5. Where the vectors u_1 and u_R are parallel to the vector i_N, and vectors u_2 and u_L are perpendicular to the vector i_N.

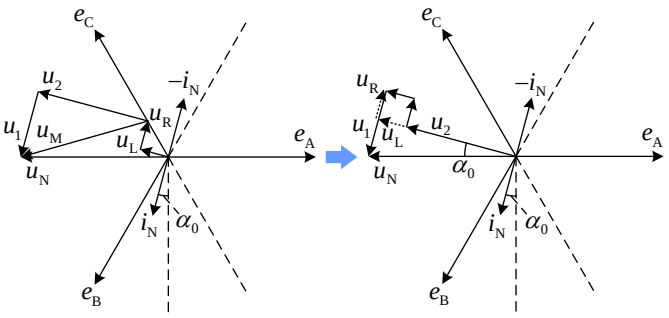


Fig. 5. Voltage and current vectors of CHMC circuit.

Therefore, it can be presented as

$$u_M = u_1 + u_2 \tag{12}$$

In this case, the active power and reactive power output by the CHMC can be rewritten as

$$\begin{aligned} p_M &= \mathrm{Re}(u_M i_N) = u_1 i_N = \frac{U_1 I_N}{2} \\ q_M &= \mathrm{Im}(u_M i_N) = u_2 i_N = -\frac{U_2 I_N}{2} \end{aligned} \tag{13}$$

Based on Fig. 5, u_1 is minimized in the right triangle formed by the voltage vectors u_1, u_2, u_L, u_R, and u_N. Restoring the controllable voltage source in Fig. 4 to the CHMC topology, let one of the cells of the CHMC as a main module output a voltage u_1, and the remaining cells of the CHMC as auxiliary modules output a voltage u_2, Fig. 6 can be drawn as follows.

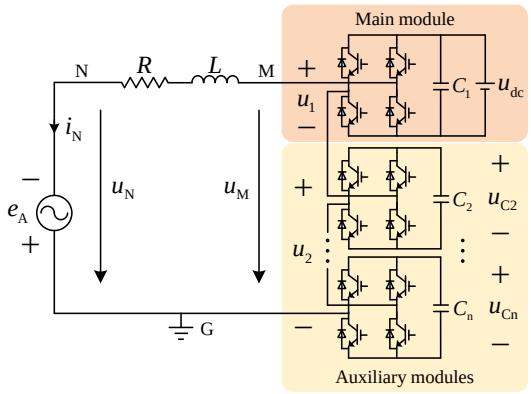


Fig. 6. Schematic diagram of CHMC with a single minimized DC source.

In this way, all required active power is supplied by the main module, and the auxiliary modules only supply reactive power. Consequently, during SLG fault suppression, only the main module needs to be equipped with a DC source to maintain its DC-link voltage stability, and the single DC source capacity is minimized due to the fact that u_1 is minimized. The DC-link capacitor voltages of the auxiliary modules are maintained on their own without the need for DC sources.

According to the damping rate not exceeding 5%, it can be presented that

$$d = \frac{1}{\omega R_0 C_0} \le 5\% \tag{14}$$

Thereby,

$$p_M = \frac{u_N^2}{R_0} \le 5\% \omega C_0 u_N^2 = 0.05 q_M \tag{15}$$

Combining this with (13), it can be obtained that

$$U_1 \le 0.05 U_2 \tag{16}$$

For a distribution network with a line-to-line voltage of 1 p.u., the amplitude of the phase voltage of the distribution network is $\sqrt{6}/3$ p.u., so the output voltage amplitude level of the CHMC needs to be greater than $\sqrt{6}/3$ p.u., i.e.,

$$\sqrt{6}/3 \le U_1 + U_2 \le 0.05 U_2 + U_2 = 1.05 U_2 \tag{17}$$

Consequently, the output voltage amplitude levels of the main and auxiliary modules need to meet $U_1 \ge \sqrt{6}/63$ p.u. and $U_2 \ge 20\sqrt{6}/63$ p.u.. I.e., the DC source voltage of the main module should be more than $\sqrt{6}/63$ p.u.. Therefore, if the number of cascades of a CHMC is N, the number of main modules can be determined to be $\lceil \mathrm{N}/21 \rceil$, and the number of auxiliary modules can be determined to be $\mathrm{N} - \lceil \mathrm{N}/21 \rceil$.

For example, in a 10kV distribution network, the amplitude of the phase voltage is not more than 8165V. Therefore, based on (17), the output voltage amplitude level of the CHMC needs to be greater than 8165V, and the output voltage amplitude levels of the main and auxiliary modules need to meet $U_1 \ge 388.81$ and $U_2 \ge 7776.2$. I.e., the DC source voltage of the main module should be more than 388.81V. Therefore, when the number of cascades of a CHMC is 10, the number of main modules is determined to be 1 and the number of auxiliary modules is determined to be 9, which can meet the above voltage amplitude requirements.

A. Evaluation and Control of Auxiliary Modules

Based on the above analysis, the controls of the main module and the auxiliary modules should be designed separately. The overall control structure of the main and auxiliary modules is drawn, as shown in Fig. 7.

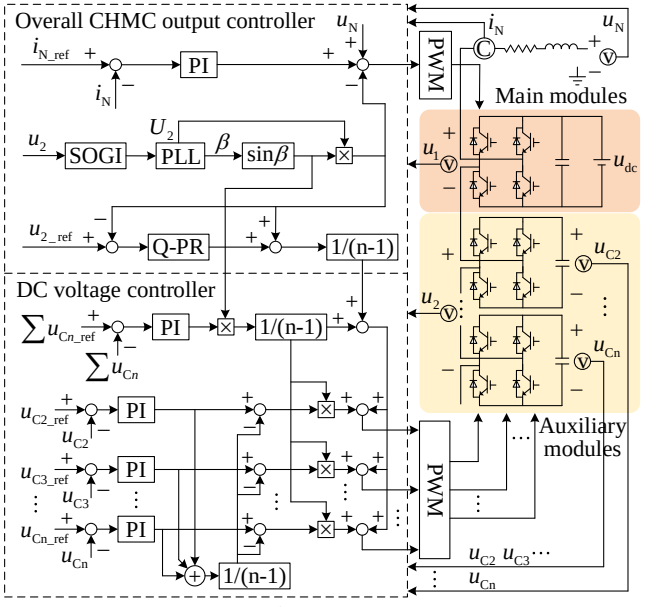


Fig. 7. Overall control structure of main and auxiliary modules.

The control target of the auxiliary modules should be its output voltage. Based on Fig. 5, the amplitude of the output voltage reference value can be calculated as

$$\begin{aligned}\left|u_{2\_\mathrm{ref}}\right| &= \left|u_{\mathrm{N}}\right|\cos\alpha_0 - \left|u_{\mathrm{L}}\right| = \left|-e_{\mathrm{A}}\right|\cos\alpha_0 - I_{\mathrm{N}}\omega L \\ &= E_{\mathrm{m}}\cos\left(\arctan\frac{1}{\omega R_0 C_0}\right) - \omega L E_{\mathrm{m}}\sqrt{\frac{1}{R_0^2}+\omega^2 C_0^2}\end{aligned} \tag{18}$$

Therefore, the output voltage reference value u_{2_ref} of the auxiliary modules can be calculated as

$$u_{2\_\mathrm{ref}} = \left|u_{2\_\mathrm{ref}}\right| sin\left(\omega t + \theta_0 - arctan\frac{1}{\omega R_0 C_0} + \pi\right) \tag{19}$$

The output multilevel voltage u_2 is filtered through a second-order generalized integral (SOGI) and a phase-locked loop (PLL) to extract the fundamental frequency component and then used as a feedback signal. The quasi-proportional resonance (Q-PR) control is used to achieve different-free tracking of AC voltage signal. Although the auxiliary modules theoretically provide only reactive power, the CHMC circuit actually generates active power losses, resulting in a slight drop in DC-link voltages of the auxiliary modules, and the degree of voltage drop varies due to the differences of active power losses in each auxiliary module circuit. By adding the DC voltage control, the DC-link voltages of the auxiliary modules can be maintained stable and balanced. In this way, the vectorial variation of the output voltage can be drawn, as shown in Fig. 8.

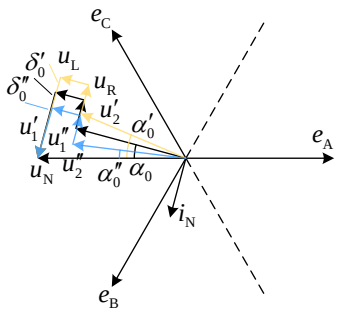


Fig. 8. Vectorial variation of CHMC circuit.

Due to the slight active losses of the CHMC circuit, the actual output voltage of the auxiliary modules is u_2'' which is not exactly perpendicular to the vector i_{N}, i.e., $\alpha_0'' < \alpha_0$, the active power output by the auxiliary modules is

$$p_2 = \frac{U_2'' I_{\mathrm{N}}}{2} cos\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0''\right) > 0 \tag{20}$$

Therefore, the DC capacitors of the auxiliary modules are generally externally discharged, so that the DC-link voltages drop to varying degrees.

The reactive power output by the auxiliary modules is

$$q_2 = \frac{U_2'' I_{\mathrm{N}}}{2} sin\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0''\right) \neq -\frac{U_2 I_{\mathrm{N}}}{2} \tag{21}$$

I.e., if the active losses of the CHMC circuit are not taken into account in the control, the active power and reactive power converted by the auxiliary modules have errors, which are

$$\begin{aligned}\Delta p_2 &= -\frac{U_2'' I_{\mathrm{N}}}{2} cos\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0''\right) < 0 \\ \Delta q_2 &= -\frac{U_2 I_{\mathrm{N}}}{2} - \frac{U_2'' I_{\mathrm{N}}}{2} sin\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0''\right) < 0\end{aligned} \tag{22}$$

Through the DC voltage control, the actual output voltage of the auxiliary modules is regulated to u_2' which is still not exactly perpendicular to the vector i_{N}, but $\alpha_0' > \alpha_0$, the active power output by the auxiliary modules is

$$p_2 = \frac{U_2' I_{\mathrm{N}}}{2} cos\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0'\right) < 0 \tag{23}$$

At this time, the DC capacitors of the auxiliary modules generally are internally charged, accordingly, the DC-link voltages rise evenly.

The reactive power output by the auxiliary modules is

$$q_2 = \frac{U_2' I_{\mathrm{N}}}{2} sin\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0'\right) \neq -\frac{U_2 I_{\mathrm{N}}}{2} \tag{24}$$

I.e., through the DC voltage control, the active power and reactive power converted by the auxiliary modules have reverse errors to compensate for the dc-link voltage drop caused by the active losses of the CHMC circuit, which can be expressed as

$$\begin{aligned}\Delta p_2 &= -\frac{U_2' I_{\mathrm{N}}}{2} cos\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0'\right) > 0 \\ \Delta q_2 &= -\frac{U_2 I_{\mathrm{N}}}{2} - \frac{U_2' I_{\mathrm{N}}}{2} sin\left(-\frac{\pi}{2} + \alpha_0 - \alpha_0'\right) < 0\end{aligned} \tag{25}$$

When the DC-link voltages rise above the reference value, the output voltage of the auxiliary modules is regulated back to u_2'', the excessive DC-link voltages are reduced. Repeat this and the DC-link voltages can remain stable and balanced at the reference value, ensuring that the reactive power is supplied by the auxiliary modules only.

B. Evaluation and Control of the main module

Due to the fluctuation of the output voltage of the auxiliary modules around the reference value u_2 caused by the DC voltage control, the output voltage of the main module should also be regulated accordingly so that the output current of the CHMC is i_{N}, ensuring that the SLG fault current is $i_{\mathrm{f}} = 0$ and the neutral point voltage is $u_{\mathrm{N}} = -e_{\mathrm{A}}$.

Therefore, the main module is used to control the output current, and the output current reference value $i_{\mathrm{N\_ref}}$ of the main module can be calculated as

$$\begin{aligned}i_{\mathrm{N\_ref}} &= I_{\mathrm{N}} sin\left(\omega t + \theta_0 - \alpha_0 - \frac{\pi}{2}\right) \\ &= E_{\mathrm{m}}\sqrt{\frac{1}{R_0^2}+\omega^2 C_0^2}\, sin\left(\omega t + \theta_0 - arctan\frac{1}{\omega R_0 C_0} - \frac{\pi}{2}\right)\end{aligned} \tag{26}$$

In this way, the output voltage of the main module can be adjusted automatically to accommodate and compensate for the fluctuation of the output voltage of the auxiliary modules, making the phase angle difference δ_0 between u_1 and i_{N} ultimately stable at zero, ensuring that the active power is supplied by the main module only.

I.e., when the output voltage of the auxiliary modules is u_2'', because the output current of the CHMC is i_{N}, the neutral point voltage is $u_{\mathrm{N}} = -e_{\mathrm{A}}$, thus the output voltage of the main module is u_1'' based on the vectorial variation of the CHMC circuit in Fig. 8, and the active power and reactive power output by the main module are

$$\begin{aligned}p_1 &= \frac{U_1'' I_{\mathrm{N}}}{2} cos\left(-\delta_0''\right) \neq \frac{U_1 I_{\mathrm{N}}}{2} \\ q_1 &= \frac{U_1'' I_{\mathrm{N}}}{2} sin\left(-\delta_0''\right) < 0\end{aligned} \tag{27}$$

where δ_0'' is the phase angle difference between u_1'' and i_{N}. Therefore, the errors of active power and reactive power converted by the main module are

$$\begin{aligned}\Delta p_1 &= \frac{U_1 I_N}{2} - \frac{U_1'' I_N}{2} cos\left(-\delta_0''\right) > 0 \\ \Delta q_1 &= -\frac{U_1'' I_N}{2} sin\left(-\delta_0''\right) > 0\end{aligned} \tag{28}$$

Since $\Delta p_1 > 0$, $\Delta p_2 < 0$, $\Delta q_1 > 0$, and $\Delta q_2 < 0$, based on (22) and (28), but the total active power and reactive power output by the CHMC are constant according to (10), $\Delta p_1 + \Delta p_2 = 0$, $\Delta q_1 + \Delta q_2 = 0$. I.e., the main module compensates for the errors caused by the fluctuation of the output voltage of the auxiliary modules, which is also in accordance with the output power conservation theorem of the CHMC circuit.

Similarly, when the output voltage of the auxiliary modules is u_2', the output voltage of the main module is u_1'. In this case, the active power and reactive power output by the main module are represented as

$$\begin{aligned}p_1 &= \frac{U_1' I_N}{2} cos\left(-\delta_0'\right) \neq \frac{U_1 I_N}{2} \\ q_1 &= \frac{U_1' I_N}{2} sin\left(-\delta_0'\right) < 0\end{aligned} \tag{29}$$

where δ_0' is the phase angle difference between u_1' and i_N. Therefore, the errors of active power and reactive power converted by the main module are

$$\begin{aligned}\Delta p_1 &= \frac{U_1 I_N}{2} - \frac{U_1' I_N}{2} cos\left(-\delta_0'\right) < 0 \\ \Delta q_1 &= -\frac{U_1' I_N}{2} sin\left(-\delta_0''\right) > 0\end{aligned} \tag{30}$$

According to the output power conservation theorem of the CHMC circuit, the main module similarly compensates for errors caused by the fluctuation of the output voltage of the auxiliary modules, i.e., since $\Delta p_1 < 0$, $\Delta p_2 > 0$, $\Delta q_1 > 0$, and $\Delta q_2 < 0$, as in (25) and (30), but the active power and reactive power output by the CHMC still are constant in accordance with (10), $\Delta p_1 + \Delta p_2 = 0$, $\Delta q_1 + \Delta q_2 = 0$.

IV. Simulation Study

The proposed method is verified through simulation on MATLAB/Simulink. The distribution network with SLG fault and CHMC with minimized DC source are built based on Fig. 1. The three-phase circuit ratio is 29.13, and the SLG short-circuit ratio is 0.17. The main parameters are shown in Table I.

TABLE I
Main Simulation Parameters

Symbol	Parameters	Value
C_0	Line-to-ground capacitance	26.49 [μF]
R_0	Line-to-ground resistance	5 [kΩ]
N	Number of H-bridges in CHMC	10
u_{CN}	DC-link voltages of CHMC	1000 [V]
C_N	DC-link capacitors	2200 [μF]
L	Filter inductor of CHMC	0.01 [H]
R	Equivalent resistor of CHMC branch	0.1 [Ω]

A. Output Performances of CHMC

Based on the simulation parameters, the active power and reactive power calculated by (10) are 24.42 kW and 290.12 kvar, respectively. Assuming that the SLG fault occurs at $t = 0.05$ s, when the CHMC starts to output current at $t = 0.1$ s, the output performances of the CHMC are shown in Fig. 9 and 10.

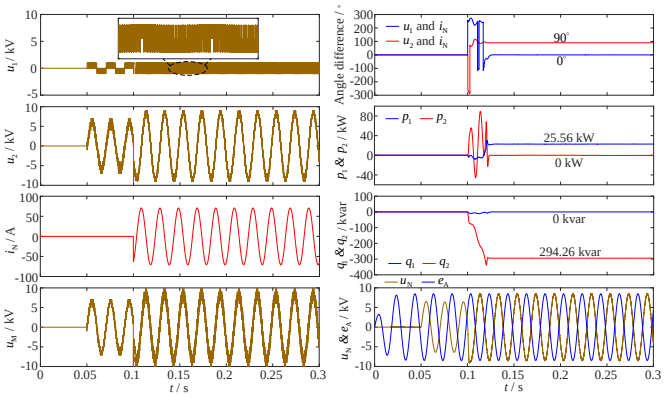


Fig. 9. Output performances of CHMC.

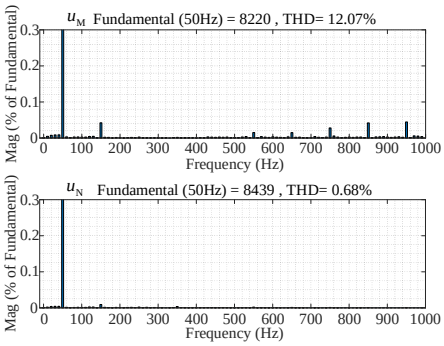


Fig. 10. Harmonics analysis of output voltages of CHMC.

The output voltages u_1 and u_2 are controlled separately, and their phase difference with output current i_N are 0° and 90°, respectively. Thus, the main module outputs only active power of 25.56 kW, and the auxiliary modules output only reactive power of 294.26 kvar, which coincides with the calculated values. The output voltage harmonics of the CHMC are effectively filtered, and the filtered output voltage u_N is equal to $-e_A$. I.e., the proposed implementation method for the main module and the auxiliary modules are validated.

B. SLG Fault Suppression Results

The SLG fault suppression results with low fault resistance of $R_f = 10\ \Omega$, medium fault resistances of $R_f = 100\ \Omega$ and $300\ \Omega$, and high fault resistance of $R_f = 5000\ \Omega$ are shown in Fig. 11 and Fig. 12.

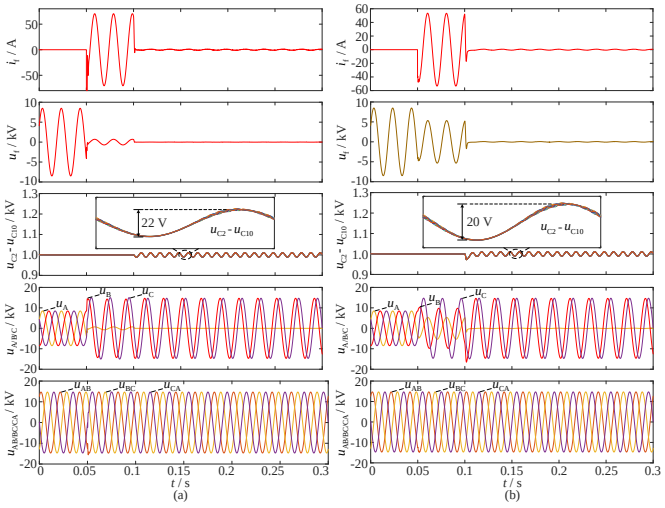


Fig. 11. Results of SLG fault current and voltage suppression under different fault resistances: (a) $R_f = 10\ \Omega$; (b) $R_f = 100\ \Omega$.

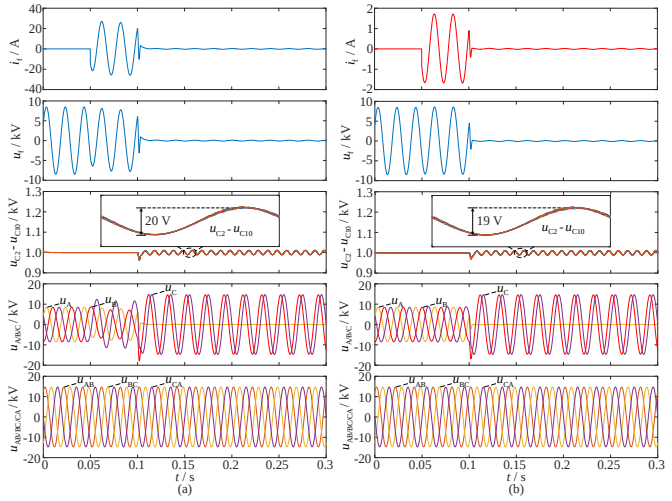


Fig. 12. Results of SLG fault current and voltage suppression under different fault resistances: (a) $R_f = 300\ \Omega$; $R_f = 5000\ \Omega$.

The SLG fault currents are limited to near zero, and the fault voltages are also suppressed to zero, which in turn causes the fault to be ineffective until it disappears completely. During this period, the DC-link voltages can be maintained at 1 kV.

V. Experiment Validation

The proposed method is further validated on a 380V physical experimental platform, as shown in Fig. 13. The three-phase circuit ratio is 25.49, and the SLG short-circuit ratio is 0.14. Moreover, the main specifications are shown in Table II.

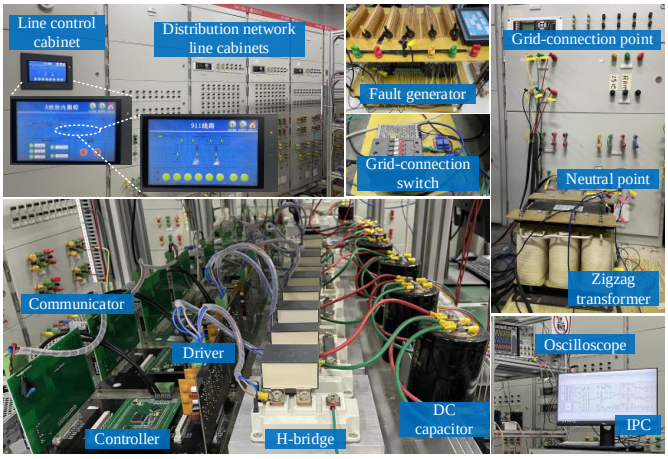


Fig. 13. Physical experimental platform.

TABLE II
Main Specifications of Experimental Platform

Symbol	Parameters	Value
C_0	Line-to-ground capacitance	19.8 [μF]
R_0	Line-to-ground resistance	800/3 [Ω]
N	Number of H-bridges in CHMC	7
u_{CN}	DC-link voltages of CHMC	60 [V]
C_N	DC-link capacitors	1000 [μF]
L	Filter inductor of CHMC	0.02 [H]
R	Equivalent resistor of CHMC branch	0.1 [Ω]

A. Output Performances of CHMC

Fig. 14 shows the output voltages of the main module and the auxiliary modules, and the output current of the CHMC. By exporting 0.5 s of .csv format data, the phase angle difference and output power of the CHMC circuit are drawn in Fig. 15. The phase difference between u_1 and i_N is 0°, and the phase difference between u_2 and i_N is 90°. The main and auxiliary modules provide active and reactive power, respectively.

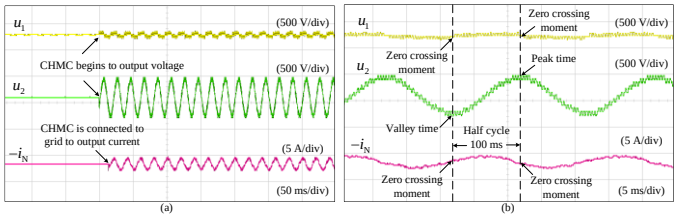


Fig. 14. Output voltages of main and auxiliary modules u_1, u_2, and current of CHMC $-i_N$, (a): regular waveforms; (b): local highlight waveform.

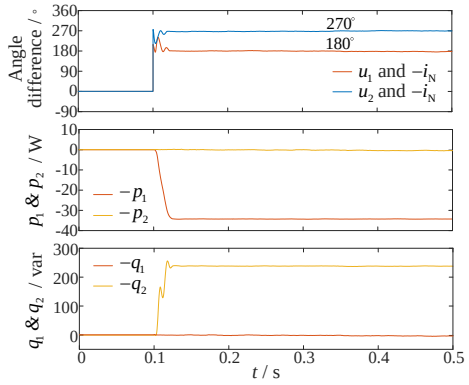


Fig. 15. Phase angle difference and output power of CHMC circuit.

Fig. 16 shows the output voltage of the CHMC, the neutral voltage, and the line-to-neutral voltage of the faulty phase. u_M is filtered to u_N, which is well regulated to $-e_A$.

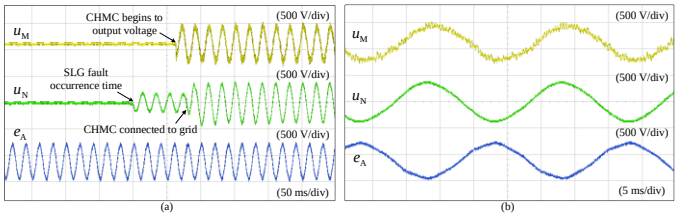
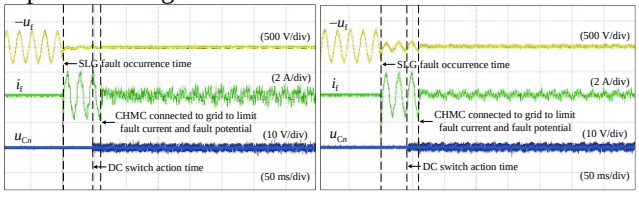


Fig. 16. Voltages of CHMC circuit, (a): regular waveforms; (b): local highlight waveform.

B. SLG Fault Suppression Results

The fault suppression results in the case of different fault resistances are shown in Fig. 17 – Fig. 19, including the faulty voltage, SLG fault current, and the DC capacitor voltages of the auxiliary modules. During the fault period, the larger the SLG fault resistance, the smaller the fault current, but the higher the fault potential. Nevertheless, the fault current and potential can be limited and suppressed simultaneously, and the DC capacitor voltages are maintained.



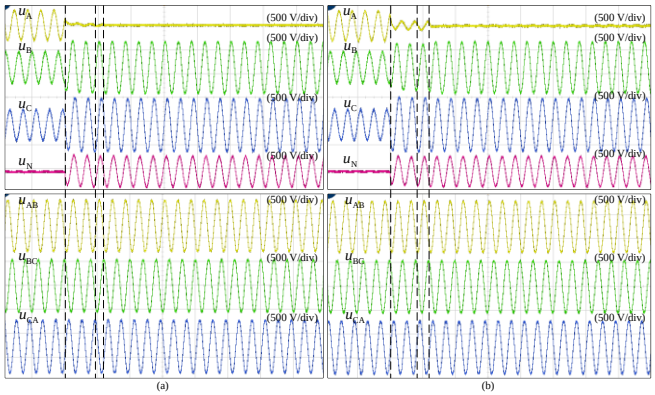


Fig. 17. SLG fault suppression results in the cases of different fault resistances, (a) $R_f = 10\ \Omega$; (b) $R_f = 50\ \Omega$.

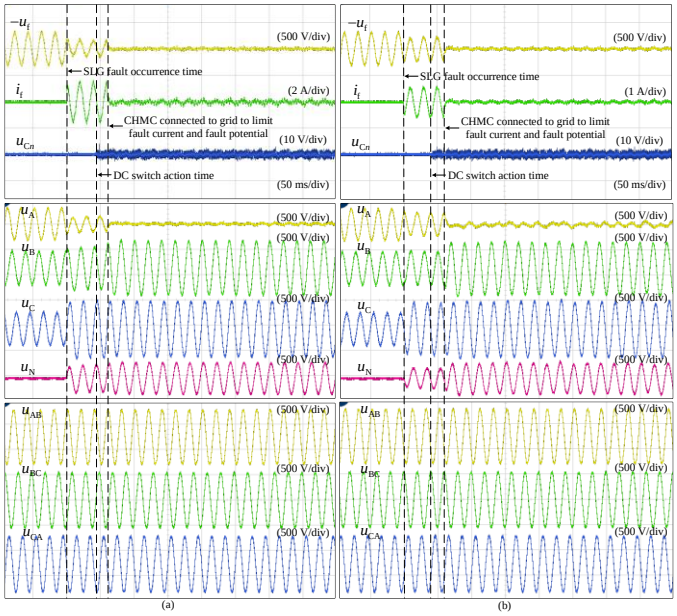


Fig. 18. SLG fault suppression results in the cases of different fault resistances, (a): $R_f = 100\ \Omega$; (b): $R_f = 500\ \Omega$.

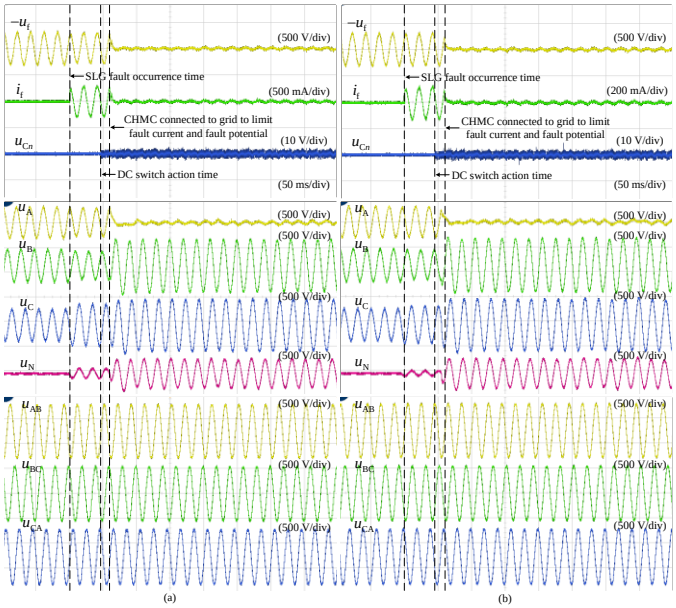


Fig. 19. SLG fault suppression results in the cases of different fault resistances, (a): $R_f = 1000\ \Omega$; (b): $R_f = 5000\ \Omega$.

C. Results Analysis and Discussion

Generally speaking, a desirable CHMC to eliminate SLG faults in the distribution network should have fewer peripheral components, optimized solutions, and reliable results. In this way, it can reduce cost, volume, and capacity while maintaining good performance. This part analyzes the implementation results to clarify the proposed method's performance according to the above-desired needs. Table III summarizes the CHMC implementation results based on the proposed and conventional method [24], where N is the number of H-bridge cascades. It can be seen that since the CHMC of the proposed method only needs to be equipped with a minimized DC source, the overall number of components, capacity, cost, and volume of the system is reduced to 1/N of the conventional method. Moreover, the table summarizes the suppression rate of fault current and potential under 10Ω, 50Ω, 100Ω, 500Ω, 1000Ω, and 5000Ω fault resistance conditions. It can be seen that the results of the proposed and conventional methods are the same in terms of fault suppression. Therefore, not only is the proposed method cost- and size-effective, but it also effectively ensures SLG fault elimination.

TABLE III
SUMMARY OF IMPLEMENTATION RESULTS FOR PROPOSED AND CONVENTIONAL METHODS

Items	Proposed method	Conventional method
No. DC sources	1	N
Total capacity of DC sources	1/N p.u.	1 p.u.
No. rectifier	1	N
Total capacity of rectifiers	1/N p.u.	1 p.u.
No. transformer windings	2	N+1
Transformer capacity	1/N p.u.	1 p.u.
DC power supply system cost	1/N p.u.	1 p.u.
DC power supply system volume	1/N p.u.	1 p.u.
Fault current and potential suppression under $R_f = 10\Omega$	93.16%	93.04%
Fault current and potential suppression under $R_f = 50\Omega$	93.65%	93.62%
Fault current and potential suppression under $R_f = 100\Omega$	94.01%	94.04%
Fault current and potential suppression under $R_f = 500\Omega$	95.29%	95.02%
Fault current and potential suppression under $R_f = 1000\Omega$	95.78%	95.34%
Fault current and potential suppression under $R_f = 5000\Omega$	95.36%	94.78%

VI. Conclusion

This paper presents a novel implementation method of single-phase CHMC for fault suppression to minimize the required DC sources based on separate control of the main and auxiliary modules of the CHMC. Simulation and experimental results demonstrate that the proposed implementation method can allocate separate modules of CHMC to output the required active and reactive power during fault suppression. The main module delivers all required active power and is supplied by only a minimized-capacity DC source. The auxiliary modules are only responsible for providing the required reactive power, which, in turn, can maintain their DC capacitor voltages without any DC source requirement. Accordingly, DC power supply cost is reduced by more than 90%. Noteworthy that the proposed method effectively suppresses the fault current and potential by more than 93% under different fault resistances, ensuring the SLG fault elimination.

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