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ORIGINAL RESEARCH

A fault detection and location algorithm for the LVDC interconnection network in rural area

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Abstract

Low voltage DC (LVDC) microgrids (MGs) can be linked together through an interconnection network to enhance the utilization of their energy resources in remote locations, particularly in rural low-income areas. However, the identification of the fault is challenging due to the fast fault transients and equipment limitations, where there are no sensors and DC circuit breakers (DCCBs) in the lines. To solve this problem, this article proposes a fault detection and location algorithm without requiring extra sensors and DCCBs in lines. The proposed algorithm uses the sensors of the interface converters to detect the fault. Following this, a coordinated current injection method is used to identify the faulty element by coordinating converters with disconnectors. This process employs two strategies "weight check" and "scope check" to minimize the time and the number of actions. The algorithm is robust to various fault impedance, fault types and network topology modifications. The effectiveness of the algorithm is validated through a series of simulation case studies.

1 | INTRODUCTION

As of 2023, approximately 770 million people do not have access to electricity, especially in rural areas of developing countries [1]. Getting access to electricity is part of the pathway to multiple development goals. Low voltage DC (LVDC) microgrids (MGs) are gaining momentum as enablers for small-scale electrification in rural areas [2]. Compared to low voltage AC MGs, they require fewer power conversion stages and simpler control algorithms, thereby having the potential to enhance efficiency and availability [3, 4]. Since individual MG may have poor resilience, geographically close MGs can be integrated through an interconnection network to form a group of networked MGs as shown in Figure 1 [5]. Such a network can provide additional flexibility and reduce the installed generation requirements by sharing available resources in each MG. In addition, the economic allocation of electric energy to loads can be optimized globally to improve efficiency [6].

However, this interconnection network also presents technical challenges, where one of the most critical challenges is to develop a reliable protection scheme. DC circuit breakers (DCCBs) are essential for interrupting DC fault currents, which are more challenging than AC systems due to the lack of a zero-crossing point [7]. Meanwhile, the DC fault current surges rapidly due to the discharge of bus capacitors but fades relatively quickly as power converters switch to the current-limiting mode, which requires the use of high-performance sensors [8]. However, such a network in rural electrification should maintain low costs, which avoids the utilization of extra sensors and DCCBs in lines. Moreover, the protection method should be flexible enough to adapt to new network configurations (e.g. the entry or disconnection of MGs).

Many DC protection methods have been proposed recently, which can be classified into passive and active methods. The most widely used passive methods are traveling-wave (TW)-based methods [9–11] and signal-processing-based methods

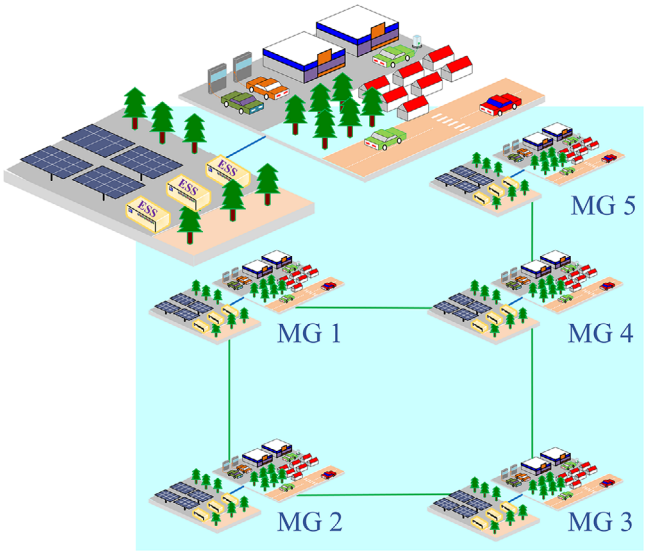

FIGURE 1 Illustration of the LVDC networked MGs.

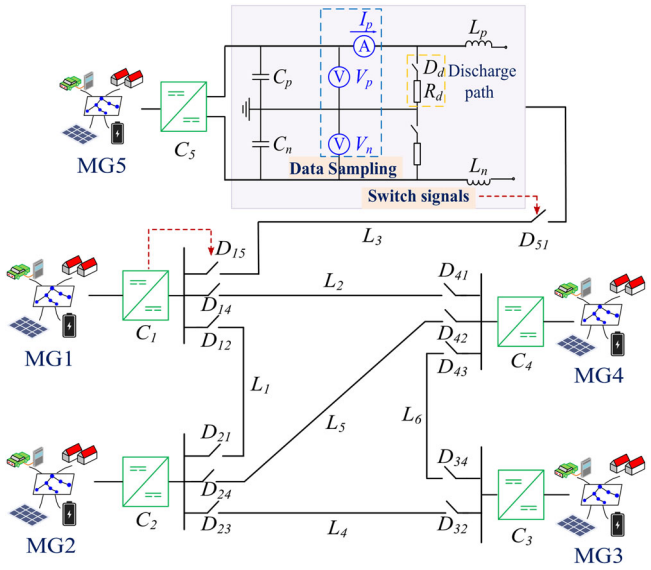

FIGURE 2 The LVDC networked MGs.

[12–17]. However, these methods require high-sampling sensors, thereby leading to increased costs. Machine learning (ML) algorithms, like neural networks [18] and fuzzy logic [19], have been employed for DC grid protection. However, these methods impose great computational demands and more importantly, they have to be tuned for the characteristics of a specific system. The differential protection method is proposed by comparing the current at both ends of the protected zone [20–22]. While this method is independent of fault impedance and network topology, it requires precise current measurement synchronization at different ends of the protected line. The event-based protection method is based on classifying the fault types at each power unit, followed by event identification techniques [23]. This method only requires the local measurements at buses without sensors in lines. However, it could be ineffective for high-impedance faults.

Active methods are mainly based on injecting a known signal and analyzing system response to identify faults [24–26]. However, the additional equipment needed for signal injection may not be permissible due to reliability concerns, and it also contributes to an increase in the total cost. This shortcoming was mitigated in [27] by using the converters as the injection source without additional equipment. However, this method was only effective for pole-to-pole faults. In addition, this method could be time-consuming to implement in complex network topology.

The aforementioned methods are sub-optimal for such networked MGs since they overemphasize the distance precision of fault location or a clearly protected boundary. As a result, they either require extra components (e.g. high sampling sensors, precise synchronization of measurements, or DCCBs), or they are ineffective for certain types of faults or network topology. In such systems, the distance between neighbouring MGs is short (e.g. 500 m in a straight line) [28]. Consequently, the main objective is to identify which bus or line is faulty rather than identifying the exact distance to the fault. Meanwhile, each MG is self-sufficient for short timescales in case of an outage of the interconnection network, allowing the protection methods to interrupt the system operation temporarily, a feature that most of the aforementioned works did not make use of. To fill this gap, this paper proposes a fault detection and location algorithm that exploits the system's features and requires no extra hardware implementation. The main contributions of this paper are:

1) The proposed algorithm only coordinates interface converters and disconnectors without requiring sensors and DCCBs in lines, thereby achieving high cost-effectiveness.
2) The proposed algorithm is robust by the fault types (Pole-to-pole (PP) fault and pole-to-ground (PG) fault) and fault impedance (Low-impedance and high-impedance).
3) A coordinated current injection method is proposed to minimize the number of actions and the time to locate the faulted buses or lines. This method is adaptable to various network configurations, enhancing its flexibility to network topology.

The rest of the paper is structured as follows. Section 2 describes the characteristics of the networked MGs. Next, Section 3 illustrates the proposed fault detection and location algorithm in detail. Section 4 shows simulation results. The paper ends with a conclusion in Section 5.

2 | SYSTEM DESCRIPTION

Without loss of generality, the networked MGs is chosen to include hybrid features of ring, mesh, and radial lines as shown in Figure 2. Since each MG might be designed following different standards, power converters are required as interface devices. The output DC-link capacitors are split into C_p and C_n to permit a bipolar network. The sub-index refers to the positive p and negative n poles, respectively. Three built-in sensors monitor the output voltage and current (e.g. V_p, V_n, and I_p) of the converter. Meanwhile, discharge resistors R_d are employed to discharge C_p and C_n, which is a typical safety feature that

allows a converter to reach a safe state when powered down. Additionally, current limiting reactors $L_{p/n}$ are added as a filter during normal operation and limit the rate of change of the fault current in case of a fault. Each line leaving a bus is equipped with a disconnector at both ends, which permits the connection and disconnection of lines. Notably, there are no sensors and DCCBs in the lines.

The network operation employs a hierarchical design, with power droop regulators integrated into each converter to facilitate power exchange across the interconnection network, in which the power reference is given by the upper controller [28]. In this paper, the upper controller is implemented into one of the converters to coordinate the actions of other devices in the network through a low-bandwidth communication system (e.g. CAN-based low-speed communication [29]). In the case of a fault, the proposed fault detection and location algorithm will be activated, which will be discussed in the following.

3 | PROPOSED FAULT DETECTION AND LOCATION ALGORITHM

The proposed fault detection and location algorithm is achieved by coordinating interface converters and disconnectors. When a fault occurs, converters can detect it and enter in blocking mode to stop feeding the fault current, making the fault current decay to zero. Then, a coordinated current injection method is proposed to locate the fault by checking buses followed by lines. Once the fault is located, it can be isolated by disconnectors and the network can be re-energized to restore normal operation autonomously. The details are described below.

3.1 | Fault detection and interruption

3.1.1 | Fault detection

The algorithm implements two methods to detect both low- and high-impedance faults: under-voltage and network current differential methods. The under-voltage method is a traditional method whose criterion is:

$$V_{p/n} < V_{thd} \tag{1}$$

where $V_{p/n}$ refers to the positive and negative pole voltages as shown in Figure 2. V_{thd} is the under-voltage threshold, which is set as 0.8 pu to take into account voltage excursions due to operational transient [30].

The under-voltage method may fail to detect high-impedance faults since converters might find a steady-state point where $V_{p/n}$ is larger than V_{thd}. To solve this problem, the network current differential method is proposed. According to Kirchhoff's current laws, the total current entering the network through converters should be equal to the current leaving it during normal operation. Thus, the net sum of current should be equal to zero. However, the high-impedance fault can make part of the current divert to the fault, thereby resulting in a significant increase in the net sum of the current. Therefore, the criterion is as follows:

$$I_{total} > I_{th} \tag{2}$$

where I_{total} is the net sum of current and I_{th} is the current threshold, which is given by:

$$I_{th} = \alpha_I \frac{V_{pn}}{Z_{Fm}} \tag{3}$$

where V_{pn} is the total DC-link voltage and Z_{Fm} is maximum fault impedance under consideration. α_I is the safety margin coefficient and is set as 0.9 to include a safety margin of 10%.

I_{total} can be calculated by the master controller after receiving the current measurement I_p from each converter. However, these measurements can be received asynchronously due to varying communication delays. This can cause I_{total} to exhibit temporary fluctuations, potentially leading to large values. To avoid maloperation, a time duration is introduced, which is typically set as between 1.5 and 3 times the communication delay [31]. In this paper, it is set to 2 times the communication delay. Given that the network current differential method depends on calculations, communication, and time duration, the network current differential method inherently introduces a detection delay. Although a delay is not acceptable for low-impedance faults due to the large current arising in the system, it is not a problem for high-impedance faults since the resulting current would not damage the system but rather increase system losses temporarily. It should be noted that only fixed-impedance faults are considered in this paper, which is a common assumption in [32–35].

3.1.2 | Fault interruption

After fault detection, all converters are immediately blocked to protect internal semiconductors and thus stop feeding current to the fault. Consequently, only DC-link capacitors $C_{p/n}$ contribute to the fault current. Both C_p and C_n discharge for a PP fault while either C_p or C_n discharges for PG faults. Thus, the PP and PG faults can be distinguished by comparing $V_{p/n}$ with V_{thd}. A PG fault can be identified if either V_p or V_n are larger than V_{thd}. Otherwise, it is a PP fault. For PG faults, the non-discharging capacitor could impact the fault location in the following. Thus, discharge resistors R_d are used to discharge all DC-link capacitors by closing disconnectors D_d, which are reopened post-discharge.

3.2 | Fault location

After the fault interruption, a coordinated current injection method is proposed to locate the fault. The upper controller can coordinate disconnectors to disconnect parts of the

$$A = \begin{array}{c} \overbrace{}^{L_1}\overbrace{}^{L_2}\overbrace{}^{L_3}\overbrace{}^{L_4}\overbrace{}^{L_5}\overbrace{}^{L_6} \\ D_{12}\,D_{21}\,D_{14}\,D_{41}\,D_{15}\,D_{51}\,D_{23}\,D_{32}\,D_{24}\,D_{42}\,D_{34}\,D_{43} \\ \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{matrix} C_1 \\ C_2 \\ C_3 \\ C_4 \\ C_5 \end{matrix} \end{array}$$

FIGURE 3 Connectivity matrix.

network, enabling the targeted current injection by corresponding converters for fault location. After the current injection, $V_{p/n}$ would rise quickly and remain steady if there is no fault on the segment. Conversely, a low-impedance fault would make $V_{p/n}$ increase slightly and decrease to zero since the injected current would be bypassed by the fault. For the high-impedance fault, $V_{p/n}$ would increase gradually due to the slower fault discharge compared to the current injection charging. Then, $V_{p/n}$ will stabilize at a steady-state point where the charging and discharging processes equilibrate. Therefore, faults can be determined by comparing $V_{p/n}$ with a predefined threshold as follows:

$$V_{p/n} < V_{thl} \tag{4}$$

$$V_{thl} = \alpha_v V_{Fm} \tag{5}$$

where V_{thl} is the voltage threshold for fault location, and V_{Fm} is the maximum DC-link voltage with the faulty part among all fault scenarios. α_v is the safety margin coefficient set as 1.1 to include a margin of 10%.

The coordinated current injection method checks buses first, followed by lines, and ends once the fault is located. All buses can be checked simultaneously by opening all the disconnectors and then injecting current into the DC-link capacitors via each converter. If the fault is on a bus, one of $V_{p/n}$ should be smaller than V_{thl}. The faulty bus is the bus that matches that voltage. Otherwise, all $V_{p/n}$ would be larger than V_{thl} and the line check process starts. Given that all $V_{p/n}$ are larger than V_{thl} due to bus check, lines can be checked by only closing their connected disconnectors and observing $V_{p/n}$, thereby reducing the process of current injections. The faulty line is one in which the corresponding $V_{p/n}$ decreases to smaller than the threshold V_{thb}.

However, line check can be a time-consuming process, especially for networks with redundant lines. Moreover, line check should be adapted to network topology given the potential for modifications in network topology (e.g. the integration of additional MGs). To solve these problems, the connectivity matrix is implemented to determine the sequence of line check, which can be derived and updated easily based on the network topology. Taking the network shown in Figure 2 as an example, the connectivity matrix is illustrated in Figure 3. The rows and columns of the matrix correspond to the system converters and disconnectors, respectively. The value '1' means that a disconnector is connected to the corresponding converter, whereas '0' means that there is no connection between them. Since each

$$\begin{array}{c} \overbrace{}^{L_1}\overbrace{}^{L_2}\overbrace{}^{L_3}\overbrace{}^{L_4}\overbrace{}^{L_5}\overbrace{}^{L_6} \\ D_{12}\,D_{21}\,D_{14}\,D_{41}\,D_{15}\,D_{51}\,D_{23}\,D_{32}\,D_{24}\,D_{42}\,D_{34}\,D_{43} \\ \begin{matrix}\text{First turn}\\ \text{Second turn}\end{matrix}\begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix} \end{array}$$

FIGURE 4 Line matrix.

line has two disconnectors, each pair of columns corresponds to a line.

Based on this matrix, two strategies are proposed to optimize the line check for different networked MGs, which can minimize the number of actions and time of fault location.

3.2.1 | Weight check

Line check process can be optimized by checking multiple lines simultaneously as each converter can check one line at a time. Therefore, it is crucial to maximize the number of converters per check by matching the converters with the lines based on the connectivity matrix. Intuitively, converters connected with fewer lines have higher priority since they have less choice. Taking Figure 2 as an example, the converter with the highest priority is C_5. According to matrix A, the first non-zero element in the fifth row indicates that C_5 is connected to L_3. Thus, C_5 is matched to L_3, and all elements corresponding to L_3 are set as zero to prevent other converters from matching with it. This procedure is repeated for other converters until all converters are paired with a line, after which the match for the first turn of check ends. In the next turn, C_3 selects L_6 and the matching process ends since all lines are chosen.

Based on the above analysis, a line matrix is formed as shown in Figure 4. By performing a sweep over this matrix row by row, line check can be achieved autonomously as shown in Figure 5a.

Assume that there are n converters and n_l lines, and each line takes t_l to be checked. If only one line is checked at a time, the time t_{all} for line check is given as:

$$t_{all} \le n_l t_l \tag{6}$$

On the other hand, the time t_w for line check using the weight check strategy is as:

$$t_w \le \left\lceil \frac{n_l}{n} \right\rceil t_l \tag{7}$$

Compared to (6), t_w is reduced at most n times, which improves the efficiency of line check greatly. However, the check process could still consume a significant amount of time if n_l is much larger than n. To solve this problem, the scope check process is proposed below.

3.2.2 | Scope check

The principle of the scope check is a two-stage process: initially narrowing down the fault's scope to one bus, and then locating

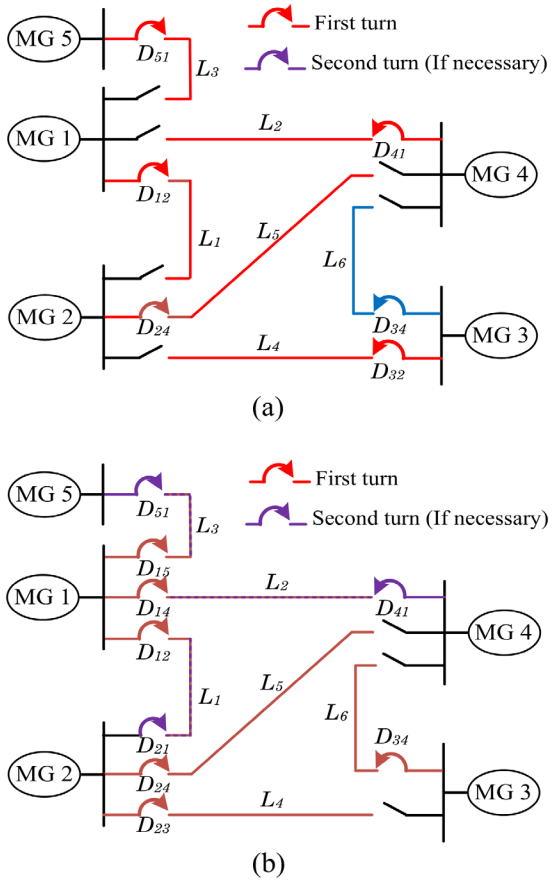

FIGURE 5 Line location. (a) Weight check. (b) Scope check.

the fault on an exact line. To be specific, all lines are chosen at the first turn check by sweeping each row of the connectivity matrix. Taking Figure 2 as an example, all lines emanating from C_1 are selected by sweeping the first row of matrix A. This process is repeated for other converters until all lines are selected as shown in the first turn in Figure 5b. Since all lines are checked at this turn, one of the DC-link voltages would decrease below V_{thl}. The fault is located on one of the lines connected to the bus matching this voltage. Then, all lines connected to that bus are checked by closing the disconnectors on the other terminal converter as shown in the second turn in Figure 5b (assume the fault occurs in L_2). $V_{p/n}$ on the faulty line would decrease below V_{thl}.

The scope check takes at most two turns to locate a fault. Thus, the time required to check the lines t_s is given by:

$$t_s \leq 2t_l \tag{8}$$

It can be seen t_s is independent of n and n_l. Compared to t_w, t_s is smaller if n_l is twice larger than n. Therefore, scope check is suitable for the network where n_L is larger than twice n, while weight check is implemented in other types of networks. By incorporating these two strategies, the line check process can be optimized efficiently. This optimization is adaptable to various network topology since the connectivity matrix can be updated based on the network configuration timely.

3.3 | System reconfiguration

Once the fault is located, all disconnectors are open and converters would inject current to pre-charge DC-link capacitors to achieve a smooth start-up. In case of a PG fault, C_p and C_n could be unbalanced since only one capacitor has increased due to current injection [36]. To address this issue, the discharge resistor would be triggered to discharge $C_{p/n}$ entirely before the pre-charge.

Then, the fault should be isolated. If the fault is on a bus, all disconnectors on that bus should open, and the corresponding converter should be blocked or powered down. If the fault is on a line, only the faulty line's disconnectors should open. This process can be easily achieved based on the connectivity matrix. Afterwards, the interconnection network can be re-energized and the networked MGs can be restored to normal operation. It is noticed that some MGs may be disconnected after fault isolation, which can affect the power-sharing of the network. Thus, the energy management system should adjust the operating power reference accordingly, which is beyond the scope of this paper. A detailed flowchart of the proposed algorithm is presented in Figure 6.

4 | SIMULATION VERIFICATION

The proposed algorithm is tested in the network MGs illustrated in Figure 2 which has a bipolar configuration with a DC-link voltage V_{pn} of 200 V [37]. The dual active bridge (DAB) converter is chosen as the interface converter for demonstration as shown in Figure 7. It is noted that other DC-DC converters with fault-blocking capabilities can be utilized without loss of generality. Switching models are considered for interface converters with a rated power of 5 kW and a switching frequency of 20 kHz [38]. Since the proposed algorithm relies exclusively on sensors embedded within the converters, the sampling frequency of sensors is aligned with the converters' switching frequency. Meanwhile, the impact of noise on sensor accuracy is negligible as converters are typically designed with strategies such as grounding, isolation, filtering, and other noise-reduction techniques to ensure reliable operation [39, 40]. The system operation is based on a hierarchical control, in which the upper controller is implemented into C_1 to manage the exchange of messages and coordination of other devices. A low-bandwidth communications system is incorporated with a delay of 10 ms [29]. Meanwhile, the operation delay for disconnectors is set as 20 ms [30]. Other key system parameters are listed in Table 1.

The proposed algorithm is tailored for faults up to 40 Ω (Z_{Fm} = 40 Ω) [41]. Thus, I_{th} for the network current differential method is set as 4.5 A (0.18 pu) based on (3). The fault location process requires the current injection of the interface converters. For the DAB converter, this can be easily achieved by using a pulse-width modulation only for the H-bridge on the primary side [42]. The peak current I_{peak} is set as 0.8 pu. Among all scenarios, the high-impedance PG fault is the most critical case as it could cause the largest increase in $V_{p/n}$. When Z_{Fm} is considered as 40 Ω, $V_{p/n}$ could increase to 41.8 V approximately.

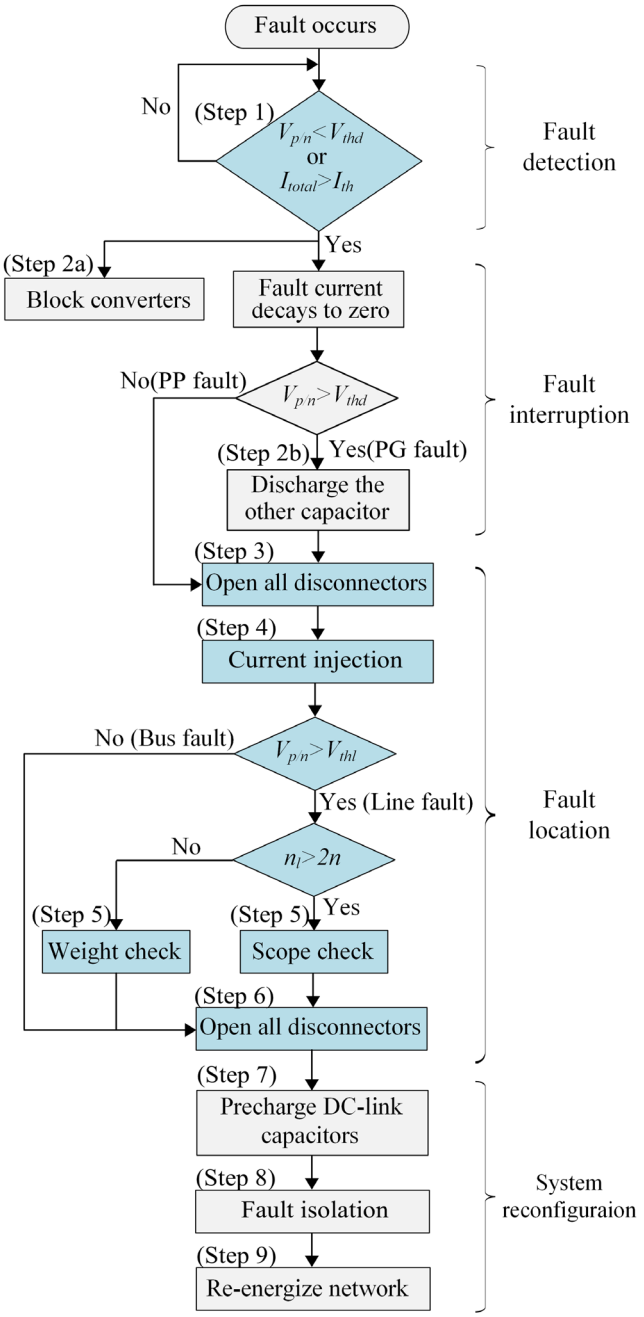

FIGURE 6 Flow chart of the proposed algorithm.

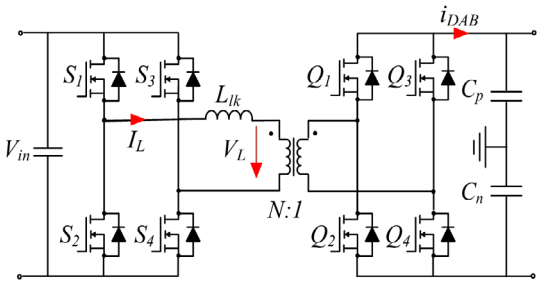

FIGURE 7 Circuit diagram of the DAB converter.

TABLE 1 System parameters.

System parameter	Description	Value
V_{pn}	DC-link voltage	200 V
P	Power range for each converter	0 ± 5 kW
f	Switching frequency	20 kHz
$C_{p/n}$	DC-link capacitor	340 μF
$L_{p/n}$	Current limiting reactor	50 μH
$L_1/L_3/L_4$	Line distance	400 m
$L_2/L_5/L_6$	Line distance	500 m
R_{line}	Equivalent impedance of line	0.565 Ω/km
V_{thd}	Under-voltage threshold	160 V
I_{th}	Current threshold	4.5 A
V_{thl}	Voltage threshold for fault location	46 V

Thus, V_{thl} is set as 46 V (0.46 pu) according to (5). A summary of algorithm parameters is given in Table 1.

A series of simulations under four cases are performed to validate the effectiveness of the proposed algorithm regardless of fault types (PP and PG faults), fault impedance (low impedance and high impedance faults) and network modification. All simulations start from the same steady-state conditions: MG 1 and MG 2 provide 4.5 kW and 4 kW, respectively, while MG 3, MG 4 and MG 5 absorb 4 kW, 2 kW and 2.5 kW, respectively.

4.1 | Case 1: Low-impedance PP fault on L_2

A low-impedance PP fault (0.5 Ω) occurs at the midpoint of L_2 at time 0.1 s as shown in Figure 8. Only V_p is illustrated since V_p and V_n are identical for PP fault. i_{DABi} represents the output current of converter i before the output capacitors as shown in Figure 7, while C_{bi} and C_i correspond to the blocking signal and the current injection signal for current i, respectively. This low-impedance fault leads to a rapid decrease in all V_p, thereby triggering the under-voltage method (step 1). Upon fault detection, converters enter blocking mode to stop feeding fault current (step 2a). As a result, DC-link capacitors C_p and C_n are discharged completely via the fault. Since both V_p and V_n are smaller than V_{thd}, the event is identified as a PP fault.

Then, the fault location process starts. All disconnectors are open, and each converter injects the current to check all buses (steps 3 and 4). A delay of 30 ms is set to ensure that all disconnectors are open before the current injection. Following the injection, all V_p rise above V_{thl}, denoting there is no fault in buses. Consequently, the line check starts. Given the number of converters n exceeds half the total number of lines n_l, the weight check should be chosen. However, to illustrate both strategies, the scope check is used in this case (step 5) while the weight check is used in the following cases. As shown in Figure 8, D_{12}, D_{14}, D_{15}, D_{23}, D_{24} and D_{34} are closed firstly. The drop of V_{p1} to zero indicates that the fault is in one line connected to MG

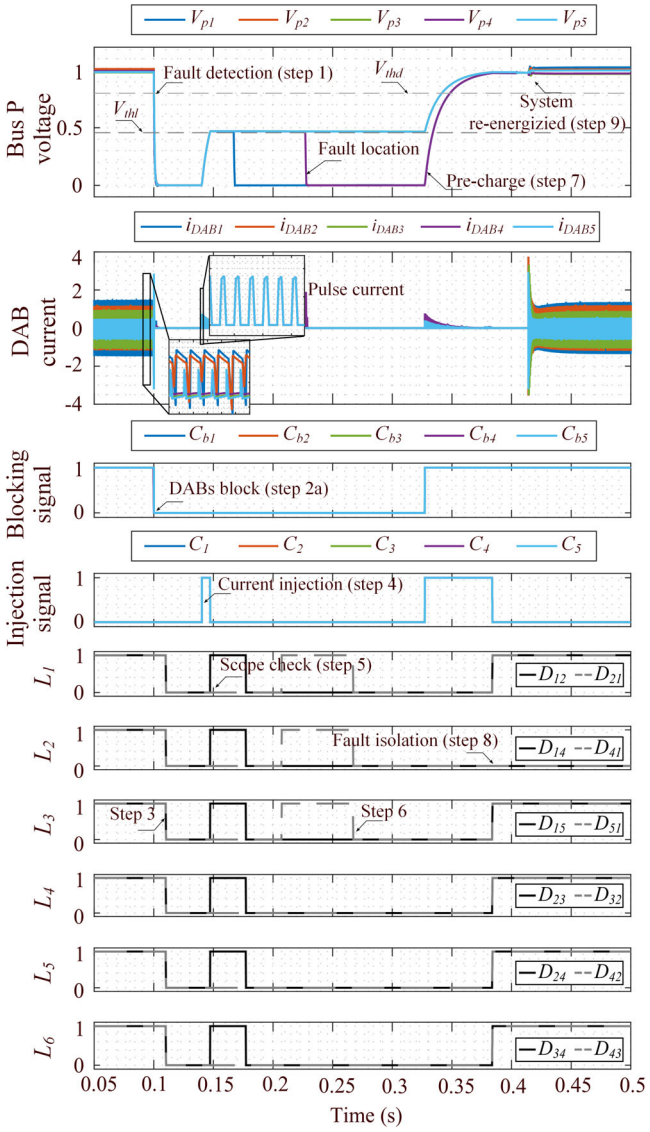

FIGURE 8 Simulation results for the low-impedance PP fault on L_2.

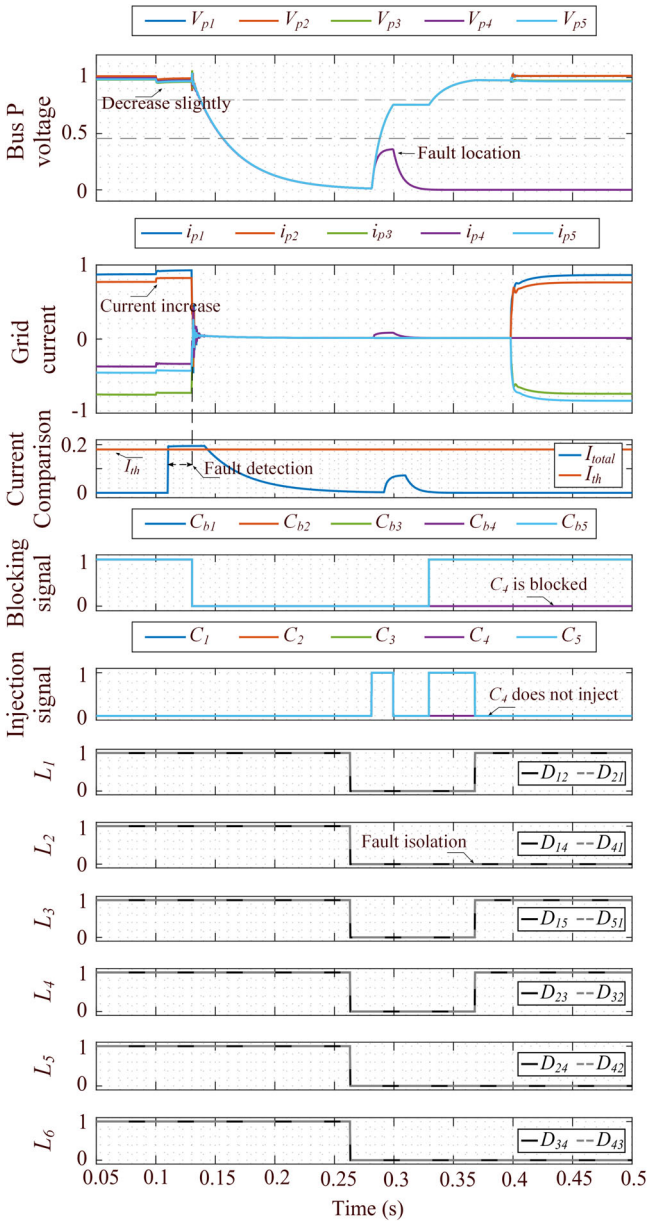

FIGURE 9 Simulation results for the high-impedance PP fault on bus 4.

1. Then, D_{51}, D_{41} and D_{21} are closed at the second turn. The subsequent fall of V_{p4} denotes the fault on L_2.

After the fault location, all disconnectors are opened (step 6), and converters inject the current to pre-charge DC-link capacitors for a smooth start-up (step 7). The fault is then isolated by keeping disconnectors D_{14} and D_{41} open while closing others (step 8). Afterwards, the network can be re-energized and restore normal operations autonomously (step 9).

4.2 | Case 2: High-impedance PP fault on bus 4

A high-impedance PP fault (40 Ω) occurs at bus 4 at time 0.1 s as illustrated in Figure 9. i_{pi} represents the output current of converter i as shown in Figure 2. Unlike the low-impedance fault described in case 1, the high-impedance fault leads to only a slight decrease in V_p. This is attributed to the converters compensating the voltage drop by injecting a larger current. Such a minor drop is insufficient to trigger the under-voltage method. Instead, I_{total} increases greatly to larger than I_{th} to trigger the network current differential method. The fault interruption process is omitted as it is similar to case 1.

Then, the fault location process starts with the bus check. Following the current injection, only V_{p4} increases slowly and then remains constant while other V_p increases continuously. Since V_{p4} is still below V_{thl} after this injection, it indicates that the fault is located at bus 4. Then, all disconnectors are opened and all converters except converter C_4 inject current to pre-charge DC-link capacitors. The remaining procedure follows the process in case 1 except for disconnectors associated with bus 4 are opened for fault isolation. It is noted that the power

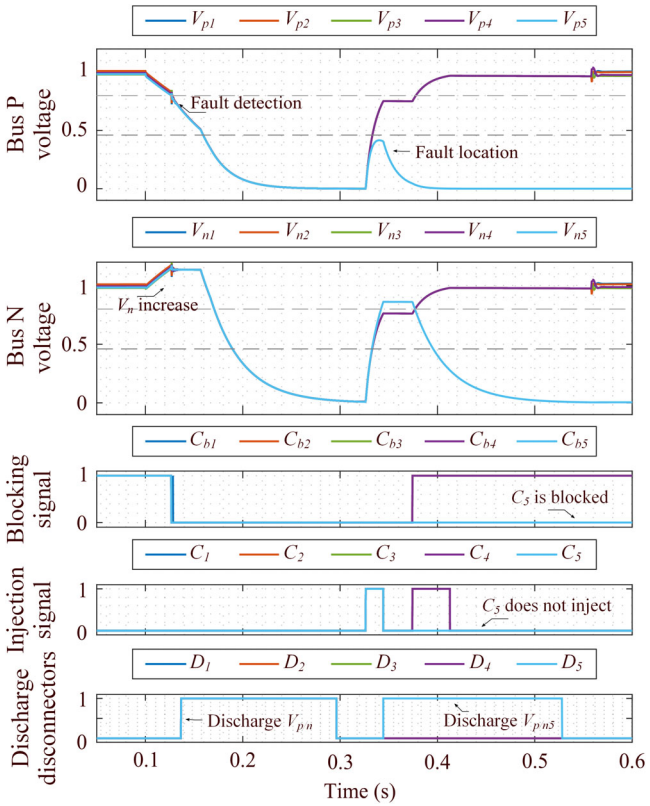

FIGURE 10 Simulation results for the high-impedance PG fault on bus 5.

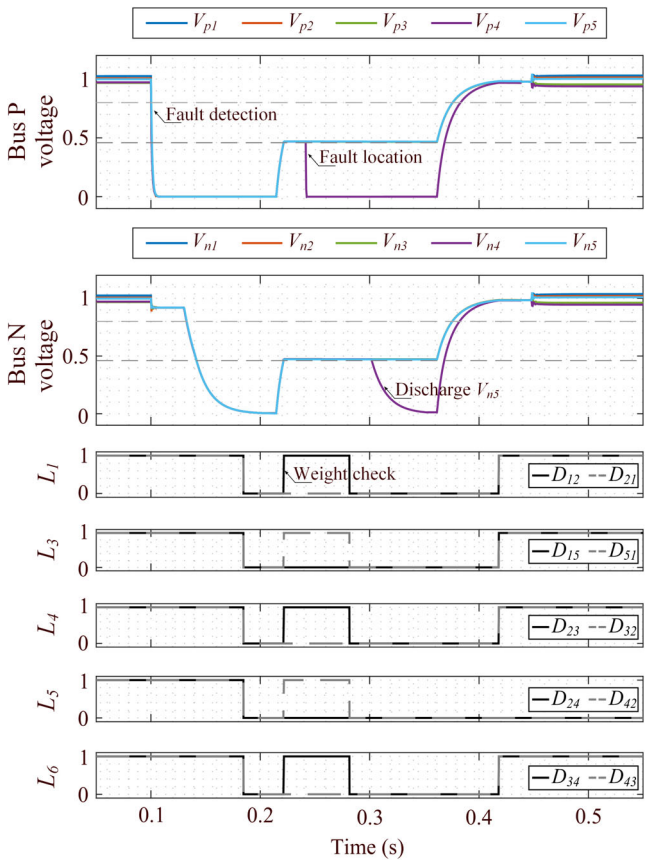

FIGURE 11 Simulation results for the low-impedance PG fault on L_5.

previously absorbed by MG 4 is now taken over by MG 5 since MG 4 has been disconnected.

4.3 | Case 3: High-impedance PG fault on bus 5

The above two cases demonstrate the proposed algorithm's efficacy for both low and high impedance PP faults on buses and lines. This case shows a high-impedance PG fault (40 Ω) at the positive line of bus 5 at time 0.1 s (see Figure 10). Compared to PP faults, this PG fault only makes V_p decrease. This could make converters inject a larger current to maintain V_{pn} at the reference value. As a result, V_n increases while V_p decreases to be smaller than V_{thd}, thus triggering the under-voltage method. Since V_n remains above V_{th}, this incident is identified as a PG fault, thereby prompting the use of discharge resistors by closing D_d to completely discharge C_n. D_d is reopened once the discharge current subsides.

Then, the fault location process starts with the bus check. It can be seen that only V_{p5} increases and then decreases while other $V_{p/n}$ increases continuously after the current injection. The trend of V_{p5} is attributed that the discharge via the high-impedance fault is slower than the charging process for the current injection. Conversely, V_{n5} continues to increase as there is no fault on C_{n5}, which causes V_{pn5} to increase and thus decrease the injected current. Consequently, V_{p5} decreases since the discharge via fault is faster than the charging process. Since V_{p5} remains below V_{thl}, the fault is located on bus 2. The rest step is similar to case 2 except discharge disconnector D_5 is closed to discharge C_{n5} entirely before capacitor pre-charge.

4.4 | Case 4: Low-impedance PG fault on L_5 for modified topology

The final case shows the low-impedance PG fault on a line within a modified network configuration where the line L_2 is removed. A low-impedance PG fault (0.5 Ω) occurs at the midpoint of the positive line in L_5 at time 0.1 s (see Figure 11). This fault leads to a rapid decrease of V_p to zero, while V_n decrease slightly after an oscillation. The under-voltage method is triggered when V_p drops below the V_{th}. The fault interruption follows the same procedures as in case 3 and is therefore not repeated here.

The fault location process then begins with the bus check. Since all DC-link voltages are larger than V_{thl} after the current injection, there are no faulty buses. Therefore, the line check starts by implementing the weight check. With L_2 removed, the connectivity matrix is updated accordingly with the third and fourth columns corresponding to L_2 deleted. This can alter the line matrix as illustrated in Figure 12. According to this line matrix, D_{12}, D_{51}, D_{23}, D_{42} and D_{34} are closed (step 5). The observation that V_{p4} drops to zero indicates that the fault is

TABLE 2 Comparison with the existing methods.

Methods	Extra devices in lines	Communication system	Reliability	Topology flexibility	Speed
Single-ended TW-based method [10]	DCCBs and sensors	No need	Robust	Fail for short lines	Fast
Double-ended TW-based method [43]	DCCBs and sensors	High bandwidth	Robust	Flexible	Fast
ML-based method [44, 45]	DCCBs and sensors	Dependent	Robust	Flexible	Fast
Injection-based method [27]	No need	Low bandwidth	Fail for PG fault	Flexible	Slow
Differential method [21]	DCCBs and sensors	High bandwidth	Robust	Flexible	Fast
Proposed method	No need	Low bandwidth	Robust	Flexible	Medium

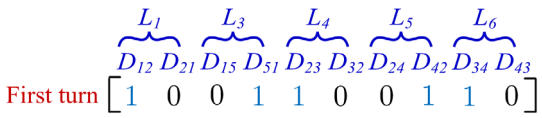

FIGURE 12 Line matrix.

on L_5. The remaining steps for system configuration follow the process in case 3 except for the disconnectors D_{24} and D_{42} are opened for fault isolation.

4.5 | Comparison with the existing methods

The above simulation results demonstrate that the proposed algorithm is robust and effective regardless of fault impedance, types, and network topology. Specifically, high-impedance PP faults can be detected using the network current differential method, while all other fault types are addressed by the under-voltage method. During the fault location process, the coordinated current injection method is capable of locating all fault types. This method incorporates a connectivity matrix that can be adapted to the network topology. Based on this matrix, the algorithm employs two strategies of weight check and scope check to minimize the actions and time for fault location efficiently.

Table 2 presents a comprehensive comparison between the proposed algorithm and other existing methods in terms of the extra devices, communication system, reliability, topology feasibility, and speed. For the communication system, double-ended TW-based methods [43] and differential methods [21] demand high-bandwidth communication systems due to fast operating speed and large amount of transferred data. In contrast, both injection-based methods [27] and the proposed algorithm do not require the rapid operating times that traveling wave and differential protection methods demand, allowing them to be effectively implemented with low-bandwidth communication systems. In terms of speed, TW-based, ML-based, and differential methods can achieve rapid fault detection and location by utilizing straightforward measurements of system conditions during a fault. However, injection-based methods sequentially inject a signal after a fault occurs. This process requires time for the signal injection and subsequent response analysis, inherently resulting in slower fault location speeds. The proposed scheme improves speed by employing two strategies based on a connectivity matrix, making it faster than traditional injection-based methods but slower than methods that rely on direct measurement. Consequently, it is classified as the 'medium' in the speed category.

According to Table 2, the proposed fault detection and location algorithm requires the least equipment, showing high cost-effectiveness. Moreover, the algorithm exhibits robustness against fault impedance and types, as well as flexibility toward network topology variations. While it may not achieve the rapid response times associated with fault transient analysis methods, its speed is sufficiently adequate for systems where each MG can independently maintain a short-term power supply during interconnection network outages. As a result, the proposed algorithm is cost-effective and feasible for the protection of the LVDC networked MGs in rural areas.

5 | CONCLUSION

This paper proposed a fault detection and location algorithm tailored to the interconnection network of the nearby LVDC MGs in rural areas lacking sensors and DCCBs in lines. Without the need for extra sensors and DCCBs in lines, the proposed algorithm coordinates built-in sensors of converters and disconnectors, which underscores its cost-effectiveness. A connectivity matrix is implemented to make this algorithm adapt to network topology modifications. Based on the connectivity matrix, two strategies of scope check and weight check are employed for different network topology. This can reduce the fault location time by almost n times compared to the conventional method, where n is the number of buses. The algorithm has been validated through a series of simulation studies, demonstrating its robustness for fault types (PP or PG fault), fault impedance (low-impednce and high-impedance), and network topology modifications. As a result, the proposed algorithm emerges as a promising protection solution for LVDC networked MGs in rural areas. In future work, the proposed scheme will be coordinated with the protection systems of individual microgrids to develop a comprehensive protection strategy for LVDC networked MGs.

AUTHOR CONTRIBUTIONS

Chengwei Liu: Methodology; resources; software; validation; visualization; writing—original draft; writing—review and editing. **Joan Marc Rodriguez-Bernuz**: Resources; supervision;

visualization; writing—original draft. **Di Liu**: Resources; validation; visualization; writing—original draft. **Saizhao Yang**: Visualization; writing—original draft. **Yitong Li**: Resources; validation; writing—original draft. **Qiteng Hong**: Writing—original draft. **Adrià Junyent-Ferré**: Methodology; supervision; writing—original draft.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interests.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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