Topology and Control of an Arm Multiplexing MMC with Full-Range Voltage Regulation

Yi Wang, *Member*, *IEEE*, Zhen Zhang, *Student Member*, *IEEE*, Yutao Xu, Yuhua Gao, *Student Member*, *IEEE*, Lie Xu, *Senior Member*, *IEEE*, Xiaoqi Xu, *Student Member*, *IEEE*

***Abstract*— The compact design of the modular multilevel converter (MMC) has drawn great attention due to the miniaturization requirement of the distant offshore wind power integration system. Only 50% submodules (SMs) in the phase leg are inserted at any instant, which results in lots of redundant SMs in the conventional MMC. Combining modular structure with device series switches (DSs) can effectively reduce the number of modules by improving their utilization. However, a fixed modulation ratio is necessary for some compact topologies to balance arm energy, and additional complicated control algorithms are required to obtain a limited voltage regulation range. This paper develops an arm multiplexing MMC (AM-MMC) with multiple arms, in which the SMs in the middle arms are assigned to operate in time-division multiplexing (TDM) modes. A multiplexed nearest level modulation (MNLM) method applied to the AM-MMC is presented to achieve full-range voltage regulation without additional energy balance control. To ensure reliable operation of TDM modes, the structure design and zero-voltage switching scheme of arm selection switches are given in detail. The feasibility and performance of the developed AM-MMC has been demonstrated on a small-scale 150V/2.75kW experimental prototype and an 85MVA/ ±35kV AM-MMC HVDC simulation system based on Matlab/Simulink.**

***Index Terms*—Modular multilevel converter (MMC), High-voltage direct current (HVDC), offshore wind power integration, compact design, arm multiplexing MMC**

I. Introduction

Modular multilevel converter (MMC) is considered as the most preferable topology for high power applications due to its modularity and scalability [1], [2]. Many HVDC projects using MMC have emerged in recent years for the connection of large onshore and offshore wind farms. However, the modularity of the MMC is restricting its further extensions, due to its large volume and weight in HVDC substations caused by numerous modules and floating capacitors [3]. With the fast development of offshore wind farms and flexible grid interconnection, it has become an increasing challenge to minimize the size and weight of the MMC [4], [5].

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Yi Wang, Zhen Zhang, Yuhua Gao, and Xiaoqi Xu are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Baoding 071003, China (e-mail: yi.wang@ncepu.edu.cn; zhen.zhang@ncepu.edu.cn; yuhua.gao@ncepu.edu.cn; xuxiaoqi@ncepu.edu.cn).

Yutao Xu is with the Electric Power Research Institute of Guizhou Power Grid Co. Ltd (e-mail: xuyt@gzsyy.csg.cn).

Lie Xu is with the Dept. of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, G1 1XW, UK (e-mail: lie.xu@strath.ac.uk).

The present research on lightweight MMC mainly focuses on two aspects. One is to decrease the capacitance of submodules (SMs) through supplementary control and the other is to make the MMC structure more compact through topology innovation. The floating capacitors typically account for more than 50% of the total size and weight of the SMs [6], [7], which first came to attention for the lightweight MMC. Several methods for capacitance reduction have been presented, including minimizing the circulating current [8], [9], injecting the harmonic voltage [10], using the novel SM [11], and adopting the arm inductor switching control [12]. As the AC and DC power exchange in the single arm and series connection of numerous capacitors in each arm are also the leading factors to determine the capacitance value, and therefore, large floating capacitors in SMs are still inevitable to limit DC voltage variations within an acceptable range [13]. In addition, these capacitance reduction approaches often bring side effects, such as increases of devices, arm currents and DC voltage ripples [14], [15].

Moreover, the MMC still consists of a total of 6N SMs and their utilization is around 50%. The compact design of the MMC structure appears to be the research trend for achieving a greater deduction of the floating capacitors. Some modified SM structures have been proposed based on the half/full bridges to reduce the number of switching devices in MMC [16], [17], but they only make limited contribution to the lightweight of the MMC. Recently, several hybrid multilevel converter topologies are presented combining the features of the two-level VSC and MMC topologies [18].

The alternate arm multilevel converter (AAC) has been proposed and analyzed in [19]–[21], which uses a hybrid cascade of the full-bridge chain links (FBCLs) and device series switches (DSs) as the bridge arm. As the non-conducting arm can be used to share the voltage across its open switches [19], the number of series devices can be reduced. The alternate conduction of the switches in different arms can approximately decrease the maximum output voltage of the FBCLs by half compared with the conventional MMC [20], thereby reducing the number of SMs. However, the AAC can only remain energy balancing at the fixed modulation ratio of $4/\pi$, and a large DC-side filter is necessary to smooth the six-pulse ripples in the DC current. An improved structure, the extended overlap AAC (EO-AAC), has been proposed to operate at a wider modulation ratio with smooth DC currents, but it increases the number of devices [22]. Then a multiplexing AAC (M-AAC) was developed in [23], which first introduced the idea of time-division multiplexing (TDM) for switches to further reduce the

number of SMs. However, the strict energy balance requirement also makes them only work at a fixed modulation index, which cannot meet the flexible regulation requirement of HVDC.

Another approach of compact design is the hybrid cascaded multilevel converter (HCMC), which introduces FBCLs at the AC side of the converter as active filters to attenuate the voltage harmonic. For the same DC link voltage, the number of SMs and floating capacitors is only one quarter of that of the conventional MMC [24], [25]. But for the series connection of large numbers of devices in the arm, dynamic device voltage balancing is required, and its capacity expansion is less flexible. Moreover, the total losses of the HCMC are relatively high compared with the AAC and MMC. The HCMC is a variant of the two-level VSC, and naturally, the three-level VSC and the five-level VSC can be improved in the same way. Then two developed topologies are the hybrid three-level converter (H3LC) and the hybrid five-level converter (H5LC) [26], [27]. By introducing the zero-state voltage, the withstand voltage of chain links in the H3LC is reduced from 50% of the DC-side voltage to 25%. Hence, the number of full-bridge submodules (FBSMs) in the conduction path can be reduced by half to obtain low conduction losses. Furthermore, two additional voltage levels are added by flying capacitors in the H5LC, and the device numbers and power losses will be further optimized.

The topology of the parallel hybrid converter (PHC) is proposed in [28], [29]. The FBCLs play the role in generating the multilevel voltage waveform, which is modified into the AC output voltage by controlling the series switches. This converter has the same number of SMs as the HCMC, and also suffers from high voltage stress on the series connected devices in the H-bridge. In addition, it requires single-phase transformers to provide the necessary isolation. Compact topologies based on the similar idea with FBCLs, DSs and single-phase transformers have been presented, including H-Bridge hybrid modular converter (HBHMC) [30], hybrid-legs bridge converter (HLBC) [31], and series bridge converter (SBC) [32]. The HBHMC and HLBC change the connection types between the FBCLs and the H-bridge shaping circuit. These topologies are often described in a single-phase structure. Then the phase units can be connected in series or parallel to form a three-phase structure, which is suitable for the applications with high-voltage & low-current or low-voltage & high-current. However, more complicated energy controls are essential for these converters.

For these newly proposed converters, while reducing the semiconductor devices and capacitors, other components have to be introduced, such as single-phase transformers and large DC-side capacitors, which offsets the lightweight effect. A switched mid-point modular multilevel converter (SMPC), without additional requirements on transformers or DC-side capacitors has been presented, which adopts a three-arm structure, and periodically changes the position of AC port through a pair of device series switches (DSs) [33]. However, the SMPC can only maintain energy balance at a fixed modulation ratio of π/2. Then an additional energy control algorithm and a strict module quantity allocation have to be implemented to obtain a limited voltage regulation range of ±10%. Furthermore, the design and reliable switching of DSs is not considered in SMPC.

The arm multiplexing MMC (AM-MMC) developed in this paper aims to improve module utilization by introducing multiplexed arms operating in time-division multiplexing (TDM) modes. By employing a modified nearest level modulation (NLM) scheme, AM-MMC can achieve modulation performance equivalent to the conventional MMC, thus ensuring a full-range voltage regulation. The according configuration and modulation methods have good scalability, and can be extended to multi-arms structures. For the practical application of this compact AM-MMC, the structure and switching strategy of arm selection switches without dynamic voltage balancing problem are further investigated.

The rest of this paper is organized as follows. Section II develops the unified structure of the AM-MMC and chooses the promising three-arm structure to investigate. Then a multiplexed nearest level modulation (MNLM) method with full-range voltage regulation is presented in Section III. The capacitor voltage fluctuation and circulating current are analyzed sequentially. In Section IV, the design and control scheme of the arm selection switches are discussed. The detailed power loss analyses and comprehensive comparison with other compact topologies are carried out in Section V. Section VI verifies and analyzes the AM-MMC with the MNLM scheme through the experiment and simulation. The conclusions are summarized in Section VII.

II. The Unified AM-MMC Topology

By increasing the number of multiplexed arms, the module utilization rate can be improved to reduce the number of modules effectively. The SMPC is a newly proposed topology comprising of three arms per phase, and it differs from the conventional MMC in working principle, module configuration, and energy characteristics [33]. Each arm of the SMPC is controlled respectively to output fixed periodic waveforms, which will be superimposed to generate complete sine waveforms, as shown in Fig.1. Although the SMPC can form the stable DC-side voltage by inserting constant number of SMs in the phase leg and does not require additional components, a fixed modulation ratio of π/2 is necessary to achieve energy balance under the asymmetrical voltages and currents between three arms. This further leads to a limited range of voltage regulation. The SM stacks are used as voltage sources, and need precise quantities to generate modulation waveforms including negative voltages. Without taking voltage regulation into consideration, the expressions for the number of SMs in each arm of the SMPC are

$$\begin{cases} N_{\text{SMPC\_au/al}} = N_{\text{HBSMs}} + N_{\text{FBSMs}} = \dfrac{U_{\text{dc}}}{2U_{\text{c}}} + \dfrac{(m_{\text{e}}\text{-}1)U_{\text{dc}}}{2U_{\text{c}}} \\ \qquad\qquad = 0.5N + 0.2854N \\ N_{\text{SMPC\_am}} = N_{\text{HBSMs}} = \dfrac{m_{\text{e}}U_{\text{dc}}}{2U_{\text{c}}} = 0.7854N \end{cases} \tag{1}$$

where N_{SMPC_au}, N_{SMPC_am} and N_{SMPC_al} are the numbers of SMs in the upper, middle, and lower arms respectively in the SMPC phase-*a* leg, N_{HBSMs} and N_{FBSMs} are the numbers of half-bridge submodules (HBSMs) and FBSMs, U_{dc} is the DC bus voltage, U_c is the rated capacitor voltage of SM and m_e is the modulation ratio with the fixed value of $\pi/2$.

Actually, it is difficult to configure a non-integer number of SMs in multiple arms. Moreover, the structure with more arms may offer superior lightweight potential. The principle and design method of the SMPC are only applicable to the three-arm structure and may not be easily scalable. This is due to the difficulty in achieving energy balance and waveform allocation for structures with more than three arms.

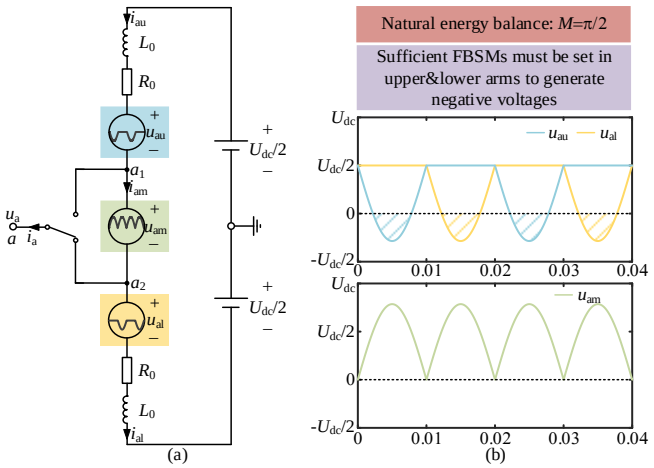


Fig. 1. (a) Structure schematics and (b) modulation waveforms of the SMPC.

To further minimize the number of SMs, an arm-extensible topology is proposed. A three-arm AM-MMC is presented first by introducing a middle arm operating as TDM mode. The AM-MMC can be modulated in a manner equivalent to a conventional two-arm MMC. Taking phase-*a* as an example, the conventional MMC consisting of two arms per phase leg is shown in Fig. 2(a). These two arms each comprises *N* SMs and an inductor L_0 in series, and they are modulated separately to synthesize *N*+1 level output voltage. Based on the NLM scheme, the inserted SM number in the upper/lower arm (N_{au}/N_{al}) can be expressed as

$$\begin{cases} N_{au} = \dfrac{N}{2} - \text{round}\left(\dfrac{u_a^*}{U_c}\right) \\ N_{al} = \dfrac{N}{2} + \text{round}\left(\dfrac{u_a^*}{U_c}\right) \end{cases} \tag{2}$$

where round (*x*) is the function of rounding the nearest integer, U_c is the rated capacitor voltage of SM, u_a^* is the reference voltage of phase-*a*.

According to (2), there are totally *N* SMs inserted in each phase leg of MMC at any instant, which means 50% SMs are usually bypassed. This indicates a poor utilization of the SMs. In addition, when the inserted SM number of one arm is greater than *N*/2, that of the other arm must be less than *N*/2. For example, while $0<u_a^*<U_{dc}/2$, $N_{au}<N/2$ and $N_{al}>N/2$. In this stage, if some of the bypassed SMs in the upper arm are inserted in the lower arm, the total SM number in each phase leg can be reduced accordingly. For this purpose, a compact MMC topology with arm multiplexing modes (AM-MMC) is developed, which is shown in Fig. 2(b). As seen, each phase leg of the AM-MMC consists of an upper, a middle and a lower arm, while only the upper and lower arms have inductors. The middle arm operates at TDM modes which can be connected to the upper arm or the lower arm using the arm selection switchers to ensure the upper and lower arms have sufficient SMs to generate the required arm voltage. For the AM-MMC shown in Fig. 2(b), the number of SMs for all the three arms can be set as *N*/2. Thus, there are 1.5*N* SMs in total per phase, which is 25% less than the conventional MMC having 2*N* SMs per phase.

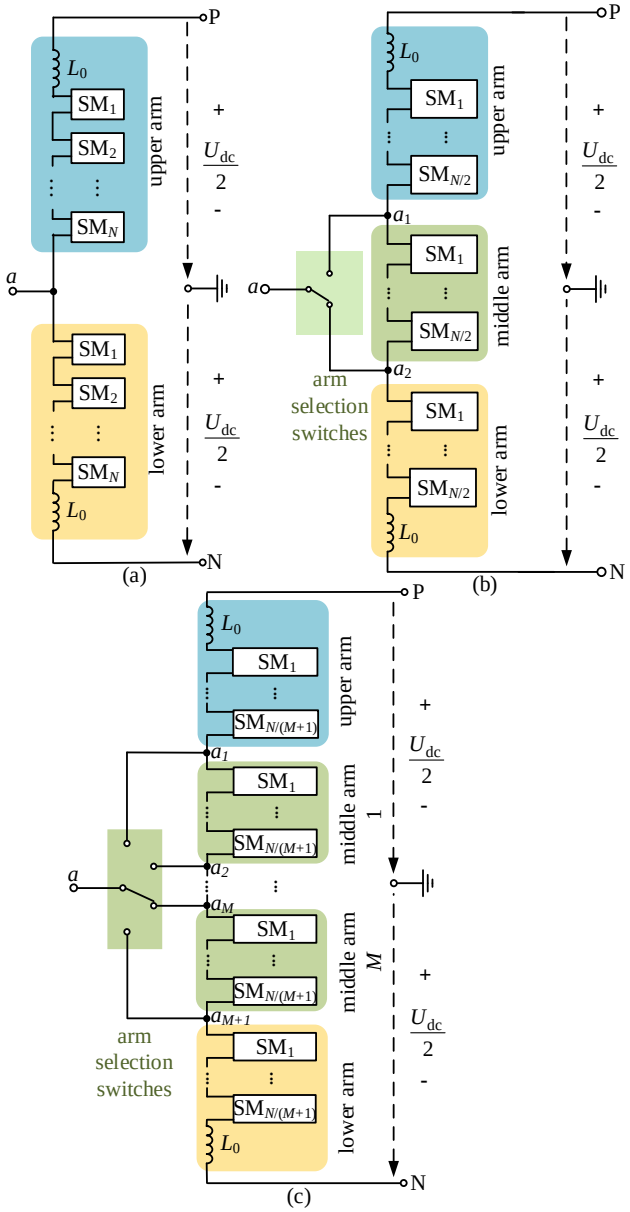


Fig. 2. Structure schematics of the single-phase MMC. (a) conventional MMC. (b) AM-MMC with one middle arm. (c) the unified AM-MMC.

The concept of arm multiplexing can be extended to AM-MMC with multiple middle arms, and a unified structure is shown in Fig. 2(c). The phase leg of the unified AM-MMC consists of one upper arm, *M* middle multiplexed arms and

one lower arm, i.e., totally M+2 arms per phase. The middle arms can be divided into two groups by conducting one of the arm selection switches to supplement the SMs of the upper and lower arms respectively. When M middle arms are all multiplexed to the upper or lower arm, there should be totally N SMs in these M+1 arms for generating maximum voltage level NU_c. Thus, each arm needs to have $N/(M+1)$ SMs. Therefore, the total number of SMs in M+2 arms per phase is:

$$N_t = \frac{M+2}{M+1}N \tag{3}$$

For the AM-MMC, the number of the inserted SMs in each phase leg is still fixed at N, thus the SM utilization rate is:

$$\lambda = \frac{N}{N_t} = \frac{M+1}{M+2} \tag{4}$$

Compared with the conventional MMC, the reduction of SMs per phase by the proposed AM-MMC is

$$N_d = 2N - \frac{M+2}{M+1}N = \frac{M}{M+1}N \tag{5}$$

According to (4), the SM utilization rate is only 50% for the conventional MMC (M = 0), and is increased to 66.7% for the AM-MMC with one middle multiplexed arm (M=1). Consequently, the total number of SMs will decrease significantly with the increasing of M. However, as shown in Fig. 2(c), each phase of the AM-MMC requires M+1 arm selection switches for the multiplexing mode switching of the M middle arms. Considering the feasibility of practical projects and the complexity of arm selection switches, this paper only develops the performance of the AM-MMC with one middle multiplexed arm, i.e. M=1, as shown in Fig. 2(b).

Different from the idea of waveform superposition in the SMPC, the arm-extensible AM-MMC is modulated according to the equivalent upper and lower arms, based on the idea of arm multiplexing. The modulation strategy of the conventional MMC can be easily adapted and transplanted. Additionally, the number of SMs per arm can be an integer value and equal, as shown in (3). This adaptability makes the AM-MMC is well-suited for implementation in various engineering applications.

III. Modulation Scheme of AM-MMC with Full-range Voltage Regulation

When dealing with the abnormal condition of voltage drop, VSCs with full-range voltage regulation will have better application prospects. The SMPC only allows a limited voltage regulation range of ±10% by injecting double frequency component. However, the AM-MMC can be modulated equivalent to a conventional MMC, thereby exhibiting similar energy balance principle and voltage regulation range. An improved AM-MMC modulation strategy, considering the TDM of middle arms, is presented based on a comprehensive analysis of its operating principle.

A. Operation principle

This paper takes phase-a as an example for the modeling and control studies of the AM-MMC. Figs. 3(a) and (b) show the modes of the middle arm multiplexed to the upper arm (mode I) and to the lower arm (mode II), respectively. These two modes are used to generate waveforms for half a cycle, with mode I for positive voltage and mode II for negative voltage.

K_{a1} and K_{a2} are the arm selection switches of phase-a, which conduct alternatively to select the arm multiplexing modes. When K_{a1} is turned off and K_{a2} is turned on, the middle arm is multiplexed to the upper arm to compose an equivalent upper arm. While flipping these two switches, i.e., K_{a1} is turned on and K_{a2} is turned off, the middle arm moves to the lower equivalent arm at this stage. These two multiplexing modes can be represented by a switching function S_a as

$$S_a = \begin{cases} 1 \text{ (multiplexing mode I)} & 0 < \omega t \le \pi \\ 0 \text{ (multiplexing mode II)} & \pi < \omega t \le 2\pi \end{cases} \tag{6}$$

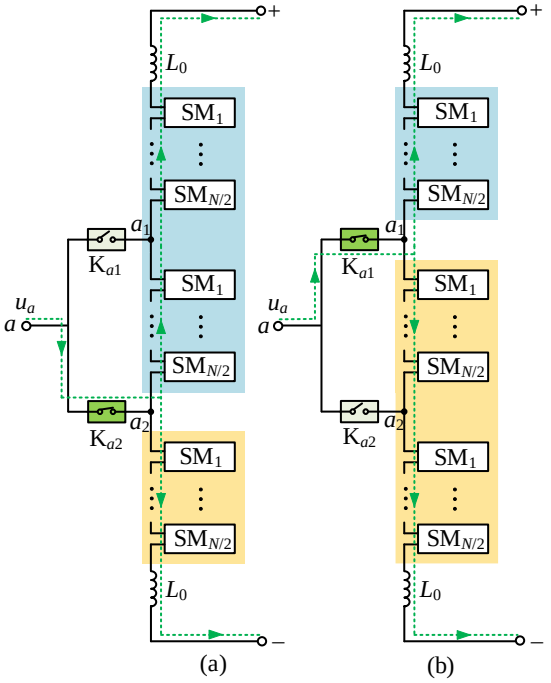


Fig. 3. Two multiplexing modes of the phase-a leg in the AM-MMC. (a) mode I. (b) mode II.

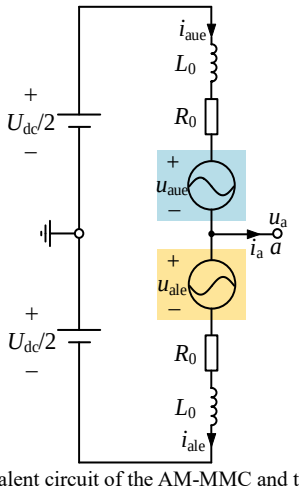


Fig. 4. Phase-a equivalent circuit of the AM-MMC and the conventional MMC.

From two multiplexing modes in Figs. 3, the modulation

scheme of the conventional MMC can be employed to the equivalent upper and lower arms of the AM-MMC, thereby maintaining same equivalent circuits of AM-MMC and MMC, as shown in Fig. 4. Similar with the conventional MMC, while neglecting the voltage drop of the arm inductance L_0 and equivalent arm resistance R_0, the voltages of equivalent arm u_{aue} and u_{ale} can also be expressed as

$$\begin{cases} u_{aue} = \dfrac{U_{dc}}{2} - u_a \\ u_{ale} = \dfrac{U_{dc}}{2} + u_a \end{cases} \tag{7}$$

where U_{dc} is the DC bus voltage and u_a is the converter phase-a output voltage. From (7), u_a can be obtained as

$$u_a = \frac{u_{ale} - u_{aue}}{2} \tag{8}$$

Equation (8) indicates that the equivalent upper and lower arms of the AM-MMC can be modulated separately to synthesize the output phase voltage.

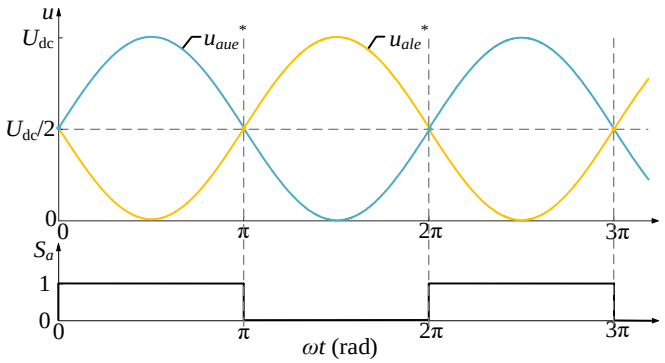


Fig. 5. Principle of determining the two multiplexing modes of AM-MMC.

The reference voltage waveforms u_{aue}^* and u_{ale}^* are shown in Fig. 5, and the multiplexing modes of middle arm can be determined accordingly. During the stage of $u_{aue}^* > U_{dc}/2$ and $u_{ale}^* < U_{dc}/2$, the inserted SMs number of the upper equivalent arm is greater than $N/2$, which requires the middle arm to operate in mode I. Likewise, during the stage of $u_{aue}^* < U_{dc}/2$ and $u_{ale}^* > U_{dc}/2$, the middle arm should be operated in mode II.

Furthermore, the multiplexing mode only needs to be switched twice in one cycle. Hence, the operating frequency of the arm selection switches is the fundamental frequency of the output voltage, which avoids the problem of the high switching loss and high-speed switching synchronization of the conventional device series switches in the VSC.

B. Multiplexed nearest level modulation

Fig. 6 illustrates the concept of the modulation according to the equivalent upper and lower arms in the AM-MMC, which takes the 11-level output voltage as an example (N = 10). According to the required equivalent voltages u_{aue}^* and u_{ale}^*, the inserted SM numbers of the equivalent upper and lower arms N_{aue} and N_{ale} are calculated at first. Using a staircase waveform to approximate the desired wave, and considering the rated capacitor voltage U_c, the number of the inserted SMs in the equivalent upper and lower arms N_{aue} and N_{ale} can be obtained as

$$\begin{cases} N_{aue} = \text{round}(\dfrac{u_{aue}^*}{U_c}) = S_a N_{am} + N_{au} \\ N_{ale} = \text{round}(\dfrac{u_{ale}^*}{U_c}) = (1 - S_a) N_{am} + N_{al} \end{cases} \tag{9}$$

where N_{aue} and N_{ale} are the numbers of the inserted SMs in the equivalent upper and lower arms respectively, N_{au}, N_{am} and N_{al} are the numbers of the inserted SMs in the actual upper, middle and lower arms, respectively.

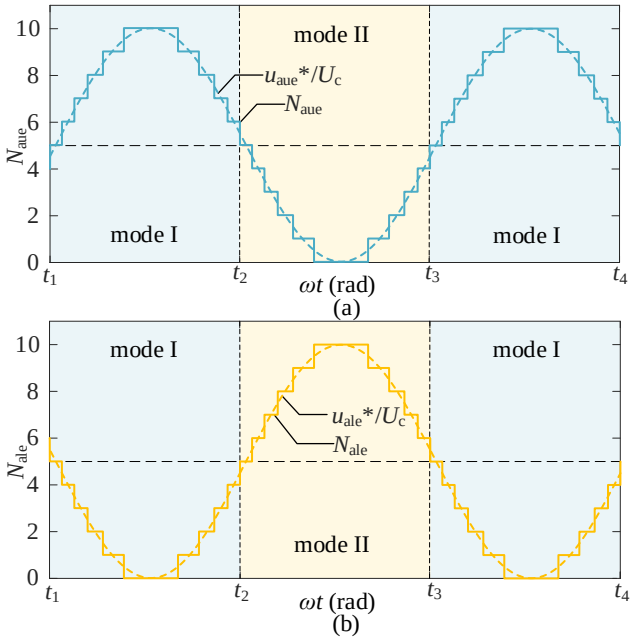


Fig. 6. Modulation principle for the MNLM method.

The multiplexing mode of the middle arm can be determined after obtaining N_{aue} and N_{ale}. Since the sum of N_{aue} and N_{ale} needs to be fixed at a constant value N to maintain same DC bus voltage of different phase legs, the multiplexing mode of the middle arms can be determined by either N_{aue} or N_{ale}. This paper uses N_{aue} as the mode selection variable, and the multiplexing mode switching principle is given as follows.

1) If $N_{aue} > N/2$, the middle arm operates in mode I, i.e., multiplexed to the upper arm, so that the equivalent upper arm has enough SMs to generate the voltage levels greater than $N/2$.

2) If $N_{aue} < N/2$, the middle arm operates in mode II, i.e., multiplexed to the lower arm for generating enough output levels.

3) If $N_{aue} = N/2$, while the previous level $N_{aue}' < N_{aue}$, such as at the instant of t_1 and t_3 in Fig. 6, the middle arm changes from mode II to mode I. And while the previous level $N_{aue}' > N_{aue}$, such as at the instant of t_2 and t_4, the middle arm changes from mode I to mode II.

It can be seen from Fig. 6 that the multiplexing mode only changes while N_{aue} steps to $N/2$, and the arm selection switches need to be flipped at this instant. Therefore, the switching frequency of these switches is the fundamental frequency of the output voltage.

The capacitor voltages in each arm can also be balanced using the capacitor voltage sorting method, as shown in Fig. 7. However, the capacitor voltage sorting of the AM-MMC is proceeded in the equivalent upper and lower arms separately, which varies with the multiplexing modes. If the middle arm is operating in mode I, there are N SMs in the equivalent upper arm and $N/2$ SMs in the equivalent lower arm. The SMs in the upper and middle arms will rotate together according to their voltage sorting sequence in the equivalent upper arm. Whereas for mode II, the SMs in the middle arm will participate in the rotating according to the voltage sorting sequence in the equivalent lower arm. Like the conventional MMC, the voltage sorting in ascending/descending order depends on the direction of the corresponding arm currents (i_{au}, i_{al}).

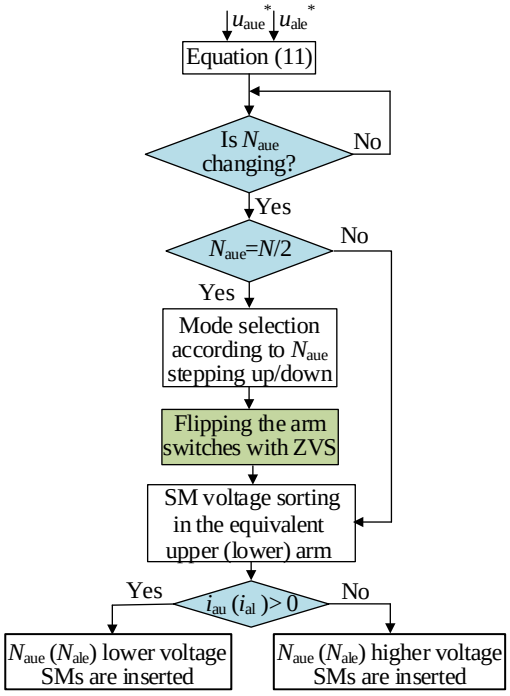


Fig. 7. Capacitor voltage balancing method.

Furthermore, the flipping of the multiplexing switches for mode changing can be implemented under zero voltage to avoid the complicated dynamic voltage balancing requirements. The zero-voltage switching (ZVS) scheme of the multiplexing mode will be illustrated in the subsequent section.

The middle arm always belongs to one equivalent arm, and completes capacitor voltages balancing in the equivalent upper/lower arm. By balancing capacitor voltages, the middle arm periodically exchanges energy with the upper and lower arms to ensure energy balance among these three arms. Different from SMPC, the AM-MMC does not employ a fixed modulation waveform in its upper, middle, and lower arms. To achieve energy balance, the selection of submodules is performed based on capacitor voltage sorting, rather than their association with a specific arm. Hence, the waveform of each arm of the equivalent arm is irregular. But the overall voltage of equivalent arm always corresponds to the modulation sine wave.

C. Analysis of arm power fluctuation and circulating current

With the proposed MNLM, the AM-MMC can be equivalent to a structure with upper and lower arms, as shown Fig.4, and has the same voltage and current expressions as the conventional MMC. Providing that circulating currents are suppressed, the currents of equivalent upper and lower arms can be expressed as

$$\begin{cases} i_{aue} = \dfrac{I_{dc}}{3} + \dfrac{I_m}{2}\sin(\omega t - \varphi) \\ i_{ale} = \dfrac{I_{dc}}{3} - \dfrac{I_m}{2}\sin(\omega t - \varphi) \end{cases} \tag{10}$$

where i_{aue} and i_{ale} are currents of equivalent upper and lower arms respectively. I_{dc} is the DC side current, I_m and φ are amplitude and initial phase angle of AC side current.

The voltages of equivalent upper and lower arms (u_{aue} and u_{ale}) can be expressed as

$$\begin{cases} u_{aue} = \dfrac{U_{dc}}{2}(1 - m\sin\omega t) \\ u_{ale} = \dfrac{U_{dc}}{2}(1 + m\sin\omega t) \end{cases} \tag{11}$$

where m is the modulation ratio of the AM-MMC.

According to (10) and (11), the instantaneous power of equivalent upper and lower arms (p_{aue} and p_{ale}) can be derived as

$$\begin{cases} p_{aue} = \dfrac{U_{dc}}{2}(1 - m\sin\omega t)\left[\dfrac{I_{dc}}{3} + \dfrac{I_m}{2}\sin(\omega t - \varphi)\right] \\ \quad = U_{dc}[\dfrac{I_{dc}}{6} - \dfrac{mI_m}{8}\cos\varphi - \dfrac{mI_{dc}}{6}\sin\omega t \\ \qquad + \dfrac{I_m}{4}\sin(\omega t - \varphi) + \dfrac{mI_m}{8}\cos(2\omega t - \varphi)] \\ p_{ale} = \dfrac{U_{dc}}{2}(1 + m\sin\omega t)\left[\dfrac{I_{dc}}{3} - \dfrac{I_m}{2}\sin(\omega t - \varphi)\right] \\ \quad = U_{dc}[\dfrac{I_{dc}}{6} - \dfrac{mI_m}{8}\cos\varphi + \dfrac{mI_{dc}}{6}\sin\omega t \\ \qquad - \dfrac{I_m}{4}\sin(\omega t - \varphi) + \dfrac{mI_m}{8}\cos(2\omega t - \varphi)] \end{cases} \tag{12}$$

To ensure the stable power exchange in equivalent upper and lower arms, their average power should be zero to avoid energy accumulation. According to the constraint, the DC current can be derived as

$$I_{dc} = \frac{3}{4}mI_m\cos\varphi \tag{13}$$

The total power and fluctuation in phase-a leg can be calculated by the sum of p_{aue} and p_{ale}, and yield as

$$\begin{aligned} \tilde{p}_{at} &= p_{aue} + p_{ale} \\ &= U_{dc}[\frac{I_{dc}}{3} - \frac{mI_m}{4}\cos\varphi + \frac{mI_m}{4}\cos(2\omega t - \varphi)] \end{aligned} \tag{14}$$

Substituting (13) into (14), the derived formula also guarantees the energy of the phase leg does not accumulate. Subsequently, the power exchange between the AC and DC sides is inherently balanced without any additional constraints, thus enabling the AM-MMC to achieve full-range voltage regulation.

The N series capacitors in the inserted SMs of phase-a leg will dampen this power fluctuation. Accordingly, it results in a double-frequency voltage fluctuation on these N capacitors. Thus, the total voltage of these N series capacitor can be supposed as

$$u_{\mathrm{at}} = U_{\mathrm{dc}} + \tilde{u}_{\mathrm{at}} = U_{\mathrm{dc}} + \tilde{U}_{\mathrm{at}} \sin(2\omega t - \varphi_{\mathrm{at}}) \tag{15}$$

where $\tilde{U}_{\mathrm{at}}$ and φ_{at} are amplitude and initial phase angle of voltage fluctuation of N capacitors. The power fluctuation can also be calculated by

$$\tilde{p}_{\mathrm{at}} = u_{\mathrm{at}} \cdot \frac{C}{N} \frac{du_{\mathrm{at}}}{dt} \tag{16}$$

According to (14) to (16), the voltage fluctuation of total N capacitors can be approximately derived as

$$\tilde{u}_{\mathrm{at}} = \frac{NmI_{\mathrm{m}}}{8\omega C} \sin(2\omega t - \varphi) \tag{17}$$

The voltage of each phase leg fluctuates at double-frequency around the DC voltage. Subsequently, the double-frequency circulating current also appears in phase leg like the conventional MMC. Assuming that the double-frequency voltage components of three phases are symmetrical, the circulating current will not flow into the DC side. Then the circulating current of each phase can be calculated by

$$i_{\mathrm{cir}} = \frac{\tilde{u}_{\mathrm{pal}}}{2\omega \cdot 2L_0} = \frac{NmI_{\mathrm{m}}}{32\omega^2 L_0 C} \cos(2\omega t - \varphi) \tag{18}$$

From the perspective of equivalent arms of the AM-MMC, they have the same exchange power as the conventional MMC. Thus, the power, total voltage fluctuation and the circulating current of phase legs are also the same forms. Since without energy balance limitation, the AM-MMC has a wide voltage regulation range as the conventional MMC, which can be verified by the experimental results of Fig. 17. However, the total number and inserting frequency of SMs are different, which results in different voltage fluctuation forms in the actual arms. During the positive half cycle of the output voltage, for the conventional MMC, 0.5N~0 SMs and 0.5N~N SMs out of N SMs are inserted in the upper and lower arms respectively. Meanwhile, the voltage fluctuation is mainly shared by the capacitors of lower arm due to their higher utilization rate. However, for the AM-MMC, the upper, middle and lower arms are all inserted with 0~0.5N SMs out of 0.5N SMs by the proposed modulation strategy. Therefore, the total voltage fluctuation is almost evenly shared by these three arms. Consequently, the capacitor voltages of the conventional MMC and the AM-MMC mainly fluctuate at fundamental frequency and double frequency respectively, which can be seen from the experimental results of Fig. 18. Compared with the conventional MMC, the AM-MMC can use SMs with less quantity but higher inserting frequency to achieve similar voltage fluctuation damping effect. Hence, there is no additional requirement in capacitors of SMs for the AM-MMC. The AM-MMC with the MNLM scheme improves the power density of the substation while maintaining its full-range voltage regulation capability.

IV. Design of the Arm Selection Switches

The dynamic voltage balancing is an important issue for DSs composed of semiconductors connected in series. The switches which turn off first or turn on last may suffer from excessive overvoltage, leading to potential malfunctions. The commutation scheme of the arm selection switches is discussed in detail to avoid dynamic voltage balancing issue.

A. The structure of the switches

As shown in Fig. 3, two arm selection switches K_{a1} and K_{a2} are connected between phase-a and the middle arm terminals a_1 and a_2. The TDM of middle arm is achieved by their alternate conduction.

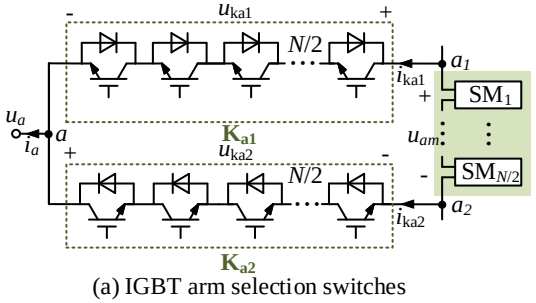
Due to the clamping of the on-state switch, the off-state switch must withstand the voltage of middle arm u_{am}. The voltages of the arm selection switches can be expressed as

$$\begin{cases} u_{\mathrm{ka1}} = S_{\mathrm{a}} u_{\mathrm{am}} \\ u_{\mathrm{ka2}} = (1 - S_{\mathrm{a}}) u_{\mathrm{am}} \end{cases} \tag{19}$$

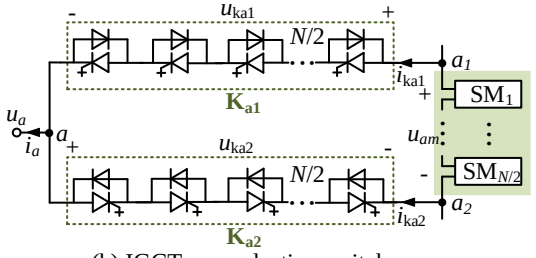
Since u_{am} is a positive voltage normally, the series devices in K_{a1} and K_{a2} only need to withstand unidirectional voltage. The phase current flows through the switch when it turns on, so the currents of these two switches can be expressed as

$$\begin{cases} i_{\mathrm{ka1}} = (1 - S_{\mathrm{a}}) i_{\mathrm{a}} \\ i_{\mathrm{ka2}} = S_{\mathrm{a}} i_{\mathrm{a}} \end{cases} \tag{20}$$

where i_{a} is the phase-a current. Fig. 8 shows the detailed structure of the arm selection switches, which are composed of N/2 full-controlled power devices connected in series.



(a) IGBT arm selection switches



(b) IGCT arm selection switches

Fig. 8. Structures of the arm selection switches.

When the multiplexing mode changes, the two switches in each phase should be flipped to alternate the phase current path. For example, in case of mode changing from I to II, the phase current is transferred from i_{Ka2} in the lower switch to i_{Ka1} in the upper switch by switching off K_{a2} and switching on K_{a1}.

In addition, each arm selection switch conducts the phase current for half a cycle, thus the rated RMS current I_{KN} of the

switch is

$$I_{KN} = \frac{I_N}{\sqrt{2}} = \frac{I_m}{2} \tag{21}$$

where the I_N is the rated rms current of the converter AC side.

According to the constraint of I_{dc} and I_m shown in (13), the currents of equivalent arms without circulating current suppression can be expressed as

$$\begin{cases} i_{aue} = \dfrac{mI_m \cos\varphi}{4} + \dfrac{I_m}{2}\sin(\omega t - \varphi) + \alpha I_m \sin(2\omega t - \varphi_{2f}) \\ i_{ale} = \dfrac{mI_m \cos\varphi}{4} - \dfrac{I_m}{2}\sin(\omega t - \varphi) + \alpha I_m \sin(2\omega t - \varphi_{2f}) \end{cases} \tag{22}$$

where α is the coefficient of double-frequency component to fundamental frequency component. Unlike the devices in selection switches conducting fundamental sine current, the IGBTs in SMs operate at high frequency switching state. The maximum RMS current of IGBTs in SMs is

$$I_{SN} \approx \frac{m\cos\varphi + \sqrt{2+8\alpha^2}}{4} I_m \tag{23}$$

Therefore, the selection switches can use the devices with a slightly lower current rating than those in SMs.

The rated voltage of the arm selection switches is the maximum voltage of middle arm u_{am_max}, and can be expressed as

$$U_{KN} = u_{am\_max} = \frac{U_{dc}}{2} \tag{24}$$

Each arm selection switch needs $N/2$ devices with the same rating as SMs to withstand its maximum voltage of $U_{dc}/2$. Accordingly, N devices need to be used for the two arm selection switches in each phase.

B. Zero-voltage Switching Scheme

According to (19) and (24), the theoretic voltage waveform of K_{a1} can be described in Fig. 9. High voltage does exist during the switching on/off process under the normal modulation. If zero-voltage switching (ZVS) could be performed at the mode changing instant, it will be of great benefit to the device safety and the snubber circuit simplification.

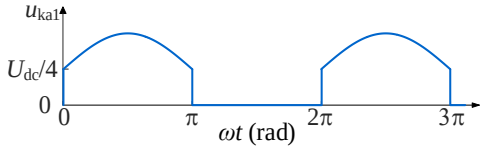


Fig. 9. Voltage waveform of K_{a1} without ZVS.

As analyzed in the MNLM scheme, the multiplexing mode changes while the numbers of inserted SMs in the equivalent upper and lower arms are both $N/2$. The off-state arm selection switch needs to withstand the middle arm voltage. Therefore, the SMs in the middle arm should all be bypassed at this instant to achieve ZVS. After the mode changing, the middle arm can insert SMs gradually to provide level superposition for the equivalent arm which generates levels greater than $N/2$. Thus, a 'transfer' of the inserted SMs between the middle arm and the upper/lower arm should be implemented before the mode changing. The ZVS scheme of the arm selection switches proposed in this paper is shown in Fig. 10. Taking the switching process from mode I to mode II as an example, the modulation principles are described below.

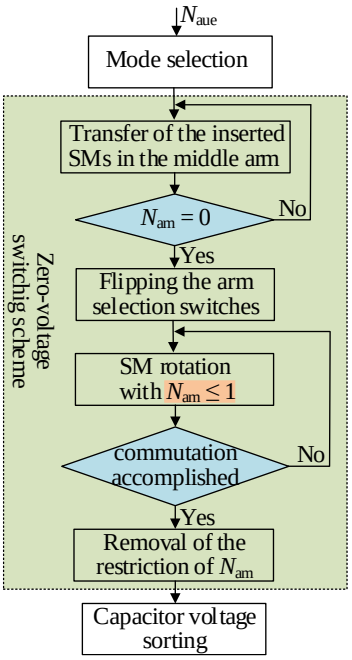


Fig. 10. Zero-voltage switching scheme.

1) If the multiplexing mode changes, i.e., N_{aue} steps to $N/2$, the 'transfer' of the inserted SMs in the equivalent upper arm is performed first. Consequently, all the SMs in the middle arm are bypassed, thus only conduction voltage drop exists between terminals a_1 and a_2. The $N/2$-level of the upper arm is generated by inserting all its own SMs. This transfer does not change the number of the inserted SMs, and has no effect on the output multilevel voltage waveform either.

2) When the transfer is finished, i.e., $N_{am} = 0$, two arm switches can be flipped by changing their driving signals to proceed commutation under zero-voltage.

3) After flipping these two switches, the middle arm can participate in the SM rotation in the lower arm. However, the number of the inserted SMs in middle arm is limited to one in the initial stage. It is aimed at limiting the switch voltage to less than U_c, to ensure the device safety in case the commutation is not fully implemented. Afterwards, the rotation of the SMs in the equivalent lower arm sorting by their voltages can be carried out without restriction.

The ZVS effectively avoids the overvoltage of each device in arm selection switches, which is necessary for the reliable operation of devices. And the restriction of $N_{am} \le 1$ in the initial rotation is applied for further avoiding the device overvoltage under abnormal conditions, e.g. the driving signal delay. Due to the ZVS could be implemented within several control cycles, it has little effect on the capacitor voltage balancing.

V. Comparison with Other Topologies

A. Comparison with the conventional MMC

A comprehensive comparison between the AM-MMC and the conventional MMC is first completed. It should be noted that the performances of the AM-MMC may vary under different modulation schemes, and this work is conducted under the MNLM scheme.

1) Numbers of semiconductor devices & capacitors

Compared with the conventional MMC, the AM-MMC with the MNLM can reduce SMs by 25% due to the increased module utilization rate that is from 50% to 66.7%. However, the arm selection switches also introduce semiconductor devices. Under the premise of using the IGBTs and capacitors with same ratings, their quantities in the AM-MMC and MMC are compared in Table I.

TABLE I
Device Quantity Comparison of Converters

Converters		Number of IGBTs	Number of capacitors
With HBSMs only	MMC	12*N*	6*N*
	AM-MMC	12*N* (9*N* for SMs and 3*N* for switches)	9*N*/2
With FBSMs only	MMC	24*N*	6*N*
	AM-MMC	21*N* (18*N* for SMs and 3*N* for switches)	9*N*/2
Hybrid of HBSMs and FBSMs	MMC (*N* HBSMs & *N* FBSMs each phase)	18*N*	6*N*
	AM-MMC (0.5*N* HBSMs & *N* FBSMs each phase)	18*N* (15*N* for SMs and 3*N* for switches)	9*N*/2

Each phase leg can reduce *N*/2 SMs with one multiplexed arm in the AM-MMC. As a result, 25% capacitors are reduced regardless of the type of SMs, which is significantly conducive to the compact and lightweight design of converters since the capacitors account for more than 50% of the total size and weight of MMC.

However, the device number reduction depends on the structure of SMs. For the HBSM based AM-MMC, the reduced *N* devices from *N*/2 SMs each phase are all "transferred" to the arm selection switches, since they are composed of *N* IGBTs. For the FBSM based AM-MMC, there are still *N* IGBTs reduction each phase as *N*/2 FBSMs consists of 2*N* IGBTs.

To reliably clear the fault current, the proportion of FBSMs of each phase must be at least 43.3% [34], which is generally set to 50% in practical MMC projects [35]. For the AM-MMC, to achieve the fault current limiting capability similar to the conventional MMC, 0.5*N* FBSMs are assembled in upper & lower arms respectively, and 0.5*N* HBSMs are assembled in middle arm. For the above-mentioned hybrid AM-MMC, it also has same IGBTs as the hybrid MMC with *N* HBSMs and *N* FBSMs.

2) Minimum capacitance requirement

The maximum variation of capacitor energy storage $\Delta E_{\mathrm{c\_max}}$ can be expressed as

$$\begin{aligned}\Delta E_{\mathrm{c\_max}} &= \frac{1}{2}C[(1+\varepsilon)U_{\mathrm{c}}]^2 - \frac{1}{2}C[(1-\varepsilon)U_{\mathrm{c}}]^2 \\ &= \frac{1}{2}CU_{\mathrm{c}}^2 \cdot 4\varepsilon\end{aligned} \tag{25}$$

where ε is the allowed fluctuation range of the capacitor voltage and can be set to 10% for both the conventional MMC and the AM-MMC [36]. As described in Section III.C, the voltage and power fluctuations of the phase leg are withstood by *N* inserted SMs, as the conventional MMC. Then the maximum energy change of the phase leg is

$$\Delta E_{\mathrm{phase\_max}} = \frac{N}{2}CU_{\mathrm{c}}^2 \cdot 4\varepsilon \tag{26}$$

The minimum capacitance requirement is usually determined by the maximum energy deviation [37], and yield as

$$C_{\min} = \frac{\Delta E_{\mathrm{phase\_max}}}{2NU_{\mathrm{c}}^2\varepsilon} \tag{27}$$

For the AM-MMC and MMC, the total power fluctuation of phase leg is completely consistent, as presented in (14). Hence, the same maximum energy change and minimum capacitance requirement can be derived for these two topologies. However, the AM-MMC reduces the number of SMs from 6*N* in the original MMC to 4.5*N*, resulting in a 25% reduction of the energy stored in the converter.

3) Power loss

To compare with other converters on a unified standard, the HBSM is selected. The number of devices in Table I are adopted without considering redundant SMs. Due to the arm selection switches only operate at fundamental frequency, their commutation loss will not be the main concern. However, the improvement of the SM utilization in the AM-MMC will increase the SM switching times, leading to a slight increase in switching loss. For the conduction loss, it depends on the total number of devices and their current RMS. The total number of devices has not changed due to the devices reduced from 0.5*N* SMs per phase are 'transferred' to the arm selection switches. Since each SM has a conductive device, the total conductive devices are still 2*N* per phase, the same as MMC. But the current RMS of the arm selection arms is lower than that of the SMs as illustrated in Section IV.A. Thus, the conduction loss of AM-MMC is similar with that of conventional MMC.

Moreover, integrated gate-commutated thyristors (IGCTs) could be a more ideal choice for the switches, as they only operate at fundamental frequency [38]. The structure of the arm selection switches with IGCT is shown in Fig. 8(b). With the inheritance of large-capacity thyristors, the voltage rating and surge capability of IGCT are higher than that of IGBT at the same current level [39], [40], which can reduce the number of series connected devices. The low on-state voltage of IGCT can also reduce the conduction loss. Besides, the relatively simple structure and manufacturing processes make

the cost of an IGCT about one-half of that of an IGBT with same capacity [41], [42].

The power loss is calculated with the mathematical method presented in [43], [44], based on the simulation system in Section VI.B. The losses of each semiconductor device are recorded and calculated, and finally summed up to obtain the total converter loss. Since the rated voltage of SMs is 4.375kV, the ABB IGBT module 5SNA2000K452300 (rated at 4.5kV, 2kA) is selected. The arm selection switches use the same type of IGBT. To present a specific comparison, the ABB IGCT module 5SHY42L6500 (rated at 6.5kV, 2.03kA) with the same current level and a higher rated voltage is also selected for the switches, and the SMs still use the IGBT module of 5SNA2000K452300. The parameters of the two semiconductor devices are derived from the datasheets [45] and listed in Table II. Then the power losses of the MMC, AM-MMC with IGBT-switches and IGCT-switches are calculated at rectifier mode with unit power factor, and given in Table III.

TABLE II
PARAMETERS OF IGBT AND IGCT

Semiconductor device	IGBT (5SNA2000K452300)	IGCT (5SHY42L6500)
Rated voltage	4.5kV	6.5kV
Max. RMS on-state current	2000A	2030A
On-state voltage (4kA,125℃)	5.8V	3.8V
Max. peak non-repetitive surge on-state current (V_D=V_R=0V, T_j=125℃, t_p=10ms)	14kA	26kA
Max. controllable turn-off current	>13kA	4.2kA
Cost	1.6 p.u. (IGBT) 0.25 p.u. (driver)	1.0 p.u. (integrated driver)

As the number of SMs is reduced by 1.5N in total, the conduction loss of the SM valve is 81.8% of that of the MMC. The reduced devices form these 1.5N SMs are transferred to the arm selection switches, but they operate with lower RMS currents, which is analyzed in Section IV.A and verified in Section VI.B. The conduction loss of IGBT-switches is about 27.3% of that of SM valve, while for IGCT-switches, this proportion is about 14.3%. Therefore, the total conduction loss of the AM-MMC with IGCT-switches is smaller than that of MMC although additional switches are adopted.

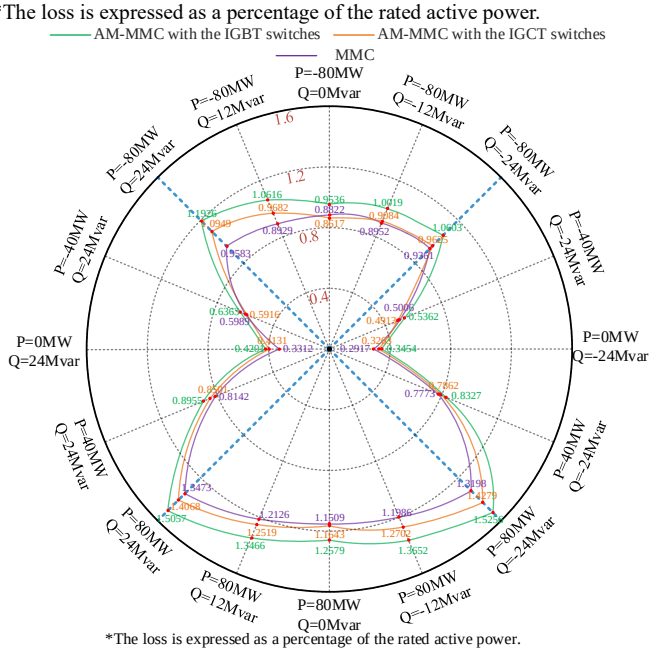
Due to the higher module utilization, the switching loss of three arms in the AM-MMC increases by about 0.04%. However, the proportion of the switching loss of AM-MMC is still much smaller than the conduction loss. The switching loss of the arm selection switches, whether composed of IGBT or IGCT, can be ignored as they only operate at fundamental frequency. Thus, the increase of the switching loss only has slight impact on the total loss.

Overall, under the unit power factor condition, the power losses of the MMC, AM-MMC with the IGBT-switches and AM-MMC with the IGCT-switches are 0.88%, 0.95%, and 0.86%, respectively.

TABLE III
POWER LOSSES AT UNIT POWER FACTOR (RECTIFIER MODE)

Converters	Conduction loss (%)			Switching loss (%)			Total loss (%)
	SM valve	Switch	Sum	SM valve	Switch	Sum	
MMC	0.86597	0	0.86597	0.01620	0	0.01620	0.88217
AM-MMC with IGBT-switches	0.70835	0.19314	0.90149	0.05183	0.00029	0.05212	0.95361
AM-MMC with IGCT-switches	0.70835	0.10124	0.80959	0.05183	0.00031	0.05214	0.86173

*The loss is expressed as a percentage of the rated active power.



*The loss is expressed as a percentage of the rated active power.

Fig. 11. Power losses of three topologies in different P-Q points.

Fig.11 further compares the power losses of three topologies under different P-Q points. The comparison results show that the loss of AM-MMC even with IGBT switches is at most 0.234% more than that of MMC under these conditions. In summary, the power losses of the AM-MMC and MMC remain almost at the same level under all operating conditions based on the MNLM scheme.

B. Comparison with other compact topologies

Other compact topologies proposed in recent years can be divided into three categories: the AAC-type, the HCMC-type and the H-bridge-type topologies. The detailed comparisons are listed in Table IV to show the effectiveness of the AM-MMC.

The DC voltage (U_{dc}), apparent power (S) and voltage stress of devices (U_{dc}/N) are the same for all the converters. One arm in the conventional MMC contains N SMs. The minimum capacitance, the energy storage, and the power loss of the MMC with HBSMs are considered as benchmarks.

The AAC-type topologies are closest to the AM-MMC in terms of working principle. Compared with the AM-MMC, the AAC and EO-AAC use 0.68N and 0.51N less SMs and their energy storages reduce by 61.47% and 47.2%

respectively. However, their device numbers are more than 150% of that in the AM-MMC, and the AAC requires a DC-side capacitor that stores about $0.121E$ energy [36]. In addition, the capacitor number advantage of AAC-type topologies is achieved by giving up forming the stable DC-side voltage, which is obtained in the MMC and AM-MMC by always inserting N SMs in the phase leg. Then the strict energy balance requirement makes the AAC only work at a fixed modulation ratio. The idea of TDM is also adopted in the M-AAC, but it also needs a large capacitor in DC-side, which makes the capacitor reduction from SMs meaningless.

The HCMC-type topologies are more like the traditional two-level VSC, rather than the MMC. The square-wave voltages at the AC side output are shaped into multilevel sinusoidal voltages using the FBCLs, which can also deal with the DC side faults. The additional voltage levels in the H3LC and the H5LC decrease the required number of FBSMs in the conduction path. Then the conduction loss is reduced as well. The latest H5LC has absolute advantages in device numbers and power losses, but with the expense of a high voltage DC-side capacitor for voltage ripple limitation and a pair of flying capacitors for two additional levels. These two components bring additional costs and limit its applications [46].

The single-phase transformers are necessary in the H-bridge-type topologies. Moreover, the transformers connected in series need be designed specially to deal with the common mode voltages and currents in an ungrounded state. In case of the series-connected topology, (the series-HBHMC and series-HLBC), three times the DC voltage is required with the same AC voltage, and the output levels are limited. Moreover, for the parallel-connected topology (the parallel-HBHMC and parallel-HLBC), a large number of devices and capacitors make the valve no longer compact. The compactness of the PHC and SBC are similar with the AM-MMC, but their energy storages are both small, which are about 27.2% and 45.6% of that in the AM-MMC respectively. The numbers of capacitors in the PHC and SBC have been significantly reduced by $3N$ and $2.5N$, which are only used to modify sinusoidal waveforms also without the ability to form the stable DC-side voltage. Hence, the DC-side capacitor is inevitable in these topologies. Besides, they need additional transformer components and H-bridge shaping circuits, and the latter brings high conduction loss. The total losses in the PHC and SBC are increased by 17.6% and 24.1% compared with the AM-MMC respectively.

Based on different improvement perspectives, the proposed SMPC and AM-MMC have a similar structure, but there are noticeable differences in terms of modulation strategy, module configuration and internal characteristics.

Fixed modulation waves for three arms in the SMPC are set to output complete sinusoidal waves, which causes that the energy between arms can only be balanced naturally at a fixed modulation ratio of $\pi/2$. For engineering applications, an energy control strategy based on double frequency component injection should be used to obtain only ±10% voltage regulation range around the modulation ratio of 1.13, which is not sufficient for addressing faults.

For the AM-MMC, with the proposed MNLM scheme, the phase leg can be completely equivalent to two voltage sources that are the same as the conventional MMC. Periodic energy exchange between the middle arm and the upper & lower arms ensures an easily achievable energy balance, and allows the AM-MMC to have full-range voltage regulation. A 25% reduction in the number of capacitors is at least achieved, and the capacitors can be further reduced by increasing the number of multiplexed arms. The AM-MMC has no additional requirements in semiconductor devices and other components, and the arm selection switches can use IGCT to obtain a lower cost and loss. Furthermore, based on the MNLM, the other control strategies of MMC are also easily adapted to the AM-MMC for circulating current suppression and fault ride-through. Compared with other novel topologies for MMC lightweight, the AM-MMC is the closest in

TABLE IV
COMPARISON WITH OTHER COMPACT TOPOLOGIES

Converters	MMC	AM-MMC (with three arms)	SMPC [33]	AAC-type			HCMC-type			H-bridge-type					
				AAC [19]–[21]	EO-AAC [22]	M-AAC [23]	HCMC (H2LC) [24], [25]	H3LC [26]	H5LC [27]	PHC [28], [29]	SBC [32]	HBHMC [30]		HLBC [31]	
												Series-HBHMC	Parallel-HBHMC	Series-HLBC	Parallel-HLBC
DC voltage	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc}	U_{dc} (the maximum ac voltage is $U_{dc}/3$)	U_{dc} (the maximum ac voltage is U_{dc})	U_{dc} (the maximum ac voltage is $U_{dc}/3$)	U_{dc} (the maximum ac voltage is U_{dc})
Apparent power	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
Voltage stress of devices	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N	U_{dc}/N
Output levels	N+1	N+1	1.13N+1	1.274N+1	1.333N+1	1.274N+1	2	3	5	N+1	N+1	0.667N+1	2N+1	0.667N+1	2N+1
Number of SMs	6N	4.5N	5.22N	3.82N	3.99N	1.91N	1.5N	0.75N	0.375N	1.5N	2.063N	N	3N	2N	6N
Number of semiconductor devices	12N	12N	16.96N	18.28N	19.74N	18.28N	12.6N	15.6N	10.5N	9N	11.25N	8N	24N	8.667N	26N
Nominal modulation index	0.9	0.9	1.13	1.274	1.333	1.274	1.27	1.26	1.24	1.05	1	1	1	1	1
Range of modulation index	0 to 1.0	0 to 1.0	1.017 to 1.243	Fixed	0 to 1.333	Fixed	0 to 1.27	0 to 1.26	0 to 1.24	Fixed	Depending on the no. of FBSMs	0 to 1.274	0 to 1.274	Over-modulation is feasible	
DC fault-tolerant capability	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Minimum capacitance	C	C	$0.8C_{(3.36N)}$ $0.24C_{(1.86N)}$	0.455C	0.604C	0.455C	0.8C	0.551C	0.372C	0.815C	0.995C	0.133C	0.133C	0.828C	0.828C
Energy storage (Only capacitors)	E	0.75E	0.5E	0.289E	0.396E	0.145E	0.199E	0.063E	0.022E	0.204E	0.342E	0.022E	0.067E	0.276E	0.828E
Power loss	P	1.081P	1.1P	1.237P	1.209P	1.814P	1.517P	1.15P	0.95P	1.271P	1.341P	0.881P	2.424P	-	-
DC-side capacitor	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Requirement of special transformer	No	No	No	No	No	No	No	No	No	No	No	Yes	No	Yes	No

characteristics to the conventional MMC, and its DSs have higher reliability with ZVS, which is beneficial for the engineering application.

VI. Verification and Studies of the AM-MMC

A. Experimental verifications

To verify the feasibility of the designed arm selection switches and the applicability of MNLM scheme, a 2.75kW/±150V three-phase AM-MMC prototype is set up based on a 7-level MMC platform, shown in Fig. 12, and its detailed experimental configuration is provided in the appendix. The structure of the main circuit is shown in Fig. 13. The prototype control system is implemented using a real-time digital controller (RTU-BOX-204), where the NLM and MNLM schemes are implemented for the conventional MMC and AM-MMC, respectively. The half-bridge SMs and the arm selection switches with IGBT are adopted in the protype.

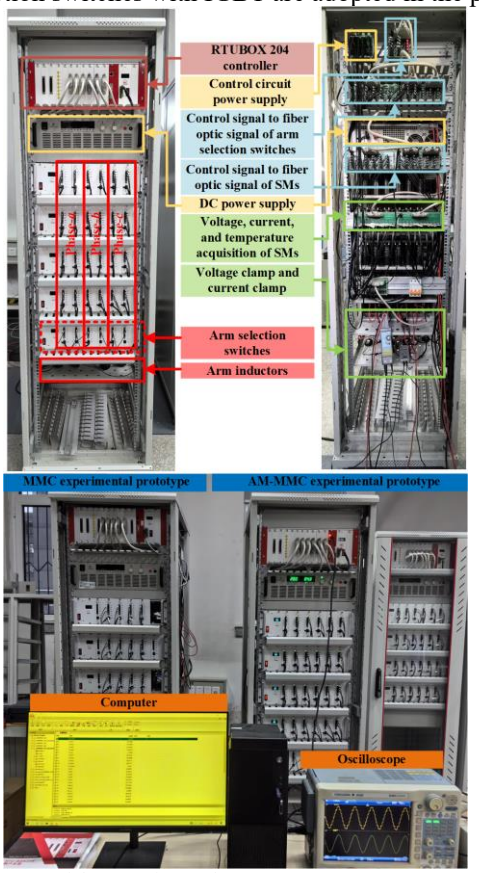


Fig.12. Structure of the experimental system.

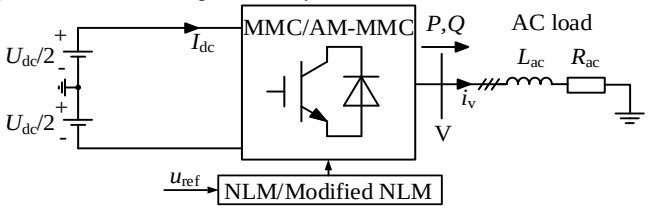


Fig.13. Structure of the experimental system.

The parameters of the experimental system are listed in Table V. The performance comparison of the AM-MMC and the conventional MMC is carried out.

TABLE V
Parameters of the Experimental Systems

Items		Values
Rated active power P_N		2.75 kW
Rated frequency f_N		50 Hz
Control circle T_c		0.05 ms
DC bus voltage $\pm U_{dc}/2$		±150 V
AC load inductance L_{ac}		15 mH
AC load resistance R_{ac}		10 Ω
Number of SMs per phase	MMC	$2N = 12$
	AM-MMC	$3N/2 = 9$
Arm inductance L_0	MMC	5.6 mH
	AM-MMC	5.6 mH
SM capacitance C_0		4.34 mF
SM capacitor voltage U_c		50 V

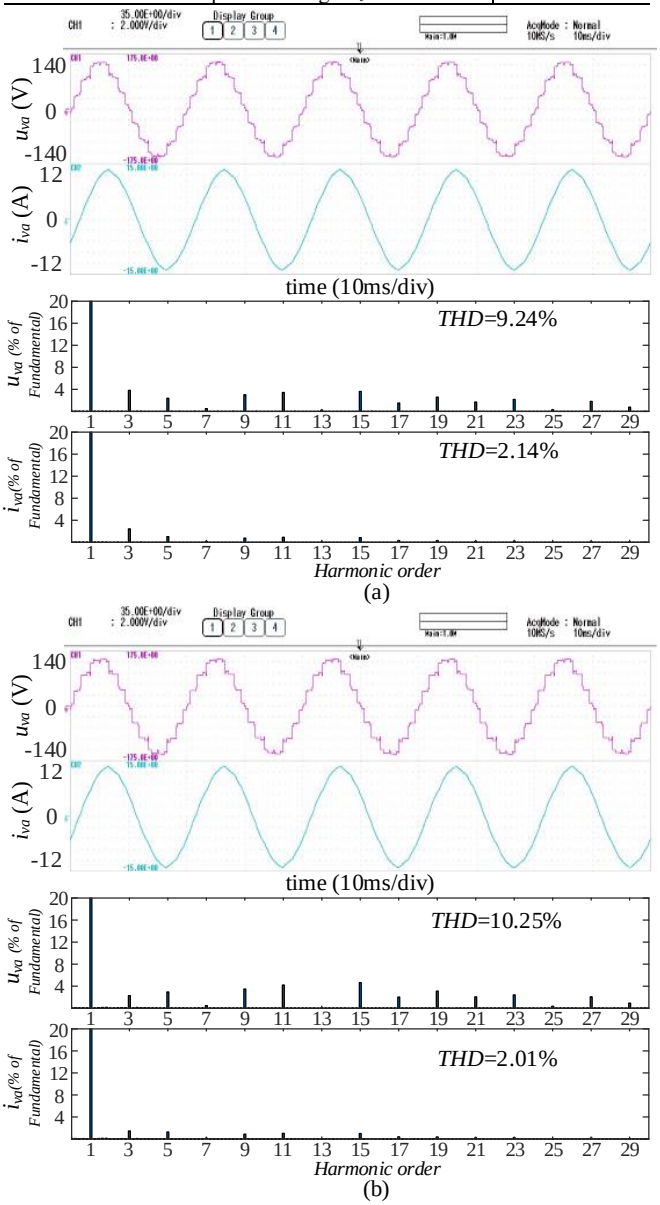


Fig. 14. Voltage waveforms (35V/div), current waveforms (3A/div) and their harmonic spectrums. (a) The MMC system. (b) The AM-MMC system.

Figs. 14(a) and (b) show the experimental waveforms of the AM-MMC and conventional MMC prototypes under same DC voltage, modulation ratio (m = 0.95) and AC load. As shown in Fig. 14, the AM-MMC with 9 SMs per phase can

output the same 7-level voltage as the conventional MMC with 12 SMs per phase. Then the harmonic spectrums of respective voltages and currents are provided. The experiments of the AM-MMC and conventional MMC with different modulation ratio are carried out to further compare their total harmonic distortion (*THD*), and the results are given in Table VI. With the MNLM, the AM-MMC and MMC are very similar in terms of harmonic content of output voltage and current. Multiple comparative experiments with different modulation ratios have also demonstrated the full-range voltage regulation of the AM-MMC based on MNLM. The slightly higher *THD* of the AM-MMC may be caused by the irregular fluctuations of the SM capacitor voltage among the three arms, especially when the modulation ratio is relatively small. Therefore, the developed MNLM enables the AM-MMC to obtain the same power quality and voltage regulation capability as the conventional MMC while reducing SMs by 25%.

TABLE VI
TOTAL HARMONIC DISTORTION OF THE TWO TOPOLOGIES

Modulation ratio *m*	*THD* of the phase-*a* voltage		*THD* of the phase-*a* current	
	MMC	AM-MMC	MMC	AM-MMC
0.8	12.69%	15.17%	6.05%	6.61%
0.85	12.65%	14.58%	3.10%	4.73%
0.9	12.12%	13.78%	3.16%	3.34%
0.93	10.18%	11.44%	2.54%	2.47%
0.95	9.24%	10.25%	2.14%	2.01%
0.97	8.72%	9.96%	1.71%	1.69%
1	8.04%	9.25%	1.54%	1.52%

The voltage waveforms of the upper, middle and lower arms in the phase-*a* leg are shown in Fig. 15. It can be seen that the total voltage of the three arms nearly maintains 300V with the sum of N_{aue} and N_{ale} being fixed at N = 6. As the middle arm operates in multiplexing mode I, the upper and middle arms generate the half-cycle multilevel voltage greater than 150V (U_{dc}/2) together. As in mode II, the middle arm is multiplexed to lower arm so that u_{aul} > 150V. In addition, the output voltages of the two combined arms are irregular, which is caused by the capacitor voltage balance strategy.

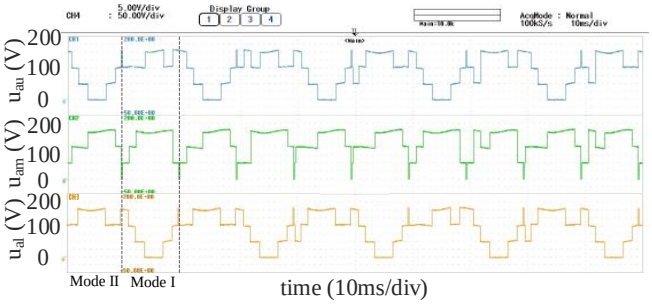


Fig. 15. Voltage waveforms (25V/div) of three arms in phase-*a* of the AM-MMC system.

To investigate the requirement of the proposed topology on the SM capacitor, Figs. 16(a) and (b) show the measured floating-capacitor voltages in phase-*a* of the AM-MMC and conventional MMC respectively, with the same capacitor. All the three arm capacitor voltages of the AM-MMC fluctuate about 5% near 50V, which are not greater than those of the conventional MMC. It confirms the effectiveness of the proposed MNLM for the capacitor voltage balancing and no additional requirement for SM capacitor.

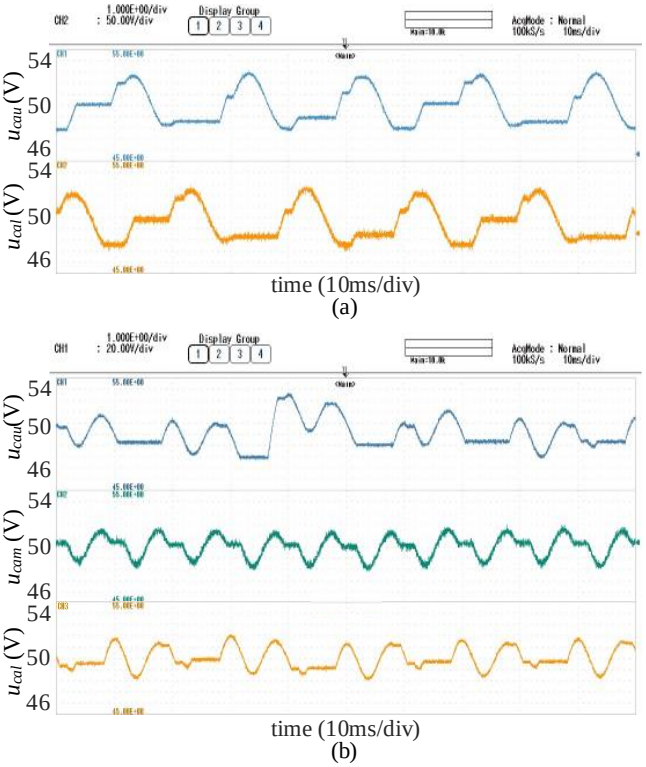


Fig. 16. Floating-capacitor voltages of the arms (1V/div) in phase-*a*. (a) The MMC system. (b) The AM-MMC system.

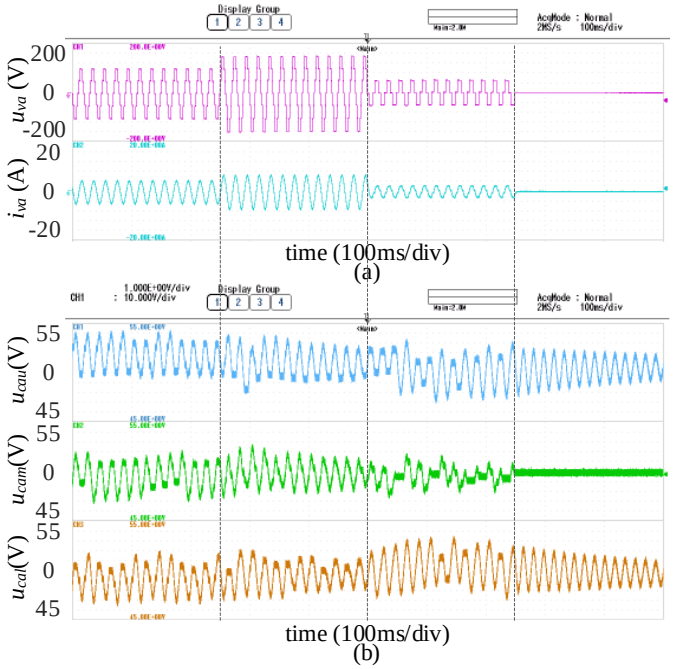


Fig. 17. (a) Voltage waveforms (40V/div), current waveforms (4A/div) and (c) floating-capacitor voltages (1V/div) during full-range voltage regulation.

Full-range voltage regulation is an advantage of AM-MMC using the MNLM, which cannot be achieved by the SMPC with the same three-arm structure. The AC port voltage, current and capacitor voltages are shown in Fig. 17. Restricted by number of SMs (*N*=6), four sets of voltage amplitudes of AC port are selected for the regulation. For the

first 250ms, phase-*a* outputs a voltage with an amplitude of 100V (m=2/3). From 250ms to 500ms, the voltage amplitude is adjusted to the maximum of 150V (m=1). In the next 250ms, the voltage amplitude is reduced to 50V (m=2/3). Finally, the output voltage is reduced to 0V (m=0). During the voltage regulation process, the capacitor voltages of three arms are maintained between 45V and 50V at a balanced value. The MNLM scheme can ensure stable operation while allowing full-range voltage regulation. In practical engineering, a sufficient number of SMs can support smoother voltage regulation.

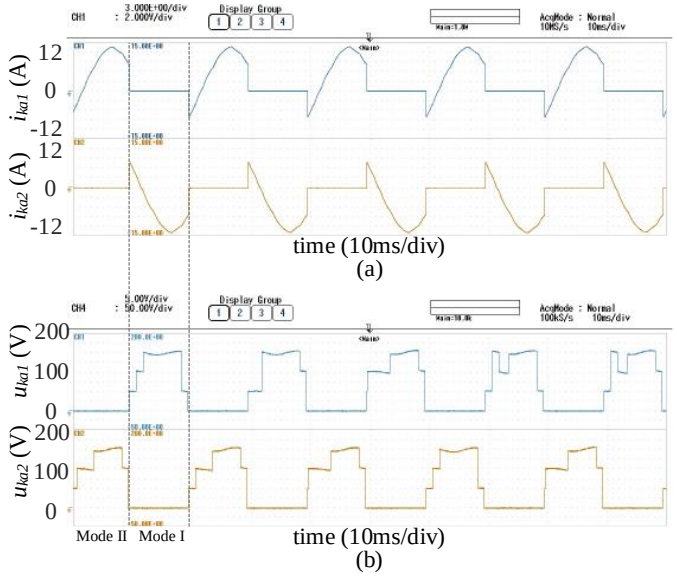


Fig. 18. Waveforms of the arm selection switches in phase-*a* of the AM-MMC system. (a) Currents of K_{a1} and K_{a2} (3A/div). (b) Voltages of K_{a1} and K_{a2} (25V/div).

The reliable operation of the arm selection switches is crucial for the practical application of the AM-MMC. Their voltage and current waveforms are shown in Fig. 18. Fig. 18 (a) shows that the arm selection switches each conduct for half a cycle. The phase current flows through the on-state switch, and the middle arm voltage is applied to the off-state switch. As shown in Fig. 18 (b), the arm selection switch K_{a1}/K_{a2} is clamed to the middle arm voltage when it is in off-state. The middle arm voltage will not become negative if its SMs do not generate negative levels. Therefore, N/2 devices are series connected in the switch to withstand the maximum middle arm voltage of U_{dc}/2. If the DC voltage needs to be decreased during dc fault ride through, the SMs with negative level output capability are better assembled in the upper and lower arms. Otherwise, the backward connected devices need to be added according to the required negative levels generated by the middle arm.

Fig. 19 shows the inserted SM number changing of the AM-MMC, which confirms the implementation of the ZVS during the period of the multiplexing mode changing. The middle arm voltage can be reduced to zero by the 'transfer' of the inserted SMs to the upper/lower arm. After the commutation of two switches under zero voltage, only one SM of the middle arm is inserted first. If the switches work properly, all SMs of the middle arm will participate in normal rotation subsequently. The ZVS scheme can ensure the safety of the switching devices.

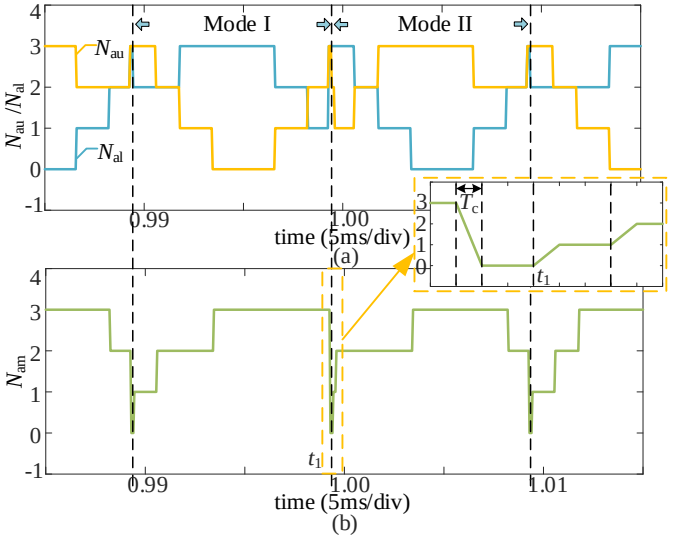


Fig. 19. The variations of the inserted SM number in the three arms of phase-*a* with ZVS control.

B. Simulation studies

To compensate the limitation of the experimental prototype, an 85MVA/±35kV AM-MMC HVDC simulation system based on Matlab/Simulink, as shown in Fig. 20, is built to show its performance of phase leg voltages, circulating currents and power losses, which are difficult to measure through experiments accurately. Furthermore, the currents of arms and switches are presented to support the power loss analysis. Meanwhile, an MMC-HVDC system with the same structure and parameters is also provided for performance comparison. The parameters of two simulation systems are listed in Table VII.

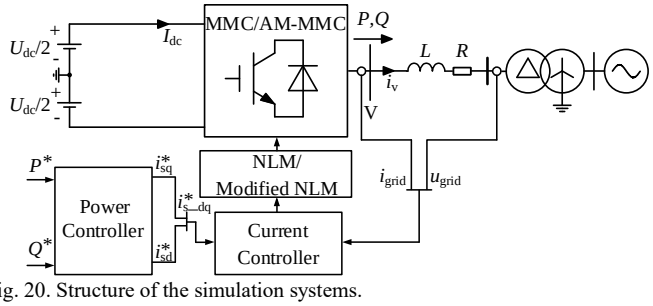


Fig. 20. Structure of the simulation systems.

TABLE VII
PARAMETERS OF THE TWO SIMULATION SYSTEMS

Items		Values
Rated active power P_N		80 MW
Rated reactive power Q_N		24 Mvar
Rated frequency f_N		50 Hz
DC bus voltage ±U_{dc}/2		±35 kV
Rated grid voltage V_{grid}		35 kV
modulation ratio m		0.816
Number of SMs per phase	MMC	2N = 32
	AM-MMC	3N/2 = 24
Arm inductance L_0	MMC	1.5 mH
	AM-MMC	1.5 mH
SM capacitance C_0		6.6 mF
SM capacitor voltage U_c		4.375 kV

Fig. 21 shows the waveforms of active and reactive power, phase-a leg voltage fluctuation (regardless of DC component), and phase-a circulating current for the two systems within 1.5s. The amplitudes of voltage fluctuation and circulating current are given in Table VIII. The amplitude of leg voltage fluctuation in the AM-MMC are almost identical to that in the MMC under three working conditions. The circulating current is generated by the voltage drop across the two arm inductances. Consequently, almost the same inductance and leg voltage fluctuation result in the generation of similar circulating currents.

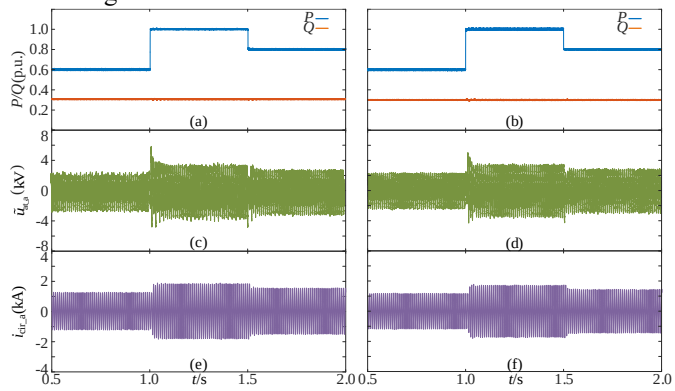


Fig. 21. (a) & (b) Waveforms of powers in the MMC HVDC system and AM-MMC HVDC system respectively. (c) & (d) Leg voltages of the MMC HV-DC system and AM-MMC HVDC system respectively. (c) & (d) Circulating currents of the MMC HVDC system and AM-MMC HVDC system respectively.

TABLE VIII
AMPLITUDES OF VOLTAGE FLUCTUATION AND CIRCULATING CURRENT

Working condition	*P*=48MW *Q*=24Mvar		*P*=80MW *Q*=24Mvar		*P*=64MW *Q*=24Mvar	
	MMC	AM-MMC	MMC	AM-MMC	MMC	AM-MMC
Voltage fluctuation amplitude $\tilde{U}_{at}$	2509V	2466V	3696V	3666V	3039V	3028V
Circulating current amplitude I_{cir}	1236A	1208A	1776A	1760A	1469A	1466A

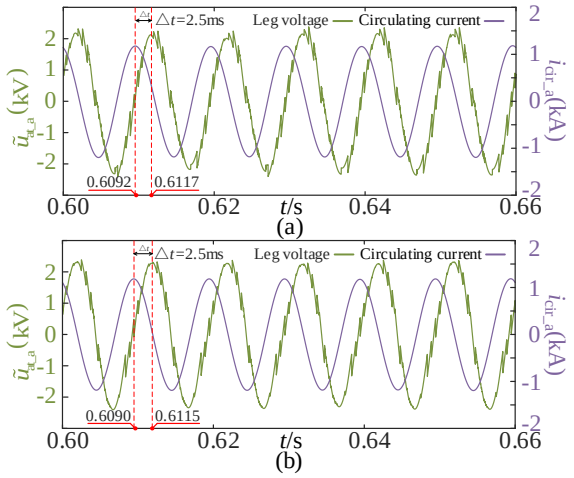


Fig. 22. Waveforms of phase-*a* leg voltage and circulating current. (a) The MMC HVDC system. (b) The AM-MMC HVDC system.

Figs. 22(a) and (b) are the partial enlargements of phase-*a* leg voltage fluctuation and circulating current from Fig. 21. Their phase voltage and circulating current all fluctuate at double-frequency. The arm inductances introduce a phase difference of 90 degree between the circulating current and the leg voltage.

Fig. 23 shows the arm currents and switch currents of phase- *a* in the two systems respectively, under the condition of rated active and reactive power. In terms of waveform and RMS value, the currents of the upper/lower arms in the AM-MMC and MMC are nearly the same, as show in Figs. 23 (a)-(d). Figs. 23 (e) and (f) show the currents of the middle arm and switches in phase-*a* respectively. The middle arm periodically switches to the equivalent upper and lower arms. Hence, its current contains half cycle upper arm current and half cycle lower arm current, and has lower amplitude and RMS value. The amplitude and RMS of the switch currents are about 61.2% and 65.6% of those of the equivalent arm current in the AM-MMC, which demonstrates the rationality of the device current rating analysis in Section IV.A.

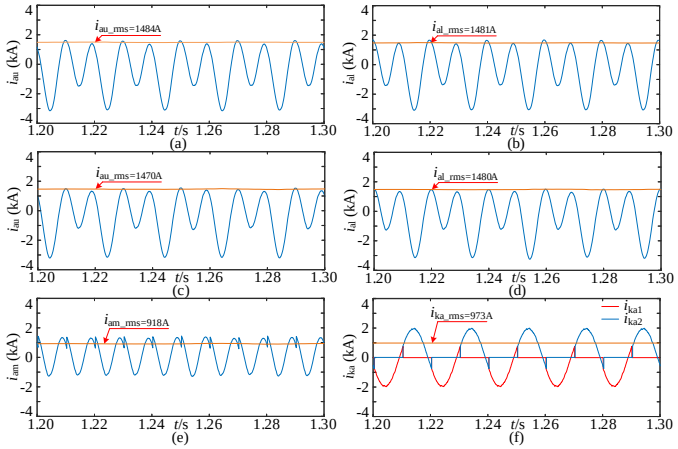


Fig. 23. Waveforms of phase-*a* currents. (a) The upper arm of MMC. (b) The lower arm of MMC. (c) The upper arm of the AM-MMC. (d) The lower arm of the AM-MMC. (e) The middle arm of the AM-MMC. (f) A pair of switches of the AM-MMC.

VII. CONCLUSION

The combination of the SM chain links and device series switches is becoming a topology trend in high power conversions to achieve compact design. This paper focuses on reducing idle SMs and improve module utilization while retaining the characteristics of traditional MMC.

Based on the idea of arm time-division multiplexing, the unified topologies of the AM-MMC, that can be extended to multiple arms, are proposed. By forming equivalent arms to the conventional MMC based on TDM of multiplexed arms, a novel modulation scheme with full-range voltage regulation is presented, which avoids the complicated waveform allocation and energy balance constraint of multi-arm structures. To realize the TDM of the middle arm, two additional arm selection switches are adopted in each phase. The structure design and the ZVS scheme, which can effectively avoid the dynamic voltage balancing, are also illustrated in detail to facilitate engineering applications. A comprehensive comparison is conducted between the AM-MMC using MNLM and other existing compact topologies to show its superiority. The experimental protype and simulation system of AM-MMC are constructed to verify the feasibility and

analyze performances, with the following conclusions presented.

1) Whether based on HBSM, FBSM, or Hybrid SM, when using the MNLM, the AM-MMC can reduce capacitors by 25% without increasing number of devices and capacitor/inductor ratings under the same converter capability. A further reduction of capacitors can be achieved by increasing arm selection switches in the unified AM-MMC topology.

2) With the MNLM scheme, experimental and simulated results show that the AM-MMC can achieve similar power quality, full-range voltage regulation, capacitor voltage, phase leg voltage, and circulating current with the conventional MMC.

3) The arm selection switches only operate at the fundamental frequency of the output voltage, which will not cause high switching loss. Furthermore, the proposed ZVS scheme can avoid the series devices suffering overvoltage at the switching instant, which can improve the practicability of the proposed AM-MMC.

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