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Monolithic modular thyristor-based DC-Hub with zero reactive power circulation

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ABSTRACT

The promising features of HVDC technology have led to the possibility of numerous renewable resources integration and enormous DC grids interconnection. In spite of the obstacles, these interconnections encounter such as the necessity to block DC faults, achieving isolation between different schemes, the ability to maintain power flow throughout different power flow profiles, and the interfacing with various infrastructures, the DC-Hub arises to overcome these interconnection obstacles being the excellent approach to enhance the DC grid capabilities. This paper proposes a new monolithic modular thyristor-based multilevel converter, which serves as the fundamental building block of the DC-Hub, offering advantages such as lower switch count, bidirectional power flow, and DC fault blocking capability. Moreover, a control algorithm, for zero reactive power circulation in the DC-Hub, is introduced. The proposed algorithm successfully mitigates the circulation of reactive power throughout the entire range of power flow. A comprehensive mathematical analysis, optimum design of converter parameters, and the proposed control technique, which suppress the circulating reactive power at full range of power flow, are illustrated. Finally, simulation modelling and hardware test rig are established to validate the claims of the DC-Hub at different normal and faulty scenarios.

1. Introduction

Recently, HVDC grids are considered the optimal solution around the globe for remote transmission of bulk power as in [1]. Owing to their uniqueness in the accessibility of offshore windfarms, enhanced power flow control as in [2], and lower transmission losses. In order to meet the rapid growth in load demand, the concept of the supergrid has drawn the attention of the academic society. It is the ideal solution to tackle the challenges that encounter the electrical schemes such as the capability to interconnect massive and remote renewable resources and ensuring the reliability and sustainability of HVDC grids unlike renewable sources connected to weak AC grids as in [3].

Multiterminal HVDC technology is one of the visions for the development of the supergrid, which encompasses a wide range of existing topologies as in [4–7]. It is obvious that multiterminal configurations still need further improvement, where their technical restrictions lie in the lack of:

- Interoperability between different HVDC vendors and topologies.
- Sustainable power flow during power reversal.
- Galvanic isolation among different networks.
- DC fault blocking capability.
- High voltage stepping.

Various converters were found in literature that interconnect multiport systems. Mainly, these converters are classified into non-isolated and isolated multiport converters. The first category includes different combinations of half-bridge and full bridge converters as shown in [8]. Another topology proposed in [9], it is based on a single-ended primary-inductor capacitor (SEPIC) to provide three-port system. Nevertheless, it is evident that it is only applicable in low power systems as well as it does not fulfil the requirement of modularity. Other topologies

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mentioned in [10], but it is evident that the aforementioned lacks the applicability in HVDC grids.

A family of non-isolated converters has been proposed in [11]. Mainly, these converters are derived from buck-boost topology as a building unit in addition to voltage doubler circuits. However, this family of converters lacks isolation, modularity and are limited to the number of ports installed. The concept of DC-DC autotransformer has been introduced in [12,13]. However, it lacks isolation owing to the nature of single stage conversion. Also, only fraction of power is transferred as discussed in [12]. On top of that, this type of converters does not satisfy the applicability of n-ports. Another idea proposed in [14], which is based on multi-active bridge (MAB). However, it lacks isolation due to absence of transformer. Also, it is not applicable in high voltage applications. On top of that, it exhibits reactive power circulation at partial power flow.

On the other hand, large number of isolated multiport topologies were found in literature based on different structures, for instance, some topologies are based on a single transformer to provide isolation as in [15–17]. It can be observed that the input ports exhibit common ground hence, this type of topologies are partially isolated. Reference [18] proposed the concept of multi-transformer based DC-DC converters (MTB). Mainly, it is composed of magnetically coupled dual active bridges (DAB). This type of converters suffers from inability for future insertion of new ports. Hence, it is not suitable for HVDC applications. Another idea proposed in [19], where it relies on series connection of DABs to form a closed ring. In spite of its open circuit failures tolerance, the topology is susceptible to power interruption due to short circuit faults at two ports or more. Additionally, the idea of multi-winding transformer (MWT) has been used as in [18,20]. The power transformer is based on two stage conversion (DC-AC-DC). However, MWT prevents future insertion of additional ports. Another technique proposed in [21,22] that enables the utilization of series connection of different sources to accommodate the integration of HVDC or MVDC. It has been widely used in the PV systems as mentioned in [23,24]. Nevertheless, this idea suffers from reliability at time of losing one of its modules. Also, the power mismatch due to different operating conditions of PV modules lead to extra footprint as shown in[24].

Based on the aforementioned discussion, the main issue with the existing research ideas in literature is the lack of modularity in the converter unit of the DC-Hub. Moreover, AC link filter was restricted to LCL filter to eliminate the circulating reactive power flow at rated power flow. Hence, the current stresses are extremely high during partial power flow.

The proposed monolithic modular thyristor-based DC-Hub (MMT-DC-Hub) utilizes antiparallel thyristors in the upper arm to replace the SMs and reduce the footprint of the converter unit. The lower arm of the converter is constituted of HB-SMs and limited number of FB-SMs for thyristor arm commutation. Thyristors are used in the upper arm owing to their high overcurrent capability, lower conduction losses, higher voltage rating and lower cost.

The main research contributions of this manuscript can be summarized as follows:

1. Proposal of a novel modular thyristor-based multilevel converter:
   - Introducing a novel architecture for the multilevel converter based on thyristors.
   - Serving as the fundamental building block of the DC-Hub.
   - Offering advantages such as lower switch count, and DC fault blocking capability.
   - Enabling bidirectional power flow, allowing energy to be transferred in both directions.
   - Improving the reliability of power flow by utilizing the proposed thyristor-based multilevel converter which Reduces conduction losses, improving overall efficiency.
   - Enhancing the reliability of power flow, ensuring continuous power transfer even during fault scenarios.
2. Introduction of an innovative control algorithm for zero reactive power circulation in the DC-Hub:
   - Developing a novel control algorithm specifically designed for the DC-Hub.
   - Effectively suppressing the circulating reactive power across the entire power flow range.
   - Reducing current stresses during partial power operation, enabling the use of semiconductors with a smaller footprint.
   - Allowing for broader applicability compared to existing schemes that only address circulating reactive power at rated power flow.

The claims of the paper are validated through three different cases. Namely, the first scenario involves the power flow reversal at rated value. The second scenario shows the zero reactive power circulation during transition from rated to partial power demand. Lastly, DC fault scenario is tested to verify the firewall to prevent fault spreading through the DC-Hub. Simulated setup is built using MATLAB/SIMULINK software package and a scaled down experimental prototype is built to show the three different tests for validation.

The rest of the paper is organized as follows: Section II illustrates the structure of the MMT-DC-Hub. Section III provides an equivalent power circuit with comprehensive mathematical analysis and the crucial conditions to suppress reactive power. Section IV provides LC filter deign as well as the optimum sizing of arm inductance and SM capacitor. Section V discusses the proposed control techniques to nullify the reactive power circulation among all ports and modifies the SM's capacitor sizing to suit the proposed control technique. Section VI validates the proposed control technique of MMT-DC-Hub at different healthy and unhealthy cases through a SIMULINK −based simulation while applying HVDC ratings. Section VII provides an experimental validation under healthy and faulty cases.

2. System overview of the proposed DC-hub

This section presents the architecture of the monolithic modular thyristor-based converter, where it allows the interconnection among multiple VSC-based HVDC networks. It is possible to construct each port using a three-phase arrangement, but an H-bridge arrangement has been chosen for the sake of simplicity as illustrated in Fig. 1.

Each leg of the converter consists of two arms, where a number of back-to-back series-connected thyristors joined together to constitute the upper arm to permit bidirectional current flow, while decreasing the switch count with minimized conduction losses. Regarding the lower arm, a hybrid MMC arm is used which consists of hybrid connection of sub-modules (SMs). Moreover, most of the SMs are HB-SMs, while a small amount of FB-SMs is used in order to enable the forced commutation process of the thyristors in both healthy and faulty cases. The total number of SMs in the hybrid MMC arm is as follows:

$$N_{ty} = N_{ry} + N_{cy} \tag{1}$$

where N_{ty} is the total number of SMs in hybrid MMC arm, N_{ry} is the number of HB-SMs which are responsible for delivering the rated DC voltage, and N_{cy} is the number of FB-SMs which are responsible for the thyristor commutation in the hybrid MMC arm in the y^{th} converter, respectively.

Furthermore, each converter is connected to VSC-based HVDC network, and its AC side is connected to an LC filter and an isolating transformer. Whereas the secondary of each transformer is connected to the global AC bus.

Fig. 2 shows the single-phase equivalent circuit of each converter in the proposed MMT-DC-Hub, where the variable capacitor represents the MMC hybrid arm. Thus, the capacitance of the x^{th} arm in y^{th} converter (C_{armxy}) can be represented as follows:

$$C_{armxy} = C_{SMy}/n_{xy} \tag{2}$$

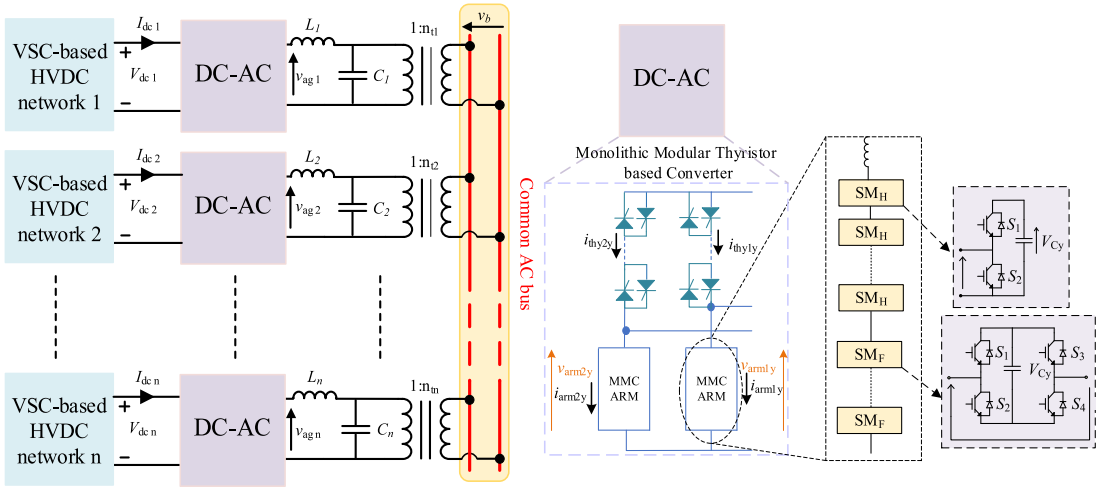


Fig. 1. Configuration of the proposed MMT-DC-Hub.

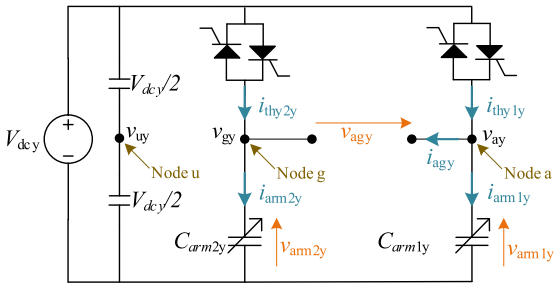


Fig. 2. Circuit diagram of the proposed converter.

where C_{SMy} is the SM capacitance in the y^{th} converter and n_{xy} is the required number of inserted SMs in the x^{th} arm in y^{th} converter. Furthermore, the nominal voltage of the SM capacitor in the y^{th} converter ($V_{c\_nominal\_y}$) can be obtained as follows:

$$V_{c\_nominal\_y} = V_{dcy}/N_{ry} \tag{3}$$

where V_{dcy} is the DC-link voltage at the y^{th} converter. Moreover, the hybrid MMC x^{th} arm voltage in the y^{th} converter (v_{armxy}) can be obtained as follows:

$$v_{armxy} = n_{xy} V_{dcy}/N_{ry} \tag{4}$$

The following two equations represent node a and node g voltages with respect to the hypothetical node u.

$$v_{auy} = v_{arm1y} - V_{dcy}/2 \tag{5}$$

$$v_{guy} = v_{arm2y} - V_{dcy}/2 \tag{6}$$

Using (4) in (5), the required number of inserted sub-modules is obtained as follows:

$$n_{1y} = N_{ry}\left(v^{*}_{auy} + 0.5\right) \tag{7}$$

where v^{*}_{auy} represents the reference waveform of output voltage v_{auy}.

In order to reduce the amount of voltage stress imposed on AC link transformer, a quasi-trapezoidal waveform is chosen. For the sake of controlling the magnitude and phase shift between the AC voltages, the firing-angle (α) has been applied as an additional control variable. Furthermore, Fig. 3 shows the reference voltage of nodes a and g with respect to the hypothetical node u as well as the output voltage waveform of the y^{th} converter. The mathematical representation of the reference waveform voltage is described in (8),

$$v^{*}_{auy} = \frac{1}{2}\begin{cases} 0, -t_{\alpha y} < t < t_{\alpha y} \\ \left(t - t_{\alpha y}\right)T_l^{-1}, t_{\alpha y} < t < T_l + t_{\alpha y} \\ 1, T_l + t_{\alpha y} < t < 0.5T_p - t_{\alpha y} - T_l - T_{cy} \\ 2N_c N_r^{-1} + 1, 0.5T_p - t_{\alpha y} - T_l - T_{cy} < t < 0.5T_p - t_{\alpha y} - T_l \\ \left(-t + 0.5T_p - t_{\alpha y}\right)T_l^{-1}, 0.5T_p - t_{\alpha y} - T_l < t < 0.5T_p - t_{\alpha y} \\ 0, 0.5T_p - t_{\alpha y} < t < 0.5T_p + t_{\alpha y} \\ \left(-t + 0.5T_p + t_{\alpha y}\right)T_l^{-1}, 0.5T_p + t_{\alpha y} < t < 0.5T_p + t_{\alpha y} + T_l \\ -1, 0.5T_p + t_{\alpha y} + T_l < t < T_p - T_l - t_{\alpha y} \\ \left(t - T_p + t_{\alpha y}\right)T_l^{-1}, T_p - T_l - t_{\alpha y} < t < T_p - t_{\alpha y} \end{cases} \tag{8}$$

where T_l is the rise/fall time of the trapezoidal waveform, T_{cy} is the commutation time of the FB-SM, T_p is the periodic time, and the corresponding time to the firing-angle α_y is given by $t_{\alpha y} = \frac{\alpha_y T_p}{2\pi}$. It is worth mentioning that the rise and falling time of the trapezoidal waveform is established based on the collective maximum of rise or fall time of the rated sub-modules inserted to build the trapezoidal waveform peak, as discussed in [25].

3. Power analysis of the proposed DC-Hub

This section provides comprehensive mathematical analysis of the monolithic thyristor-based multiport DC-hub as well as the essential conditions to eliminate the reactive power at rated power flow. The power flow analysis is applicable whatever the configuration of the converter used. Moreover, it discusses the transformation necessary to accommodate the monolithic modular thyristor-based converter in VSC-based DC-Hub.

3.1. Equivalent circuit analysis of the DC-Hub

Fig. 4 illustrates the simplified power circuit of the considered DC-Hub, where fundamental harmonic analysis is adopted to simplify derivation. Moreover, each converter generates a fundamental AC voltage depicted as follows:

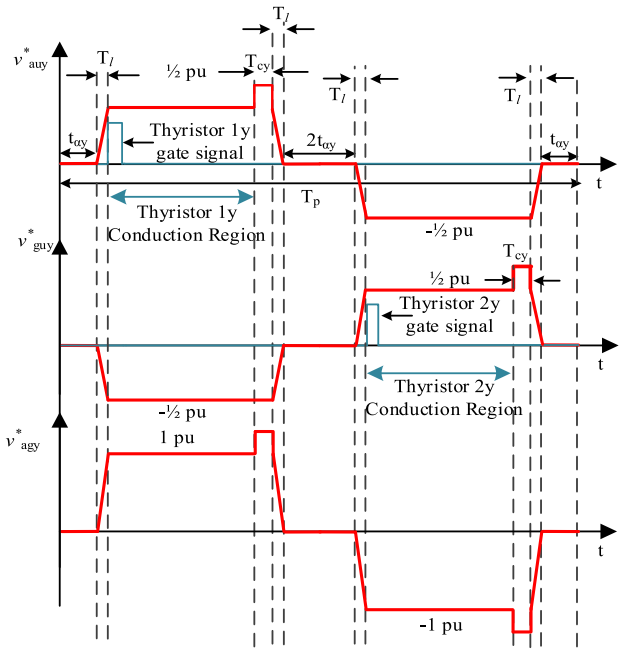


Fig. 3. Key waveform of the reference output voltage.

$$v_{agy} = \sqrt{2}V_y^m \sin\left(2\pi f_o t + \phi_{vy}\right) = \sqrt{2}V_y^r M_y \sin\left(2\pi f_o t + \phi_{vy}\right) \tag{9}$$

where, v_{agy} represents the fundamental component of y^{th} port AC voltage, V_y^m is the RMS value of the voltage fundamental component, while V_y^r represents the rated RMS value of voltage fundamental component, M_y is the modulation index, ϕ_{vy} is the relative phase shift, and f_o represents the operating frequency of all AC signals.

Additionally, the RMS value of the voltage fundamental component can be obtained as follows:

$$V_y^m = M_y V_y^r = M_y V_{dcy}/\sqrt{2} \tag{8}$$

In a d-q frame which is aligned to the global reference angle, the AC voltage phasor $\bar{v}_{agy}$ of the instantaneous voltage v_{agy} of y^{th} port is described below:

$$\bar{v}_{agy} = M_y V_y^r \angle\phi_{vy} = M_y V_y^r \cos\phi_{vy} + jM_y V_y^r \sin\phi_{vy} \tag{9}$$

Moreover, the fundamental AC bus voltage $\bar{v}_b$ can be obtained by applying KVL in loop 1 as follows:

$$\bar{v}_{agy} - \bar{v}_b = j\omega_o L_y \bar{i}_{agy} = j\omega_o L_y I_y^m \left(\cos\phi_{iy} + j\sin\phi_{iy}\right) \tag{10}$$

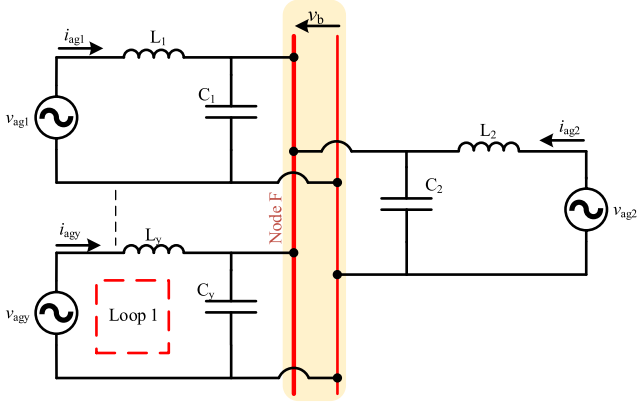


Fig. 4. Simplified power circuit of the proposed converter.

where ω_o represents the fundamental angular frequency, L_y represents the filter inductance of y^{th} port, I_y^m and ϕ_{iy} are the RMS value and phase shift of the output current fundamental component with respect to AC bus of y^{th} port.

Assuming that $\bar{v}_b$ is the reference point with zero phase shift. Therefore, the AC bus voltage can be simplified as a real component as follows:

$$\bar{v}_b = V_{b\_real} + jV_{b\_imag} = V_{b\_real} = V_b \tag{11}$$

Using (9) in (10), y^{th} port's real and imaginary components of the output current can be deduced as follows:

$$I_y^m \cos\phi_{iy} = M_y V_y^r \sin\phi_{vy}/\omega_o L_y \tag{12}$$

$$I_y^m \sin\phi_{iy} = V_b - M_y V_y^r \cos\phi_{vy}/\omega_o L_y \tag{13}$$

The apparent power for converter connected to y^{th} port can be calculated as follows:

$$\begin{aligned} S_y &= \bar{v}_y \bar{i}_y^* \\ &= \left(M_y V_y^r \cos\phi_{vy} + jM_y V_y^r \sin\phi_{vy}\right) * \left(\frac{M_y V_y^r \sin\phi_{vy} - j(V_b - M_y V_y^r \cos\phi_{vy})}{\omega_o L_y}\right) \end{aligned} \tag{14}$$

where S_y is the apparent power of y^{th} port. The active and reactive power of the y^{th} port are deduced by substituting (12) and (13) in (14) as follows:

$$P_y = \frac{V_b M_y V_y^r \sin\phi_{vy}}{\omega_o L_y} \tag{15}$$

$$Q_y = \frac{\left(M_y V_y^r\right)^2 - V_b M_y V_y^r \cos\phi_{vy}}{\omega_o L_y} \tag{16}$$

It can be observed from (16) that the reactive power can be nullified by maintaining the following criteria:

$$\left(M_y V_y^r\right)^2 = V_b M_y V_y^r \cos\phi_{vy} \tag{17}$$

From the previous condition, the phase shift $\left(\phi_{vy}\right)$ is calculated as follows:

$$\phi_{vy} = \text{acos} M_y V_y^r / V_b \tag{18}$$

3.2. Sinusoidal to quasi-trapezoidal transformation

In order to accommodate the utilization of monolithic modular thyristor-based converter in the VSC-based DC-Hub. It is mandatory to transform the control variable from modulation index (M_y) to its equivalent firing-angle (α_y) in the quasi-trapezoidal waveform. On the other hand, the equivalent phase shift of the AC voltage at port y (ϕ_{vy}) with respect to AC bus voltage remains unchanged.

By equating the RMS value of the fundamental component of voltage waveform with its quasi-trapezoidal equivalent, the following can be obtained:

$$\frac{M_y V_{dcy}}{\sqrt{2}} = \frac{4V_{dcy}}{\pi\sqrt{2}} \cos\alpha_y \tag{19}$$

Consequently, the equivalent firing-angle (α_y) is modelled as follows:

$$\alpha_y = \text{acos}\frac{\pi M_y}{4} \tag{20}$$

Moreover, the output AC current exhibits a phase shift with respect to the AC bus voltage due to the presence of d-q components of the current. Hence, the RMS value of the output current can be defined by using (12), (13) and (20) as below:

$$I_y^m = \sqrt{\frac{V_b^2 - \frac{4}{\pi}V_b V_y^r \cos\alpha_y \cos\phi_{vy}}{\omega_o^2 L_y^2}} \tag{21}$$

Furthermore, the output current phase shift with respect to the AC bus voltage $\left(\phi_{iy}\right)$ can be obtained as follows:

$$\phi_{iy} = \operatorname{atan}\frac{\frac{4}{\pi}V_y^r cos\alpha_y \sin\phi_{vy}}{V_b - \frac{4}{\pi}V_y^r cos\alpha_y \cos\phi_{vy}} \tag{22}$$

Hence, the relative phase shift of the output current with respect to the output voltage $\left(\phi_{ry}\right)$ can be computed as follows:

$$\phi_{ry} = \phi_{vy} - \operatorname{atan}\frac{\frac{4}{\pi}V_y^r cos\alpha_y \sin\phi_{vy}}{V_b - \frac{4}{\pi}V_y^r cos\alpha_y \cos\phi_{vy}} \tag{23}$$

4. Optimum design of MMT-based converter parameters

In this section, a detailed analysis of the inductor and capacitor design of the LC filter is provided as well as the hybrid MMC arm capacitor and its inductor sizing.

4.1. Design of LC filter

The AC filter inductance L_y is designed to obtain the rated power (P_y^r), where $M_y = 1$. Therefore, the general formula for designing the inductance for the converter can be deduced from (15) as follows:

$$L_y = V_b^r V_y^r \sin\phi_{vy}/\omega_o P_y^r \tag{24}$$

where P_y^r is port y rated active power and V_b^r is the rated bus voltage. Moreover, using (18), it is possible to rearrange (24) as follows:

$$L_y = V_b^r V_y^r \sin\operatorname{acos}\frac{V_y^r}{V_b^r}/\omega_o P_y^r \tag{25}$$

On the other hand, the AC filter capacitance is designed to compensate the reactive power at rated power flow. Furthermore, by applying KCL at node F, the capacitor voltage can be calculated as follows:

$$j\omega_o V_b^r \sum_{y=1}^{N} C_y = \sum_{y=1}^{N} \bar{i}_{agy} \tag{26}$$

where C_y is the filter capacitor of port y. Using the port's current in (12) and (13), while regarding that each port capacitor C_y is designed to compensate the reactive power generated by its own inductance L_y, the capacitor voltage becomes:

$$\omega_o V_b^r C_y = \frac{V_b^r - M_y V_y^r \cos\phi_{vy}}{\omega_o L_y} \tag{27}$$

By substituting (18) and (25) in (27), the filter capacitor of the converter can be deduced as follows:

$$C_y = \frac{P_y^r\left(V_b^r - \left(\frac{V_y^r}{V_b^r}\right)^2\right)}{\omega_o\left(V_b^r\right)^2 V_y^r \sin\operatorname{acos}\frac{V_y^r}{V_b^r}} \tag{28}$$

4.2. SMs' capacitance design

The SM capacitor of the hybrid MMC arm plays a crucial role in diminishing the voltage ripple in the MMC arm. Based on the trapezoidal voltage reference illustrated in (8), the general formula of capacitor voltage ripple is expressed as follows:

$$\Delta V_{c\_y} = \frac{1}{C_{SMy}}\int \frac{n_{xy}(t)}{N_{ty}} I_{armxy} dt \tag{29}$$

Furthermore, due to the connection of LC filter at the output AC side of each converter, it is safe to assume that the current is in the form of sinusoidal waveform, which can be described as follows:

$$i_{agy} = \sqrt{2} I_y^m \sin\left(\omega_o t + \phi_{ry}\right) \tag{30}$$

Moreover, the crucial intervals that lead to transient states in the SM capacitor are the rise/fall periods, the firing-angle period and commutation time. However, it is safe to assume that the impact of the rise/fall time is insignificant with respect to the commutation time and the firing-angle period. Hence, the rise/fall periods are neglected. Furthermore, it is evident that the MMC arm current and thyristor current share the same AC current function described in (30). Hence, by using (8) and (30) in (29), the capacitor voltage ripple can be obtained as follows:

$$\begin{aligned}\Delta V_{cy} = \frac{\sqrt{2} I_y^m}{C_{SMy} N_{ty}} \Bigg(& \int_0^{t_{\alpha y}} \frac{N_{ry}}{2} \sin\left(\omega_o t + \phi_{ry}\right) dt + \int_{\frac{T_p}{2} - T_l - T_{cy} - t_{\alpha y}}^{\frac{T_p}{2} - T_l - t_{\alpha y}} N_{ty} \sin\left(\omega_0 t + \phi_{ry}\right) dt \\ & + \int_{\frac{T_p}{2} - t_{\alpha y}}^{\frac{T_p}{2}} \frac{N_{ry}}{2} \sin\left(\omega_o t + \phi_{ry}\right) dt \Bigg)\end{aligned} \tag{31}$$

By solving and simplifying (31), the SM capacitor voltage ripple becomes:

$$\begin{aligned}\Delta V_{cy} = \frac{\sqrt{2} I_y^m}{\omega_o C_{SMy} N_{ty}} \big(& N_{ry}\cos\phi_{ry} + N_{ty}\cos\left(\phi_{ry} - \alpha_y\right) - N_{ty}\cos\left(\phi_{ry} - \left(\omega_0 T_{cy} + \alpha_y\right)\right) - N_{ry}\cos\alpha_y \cos\phi_{ry} \big)\end{aligned} \tag{32}$$

While the required percentage of the SM capacitor's voltage ripple can be determined as follows:

$$k = \frac{\Delta V_{cy} N_{ry}}{V_{dcy}} \tag{33}$$

Thus, the resultant SM capacitance can be given by:

$$\begin{aligned}C_{SMy} = \frac{\sqrt{2} I_y^m N_{ry}}{\omega_o k V_{dcy} N_{ty}} \big(& N_{ry}\cos\phi_{ry} + N_{ty}\cos\left(\phi_{ry} - \alpha_y\right) - N_{ty}\cos\left(\phi_{ry} - \left(\omega_0 T_{cy} + \alpha_y\right)\right) - N_{ry}\cos\alpha_y \cos\phi_{ry} \big)\end{aligned} \tag{34}$$

4.3. Arm inductance design

The function of the arm inductor in the hybrid MMC arm is to diminish the circulating current. Furthermore, it limits the current fall rate below the ramp rate of thyristor and above minimum fall rate of current throughout commutation period. Fig. 5 shows a simplified circuit which is used to analyze the circulating current during transient period. Moreover, by applying KVL in loop 2, the following equation can be obtained:

$$V_{dcy} = L_{ay}\frac{di_{circxy}}{dt} + \frac{1}{C_{armxy}}\int i_{circxy} dt + v_{c\_initial} + i_{circxy} R_{Lay} \tag{35}$$

where R_{Lay} is the parasitic resistance of the arm inductor. Considering (35), the differentiation of both sides results in:

$$L_{ay}i''_{circxy} + i'_{circxy}R_{Lay} + \frac{1}{C_{armxy}}i_{circxy} = 0 \tag{36}$$

The natural response of (36) can be deduced as follows:

$$i_{circxy} = \frac{2kV_{dcy}}{H}e^{-\frac{R_{Lay}}{2L_{ay}}t}\sin\left(\frac{Ht}{2L_{ay}}\right) \tag{37}$$

$$H = \sqrt{R_{Lay}^2 - 4L_{ay}C_{armxy}^{-1}}$$

$$\frac{dL}{dL_{ay}} = \frac{4kV_{dcxy}e^{\left(-\frac{R_{Lay}atan\left(\frac{H}{R_{Lay}}\right)}{H}\right)}}{C_{armxy}R_{Lay}^3\left(1-\frac{-R_{Lay}^2+\frac{4L_{ay}}{C_{armxy}}}{R_{Lay}^2}\right)^{\frac{3}{2}}} + \frac{2kV_{dcxy}e^{\left(-\frac{R_{Lay}atan\left(\frac{H}{Rl}\right)}{H}\right)}\left(\frac{2}{C_{armxy}\left(\frac{-R_{Lay}^2+\frac{4L_{ay}}{C_{armxy}}}{R_{Lay}^2}-1\right)\left(-R_{Lay}^2+\frac{4L_{ay}}{C_{armxy}}\right)} - \frac{2R_{Lay}atan\left(\frac{H}{R_{Lay}}\right)}{C_{armxy}\left(R_{Lay}^2-\frac{4L_{ay}}{C_{armxy}}\right)^{\frac{3}{2}}}\right)}{R_{Lay}\left(1-\frac{-R_{Lay}^2+\frac{4L_{ay}}{C_{armxy}}}{R_{Lay}^2}\right)^{\frac{1}{2}}} + \lambda\frac{N_{cy}V_{dcy}}{L_{ay}^2N_{ry}} = 0 \tag{41}$$

Moreover, by differentiating (37) with respect to time and equating it to zero. The instant at which the circulating current is at its peak can be deduced as described below:

$$t_{i_{circxy\_max}} = \frac{2L_{ay}}{H}\text{atan}\frac{H}{R_{Lay}} \tag{38}$$

Therefore, using (38) in (37) to find a relation that computes the peak of the circulating current as follows:

$$i_{circxy\_max} = \frac{2kV_{dcy}}{H}e^{\frac{-R_{Lay}}{H}atan\frac{H}{R_{Lay}}}*sinatan\frac{H}{R_{Lay}} \tag{39}$$

It can be observed that the peak value is affected by the voltage ripple factor k and the arm inductance L_{axy}. It can be solved numerically to evaluate the required arm inductance at the chosen peak value of circulating current.

Moreover, by using the criteria discussed in [26], the number of SMs which is dedicated for thyristor commutation (FB-SMs) can be determined as follows:

$$\frac{i_{thy\_1,2y}}{T_{cy}-T_f} \le \frac{N_{cy}V_{dcy}}{L_{ay}N_{ry}} \le \zeta \tag{40}$$

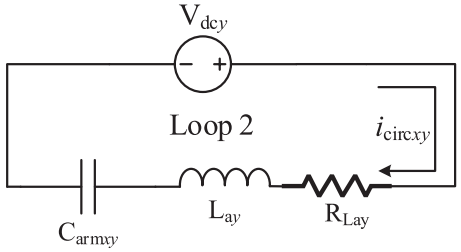


Fig. 5. Leg's simplified circuit during transient.

where ζ is the maximum ramp rate of thyristor current and T_f is the thyristor turn-off time.

Based on (39) and (40) a minimization problem is established to minimize the circulating current subject to constraints of (40). Thus, lagrange multiplier technique is used to solve the minimization problem as follows:

$$L = i_{circxy\_max} + \lambda\left(-\frac{N_{cy}V_{dcy}}{L_{ay}N_{ry}} - \zeta + \frac{i_{thy_{1,2y}}}{T_{cy}-T_f}\right) \tag{41}$$

The aforementioned formula is solved with respect to L_{ay}, N_{cy}, T_{cy}

$$\frac{dL}{dT_{cy}} = -\lambda\frac{i_{thy_{1,2y}}}{\left(T_{cy}-T_f\right)^2} = 0$$

$$\frac{dL}{dN_{cy}} = -\lambda\frac{V_{dcy}}{L_{ay}N_{ry}} = 0$$

$$\frac{dL}{d\lambda} = -\frac{N_{cy}V_{dcy}}{L_{ay}N_{ry}} - \zeta + \frac{i_{thy_{1,2y}}}{T_{cy}-T_f} = 0$$

5. Proposed active power flow control with zero reactive power circulation technique

This section illustrates extensively the proposed algorithm of nullifying the reactive power circulation in full range of active power flow. Additionally, it illustrates the necessary derivation and modification on SM capacitor sizing to achieve sizing equation that is independent of number of ports.

Mainly, the proposed technique is based on varying the voltage at the common AC bus (V_b) by solving the power flow equations to find the required values for the control variables (α_y and ϕ_{vy}) that satisfy the power references. It can be observed that the active power flow formula as in (15) is a multivariable function, where $P_y = f(V_b, \alpha_y, \phi_{vy})$. Similarly, the reactive power flow is a multivariable function as in (16), where $Q_y = g(V_b, \alpha_y, \phi_{vy})$. On other hand, the AC bus voltage is implicitly a function of $2n$ variables, where $V_b = h(\alpha_1, \phi_{v1}, \cdots, \alpha_n, \phi_{vn})$. Therefore, the proposed algorithm is based on solving $2n+1$ equations, where the equations used are listed below:

- AC bus voltage as in (26) as $h(\alpha_1, \phi_{v1}, \cdots, \alpha_n, \phi_{vn})$
- Active and Reactive power flow as shown in (15) and (16).

The control hierarchy can be summarized in 3-Level system. The first

level is for monitoring, where it is responsible to handle on-time measurements of DC link at each port as well as the ports that are currently connected to the DC-Hub. Additionally, it is fed by the required power flow reference values. The second level is known as lower brain function, where it is responsible to calculate and determine the required values for the control variables of each port, as illustrated in Section 3, based on the data collected by the monitoring level. Consequently, this level represents the main innovative aspect of the control algorithm since it assumes responsibility for mitigating reactive power circulation under any operating condition. The third level is responsible for waveform generation depending on the evaluated control variables and handles the balancing algorithm to provide proper switching sequence of IGBTs and thyristors. It is worth noting that the utilized balancing algorithm corresponds to the sorting method commonly employed for the conventional MMC [27–29]. An overall block diagram that explains and summarizes the proposed control algorithm is shown in Fig. 6. Based on the proposed algorithm, sizing of capacitors in SM is affected by nullifying each $\left(\phi_{ry}\right)$ as follows:

$$C_{SMy}=\frac{\sqrt{2}I_y^m N_{ry}}{\omega_o k V_{dcy} N_{ty}}\left(N_{ry}-N_{ry}\cos\alpha_y+N_{ty}\cos\alpha_y-N_{ty}\cos\left(\omega_0 T_{cy}+\alpha_y\right)\right) \tag{42}$$

Also, by substituting (18), (20) and (21) in (41), the sizing is modified into the following

$$C_{SMy}=\frac{4N_{ry}\cos\alpha_y\sqrt{\cos^{-2}\phi_{yy}-1}}{\pi\omega_o^2 L_y k N_{ty}}\left(N_{ry}-N_{ry}\cos\alpha_y+N_{ty}\cos\alpha_y-N_{ty}\cos\left(\omega_0 T_{cy}+\alpha_y\right)\right) \tag{43}$$

6. HVDC simulation validation

This section validates the proposed algorithm of zero reactive power circulation in the isolated monolithic modular thyristor-based DC-Hub in the field of HVDC using MATLAB/SIMULINK model. The simulation model is based on 3-port system with 401-Level, where each hybrid MMC arm has 400 HB-SMs and 40 FB-SMs. DC link voltage of 500 kV is chosen for all VSC-based HVDC networks. The parameters used in simulation are summarized in Table 1, where the SMs' capacitance is designed based on (42). Furthermore, the LC filter of each port is based on the criteria depicted in (25) and (28). Different healthy operation scenarios are studied for validation.

6.1. Bidirectional power flow at rated power

This subsection shows the uninterruptible operation of power flow reversal at the rated value of each port. The active and reactive power flow of ports 1, 2 and 3 are shown in Fig. 7 part (a). It can be observed that the power flow is from port 1 to ports 2 and 3 then the power flow is reversed at t = 0.5 s smoothly without any interruption.

Moreover, the reactive power is maintained at zero before and after power reversal. Furthermore, the DC link voltages and currents of each port are shown in Fig. 7 part (b). It is evident that the current reverses its polarity corresponding to direction of power flow. The DC link voltages remain unchanged due to the nature of VSC-based HVDC networks.

Table 1
Simulation prototype parameters.

Parameter	Description	Value
P_1	Rated power of port 1	500MW
$P_2 = P_3$	Rated power of ports 2 and 3	250MW
$V_{dc1} = V_{dc2} = V_{dc3}$	DC link voltage of port 1, 2 and 3	500kV
V_b	Rated RMS Voltage of common AC bus	430kV
f	Switching Frequency	450Hz
Thyristor part number	5STP 12F4200	–
L_1	LC Filter inductance of port 1	58mH
$L_2 = L_3$	LC Filter inductance of ports 2 and 3	117mH
C_1	LC Filter capacitance of port 1	0.65μF
$C_2 = C_3$	LC Filter capacitance of ports 2 and 3	0.325μF
$n_{t1} = n_{t2} = n_{t3}$	Transformer turns ratio	1 : 1
$T_{l1} = T_{l2} = T_{l3}$	Trapezoidal rise time	10μs
T_{dwell}	Sub-module step time	0.025μs
$T_{c1} = T_{c2} = T_{c3}$	Thyristor commutation Time	500μs
$N_{t1} = N_{t2} = N_{t3}$	Total number of SMs per arm	440
$N_{r1} = N_{r2} = N_{r3}$	Number of SMs for rated DC-link voltage	400
C_{SM1}	SM capacitance of bridge 1	8.3mF
$C_{SM2} = C_{SM3}$	SM capacitance of bridge 2 and 3	4.1mF

6.2. Partial power flow

This subsection validates the proposed algorithm during partial power flow. In this case, a step-change in the magnitude of the power flow from port 1 to ports 2 and 3 is applied. The amount of power flow is shown in Fig. 8 part (a). It can be observed that the rated power flow is from port 1 to ports 2 and 3, where it exhibits zero reactive power during rated power flow. After that, a step-change in the amount of power is applied at t = 0.5 s. It is notable that the reactive power remains zero. Furthermore, the AC output voltages along with AC bus voltage are shown in Fig. 8 part (b), where a change in firing-angle is observed at t = 0.5 s to accommodate the change in the magnitude of power flow. Additionally, it is evident that the capacitors' ripple in the SMs are maintained less than the criteria 10 % as shown in Fig. 8 part (c).

6.3. DC pole-to-pole fault

This subsection provides evidence that proves the capability of the continuous power flow in face of DC pole-to-pole fault at one of the ports. The power is assumed to be from port 1 to ports 2 and 3. A DC pole-to-pole fault is applied at port 2. The DC link voltages and currents are shown in Fig. 9 part (a). It can be observed that at the instant of fault initiation, the DC current of port 2 increases but limited by fault detection. Whereas the controller inserts the FB-SMs with their negative

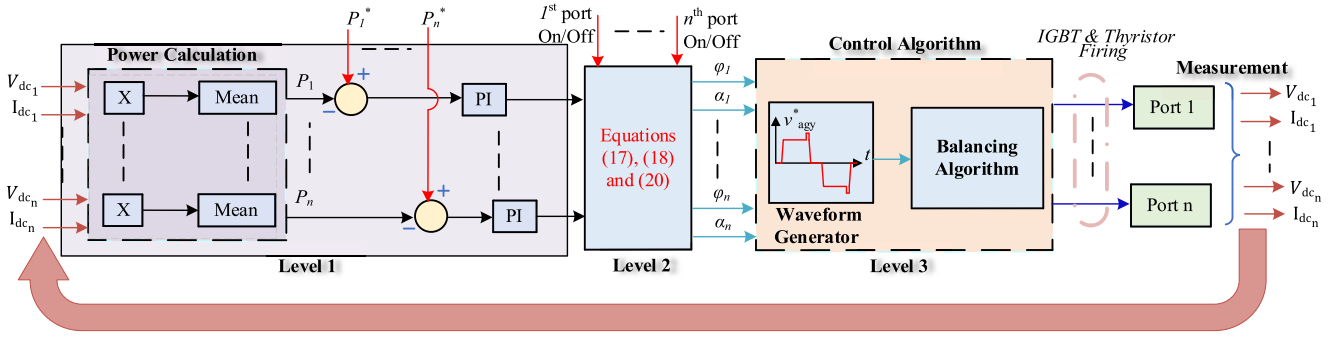


Fig. 6. Power flow control algorithm.

Fig. 7. Simulation of performance behavior of the proposed DC-DC converter at bidirectional power flow, (a) active and reactive power flow and (b) DC link voltages and currents.

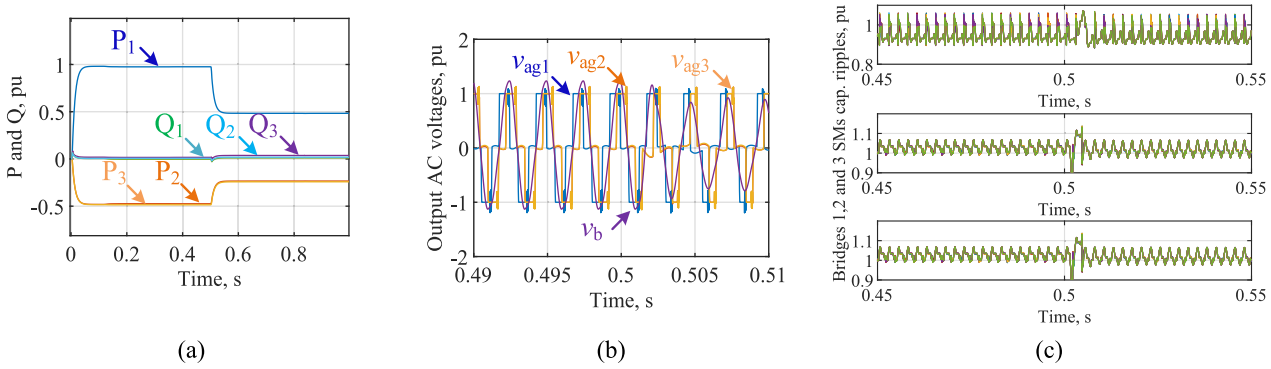


Fig. 8. Simulation results in case of partial power flow, (a) active and reactive power flow, (b) AC output voltages and (c) SMs capacitor voltages.

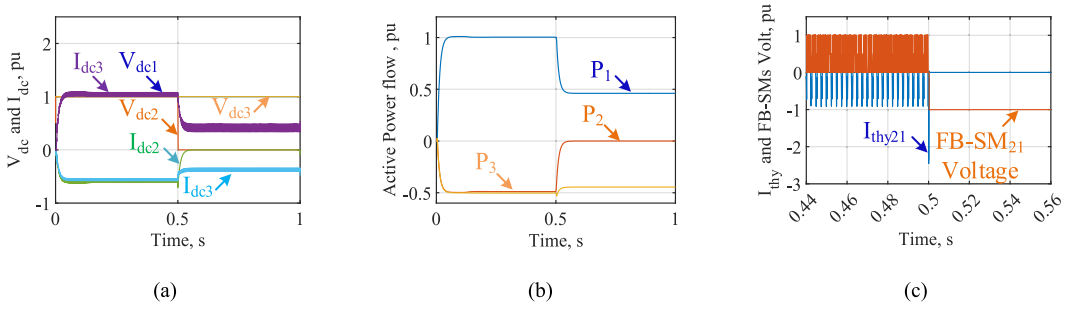


Fig. 9. Simulation results under unhealthy scenario, (a) DC-link voltages and currents, (b) Active power flow and (c) Arm 21 FB-SM voltage and thyristor current.

voltage polarity to suppress the rate of rise of the short-circuit current and force turn off the thyristors where the power flow is updated as shown in Fig. 9 part (b). At the instant of fault detection, the FB-SM voltage is reversed to limit the current and force turn-off the upper arm thyristors in bridge 2 as depicted in Fig. 9 part (c).

7. Experimental setup validation

A hardware test rig is designed for further validation of the proposed control technique. The block diagram of the overall experimental prototype is shown in Fig. 10, while the experimental test rig is shown in Fig. 11. The hardware test rig is composed of 3 ports, where converters are based on 3-Level for simplicity. Each hybrid MMC arm has 2 HB-SMs and 1 FB-SMs. Two thyristors connected back-to-back, are used for each upper arm. A DC link voltage of 150 V at all three grids. The parameters are listed in Table 2. Moreover, the LC filter is based on the criteria provided in (25) and (28). Healthy scenarios are employed at different power flow conditions. Also, an unhealthy scenario is tested to verify the capability of DC fault blocking and reliability of the proposed DC-Hub based on monolithic modular thyristor-based converter.

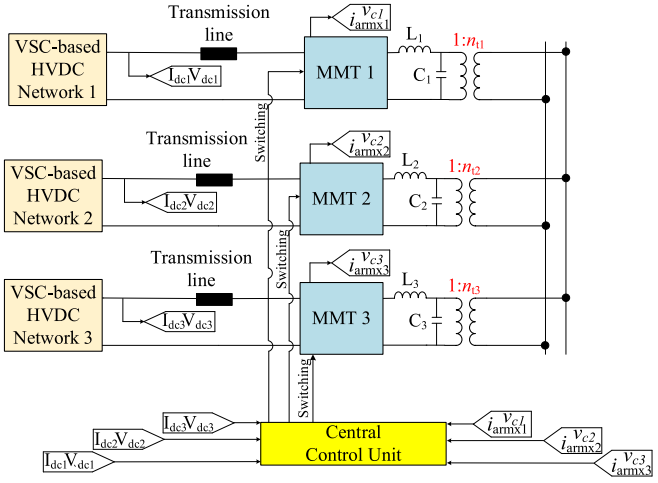


Fig. 10. Overall block diagram representing control and hardware experimental test rig.

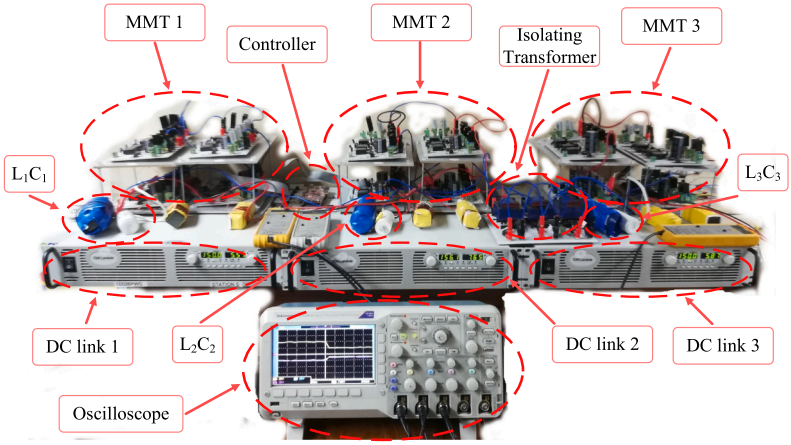


Fig. 11. Experimental test rig.

Table 2
Hardware prototype parameters.

Parameter	Description	Value
P_1	Rated power of port 1	$400W$
$P_2 = P_3$	Rated power of ports 2 and 3	$200W$
$V_{dc1} = V_{dc2} = V_{dc3}$	DC link voltage of ports 1, 2 and 3	$150V$
f	Switching Frequency	$450Hz$
Thyristor part number	BT152	–
L_1	LC Filter inductance of port 1	$3.9mH$
$L_2 = L_3$	LC Filter inductance of ports 2 and 3	$7.9mH$
C_1	LC Filter capacitance of port 1	$5.4\mu F$
$C_2 = C_3$	LC Filter capacitance of ports 2 and 3	$2.7\mu F$
n_t	Transformer turns ratio	1 : 1
$T_{l1} = T_{l2} = T_{l3}$	Trapezoidal rise time	$10\mu s$
T_{dwell}	Sub-module step time	$5\mu s$
$T_{c1} = T_{c2} = T_{c3}$	Thyristor commutation Time	$200\mu s$
N_{thy}	Number of thyristors per Arm	2
$N_{t1} = N_{t2} = N_{t3}$	Total number of SMs per arm	3
$N_{r1} = N_{r2} = N_{r3}$	Number of SMs for rated DC link voltage	2
$C_{SM1} = C_{SM2} = C_{SM3}$	SM capacitance of bridges 1, 2 and 3	$330\mu F$
L_{arm}	Arm inductance	$360\mu H$
P_1	Rated power of port 1	$400W$

7.1. Bidirectional power flow at rated power

To verify the bidirectional power flow capability with zero reactive power, the power flow between port 1, 2 and 3 is reversed at the rated value. The active and reactive powers are shown in Fig. 12 parts (a) and (b), respectively.

It can be inferred from the result that the power flow reversal is uninterruptible and zero reactive power is maintained after reversal. Moreover, the AC output voltages and AC bus voltage are shown in Fig. 12 part (c). It can be observed that the phase shift changes its sign with respect to AC bus for power reversal whilst the firing-angles are maintained constant.

7.2. Partial power flow

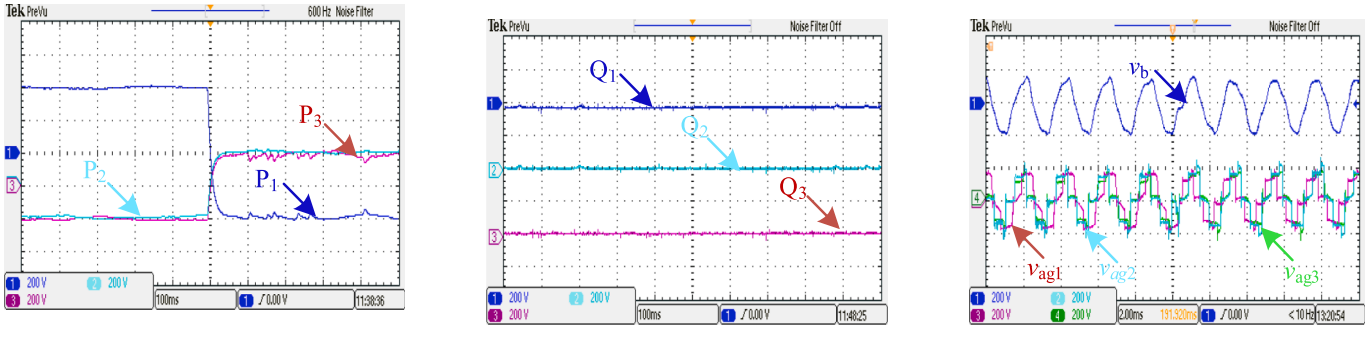
The direction of power flow is assumed from port 1 to ports 2 and 3. A step change is applied, where the amount of power is reduced to half the rated value for all ports. The active and reactive power are shown in Fig. 13 parts (a) and (b).

It can be observed that the change in active power is instantaneous which proves the continuity of power flow against any step change in its magnitude. On top of that, the reactive power remains zero before and after the step change. The output AC voltages and AC bus are shown in Fig. 13 part (c). It can be inferred that the firing-angle changes corresponding to accommodate the change in power flow magnitude.

7.3. DC pole-to-pole fault at one of the ports

The power flow is assumed from port 1 to ports 2 and 3 where a DC fault occurs at port 2. The amount of active power flow at ports 1, 2 and 3 are shown in Fig. 14 part (a). As well as the submodule voltage behavior of the faulty port is shown in Fig. 14 part (b).

It can be observed that at the instant of the fault detection, the central control unit changes the reference value of port 1 to supply only port 3. On the other hand, The MMC arm voltage of FB-SM and the corresponding thyristor current in converter of port 2 are depicted in Fig. 14 part (b). It is clear that the MMC arm generates negative voltage



(a) (b) (c)

Fig. 12. Experimental results at rated power flow reversal, (a) active power flow at ports 1,2 and 3, (b) reactive power flow at ports 1,2 and 3, and (c) output AC voltages and AC bus.

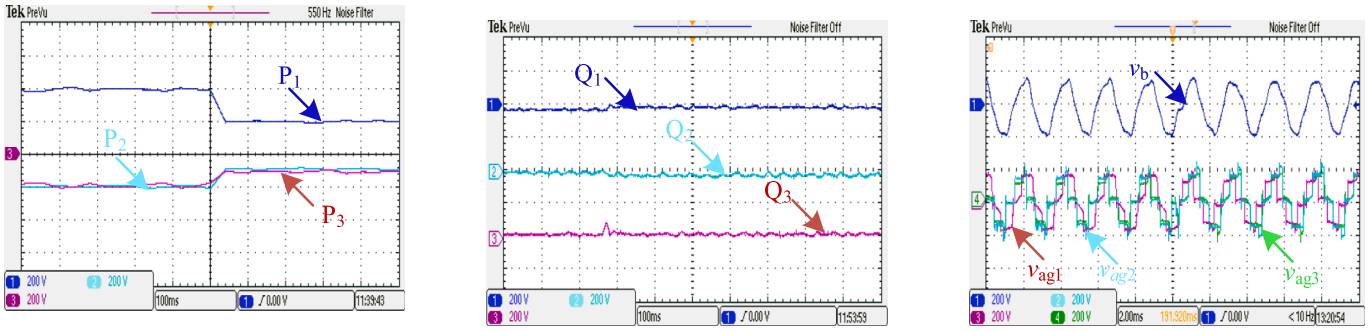


Fig. 13. Experimental results at partial power flow, (a) active power flow at ports 1,2 and 3, (b) reactive power flow at ports 1,2 and 3, and (c) output AC voltages and AC bus.

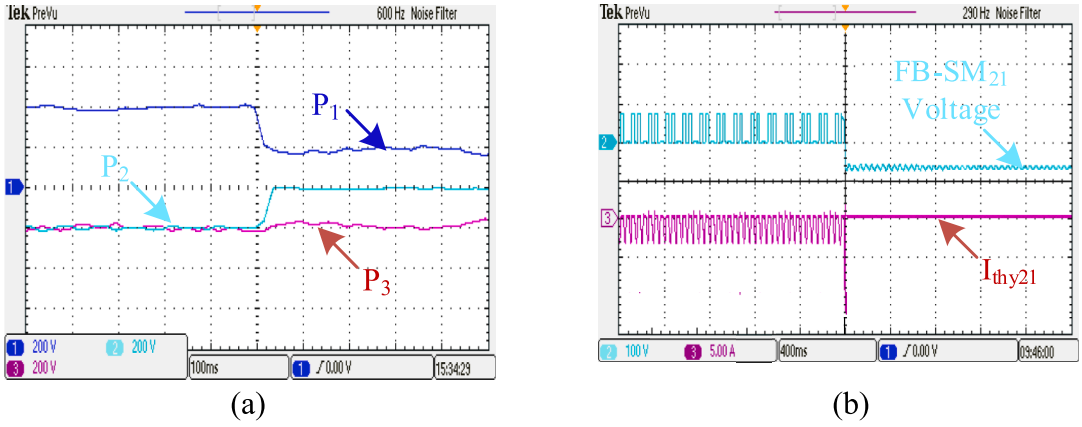


Fig. 14. Experimental results at DC pole-to-pole fault, (a) Active power flow of ports 1, 2 and 3, and (b) FB-SM voltage and thyristor current.

at the instant of fault detection, where the thyristor current is decreased to zero. Henceforth, reliability of power flow is achieved during fault.

8. Comparative study

An extensive comparative analysis is conducted to highlight the advantageous features of the proposed monolithic building unit compared to other pre-existing building units, specifically with regard to number of IGBTs, total semiconductor losses, overall semiconductor cost, and number of SM capacitors. The converters subjected to comparison encompassed HB-MMC [30], FB-MMC [31,32], CTB [33,34], TAC /SSMMC [35–37], and TH-MMC (third variation described in the patent) [38,39]. It is important to note that the comparison is performed under the assumption of a single-phase configuration. The loss assessment is carried out at the rated power, employing the trapezoidal waveform technique in conjunction with the LCL filter for all studied converters. As a result, the current and the voltage are in phase, maintaining zero reactive power circulation at the rated power. Additionally, due to the utilization of the trapezoidal waveform control, semiconductor switching occur exclusively during the ramp time of the waveform, rendering it negligible for all converters.

The calculations for average conduction losses are derived from [40] and can be expressed as follows:

$$P_{cond_{avg}} = \frac{1}{T_b}\int_0^{T_b} p_{cond_{inst}}(t)dt \tag{44}$$

where the instantaneous conduction losses ($p_{cond_{inst}}$) can be obtained as follows:

$$p_{cond_{inst}}(t) = v_{cond}(i_x(t))i_x(t)D(t) \tag{45}$$

where $i_x(t)$ represents the instantaneous current flowing through the power devices, $D(t)$ represents the duty ratio, which relies on the utilized modulation technique, while the conduction voltage (v_{cond}) can be derived as follows:

$$v_{cond}(i_x(t)) = V_{cond0}(T_{ref}) + i_x(t)r_{cond}(T_{ref}) \tag{46}$$

The coefficients V_{cond0} and r_{cond} are acquired from the datasheet of each semiconductor device, while T_{ref} is uniformly set to 125 degrees for all devices used. The comparative analysis is conducted using practical ABB devices, as described in Table 3. A 60 MW system with a ±30 kV DC link is established, with a switch or thyristor voltage of 2 kV. The summary of the comparative analysis among these converters is presented in Table 4.

When considering the number of SM capacitors, HB-MMC and FB-MMC employ the highest quantity, while the other topologies use approximately half the count, except for the CTB topology, which has the lowest count. However, it should be noted that the CTB converter has a significant drawback of requiring two DC link capacitors. In terms of cost considerations, the FB-MMC has the highest cost, while the proposed converter and TAC/SSMMC offer the most economical solutions. Additionally, the proposed converter has the lowest overall semiconductor losses and only requires two arm inductors per bridge. Based on the aforementioned discussion, it is clear that the proposed converter demonstrates the lowest total semiconductor losses and the least overall semiconductor cost. This highlights that the proposed building unit is a superior solution for the DC-Hub for interconnecting different VSC-based HVDC networks. To summarize the strength points of the

Table 3
ABB semiconductors parameters.

Semiconductor type	IGBT Module5SNA 1500G450350		Bidirectional Thyristor5STB 18 N4200	Phase Control Thyristor5STP 12F4200	Diode5SDF 13H4501
	IGBT	Diode			
Max voltage (V)	4500		4200	4200	4500
RMS Current (A)	1500		3020	1860	1900
On-state voltage (V) at 125 °C at 1500 A	3.55	2.8	1.4	1.85	2.1
On-state resistance at 125 °C (mΩ)	0.1	0.1	0.285	0.545	0.48
Cost/unit ($)	2162.41		1691.39	296.53	741.86

Table 4
Key feature comparison of considered converters.

Converter Type	HB-MMC [30]	FB-MMC [31,32]	CTB [33,34]	TAC/SSMMC [35–37]	TH-MMC [39,41]	Proposed converter
No. of SM Capacitors	30 × 4	30 × 4	15 × 2	30 × 2	15 × 4	33 × 2
Type of SWs	IGBT	IGBT	IGBT	IGBT	IGBT, SCR, Diodes	IGBT & SCR
No. of Bidirectional Thyristors	None	None	None	None	None	30x2 =60
No. of Thyristors with Antiparallel Diodes	None	None	None	None	15 × 4 = 60	None
No. of Limb Inductors	4	4	2	2	4	2
No. of DC Link Capacitors	None	None	2	None	None	None
Losses of HB-SMs	283.18 kW	None	None	141.85 kW	None	165.4 kW
Losses of FB-SMs	None	509.1 kW	0.442 kW	None	254.54 kW	None
Director Switches	None	None	282.66 kW	141.33 kW	None	None
Losses of Thyristors	None	None	None	None	103.36 kW	66.73 kW

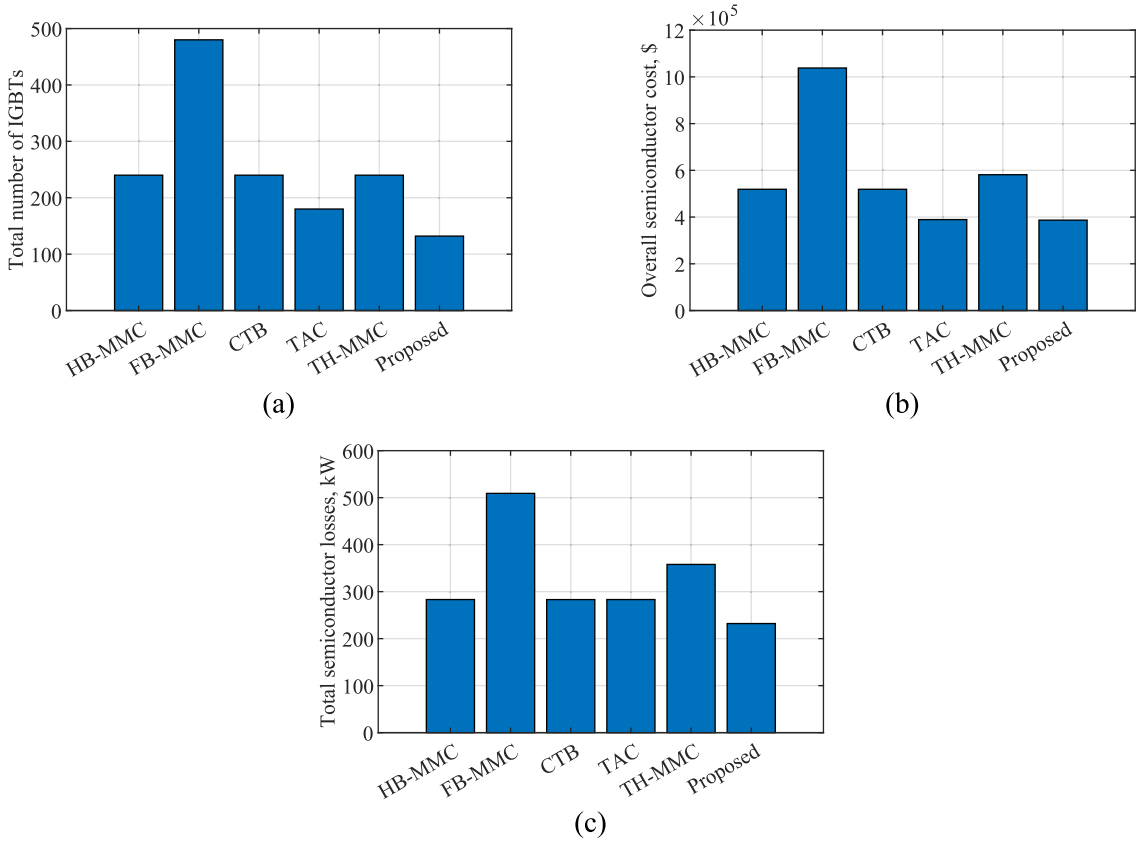


Fig. 15. Bar chart representation of (a) total number of IGBTs, (b) overall semiconductor cost and (c) overall semiconductor losses.

proposed system, Fig. 15 parts (a), (b) and (c) highlights the advantages of the proposed building unit in points of total number of IGBTs, overall cost and overall semiconductor losses.

9. Conclusion

In this paper, a new approach has been proposed for a modular multilevel converter unit in the VSC-based DC-Hub, utilizing thyristor arms to reduce the number of semiconductors while maintaining lower

losses and enabling bidirectional power flow. The design of the LC reactive power filter was also discussed in detail. Furthermore, a novel control technique was introduced to eliminate reactive power circulation across the entire power range, resulting in reduced semiconductor footprint. The implementation of a forced-commutation technique enables DC fault blocking capability, enhancing power flow reliability and ensuring uninterrupted power supply even during emergencies at one port. When a faulty bridge is detected, it is blocked, and the central control unit adjusts its reference accordingly based on power sharing requirements. Additionally, a comprehensive mathematical derivation was provided to ensure the modularity of the DC-Hub building unit and optimal parameter sizing. To validate the proposed control algorithm, MATLAB/SIMULINK simulations and a small-scale experimental model are developed. Finally, a comparative study was held among the proposed converter in comparison with HB-MMC, FB-MMC, CTB, TAC and TH-MMC, it was proven that the proposed converter unit is superior in the aspects of total number of IGBTs being used (1 3 2) while the closest one is the TAC which required a total of (1 8 0) which highlights that the proposed building unit is approximately 30% less IGBTs. Also, it was shown that the proposed building unit yields the smallest semiconductor losses (232.1kW), whereas the closest converters are HB-MMC, CTB and TAC with losses (283.18kW) which highlights that the proposed building unit for DC-Hub yields reduced losses approximately (20%).

CRediT authorship contribution statement

Mohamed G. Abdel-Moneim: Writing the analytical approach of the proposed idea. **Mohamed Mansour:** Building the simulation verification setup and providing the experimental results through a scaled down hardware test rig. **F. Alsokhiry:** Providing the literature review and insights. **Ayman S. Abdel-Khalik:** Supervision over the experimentation setup. **Khalifa AlHosani:** Funding the resources of the paper publication and experimentation. **Khaled H. Ahmed:** Supervision over the analytical approach of the proposed idea.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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