RFSoC with PYNQ: Research, Development, and Learning

Louise Crockett, Bob Stewart : University of Strathclyde, Glasgow, Scotland, UK.

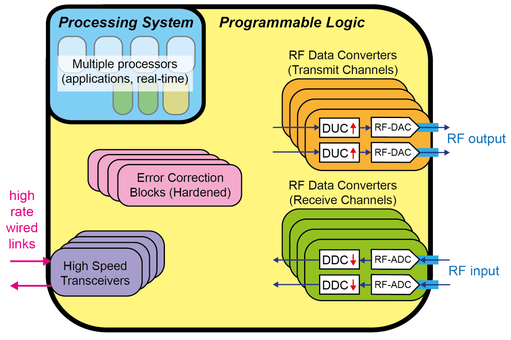
StrathSDR

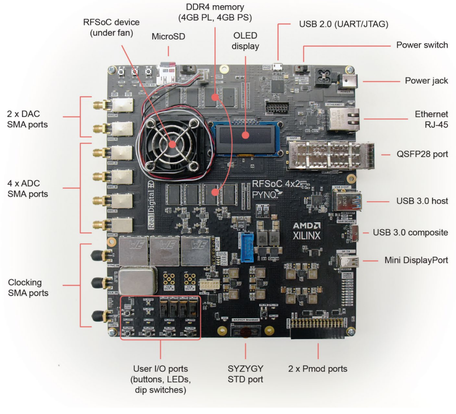
Over the past ~5 years, StrathSDR has worked extensively with the AMD Zynq UltraScale+ Radio Frequency System on Chip (RFSoC). This platform has proven to be a great tool for research, development, and learning around Software Defined Radio (SDR), in conjunction with the PYNQ software / hardware framework. The poster features examples and highlights community resources that we have developed.

A Radio Frequency System on Chip

A major advantage of the RFSoC architecture is that all of the processing takes place on the same chip. This means that high with high sampling rates can be moved around efficiently.

The RF Data Converters provide up to 16 transmit and 16 receive channels, depending on the device.





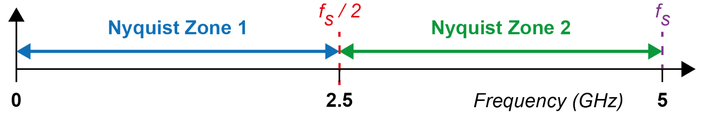
Several RFSoC development boards are available. The **RFSoC 4x2** board is an initiative of *AMD University Program* and is available at relatively low cost for academic institutions.

The RFSoC 4x2 includes:

- 4 transmit channels
- 2 receive channels
- Peripheral interfaces
- High speed interfaces.

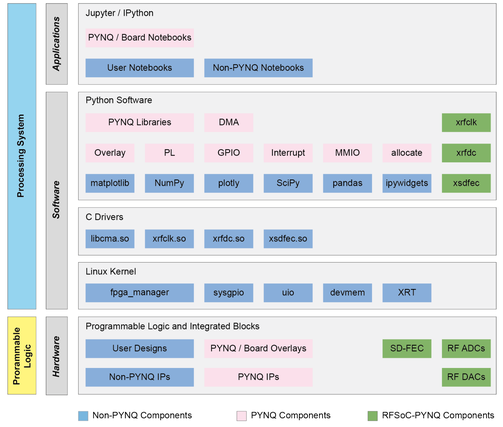
Direct RF Sampling at "GHz" Rates

The RF-DACs and RF-ADCs can sample at up to 10 Gsps and 5 Gsps respectively. Both can operate in the 2nd Nyquist zone, so most low / mid band signals can be directly generated and received *without* analogue modulation and demodulation.



PYNQ – Python Productivity for Zynq

PYNQ is a framework of software and hardware elements, created by AMD to make working with their SoC devices easier. The user interface is Juptyer, running on the RFSoC with interaction via a web browser. Engineers use drivers to interact with on-chip hardware resources, and can create software and visualisations, as well as developing their own hardware designs using custom blocks in the PL.



RFSoC-PYNQ – Teaching & Learning; Resources

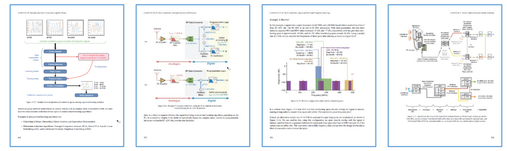
In 2023, StrathSDR published a book in collaboration with AMD. The book is a reference and learning resource for students and professionals working with RFSoC. It includes accompanying practical materials (reference designs, Jupyter notebooks, simulation examples) and can be downloaded as a **free PDF** from:

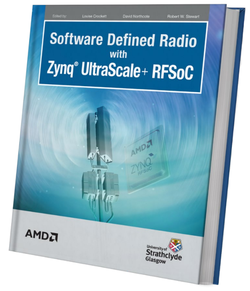
www.rfsocbook.com

Further resources are available from our GitHub repo:

www.github.com/strath-sdr

We find PYNQ to be an accessible "way in" for education.





RFSoC-PYNQ – R & D Examples

Jupyter was used to make an interactive **Frequency Planning** tool (bottom). It enables designers to select the best clock and sampling parameters to avoid frequency domain artefacts that would adversely affect signal quality (non-linear analogue behaviour, PLL spurs, and so on).

PYNQ-RFSoC is the basis of a **single-chip Spectrum Analyser** application (right). The RF-ADCs capture radio data which is then displayedas a spectrum and spectrogram. This application features a Voila dashboard to make user interaction easy and intuitive. An extended feature of this design is to overlay spectrum allocations from the regulator database.

Various different communications designs and subsystems can be created, with user control, the ability to capture live data from the chip, and display visualisations.

Other examples designs include QPSK, BPSK, OFDM radios, use of the SD-FEC block for 4G / 5G error correction coding and decoding, and high speed offload of radio data from the RFSoC 4x2 to a host computer. An architecture for the **OFDM radio** is shown here (bottom right).