# EVALUATION OF TRAVELLING WAVE PROTECTION PERFORMANCE IN CONVERTER-DOMINATED NETWORKS

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## Abstract

This paper presents a comprehensive study to investigate the travelling wave protection performance in networks with high penetration of Converter-Based Resources (CBRs). Representative network models are developed in the sub-step environment of the Real-Time Digital Simulator (RTDS) and realistic Hardware-in-the-Loop (HiL) tests are conducted on a pair of travelling wave relays (TWRs) to emulate realistic system and fault scenarios. The studies have been conducted in two stages: firstly, systematic tests with a total number of 300 cases have been conducted to have a high-level assessment of TWRs' performance under different fault conditions, e.g. varied fault types, fault positions, Fault Inception Angles (FIAs), and fault resistances; and secondly, detailed investigation has been conducted on selected and representative cases to understand the impact of various factors, e.g. the line-end transformer, system fault levels, converter controls and external faults, on the protection performance. Based on the test results and analysis, it was found that the performance of the TWR is largely unaffected by the variation of system fault levels and converter control strategies, but the connection of the line-end transformer and the low FIAs present challenges for the healthy operation of TWRs in some conditions. Although the tests were conducted for a pair of specific commercially available TWRs, the results have been analysed in a generic manner, so the findings will not only facilitate understanding the benefits/limitations of travelling wave protection in the network with high amounts of CBRs, but also provide a valuable reference for system operators to select the protection solutions in the future.

## 1 Introduction

Motivated by the ambitious target of achieving net-zero operation, a rapid increase in renewable generation can be observed in the global energy market. Those Renewable Energy Sources (RESs) are conventionally connected to the power system using power electronic converters. Compared to a well-understood fault response of Synchronous Generators (SGs), the fault signatures of CBRs are highly dependent on their embedded controllers, which are determined by the local grid code requirements, implemented control frame and current limiting strategy [1]. Additionally, because of the limited thermal capability of power electronic devices, the CBRs cannot generate fault currents higher than 1.5 pu, which is significantly smaller than the short-circuit currents from SGs [2]. The non-unified and limited fault currents from CBRs can pose severe challenges to the reliable operation of existing AC protection devices. For example, as reported in [3] - [5], the connection of CBRs can lead to a range of protection system issues, such as the failed detection and/or coordination of over-current protection, the under/over-reach and phase selection of distance protection, and the failed operation of the differential protection during internal faults.

Unlike conventional phasor-based protection, travelling wave protection does not rely on the fundamental-frequency voltages and currents during faults. Instead, it uses the high-frequency transients generated by faults, so its performance is expected to be largely unaffected by the changes in system fault levels and converter control strategies [6]. Additionally, given the fast propagation speed of travelling wave (TW) (i.e., close to the speed of light in overhead lines), the TWR can detect faults significantly fast (i.e., typically a few milliseconds [7]), which is difficult to be achieved for the phasor-based relays. For the benefits, the research on travelling wave protection has raised sufficient interest of scholars and engineers such as in [8][9]. However, those works are based on pure-simulation-based studies, and the HiL tests have not been conducted. The HiL-based tests are implemented in [10] - [14] to evaluate the functions and performance of the TWRs. In [10], the playback function of the relay is used by injecting the pre-recorded fault event files. The approach does not require the physical test setup, but it limits the flexibility and repeatability of tests [11]. The simulator-based HiL tests are implemented in [11] - [14] to address this test limitation, where the injected currents are created from real-time simulators such as the RTDS. Compared to the playback function-based tests, the simulator-based tests have the advantage of changing the system and fault parameters flexibly, and thus, it enables injecting a large number of tests in real time [11]. However, all works in [11] - [14] only study a limited number of cases and the impacts of CBRs on travelling wave protection have not been considered.

In this paper, comprehensive and realistic HiL tests are conducted to evaluate the performance of the travelling wave

differential protection function in a pair of commercially available relays, which includes a systematic test with 300 cases to get an overall understanding of relay performance in different system and fault conditions (i.e., different fault types, locations, resistances, FIAs) and a detailed test with selected cases to identify the impacts of other factors (i.e., converter-interface transformer, converter control, fault level and external fault). The studied network model is developed in the sub-step environment of the RTDS with a simulation step of 4 $\mu s$ and the model of Frequency-Dependent Phase Domain (FDPD) Line is implemented to accurately replicate the travelling wave responses in a real system, which are designed based on the realistic line and tower data of the overhead line between the Spittal and Thurso South substations in Scotland.

The rest of the paper is structured as follows: Section 2 overviews the principles of the travelling wave differential module of the tested relay; Section 3 proposes the network model in RTDS and the HiL setup in the tests; Section 4 discusses the information of the studied cases and the HiL test results; and the conclusion is provided in Section 5.

## 2. Travelling Wave Differential Scheme

Three security layers are applied in the investigated TW differential scheme to distinguish the internal and external faults and to ensure protection security which includes the judgement based on the results of travelling wave differential protection (i.e., 1st layer), travelling wave-based fault location strategy (i.e., 2nd layer) and polarity comparison-based algorithm (i.e., 3rd layer).

### *2.1 Travelling Wave Differential Protection*

Compared to the Voltage Transformers (VTs), the frequency bandwidth of Current Transformers (CTs) is more adequate to capture the TWs [15], therefore, the current travelling waves measured by CTs are used as the inputs of the studied TWRs.

In the studied TW differential scheme, two terms, i.e., the operating term and the restraining terms, are defined in (1) to (4), where $I_{TWR1}$ and $I_{TWR2}$ are the current TWs measured by TWR1 and TWR2; $I_{OP}$ is the operating term of travelling wave differential protection; $I_{RT-TWR1}$ and $I_{RT-TWR2}$ are the restraining terms of TWR1 and TWR2; $\Delta t$ is the time difference between the initial travelling waves of TWR1 and TWR2, which introduces a time shift to align the initial travelling waves of both relays; $TWLPT$ is the travelling wave line propagation time, which is defined as the time of travelling wave propagating through the whole length of the protected line; $I_{RT}$ is the restraining term, which is obtained by applying the 'maximum' logic to $I_{RT-TWR1}$ and $I_{RT-TWR2}$.

$$I_{OP(t)} = I_{TWR1(t\pm\Delta t)} + I_{TWR2(t)} \quad (1)$$

$$I_{RT-TWR1(t)} = \left|I_{TWR1(t-TWLPT)} - I_{TWR2(t)}\right| \quad (2)$$

$$I_{RT-TWR2(t)} = \left|I_{TWR2(t-TWLPT)} - I_{TWR1(t)}\right| \quad (3)$$

$$I_{RT(t)} = max\left(I_{RT-TWR1(t)}, I_{RT-TWR2}(t)\right) \quad (4)$$

The travelling wave scenarios under internal and external faults are shown in Fig. 1 (a) and (b), which are used to facilitate the understanding of (1) to (4). From Fig. 1 (a), the

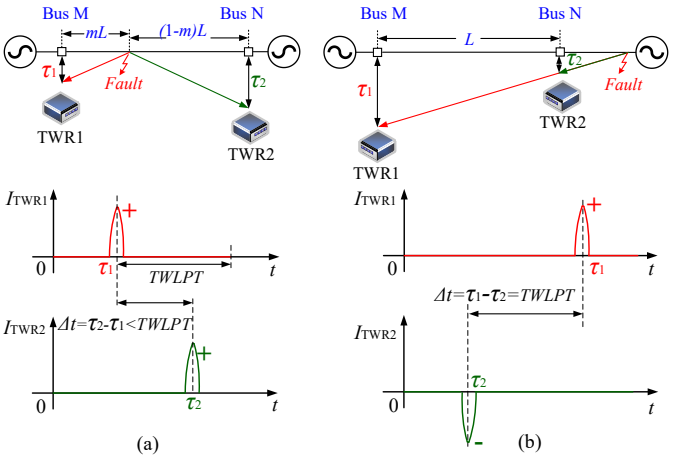


Fig. 1 Travelling waves measured by TWR1 and TWR2 in, (a) internal faults, and (b) external faults at Bus N side

polarities of $I_{TWR1(\tau_1)}$ (i.e., $I_{TWR1(t+\Delta t)}$ in (1)) and $I_{TWR1(\tau_2)}$ (i.e., $I_{TWR2(t)}$ in (1)) in internal faults are both positive, which will increase the magnitude of the operating term, $I_{OP}$, to a great value, and further result in the successful fault detection of the travelling wave differential scheme. For the external fault, such as in Fig. 1 (b), the polarities of initial TWs are opposite, which results in a very small operating term after summing. While the maximum magnitude of the restrain term will be close to the sum of the initial TWs of two relays. Therefore, the operation of the travelling wave differential protection will be restrained for external faults.

### *2.2 Travelling Wave Fault Location*

The applied travelling wave fault location algorithm (i.e., the 2nd security layer) is realised using the double-ended travelling wave-based method as proposed in (5)(6), where the lattice diagram in Fig. 1 (a) is used in the derivation.

$$mL = \frac{L}{2}\left(1 + \frac{\tau_1 - \tau_2}{TWLPT}\right) \quad (5)$$

$$(1-m)L = \frac{L}{2}\left(1 - \frac{\tau_1 - \tau_2}{TWLPT}\right) \quad (6)$$

For internal faults, the values of $m$ and $(1-m)$ in (5) and (6) range between 0 to 1 (not including 0 and 1), while the calculated $m$ will equal either 0 or 1 in external faults. By applying this logic, the relay will not operate when the results of layer 1 and layer 2 are not aligned.

### *2.3 Polarity Comparison-based Algorithm*

The implemented 3rd security layer is developed to address the protection challenge caused by the faults at the parallel line (i.e., as the fault condition in Fig. 2), where the propagation path and polarities of initial TWs are highlighted.

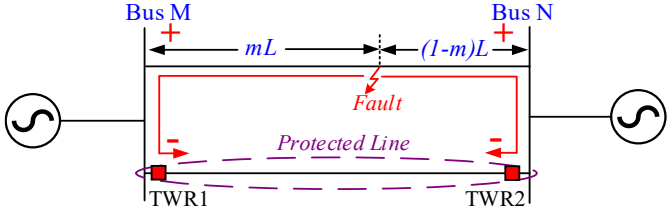


Fig. 2. Current TWs for faults at the parallel line

For the fault in Fig. 2, where the TW polarities of TWR1 and TWR2 are the same and the time difference between the two relays is smaller than the TWLPT, the relays will detect the fault at the parallel line as an internal fault and trip the protected line falsely. To avoid maloperation, the 3rd security layer is developed by comparing the polarities of initial current TWs and the pre-fault voltage at the fault location.

For internal faults on the protected line (i.e., assuming a positive pre-fault voltage at the fault point), the reduced voltage at the fault point will generate a negative polarity TW propagating towards two ends of the protected line. Because the positive direction in the TW measurement is towards the inner side of the protected line, positive TWs are expected for internal faults. However, TWs with the negative polarity of TWR1 and TWR2 are induced by faults on the parallel line (as shown in Fig. 2), which are against the polarity of the positive pre-fault voltage. Therefore, it can be concluded that the consistent polarities between the pre-fault voltage and the initial TWs are observed in internal faults, while opposite polarities exist for faults on the parallel line. It needs to be highlighted that the analysis in Section 2.3 assumes the pre-fault voltage is positive, but the above conclusion also exists for faults with a negative-polarity pre-fault voltage at the fault point.

## 3 Model Development and HiL Setup

### *3.1 Network Model Development in RTDS*

The sub-step RTDS network model used in the tests is presented in Fig. 3. The model can be configured flexibly to represent systems with different fault levels, CBRs with varied control strategies, and faults with different locations, FIAs, resistances and types.

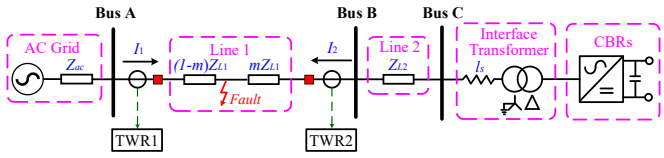


Fig. 3 Sub-step network model used for travelling wave relay testing

*3.1.1 Modelling of the Converter Control Strategy:* So far, Great Britain's (GB's) grid code only requires injecting positive-sequence active and reactive currents during faults (i.e., balanced current controller), where the amounts of injected currents are dependent on the retained voltage level and the pre-defined injection curve. The Balanced Current controller simplifies the design of the converter control as only the positive-sequence currents are regulated during faults, but it could result in various issues because of the lack of negative-sequence currents such as the overvoltage of the healthy phases and the DC-side voltage oscillation [16]. Therefore, the injection of negative-sequence current has been formally suggested in some newly published international standards, such as in the IEEE Std 2800-2022 [17]. Considering the future trend of the negative-sequence current injection and the possibility of different converter operating modes, a flexible controller reported in [4] is implemented in the developed converter model to realise different converter operating modes including the balanced current mode, constant active power mode and constant reactive power mode, and thus allow the investigation of the converter controller's impact on the protection scheme under test.

*3.1.2 Modelling of the FDPD Line:* As reported in [13], the FDPD line model can represent the dynamic behaviour of TWs accurately over a wide range of frequencies, therefore, the FDPD model is selected in RSCAD (i.e., the software intended for RTDS) to represent Line 1 and Line 2 in Fig. 3. To validate the accuracy of line configuration, the calculated impedances from RSCAD are compared to the realistic line data as in Table 1, where the $Z_L^+$ and $Z_L^0$ are the total positive and zero-sequence line impedances, and $X_c^+$ and $X_c^0$ are the total positive- and zero-sequence capacitive line reactances.

Table 1 Calculated results from RSCAD and realistic line data

| | $Z_L^+$ (Ω) | $Z_L^0$ (Ω) | $X_c^+$ (Ω) | $X_c^0$ (Ω) |
|---|---|---|---|---|
| RSCAD | $5.1\angle 84.5^\circ$ | $13.5\angle 81.0^\circ$ | 29602.1 | 42576.2 |
| Realistic Data | $5.1\angle 84.6^\circ$ | $12.3\angle 81.0^\circ$ | 29342.7 | 40584.1 |

As presented in Table 1, the difference between the simulated positive-sequence line impedance and capacitive reactance is neglectable and a minor difference exists between the zero-sequence impedance and capacitive reactance. As discussed in [18], the zero-sequence parameters of a line are highly dependent on the earthing resistance, which changes with the soil type, temperature, and moisture content in the soil. In this study, the ground resistivity is set to $1000\ \Omega \cdot m$, which is one of the typical values defaulted in the RSCAD software to emulate the dry sandy and gravel earthing conditions.

*3.1.3 Modelling of Line Termination:* When TWs encounter the discontinuity points in the overhead line such as the busbar and transformers, the incident current TWs will be reflected. The reflection factors of current TWs are depicted in (7), where $I_{in}$ and $I_{re}$ are the incident and reflected current TWs, $Z_C$ is the characteristic impedance of the overhead line and $Z_T$ is equivalent impedance behind the discontinuities.

$$\Gamma_I = \frac{I_{re}}{I_{in}} = \frac{Z_C - Z_T}{Z_C + Z_T} \tag{7}$$

From (7), the reflections of current TWs are dependent on the combined effect of the line characteristic impedance and the equivalent impedance behind the discontinuities such as the busbar and transformer in Fig. 3. Therefore, it is critical to model the line terminating condition accurately in TWR tests.

When testing the phasor-based protection, the AC grid is conventionally simplified as an ideal AC source with a lumped serial impedance. However, such simplification can result in unrealistic reflections of TWs at the line terminal since that lumped source impedance will have significant impacts on the termination impedance behind the busbar and further affect the magnitude of the reflection factor [13]. Therefore, this paper adopts another way to model the source impedance (i.e., the $Z_{ac}$ in Fig. 3), where the source impedance is represented using a section of the FDPD line and its magnitude can be controlled by governing the line length. This representing approach has also been implemented and validated in the RTDS-based TWRTs conducted by the RTDS company [19]. Except for the modelling of the source impedance, the way to

model the interface transformer between the converter and the overhead line is also important in travelling wave relay tests. As reported in [20], the power transformer has a high characteristic impedance for TWs, which can significantly reduce the magnitude of the TWs measured by the TWR at the converter side (i.e., the TWR2 in Fig. 3) and thus lead to the failed operation of TWRs. To further reflect the high-frequency effects of the transformer on TWs, a serial inductor, i.e., the $l_s$ in Fig. 3, was connected in the network to represent the internal impedance of transformer, whose impedance changes with the frequency variation. Additionally, to further analyse the impact of other factors in addition to the potential failed tripping resulting from the transformer, another segment of the overhead line, i.e., Line 2 in Fig. 3, was added to the network model, which could provide a time shift to avoid the full overlap of the incident and reflected travelling waves detected by the TWRs.

### *3.2 HiL Setup for Travelling Wave Relay Tests*

The overall HiL setup for relay tests is presented in Fig. 4, where the developed network model in RSCAD is simulated in real time using the NovaCor simulator. The voltages and currents are measured at two ends of the protected line, where the VT and CT are represented using the gain blocks in RSCAD as the practice in [13][19]. Given the fact that the voltage range of the analogue GIGA -Transceiver Analogue Output (GTAO) card is ±10V, the voltage and current from the gain models are further scaled down by a scaling factor defined in the virtual GTAO model so that they are within the required range and can be appropriately output by the GTAO card. In travelling wave relay tests, the analogue amplifiers are not used (and not required) as their limited bandwidth will attenuate the high-frequency travelling waves of the voltage and current. Instead, a dedicated low-level interface with a fixed voltage and current gains of 73.44 and 64.67 was supplied by the vendor and used to connect the GTAO outputs and the relay low-level inputs. The fibre-based communication link was created between two travelling wave relays to transmit the 1 MHz voltage and current measurement. The relay tripping output and other signals of interest are fed back to the NovaCor rack by the Gigabit-Transceiver Front Panel Interface (GTFPI) card, which is monitored and recorded for evaluating the performance of the investigated TW relays.

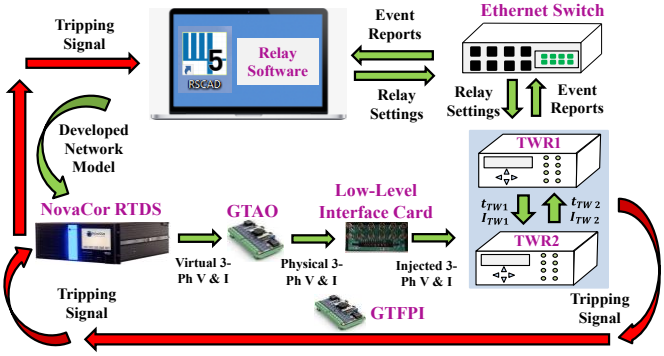


Fig. 4 HiL setup for lab-based travelling wave relay tests

In addition, to facilitate the testing of a large number of cases, the simulation and data collection process are automated by a set of scripts developed in RSCAD. Furthermore, MATLAB files have also been developed to automatically analyse the recorded testing results, which can import the recorded data, interpret the tripping action, calculate the tripping time, and indicate whether the performance has met specified tripping requirements.

## 4 Results and Analysis

This section presents cases to evaluate the TWR's performance, which includes systematic tests with a total number of 300 cases and detailed tests with selected cases.

### *4.1 Results of Systematic Tests*

*4.1.1 Cases in the systematic tests:* The network in Fig. 3 is implemented in the systematic tests, where parameters of the studied network are presented in Table 2, and a grid-following converter (GFL) is connected to the power system. In systematic tests, the GFL only injects the positive-sequence currents during faults by following the equations in (8) and (9), which is designed based on the injection curve in the GB's grid code [21]. In (8) and (9), the $i_{qr}^{+}$ and $i_{dr}^{+}$ are the positive sequence reactive and active current references, and $v^{+}$ is the positive-sequence voltage magnitude at the grid entry point.

$$i_{qr}^{+}(pu) = -2.5v^{+} + 2.25, 0 \le i_{qr}^{+} \le 1 \quad (8)$$

$$i_{dr}^{+}(pu) = \sqrt{1.2^2 - \left(i_{qr}^{+}\right)^2} \quad (9)$$

The cases included in the systematic tests are presented in Table 3, where the SCR equalling 3 is selected to emulate a weak system, and different fault types, positions, FIAs and resistance are included in the tests. The definition of FIAs in different types of faults is presented in Appendix A.

Table 2 Parameters of the studied network in systematic tests

| Parameters | Definition | Values |
|---|---|---|
| $V_{LL}$ | Nominal system line-to-line voltage | 275 kV |
| SCR | Short Circuit Ratio | 3 |
| $L_{Line1}$ | Length of Line 1 (FDPD line) | 12.1 km |
| $L_{Line2}$ | Length of Line 2 (FDPD line) | 4 km |
| $l_s$ | Inductance of the serial inductor | 0.0341 H |
| $S_{GFL}$ | Apparent power of the GFL | 839 MVA |

Table 3 Cases included in systematic tests

| Parameters | Settings |
|---|---|
| Faulted line | Line 1 |
| Fault position | 10%, 50%, 90% |
| Fault types and FIAs | AG faults – 5°, 6°, 7°, 9°, 11°<br>AB faults – 1°, 2°, 3°, 4°, 5°<br>ABG faults – 1°, 2°, 3°, 4°, 5°<br>ABCG faults – 0°, 10°, 20°, 30°, 40° |
| Fault resistance | 0 Ω, 25 Ω, 50 Ω, 75 Ω, 100 Ω |

*4.1.2 Results of the systematic tests:* The systematic test results are presented in Fig. 5, where the number of healthy trips (i.e., defined as the scenarios where both TWRs can trip for internal faults) is accounted. In the results, for each combination of individual fault resistance and FIA, the total number of the studied cases is three, therefore, it can be concluded that the TWRs can trip all faults with investigated fault resistance and FIA if the number of the individual bar reaches three. From the results in Fig. 5, the following conclusions can be observed.

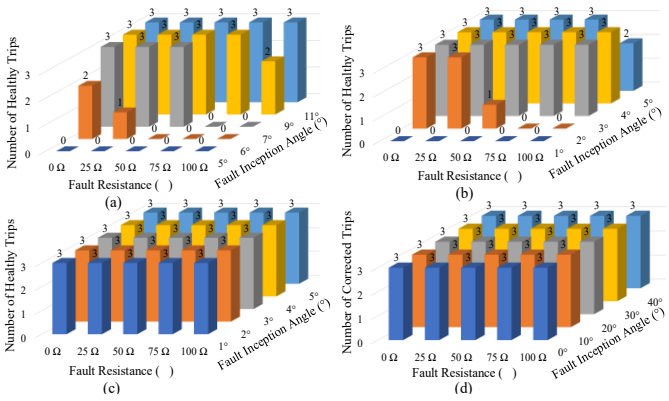


Fig. 5 Results of healthy trips in systematic tests, (a) AG faults, (b) AB faults, (c) ABG faults, (d) ABCG faults

1) The minimum FIAs of AG and AB faults are 6° and 2°. Compared to AG faults (or generally Single-Phase-to-Ground (SPG) faults), the minimum FIAs are lower than AB faults (or generally Phase-to-Phase (PP) faults).
2) The relay performance is improved as the increase of FIAs and the decrease of the fault resistance in SPG and PP faults.
3) The relay can trip all cases in ABG and ABCG faults.

Based on the research in [22], the impacts of fault resistance and FIAs can be quantified using (10), where the $I_{TWR}$ is the current TWs seen by the relay; $V_{sys}$ is voltage magnitude at the fault position for the faulted loop; $R_F$ is the fault resistance; $Z_C$ is the characteristic impedance of the overhead line; $\Gamma_I$ is the reflection factors of current TWs calculated in (7); and $CTR$ is the ratio of the implemented CT.

$$I_{TWR} = \frac{\sqrt{2}V_{sys} \cdot sin(FIA)}{Z_C + 2 \cdot R_F} \times \frac{(1+\Gamma_I)}{CTR} \tag{10}$$

From (10), it is clear that for the same type of faults, a smaller FIA (i.e., the FIA close to 0°) and a greater fault resistance can reduce the magnitude of current TWs measured by the TWRs, and the PP faults can induce a higher-magnitude TW with the same FIA compared to the SPG faults since the $V_{sys}$ in PP fault represent the phase-to-phase voltage while it refers to the phase-to-ground voltage in SPG faults. That analysis can be used to explain the observations of 1) and 2). Compared to the SPG and PPG faults, where the definition of FIAs is clear (i.e., the FIAs of SPG and PP faults refer to the FIA of the faulted phase and faulted phase-to-phase voltage respectively), the FIAs of ABG and balanced faults are ambiguous as more than one fault inception angle parameters are involved in faults. For example, in Phase-to-Phase-to-Ground (PPG) faults, the phase-to-ground and phase-to-phase faulted loops are both involved, therefore, the FIAs of PPG faults can refer to the inception angles of either faulted phase-to-ground or phase-to-phase voltages. In balanced faults, the three-phase voltages are symmetrical, therefore, the FIAs can refer to the inception angles of any faulted phase voltage. For the above reasons, the TWs can always detect the TWs in PPG and balanced faults regardless of the FIAs when the faults occur, which results in observation 3). Additionally, it should be noted that in system operational practice, short-circuit faults are much more likely to occur at large FIAs as the occurrence of most faults requires high voltage to cause insulation breakdown [23].

### *4.2 Results of Detailed Tests*

*4.2.1 Impact of the transformer:* The cases used to evaluate the impact of the transformer on TWRs are presented in Table 4, where the network in Fig. 3 is used and the GFL that adopts the GB grid code-based balanced current controller is connected and the network parameters are shown in Table 2.

Table 4 Cases to evaluate the impacts of the transformer

| Case | Line 1 Length | Line 2 Length | Fault Type | Fault Resistance | FIA | Fault Position | Relay Trips? |
|---|---|---|---|---|---|---|---|
| A1 | 12.1 km | 4 km | AG | 0 Ω | 90° | 10% | Yes |
| A2 | 12.1 km | 0 km | AG | 0 Ω | 90° | 10% | No |
| A3 | 12.1 km | 4 km | AB | 0 Ω | 90° | 10% | Yes |
| A4 | 12.1 km | 0 km | AB | 0 Ω | 90° | 10% | No |

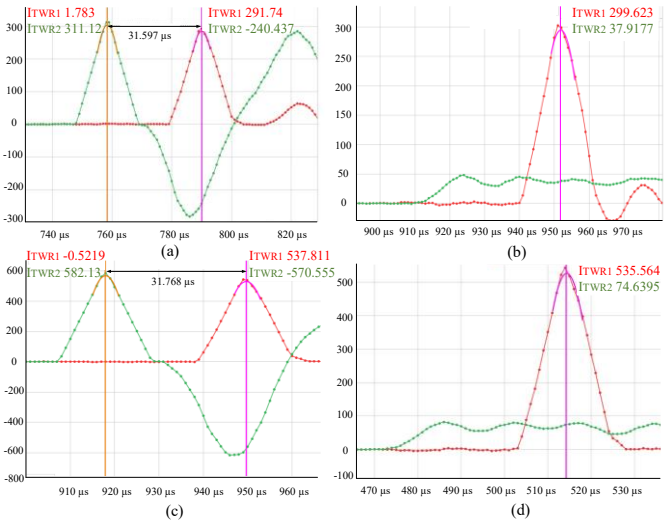


Fig. 6 TWs for the cases in Table 4, (a) Case A1, (b) Case A2, (c) Case A3, and (d) Case A4

In the tests, the FIAs and resistances are set to 90° and 0 Ω respectively to emulate ideal conditions, where the TWs are expected to have the most significant magnitude. From the test results, the investigated TWRs failed to trip when the Line 2 length was reduced to 0 km as shown in Cases A2 and A4. To analyse the sources behind failed trips, the TWs measured by two relays are plotted in Fig. 6, where $I_{TWR1}$ and $I_{TWR2}$ are the current travelling waves measured by TWR1 and TWR2.

By comparing the TW results in Fig. 6 (a) to Fig. 6 (b) and Fig. 6 (c) to Fig. 6 (d), it is observed that the connection of the transformer in Fig. 3 can reduce the magnitude of the TWs significantly and distort the shape of TWs. The sources behind such magnitude cancellations can be explained by (7). Because of the significant impedance of the transformer for TWs, the $Z_T$ in (7) will be sufficiently higher than the magnitude of $Z_C$, which results in the value of the reflection factor, $\Gamma_I$, closes to -1. Therefore, the reflected TW will have a similar magnitude but an opposite polarity compared to the incident TW, which leads to the magnitude of the measured TWs (i.e., equalling the sum of the incident and reflected TWs) decreasing significantly. Additionally, as displayed in Fig. 6 (a) and (c), the TWs can be easily observed and measured by both relays after inserting a 4 km overhead line between the protected line and the transformer as it provides a time shift between the incident and reflected TWs and thus addresses the issues of the magnitude cancellation between the incident and

reflected TWs. The aforementioned issue is also reported in [20], where a travelling wave overcurrent protection element is proposed to address the challenges raised by the connection of the transformer.

*4.2.2 Impact of the system fault level:* The cases in Table 5 are used to evaluate the impact of the system fault level, where SCRs from 2.5 to 5 are used to emulate the weak (i.e., SCR $\leq$ 3) and strong (i.e., SCR>3) AC system conditions, the Line 2 length of 4 km is implemented for all cases and the GFL with the grid-code balanced current controller is adopted in Cases B1 to B8. Based on the results in Fig. 5, the relay can trip all cases in PPG and balanced faults, therefore, only SPG and PP faults are selected in this section and the FIAs of 6° and 2° are used in tests, which are the minimum FIAs of AG and AB faults with an SCR of 3. Based on the results, the TWRs can trip all faults.

Table 5 Cases to evaluate the impacts of the system fault level

| Case | SCR | Line 1 Length | Fault Type | Fault Resistance | FIA | Fault Position | Relay Trips? |
|---|---|---|---|---|---|---|---|
| B1 | 2.5 | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| B2 | 3 | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| B3 | 4 | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| B4 | 5 | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| B5 | 2.5 | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |
| B6 | 3 | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |
| B7 | 4 | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |
| B8 | 5 | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |

To further investigate the impact of fault level on TW relays, the minimum FIAs of all cases in Table 5 are tested by applying the FIA of a fault from 0° and increasing the FIA gradually with a step of 1° until the relay trips. In this process, the first FIA enabling relay trip is recorded as the minimum FIA of the investigated case. From the tests, the minimum FIAs of AG and AB fault cases remain at 6° and 2° despite the variation of fault levels. The magnitudes and the time difference between the initial TWs of two TWRs for the cases in Table 5 are summarised in Table 6, where the fault locating error is calculated by (11). In this equation, the $L_F$ is the actual fault location (i.e., 12.1 km×90%); $L_{TWR1}$ is the relay detected fault distance of TWR1; and $L_T$ is the total length of the protected line (i.e., 12.1 km).

$$Error(\%) = \frac{L_F - L_{TWR1}}{L_T} = \left|\frac{12.1 \times 90\% - L_{R1}}{12.1}\right| \times 100 \quad (11)$$

Table 6 Magnitudes, time difference of initial TWs and calculated fault distance by TWR1

| Case | $I_{TWR1}$ | $I_{TWR2}$ | Time Difference | Fault Distance for TWR1 | Locating Error |
|---|---|---|---|---|---|
| B1 | 30.9878 A | 51.5240 A | 31.791 $\mu s$ | 10.629 km | 2.157 % |
| B2 | 28.8426 A | 49.4933 A | 31.939 $\mu s$ | 10.651 km | 1.975 % |
| B3 | 31.5817 A | 53.5678 A | 31.756 $\mu s$ | 10.624 km | 2.198 % |
| B4 | 31.4127 A | 53.0168 A | 31.862 $\mu s$ | 10.640 km | 2.066 % |
| B5 | 27.7700 A | 49.8727 A | 31.637 $\mu s$ | 10.607 km | 2.339 % |
| B6 | 29.6163 A | 49.9547 A | 31.672 $\mu s$ | 10.612 km | 2.298 % |
| B7 | 28.6931 A | 51.0115 A | 31.773 $\mu s$ | 10.627 km | 2.173 % |
| B8 | 25.9203 A | 46.7068 A | 31.759 $\mu s$ | 10.625 km | 2.190 % |

According to the results in Table 6, where the magnitudes of initial TWs of TWR1 and TWR2 under different fault levels are close, and the same minimum FIAs are observed for all varied fault levels, it can be concluded that the fault level variation appears to have negligible effects on TWRs.

*4.2.3 Impact of the converter control strategy:* In this section, three different control strategies in [4], including the balanced current (BI) mode to inject balanced currents, constant active power (CP) mode to suppress the ripples on the injected active power and constant reactive power (CQ) mode to suppress the ripples on the delivered reactive power, are implemented to the connected CBR in Fig. 5. The information and results of studied cases are shown in Table 7, where the grid SCRs and Line 2 length for Cases C1 to C6 are set to 3 and 4 km.

Table 7 Cases to evaluate the impacts of converter control strategies

| Case | GFL Control | Line 1 Length | Fault Type | Fault Resistance | FIA | Fault Position | Relay Trips? |
|---|---|---|---|---|---|---|---|
| C1 | BI | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| C2 | CP | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| C3 | CQ | 12.1 km | AG | 0 Ω | 6° | 10% | Yes |
| C4 | BI | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |
| C5 | CP | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |
| C6 | CQ | 12.1 km | AB | 0 Ω | 2° | 10% | Yes |

From the results in Table 7, the TWRs can trip all fault cases as expected. By increasing the FIA of a fault from 0° with a step of 1° as it was done in Section 4.2.2, the minimum FIAs for Cases C1 to C3 all equal 6° and the minimum FIAs in Cases C4 to C6 are all 2°. Additionally, by observing the results in Table 8, where the magnitudes, time differences of initial TWs and the calculated fault distance by TWR1 are included, it can be summarised that TW relay's performance is largely unaffected by the changes in converter control strategies, which is one of the main benefits of TW protection in future power systems with high penetration of CBRs.

Table 8 Magnitudes, time difference of initial TWs and calculated fault distance by TWR1

| Case | $I_{TWR1}$ | $I_{TWR2}$ | Time Difference | Fault Distance for TWR1 | Locating Error |
|---|---|---|---|---|---|
| C1 | 28.8426 A | 49.4933 A | 31.939 $\mu s$ | 10.651 km | 1.975 % |
| C2 | 31.3502 A | 52.5826 A | 31.808 $\mu s$ | 10.632 km | 2.132 % |
| C3 | 30.8204 A | 51.6346 A | 31.768 $\mu s$ | 10.626 km | 2.182 % |
| C4 | 29.6163 A | 49.9547 A | 31.672 $\mu s$ | 10.612 km | 2.298 % |
| C5 | 27.9618 A | 49.1920 A | 31.691 $\mu s$ | 10.615 km | 2.273 % |
| C6 | 27.8913 A | 49.6873 A | 31.641 $\mu s$ | 10.608 km | 2.331 % |

*4.2.4 Impact of the external faults:* in addition to protection sensitivity, protection security should also be considered for evaluating the relay performance. The cases in Table 9 and The network model in Fig. 7 are used to investigate the impacts of the external faults. In severe external faults, the TW relays at Bus A and Bus B are expected to detect TWs with high magnitudes and opposite polarities. The clear polarity difference between detected TWs will result in a small operating current and a high restraining current, based on which the TW relays can identify the external faults easily. To emulate the most challenging scenario, where the fault generates minimum detectable TWs, the AG faults with minimum FIAs (i.e., 6°) are selected in the tests.

Table 9 Cases to evaluate impacts of external faults

| Case | Line 1 & 3 Length | Line 2 Length | Fault Type | Fault Resistance | FIA | Fault Position | Relay Trips? |
|---|---|---|---|---|---|---|---|
| D1 | 12.1 km | 4 km | AG | 0 Ω | 6° | 10% | No |
| D2 | 12.1 km | 4 km | AG | 0 Ω | 6° | 20% | No |
| D3 | 12.1 km | 4 km | AG | 0 Ω | 6° | 30% | No |
| D4 | 12.1 km | 4 km | AG | 0 Ω | 6° | 40% | No |
| D5 | 12.1 km | 4 km | AG | 0 Ω | 6° | 50% | No |

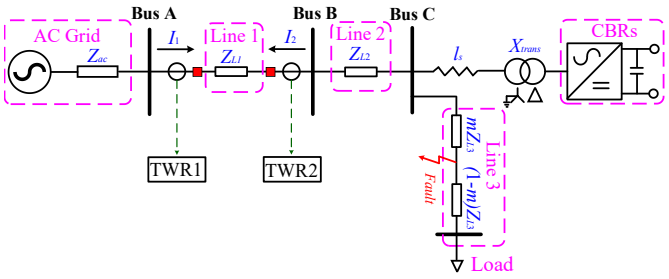


Fig. 7 Network model to evaluate impacts of external faults

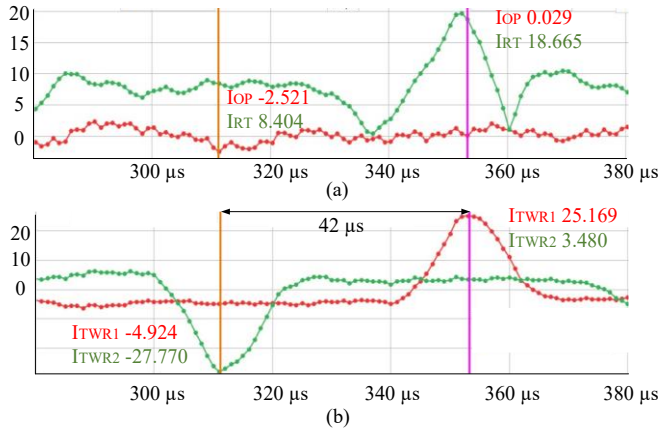


Fig. 8 Results of Case D1 in Table 9, (a) operating and restrain terms, and (b) initial current TWs of TWR1 and TWR2

The operating and restraining quantities of the travelling wave differential module of Case D1 are calculated based on (1) to (4), which are plotted in Fig. 8 (a). According to Fig. 8 (a), the magnitude of the operating term, i.e., $I_{OP}$, oscillates close to 0 A and is lower than the magnitude of restraining term, i.e., $I_{RT}$. Additionally, the time difference between two initial TWs equals 42 $\mu s$ (i.e., equalling the TWLPT setting in TWRs) as shown in Fig. 8 (b), which results in the TWR1 and TWR2 locating the fault as an external fault at Bus B side. Therefore, the TW relays are successfully restrained as expected. Similar results were observed for other cases in Table 9. Therefore, from tests, the TWRs did not operate for all applied external fault cases, and thus, have a good security performance.

## 5 Conclusion

In this paper, comprehensive RTDS-based HiL tests have been presented to evaluate the performance of the travelling wave protection in the network with CBRs. To emulate the realistic behaviours of TWRs, the FDPD line model has been implemented in the developed RTDS network model and the high-frequency effects have been considered. The HiL tests have been conducted in two stages, i.e., a systematic study stage with 300 cases to provide a high-level insight into travelling wave differential protection performance under different fault conditions, and a detailed study stage to investigate the impacts of specific factors, e.g. the influence of the transformer, fault level, converter control strategy, and external faults on TWRs' performance. Based on the test results, it can be concluded that the TWRs have a good sensitivity over a wide range of FIAs and fault resistances, satisfying performance under external faults, and their impacts have not been affected by the fault level variation nor the changes in the converter control. This makes the TW protection particularly applicable in future weak systems dominated by CBRs. Furthermore, it was found that the performance of TWRs could be compromised when the protected line is solely terminated by a transformer as it could lead to the cancellation of incident and reflected TWs. This could be mitigated when a parallel line is connected as it could provide another path for TWs, so these factors should be considered during the design phase for implementing TWRs.

## 6 Acknowledgements

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## Appendix A

In the general case of a sinusoidal waveform, the fault inception angle (FIA) is defined as the angle between the positive zero crossing of the voltage waveform and the time instant of the fault inception as illustrated in Fig. A1. However, in some types of faults, such as in the phase-to-phase-to-ground and balanced faults, more than one faulted loop will be involved, which might lead to an ambiguous understanding of the FIA. The definition of the FIA under different types of faults in this paper is defined below.

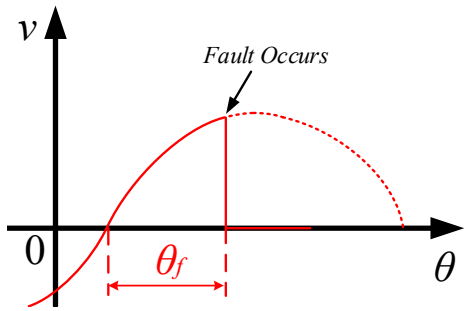


Fig. A1 General expression of the FIA for a sinusoidal waveform

➢ *AG Faults*

In the case of an AG fault, the meaning of FIA is unambiguous as only phase-A waveform is involved, i.e., the faulted phase voltage. Therefore, the FIA can be understood as the angle between the positive zero crossing of the phase-A voltage and the time instant of the fault inception.

➢ *AB Faults*

In the case of an AB fault, the meaning of FIA is also unambiguous with only one voltage waveform involved, i.e., the line voltage between phase A and phase B. In this case, the FIA of an AB fault is defined as the angle between the positive zero crossing of the phase-A-to-phase-B voltage and the time instant of the fault inception.

➢ *ABG Faults*

With an ABG fault, additional clarification is needed as more than one voltage is involved and it is impossible to have the same inception angle for a phase-A-to-ground current loop and the phase A-to-phase-B current loop. For this reason, it has been assumed that the inception angle is defined with respect to faulted line voltage rather than one of the phase voltages.

➢ *Balanced Faults*

In a balanced three-phase fault, there is an angle shift of $120^{\circ}$ between the neighbouring phases. In this case, it is assumed that the FIA of phase-A voltage represents the FIA of the three-phase fault. For example, the FIA of $30^{\circ}$ refers to the scenario where the FIAs of the phases A, B and C are $30^{\circ}$, $-90^{\circ}$ and $150^{\circ}$ respectively.