Fault Tolerant Superconducting Busbar with Reduced Self-Field Effect on Critical Current Design For All Electric Aircraft

Gaurav Gautam, Min Zhang, Weijia Yuan, Graeme Burt and Daniel Malkin

***Abstract*—High Temperature Superconductors (HTS) are promising solution for high current applications such as in all-electric aircraft. According to Paschen's law of voltage breakdown, low voltage is recommended for electric aircraft and high current is required to provide sufficient thrust. A superconducting high current low voltage DC busbar for electric aircraft power distribution system design is proposed and tested in liquid nitrogen at range of 77 K temperature. The emphasis gives to create a design that allows modularity, ride through transients or fault events and reduced effect of self-field on critical current (IC). Design is developed through finite element modelling (FEM) using COMSOL software to study effect of gap between HTS tapes on critical current. A prototype is developed, and experimented with 1 kA at 77K, which measured V-I characteristics and tested against fault current.**

***Index Terms*—Critical current (IC), all-electric aircraft, self-field, high temperature superconductor (HTS).**

I. Introduction

THE emission of gases and particles from aviation plays substantial role in climate warming. Notably, CO_2 is key pollutant within aviation, bearing a significant level of responsibility for net anthropogenic forcing. Beyond CO_2, non-CO_2 pollutants further contribute to complex dynamics of global warming, culminating in an overall impact from aviation on radiative forcing (RF). To quantify this intricate interplay is radiative forcing, in watts per square meter (W/m^2) [1]. The Radiative Forcing Index (RFI) serves as a representative measure of this ratio. Data from 2005 reveals that aviation's CO_2 emissions accounted for approximately 1.6 % of the total global anthropogenic CO_2 RF during that period. Aviation's net RF stood at an estimated 4.9% of the total anthropogenic RF [2].

"Flightpath 2050" Europe's vision for aviation, set ambitious goal for 2050, by stating 75% reduction in CO_2 emissions per passenger kilometre. Also, reduction of nitrogen oxide (NOx) emission by 90% and reduction in noise emission by 65% compared to aircrafts in 2000 [3]. To achieve these goals, aviation electrification presents itself as a viable solution. Electrification in aircraft can be initiated by electrifying subsystems of aircraft and then gradually replace traditional propulsion jet engine with propulsion electric motors. Aircraft whose subsystems replaced with electric systems apart from jet propulsion system, are known as More Electric Aircraft (MEA). Compare to traditional jet engine aircraft MEA are more efficient and produce less noise [4], [5]. Thrust generation through electric power in aircrafts are classified as Hybrid Electric Aircraft (HEA) and All Electric Aircraft (AEA) [6]. HEA requires aviation fuel and jet engine to generate power, whereas AEA replaces jet engine with onboard source of power. The roadmap of these technologies, as detailed in [7], provides a clear overview of the anticipated power and voltage levels for different categories of aircraft. For large aircraft which can carry up to 300 passengers, distributed propulsion system is proposed with required power more than 10 MW and voltage range is 2-5 kV [6]. Architectures for distributed propulsion system for all electric aircrafts explored in [8]–[11]. Superconductivity can be used to support such architectures, as it provides high power to weight ratio for architecture components like power distribution system and motors [12]–[14]. DC power distribution system for all-electric aircraft is prominent due to technical maturity of converters [15]. This requires a high amount of current to be carried from source to propulsion unit. High Temperature Superconductor (HTS) provides adequate solution to transfer high current efficiently, as they offer no losses while carrying DC current with less space and weight.

However, HTS is an adequate solution for high current applications, there are challenges associated with it. HTS tape critical current is limited by few hundred amperes, to use them for high current applications, there is a need for stacking them together in parallel. There are three main approaches to group them together: Co-axial winding concept [16], Robel concept [17] and stack concept [18]. S I Schlachter et al' have done work with HTS superconducting busbars, 13.3 kA and 20 kA busbars have been demonstrated [19], [20]. Design with reduce effect of self-field on IC and fault tolerant design are not well explored.

DC high current superconducting busbar design is proposed in this work. This paper is divided in two parts: in section II effect of self-field on critical current and how to reduce this effect explained with modelling and a prototype is developed and tested. Section III explains how fault tolerance achieved through design and experimental results shows it's ride through capability during fault event. Conclusion is discussed in Section IV.

This work was supported by University of Strathclyde and GKN Aerospace.

Gaurav Gautam, Min Zhang, Weijia Yuan and Graeme Burt are with the Department of Electronic and Electrical Engineering, University of Strathclyde, 204 George St, Glasgow, G1 1RX, U.K. (e-mail: gaurav.gautam@strath.ac.uk; weijia.yuan@strath.ac.uk)

Daniel Malkin is with GKN Areospace, Taurus Rd, Patchway, Filton, Bristol BS34 6FB, U.K.

II. Design Validation

FEM is used to develop an electromagnetic model, to understand effect of self-field on IC when multiple HTS tapes stack together in parallel.

A. Finite Element Modelling (FEM)

An electromagnetic model is developed using COMSOL, T-A formulation is used for busbar modelling [21]. Current distribution is calculated with current potential vector T, through Eq.(1), where J is current density.

$$J = \nabla \times T \tag{1}$$

Magnetic field (B) distribution is calculated with magnetic vector potential A, through Eq.(2).

$$B = \nabla \times A \tag{2}$$

J_c is field dependent current density (A/m^2) at 77K and used to calculate field dependant critical current (IC) with Eq. 3, delta is HTS thickness $(1\mu m)$.

$$\int J_c * delta = IC \tag{3}$$

With help of electromagnetic model, effect of gap between HTS tapes on field dependent critical current is studied. This effect becomes more prominent while stacking multiple HTS tapes for high current application as shown in Fig. 1, where 10 and 5 HTS tapes modelled with a gap of $1\mu m$ & $100\mu m$. Effect of self-field on critical current increases as number of HTS tapes increases. Simulation validates that IC can be increased with change in design through add a gap between HTS tapes. Relationship of field dependent critical current with applied current is shown in Fig.1. Applied current is increasing with time, so the field due to applied current. Consequently, the field dependent critical current is decreasing. Field dependent Critical current can increase or decrease by change in self-field produced by busbar and self-field can change by adding gap between HTS tapes. Increase in gap between HTS tapes reduces field and increases IC as shown in Fig.1. This gap can be created with copper put in between HTS tapes, which adds fault tolerance in design. This will further explored in section-III. As field decreases influence of Lorentz forces also reduces. COMSOL software is used to implement FEM, to propose an efficient superconducting busbar design.

TABLE I
PARAMETERS USED IN SIMULATION AND EXPERIMENTS

Parameters	Simulation	Cu b/w HTS Design	HTS Design
No. of HTS Tapes	10	10	10
No. of CU Tapes	-	9	0
IC Single HTS	100A	100A	100A
Operating Temperature	77K	77K	77K
Total Applied Current	1kA	1kA	1kA
Gap Between HTS Tapes	1μm, 100μm	100μm	no gap
Critical Current	830A, 875A	840A	720A
Thickness of CU & HTS	1μm	100μm, 53μm	0, 53μm

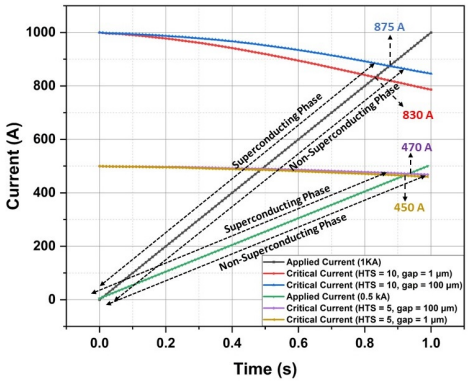

Fig. 1. Relationship of field dependent critical current w.r.t applied current.

B. Mechanical Layout and Experimental Validation

Two prototypes have been developed and tested, one with 10 HTS tapes and another with 9 copper tapes sandwich between 10 HTS tapes. Both samples are stacked and soldered together in parallel as shown in Fig.2. 1kA current is applied through the prototype and V-I characteristics are measured. TDK-GSP10-1000-3P400, programmable 10 kW high current (1kA) and low voltage (0 - 10 V) DC power supply is used for experiments. Power supply allows USB interface and integrate with LabView environment for communication. Shunt is used to measure current and voltage is measured through voltage taps. National Instruments, NI-9238 voltage input module with cDAQ-9174 is used to acquire voltage and current data. Liquid Nitrogen (LN2) in open bath cryostat is used for experiments and schematic of setup is shown in Fig. 3. Experimental result shows effect of adding gap between in HTS tapes for high current application. IC test conducted on two designs, one

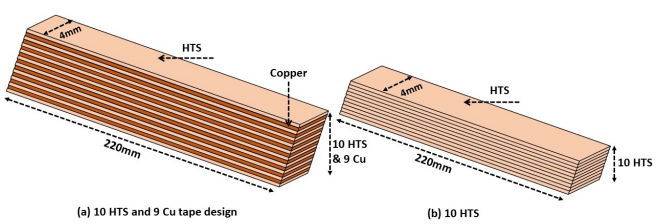

Fig. 2. Mechanical design with copper tapes sandwich between HTS tapes and HTS tapes.

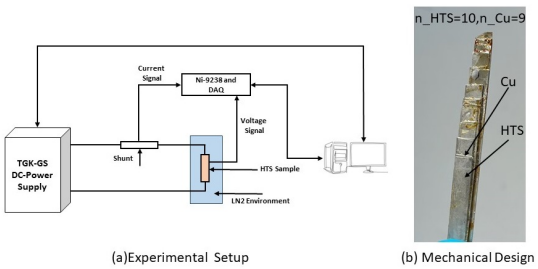

Fig. 3. Experimental setup and designed prototype.

with gap is introduced in between HTS with 100 µm thick and 4 mm wide copper tape, whereas in another design only HTS tapes are used. 4 mm wide 2G HTS (REBCO) shanghai superconductor is used to perform all experiments.

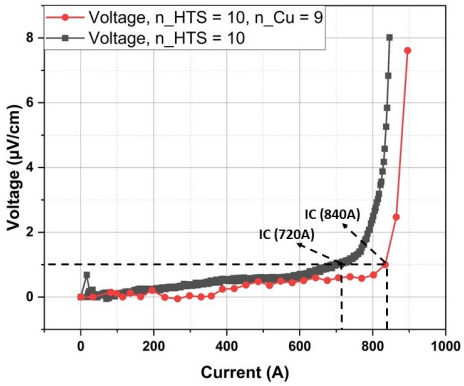

Fig. 4. V-I characteristics of 10 HTS tapes and 9 Cu tapes sandwich between 10 HTS tapes.

As shown in Fig. 4, IC of 10 HTS tapes design and 9 Cu tapes sandwich between 10 HTS tapes design are 720A and 840A. Parameters used for simulation and experiments are mentioned in Table I. Terminal losses are not modelled in simulation, so difference in results will contribute due to inhomogeneous material and unequal distribution of current due to inhomogenous soldering between HTS tapes. Result shows that effect of gap between HTS tapes on overall IC for high current application where multiple HTS tapes are used.

III. Fault Tolerant Principle and Analysis

Effect on field dependent IC by adding copper in between HTS tapes is explained in earlier section. This also helps to add fault tolerance in the design, explained in this section. Due to power supply limitation fault test conducted with two samples contains 5 HTS tapes and 4 copper tapes sandwich in between 5 HTS tapes.

A. Working of Fault Tolerant Design

When current in HTS exceeds through critical current, it starts generating a voltage and corresponding resistance, which is exponential in nature. This behaviour can be predicted with E-J power law and expressed through Eq. 4. Here J is current density, Jc is field dependent current density, E_0 is electric field criteria $(1\mu V/cm)$.

$$\rho_{sc} = \frac{E_0}{J_c}\left(\frac{J}{J_c}\right)^{(n-1)} \tag{4}$$

Due to change in voltage a resistance starts appearing and current starts diverting from superconducting layer to metal layers. An alternate path called stabilizer, carry extra current that diverts from superconducting layer and helps to save HTS from burn.

Working principle of fault tolerant mechanism, can be understood with the help of Fig. 5. HTS tapes acts as variable resistor whose resistivity depends upon applied current. During

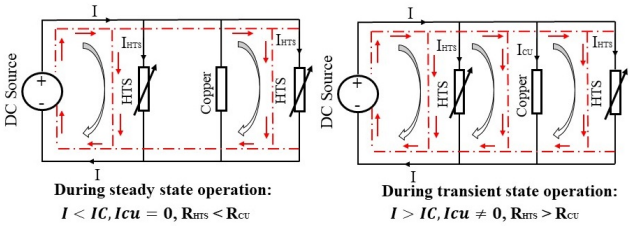

Fig. 5. Working principle of steady state and fault (transient) state operation.

steady state condition $I < IC$ (I is applied current and IC is critical current), current only flows through HTS tapes as $R_{HTS} < R_{CU}$. During fault or transient condition $I > IC$ and resistance $R_{HTS} > R_{CU}$ that forces current to flow through low resistive path. Under such condition, copper stabilizer helps to carry extra current from fault which eventually save HTS from burn.

IC test conducted on two samples with 5 HTS tapes and 4 copper tapes sandwich between 5 HTS tapes as shown in Fig. 6. From results, we can predict that current flows only through HTS tapes in both sample during steady state, as voltage is non linear w.r.t to current. In copper voltage-current relationship is linear. Therefore, voltage-current relationship helps to predict that current is flowing through HTS and not in copper. These sample results are comparable with modelling results as shown in Fig. 1.

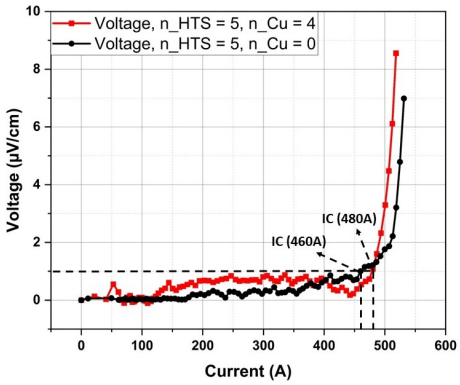

Fig. 6. V-I characteristics of 5 HTS tapes and 4 Cu tapes sandwich between 5 HTS tapes.

B. Experimental Results: Fault State Analysis

A fault test conducted on both samples that have been used to do IC test, shown in Fig. 6. As mentioned in section II.B mechanical layout and experimental validation, same setup is used to generate fault current as shown in Fig. 3. High current pulse is generated for 1ms with programmable power supply which provides a range of slew rate, 0.0001 - 999.99 A/msec. A predetermined current limit is set and time period of current pulse is controlled by adjusting slew rate. Operation of power supply is controlled through LabVIEW program. Superconducting busbar sample is connected in series with power supply as shown in Fig.3. IC of both samples shown

in Fig. 6, is maximum current that these samples carry safely are 460A and 480A. Current above IC treated as fault current. Busbar operates in superconducting state, maintaining its superconducting properties called normal zone. However, when current through HTS exceeds critical current it transitions to the fault zone, as shown in Fig. 7. In fault zone, the HTS material is no longer in a superconducting state and exhibits resistive behavior.

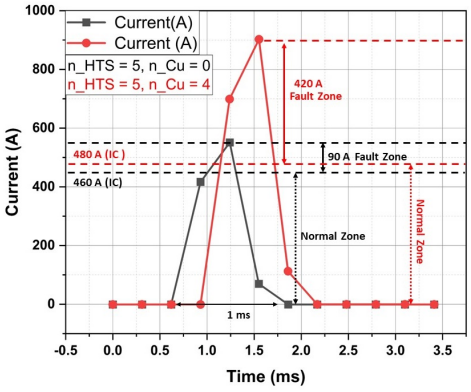

Fig. 7. Fault test on 5 HTS tapes and 4 Cu tapes sandwich between 5 HTS tapes.

A series of fault test has been conducted with different magnitude of fault currents. Fig.7 shows maximum peak current tolerate by both samples before burn. Sample with copper sandwich in between HTS tapes have more fault tolerance compare to sample that contains only HTS tapes and compared in table II. Power loss during fault test is shown in Fig. 8, power loss tolerance of Cu sandwich in between HTS tapes design is more as compare to 5 HTS tape design.

TABLE II
RESULT COMPARISON

Parameters	5 HTS Tapes	4 Cu Tapes b/w 5 HTS Tapes
Critical current	460 A	480 A
Max Fault Tolerance	90 A	420 A
Width of HTS, Cu Tape	4mm, 0	4mm, 4mm
Thickness of HTS, Cu Tape	53 μm,0	53 μm, 100μm
Fault Tolerance Compare to IC	19.5 %	87.5 %
Max Power Loss Tolerance	0.025 W/cm	9 W/cm
Max Heat Tolerance	14.7 J/cm	0.032 J/cm

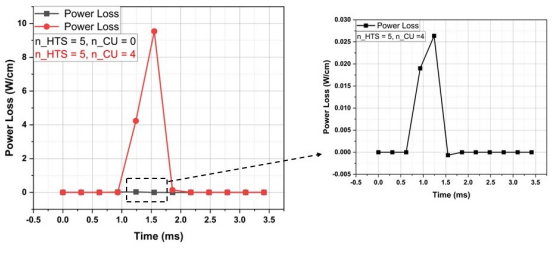

Fig. 8. Power loss during fault test.

Heat loss generated during fault test is shown in Fig. 9, showing higher thermal stability and tolerate higher heat loss. Results demonstrate that adding extra layer of copper between

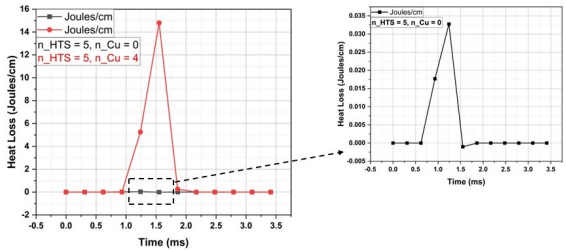

Fig. 9. Heat loss during fault test.

HTS tapes offers not only a fault-tolerant design, but also a design with higher tolerance for power and heat loss compare to busbar design which contain only HTS tapes.

IV. CONCLUSION

A superconducting busbar design is proposed for all-electric aircraft using 2G HTS (REBCO) tapes. In high-current scenarios, there is a requirement of stacking multiple HTS tapes in parallel. This arrangement of multiple HTS tapes, reduces field dependent critical current due to influence of self-field generated by high current flowing through HTS tapes. A solution has been proposed and implemented to reduce effect of self-field. This involves introducing a gap between HTS tapes with copper, which is not only increasing the field dependent critical current but also make a fault tolerant design. The results demonstrate that this design effectively riding through transient events and tolerate more heat and power loss which prevents HTS from burn. Future plan, includes implementing joints to connect multiple such modules.

ACKNOWLEDGMENTS

This Project is funded by University of Strathclyde and GKN Aerospace.

REFERENCES

[1] Fuglestvedt, JS. Berntsen, TK. Isaksen, ISA. Mao, H. Liang, XZ. Wang, WC, "Climatic forcing of nitrogen oxides through changes in tropospheric ozone and methane: Global 3D model studies," *J. Atmospheric Environment*, vol. 33, issue. 6, pp. 961-978, 1999.

[2] David S. Lee, Manchester Metropolitan University, UK, [Online]. Available: http://assets.publishing.service.gov.uk/government/uploads/system/uploads/attachment-data/file/813342/non-CO2-effects-report.pdf

[3] European commission 2011, flight path 2050 europe vision for aviation. *Report of the high level group on aviation research*, DOI:10.2777/50266.

[4] P. Wheeler and S. Bozhko, "The more electric aircraft: Technology and challenges," in *IEEE Electrific. Mag*, vol. 2, no. 4, pp. 6-12, dec. 2014.

[5] C. Cecati, S. Song and G. Buticchi, "Special Issue on More Electric Aircraft," in *IEEE Transaction on transportation Electrification*, vol. 6, no. 4, pp. 1382-1385, Dec. 2020, doi: 10.1109/TTE.2020.3026761.

[6] G. Buticchi, P. Wheeler and D. Boroyevich, "The More-Electric Aircraft and Beyond," in Proceedings of the*IEEE*, vol. 111, no. 4, pp. 356-370, April 2023, doi: 10.1109/JPROC.2022.3152995.

[7] Electrical Power Systems, INSIGHT, U.K. Aerosp. Technol. Inst. HQ, Cranfield, U.K., 2018, vol. 7.

[8] T. C. cano et al, "Future of electrical aircraft energy power systems: an architecture review," in *IEEE Transaction on transportation Electrification*, vol. 7, no. 3, pp. 1915-1929, sept. 2021, doi: 10.1109/TTE.2021.3052106.

[9] H. Schefer, L. Fauth, T. H. Kopp, R. Mallwitz, J. Friebe, and M. Kurrat, "Discussion on electric power supply systems for all electric aircraft," in *IEEE Access*, vol. 8, pp. 84188–84216, 2020, doi: 10.1109/ACCESS.2020.2991804.

[10] D. C. loder, A. bollman and M. J. armstrong,“Turbo-electric distributed aircraft propulsion: microgrid architecture and evaluation for ECO-150,” in *2018 IEEE Transportation electrification confrence and EXPO (ITEC*, long beach, CA, USA, 2018, pp. 550-557, doi: 10.1109/ITEC.2018.8450180.

[11] M. armstrong et. al,“Architecture, voltage, and components for a turboelectric distributed propulsion electric grid: final report,” Rolls-royce north american technologies, indianapolis, IN, NASA/CR–2015-218440, july 2015.

[12] R. Sugouchi et al.,“Conceptual design and electromagnetic analysis of 2 MW fully superconducting synchronous motors with superconducting magnetic shields for turbo-electric propulsion system,”in *IEEE Trans. Appl. Superconductivity*, vol. 30, no. 4, pp. 1–5, Jun. 2020, doi: 10.1109/TASC. 2020.2974705.

[13] S. Zanegin, N. Ivanov, D. Shishov, I. Shishov, K. Kovalev, and V. Zubko,“Manufacturing and testing of AC HTS-2 coil for small electrical motor,”in *J. Supercond. Novel Magn.*, vol. 33, no. 2, pp. 355–359, Feb. 2020, doi: 10.1007/s10948-019-05226-1.

[14] F. Weng, M. Zhang, T. Lan, Y. Wang, and W. Yuan,“Fully superconducting machine for electric aircraft propulsion: Study of AC loss for HTS stator,”in *Superconductor Sci. Technol.*, vol. 33, no. 10, Oct. 2020, Art. no. 104002, doi: 10.1088/1361-6668/ab9687.

[15] Y. L. Ogundiran, A. Griffo, J. Wang, S. Sundeep, F. Bruder-Mandler and T. Groh, ”Insulation Monitoring in Ungrounded Electrical System for More Electric Aircrafts,” 2023 IEEE Workshop on Electrical Machines Design, Control and Diagnosis (WEMDCD), Newcastle upon Tyne, United Kingdom, 2023, pp. 1-5, doi: 10.1109/WEMDCD55819.2023.10110936.

[16] Y. S. Choi, D. L. Kim, H. S. Yang, S. H. Sohn, J. H. Lim and S. D. Hwang, ”Progress on the Performance Test of KEPCO HTS Power Cable,” in IEEE Transactions on Applied Superconductivity, vol. 21, no. 3, pp. 1034-1037, June 2011, doi: 10.1109/TASC.2010.2093496.

[17] S. Sahoo, X. Zhao, and K. Kyprianidis, “A Review of Concepts, Benefits, and Challenges for Future Electrical Propulsion-Based Aircraft,” Aerospace, vol. 7, no. 4, p. 44, Apr. 2020, doi: 10.3390/aerospace7040044.

[18] M. J. Wolf, W. H. Fietz, C. M. Bayer, S. I. Schlachter, R. Heller and K. -P. Weiss, ”HTS CroCo: A Stacked HTS Conductor Optimized for High Currents and Long-Length Production,” in IEEE Transactions on Applied Superconductivity, vol. 26, no. 2, pp. 19-24, March 2016, Art no. 6400106, doi: 10.1109/TASC.2016.2521323.

[19] S. I. Schlachter, J. Brand, S Elschner, S. Fink, B. Holzapfel, A. Kudymow and J. Willms, ”HTS CroCo: Test of a DC-HTS Busbar Demonstrator for Power Distribution in Hybrid-Electric Propulsion Systems for Aircraft,” in IOP Conference Series: Materials Science and Engineering, vol. 1241, no. 1, pp. 012037, May 2022, doi: 10.1088/1757-899X/1241/1/012037.

[20] S. Elschner et al., ”3S–Superconducting DC-Busbar for High Current Applications,” in IEEE Transactions on Applied Superconductivity, vol. 28, no. 4, pp. 1-5, June 2018, Art no. 4800805, doi: 10.1109/TASC.2018.2797521.

[21] F. Liang, S. Venuturumilli, H. Zhang, M. Zhang, J. Kvitkovic, S. Pamidi, Y. Wang, W. Yuan, ”A finite element model for simulating second generation high temperature superconducting coils/stacks with large number of turns,” J. Appl. Phys, 28 July 2017; 122 (4): 043903, doi.org/10.1063/1.4995802