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Original article

A new hybrid multilevel thyristor-based DC-DC converter

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ABSTRACT

The rapid growth in HVDC grids is becoming inevitable for long-distance power transmission. Therefore, the idea of interconnection between the point-to-point links becomes essential. However, these point-to-point connections face several challenges such as the requirement of DC fault blocking capability, interfacing of different grounding schemes, offering multi-vendor interoperability, and difficulty to achieve high DC voltage stepping. DC-DC converters are considered the optimum solution to tackle these challenges in DC grids interconnection. In this paper, a new hybrid modular DC-DC converter is proposed that achieves a low number of semiconductors, low losses, and cost in comparison to other DC-DC converters due to the utilization of thyristors. The new DC-DC converter consists of two hybrid MMC bridges connected through an isolating transformer. Each MMC bridge is comprised of half bridge submodules and bidirectional thyristors. Detailed mathematical analysis, design, and control are illustrated. A comparison is carried out between different topologies in terms of semiconductor count, power loss, and cost. Also, both simulation model and experimental test rig are built to validate the proposed hybrid modular DC-DC converter under different scenarios. Finally, another variant of the hybrid-thyristor based converter (version two) is proposed for multiport DC-Hub application to achieve DC fault blocking without turning off all connected bridges.

1. Introduction

Enormous growth in renewable energy resources has led to massive investment in the infrastructure of energy transmission due to the location of renewable resources, which is usually very far from load centers. HVDC grids are the most efficient solution [1] for long-distance transmission. Voltage source converters (VSCs) are increasingly becoming the advanced technology to build HVDC grids specially with the recent advancement in modular multilevel converters (MMCs) [2]. The possibility of deploying a DC grid from the interconnection of different HVDC grids becomes a fact. However, the conventional back-to-back connection offers limited capability in the interconnection between different vendors and hinders the capability of fault isolation. Therefore, the need for DC-DC converters arises with different advantages such as: providing interoperability, galvanic isolation and blackout spreading prevention, continuous power flow, DC voltage stepping and allowing different grounding schemes.

Generally, extensive studies have been carried out on DC-DC converters for HVDC transmission in the last couple of years. These DC-DC converters can be classified into two main categories. The first one represents the non-isolated DC-DC converters as in [3]. Resonant-based converters rely on multistage conversion (DC-AC-DC). Single resonant tank, as discussed in [4], suffers from high electrical stresses across passive components due to bulk power transfer. Henceforth, this type of converter is limited for medium power applications. Moreover, multi-tank resonant converters [5] reduces the complexity of the design, but suffers from uneven distribution of current flow in semiconductors. Moreover, the DC-DC autotransformer described in [6], is constituted of a number of converters on both sides. The series connection of the converters reduces the sizing but restricts this type to low and medium power. On top of that, another topology has been introduced in [7], which consists of a half-bridge MMC (HB-MMC) connected to a full-bridge MMC (FB-MMC). A modification has been done, where the second stage was replaced by a conventional H-bridge to reduce the

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number of semiconductors with the feature of zero voltage switching as proposed in [8]. However, the existence of DC capacitors limits both topologies to medium voltage applications. Furthermore, DC choppers are based on using SMs instead of conventional switches as described in [9]. Therefore, it can be deduced that all converters under this category do not provide isolation between DC grids due to the absence of an isolating transformer, which is a major flaw.

The second category is based on isolated DC-DC converters. Normally, this category relies on a two-stage conversion DC-AC-DC with an isolating transformer in between. In this category, DC fault blocking is achieved by disabling both bridges. The basic topology in this category is the conventional dual active bridge (DAB) [10], where each arm of the bridge consists of series connection of IGBTs. Furthermore, a modified form of DAB has been proposed in [11], where it allows the connection to line-commutated HVDC networks. However, DAB topologies have some problematic issues of dynamic voltage sharing across the series switches in the application of high voltage. In addition, two-level converters led to significant voltage stresses across the isolating transformer. Henceforth, the MMC-DAB [12] technology has emerged to solve the dynamic voltage sharing issue and voltage stresses presented in conventional DAB. The conventional MMC-DAB topology is based on half-bridge sub-modules (HB-SMs) as in [13] for half-bridge MMC (HB-MMC), however, it suffers from high losses due to the increased number of switching devices. Besides, another topology modification has been proposed in [14] which uses current source MMC (CS-MMC) at one side and the other side is the normal HB-MMC to provide connection capability to line commutated HVDC networks. However, it suffers from large sizing in SM of CS-MMC. On the other hand, full-bridge MMC (FB-MMC) emerged as in [15,16] to allow DC fault blocking without disabling both bridges and allows DC link voltage reversal. But the cost and losses have increased significantly. Moreover, another topology has been proposed in [17], known as alternative arm modular multilevel converter (AAC). Mainly, it is designed to reduce the number of full-bridge sub-modules (FB-SM) by replacing some of them with a series connection of switches. This modification led to maintaining the DC fault blocking capability with reduced losses in comparison with FB-MMC. Nevertheless, the overall efficiency is smaller than half-bridge based MMC (HB-MMC). Besides, the DC-link capacitors utilization increases the cost and the volume of the converter. Also, it increases the transient peak current during DC fault. A development has been proposed in [18] to the AAC, named extended overlap AAC (EO-AAC), to eliminate the DC link capacitors, however, an increased number of FB-SMs is utilized in order to increase the overlap periods between the upper and lower arms. Nevertheless, an idea is proposed which suggested the replacement of director switches of AAC with thyristors and antiparallel diodes as in [19,20], which can named as Thyristor-based MMC (TH-MMC). However, the problematic issue of large number of semiconductors persists due to FB-SMs utilization. It should be noted that the FB-SMs utilization in the previous topologies provides no additional advantage because as mentioned earlier all DC-DC converters achieve DC fault blocking by disabling both bridges without the need for FB-SMs.

Moreover, some researchers in [21,22] suggested a new topology named, controlled transition bridge (CTB) converter, where it utilizes director switches (series connection of IGBTs) in the arms as the main power path while using a chain link of FB-SMs to provide step changes in voltage in order to reduce stresses across isolating transformer. This topology achieves reduced SM sizing in comparison with HB-MMC. However, the DC link capacitors represent a major issue in HV applications. Furthermore, it was suggested in [23] to replace the director switches in the CTB with a series connection of back-to-back thyristors to provide a new configuration named, an Active Forced Commutated hybrid converter (AFC). In this case, the chain-link of FB-SMs is responsible for forcing commutation of the thyristors in addition to providing step changes in the voltage. However, the DC link capacitors issue is still unresolved. Additionally, the idea of Neutral Point Clamped (NPC) has been modified in [24,25], where it is known as Modular Embedded Multilevel Converter (MEMC). Mainly, it involves the replacement of IGBTs with thyristors and antiparallel diodes. Also, it replaces the DC link capacitors with MMC-SMs. Besides, another converter is proposed in [26,27], which is a modification on the conventional MMC named as Transition Arm Converter (TAC). Also, the same structure has been proposed under different name as Switched Star Modular Multilevel Converter (SSMMC) [28]. Mainly, it replaces one of the arms of MMC (the lower or the upper arms) with series connection of IGBTs to reduce the cost and size of the HB-MMC. Furthermore, another idea is proposed in [29,30] that replaces normal MMC arms by a series connection of power groups (PG). Each PG is comprised of a thyristor valve (series connection of bidirectional thyristors) in parallel with MMC-SMs leading to a new configuration known as thyristor-based power group (TH-PG). The MMC-SMs contains a majority of HB-SMs with a minority of FB-SMs for thyristor commutation. This topology allows a lower losses path at full DC link voltage. However, it suffers from the huge cost of semiconductors.

It is evident that the converters presented in literature review fail to solve the following issues in one converter:

- Increased number of switches which increases the cost, losses, size and weight of the converter.
- Presence of DC link capacitor, which increases the volume, cost of the converter and causes high transient current in case of DC fault due to the capacitance discharge.
- The presence of voltage stresses across transformer.

In this paper, a new isolated hybrid thyristor-based DC-DC converter is proposed for interconnection between VSC-HVDC networks. It replaces the upper arms of the conventional MMCs with thyristor devices. The proposed converter utilizes only HB-SMs to reduce the losses, and cost of the converter. The contribution of the paper is summarized as follows:

- Proposing a new isolated hybrid thyristor-based DC-DC converter that achieves low cost, low conduction losses, and low semiconductor count.
- Developing full parameter design for the proposed converter including the utilized LCL filter at the AC link.
- Developing two control techniques for different operating conditions including detailed mathematical analysis.
- Providing comparative study between HB-MMC, FB-MMC, TAC/SSMMC, CTB, TH-MMC including semiconductor count, power loss, and cost.
- Proposing a new variant of the proposed converter intended for utilization in multiport DC-Hub to provide DC fault blocking capability without turning off all bridges.

This paper is organized as follows. Section II provides a basic analysis of the proposed DC-DC converter. Section III provides an equivalent power circuit with detailed analysis for power flow and condition of zero reactive power. SM sizing and arm inductance design are derived and discussed in section IV. Section V shows the different power flow control techniques. Section VI presents simulation validation of the proposed DC-DC converter at HVDC ratings. Section VII shows the experimental results of the proposed DC-DC converter. Section VIII provides a detailed comparison between different existing converters and the proposed one. Section IX provides illustration of version two of the proposed converter that is utilized in multiport DC-Hub.

2. Proposed DC-DC converter topology analysis

2.1. Architecture of the proposed DC-DC converter

The proposed hybrid multilevel thyristor-based DC-DC converter,

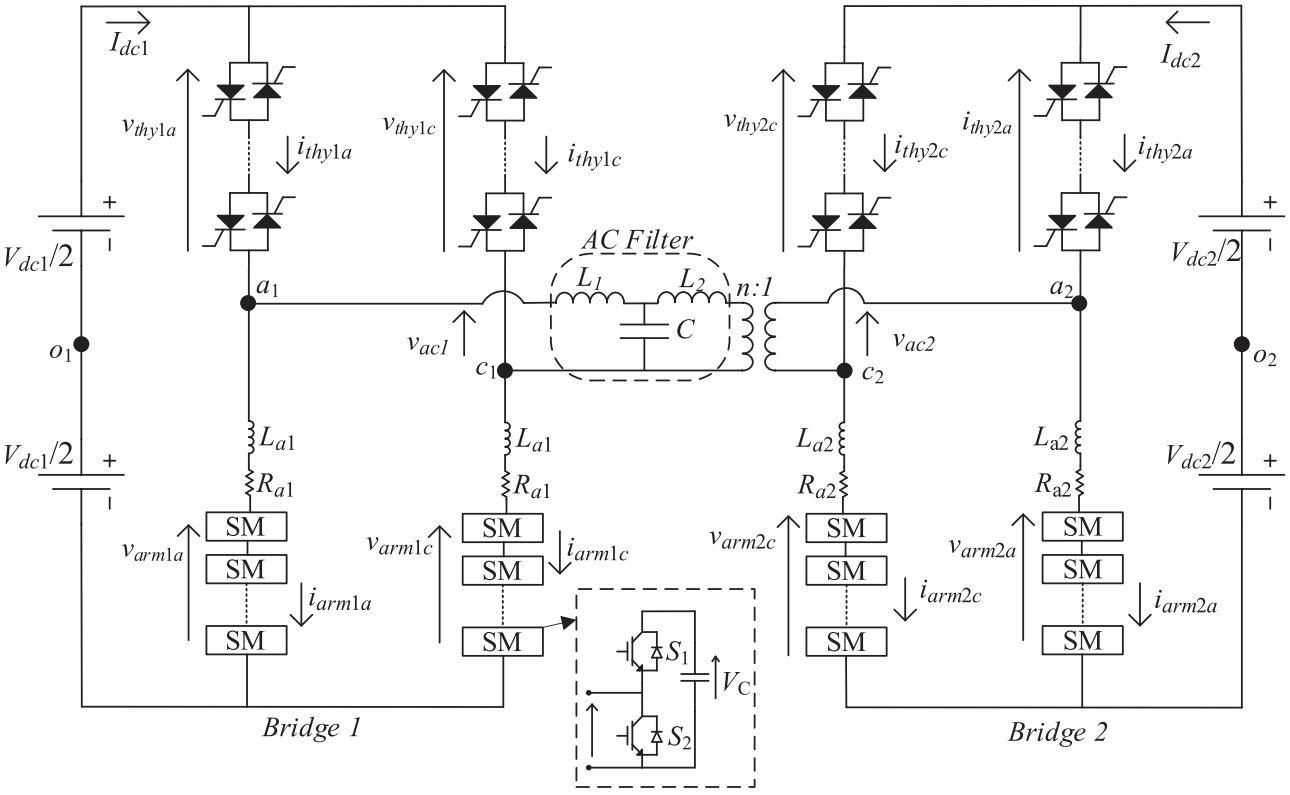

Fig. 1. The proposed hybrid multilevel thyristor-based DC-DC converter architecture.

shown in Fig. 1, is utilized to connect different VSC-HVDC based networks. The converter consists of two H-bridges (bridge 1 and bridge 2), where each bridge can be configured as a three-phase bridge. However, an H-bridge configuration is adopted in this paper for simplicity (only two legs are considered: leg (a) and leg (c)). Each bridge leg comprises two arms, where the upper arm consists of a series connection of back-to-back thyristors for bidirectional current flow and achieving lower conduction losses. On the other hand, the lower arm is comprised of only HB-SMs to reduce the number of semiconductor count. This arm participates in the power delivery through the converter and is responsible for force commutation of the thyristor arms. Both H-bridges are connected at the AC-link via an isolating transformer and an LCL filter to nullify the reactive power at rated power flow.

2.2. Basic operation of the proposed DC-DC converter

Trapezoidal waveform is adopted in the operation of the proposed DC-DC converter due to the gained advantages of higher power transferred, lower SM capacitors utilization, and low voltage stress across the isolating transformer. The operation waveforms of a single bridge are depicted in Fig. 2 including the output and the arms voltage and current waveforms, where the dotted lines indicate that a thyristor arm is in a conduction state. The firing time (t_α) is introduced to provide an additional control variable (controlling the magnitude and phase shift of the output AC trapezoidal waveform), where v_{ac1} and i_{ac1} are the output AC voltage and current of bridge 1, respectively. v_{ao1} is the voltage of leg (a) in bridge 1, v_{arm1a} and i_{arm1a} is the voltage and current of MMC arm a in bridge 1, respectively. v_{thy1a} and i_{thy1a} are the voltage and current of the thyristor valve in leg (a) of bridge 1, respectively, I_p is the peak of the AC current. T_r is the rise/fall time, T_b is the periodic time, T_c is the time of commutation. It is worth noting that all waveforms of leg (c) can be found by applying 180 degrees phase shift to leg (a) waveforms. The periodic time of the output trapezoidal waveform is divided into 7 sections (from section (a) to (h)) as depicted in Fig. 2 to clearly illustrate the operation of each bridge in the proposed converter. Also, the current paths of each section is clearly illustrated in Fig. 3, where also, the dotted paths and arrows indicate that a thyristor arm is in conduction state:

i. *Section (a)*

Thyristor valve 1a is conducting with MMC arm 1c (all SMs of MMC arm 1c are bypassed), while MMC arm 1a is generating a voltage of V_{dc1} as shown in Fig. 3(a).

i. *Section (b)*

MMC arm 1a produces a voltage of $V_{dc1}+\Delta V$ to force commutation to thyristor valve 1a as shown in Fig. 3(b). It should be noted that if the arm current before commutation is negative MMC arm 1a should produce a voltage of $V_{dc1}-\Delta V$.

i. *Section (c), (d)*

Both thyristor valves are in a non-conducting state, while both MMC arms generate the required steps of the trapezoidal waveform as shown in Fig. 3(c) and (d). The difference between sections (c) and (d) is the direction of the arm current.

ii. *Section (e)*

Thyristor valve 1c is conducting with MMC arm 1a (all SMs of MMC arm 1a are bypassed), while MMC arm 1c is producing a voltage of V_{dc1} as shown in Fig. 3(e).

v. *Section (f)*

MMC arm 1c produces a voltage of $V_{dc1}+\Delta V$ to force commutation to thyristor valve 1c as shown in Fig. 3(f). Similarly, if the arm current before commutation is negative MMC arm 1c should produce a voltage of $V_{dc1}-\Delta V$.

w. *Section (g), (h)*

Similar to sections (c) and (d), both thyristor valves are in a non-conducting state, while both MMC arms generate the required steps of the trapezoidal waveform as shown in Fig. 3(g) and (h), where also the difference between section (g) and (h) is the direction of current.

2.3. Mathematical analysis

An equivalent circuit is employed for the converter as shown in Fig. 4 for the sake of the analysis. Each MMC arm is approximated as a variable capacitor. Hence, the capacitance of the i^{th} converter and j^{th} arm (C_{armij}) can be represented as follows:

$$C_{armij} = \frac{C_{SM}}{n_{ij}} \tag{1}$$

where, n_{ij} is the number of inserted submodules in the i^{th} converter and j^{th} arm and C_{SM} is the submodule capacitance.

Moreover, the nominal SM capacitor voltage in the i^{th} converter ($V_{cnominal_i}$) can be represented as follows:

$$V_{c_{nominal_i}} = \frac{V_{dc_i}}{N_{r_i}} \tag{2}$$

where, $V_{dc}i$ is the DC-link voltage in the i^{th} converter and N_{r_i} is the number of SMs required to generate the rated i^{th} DC link voltage. Ideally, the MMC arm voltage of the i^{th} converter and j^{th} arm (v_{armij}) can be represented as follows:

$$v_{armij} = \frac{n_{ij} V_{dc_i}}{N_{ri}} \tag{3}$$

Applying KVL in loops 1 and 2, the output voltage of leg (a) and (c) are represented as follows:

$$v_{ao_i} = v_{armia} - \frac{V_{dc_i}}{2} \tag{4}$$

$$v_{co_i} = v_{armic} - \frac{V_{dc_i}}{2} \tag{5}$$

Using (3) in (4) and (5), the number of inserted SMs is obtained as follows:

$$n_{ia} = N_{r_i}\left(v^*_{ao_i} + \frac{1}{2}\right) \tag{6}$$

$$n_{ic} = N_{r_i}\left(v^*_{co_i} + \frac{1}{2}\right) \tag{7}$$

where, $v^*_{ao}i$ and $v^*_{co}i$ are the reference waveforms of output voltages $v_{ao}i$ and $v_{co}i$ ($v^*_{ao}i = \frac{v_{aoi}}{V_{dci}}, v^*_{co}i = \frac{v_{coi}}{V_{dci}}$).

$$v^*_{ao_i} = \frac{1}{2T_r}\begin{cases} 0, & -t_\alpha < t < t_\alpha \\ t - t_\alpha, & t_\alpha < t < T_r + t_\alpha \\ T_r, & T_r + t_\alpha < t < 0.5T_b - t_\alpha - T_r - T_c \\ \frac{2(N_{T_i} - N_{ri})}{N_{ri}} T_r + T_r, & 0.5T_b - t_\alpha - T_r - T_c < t < 0.5T_b - t_\alpha - T_r \\ -t + (0.5T_b - t_\alpha), & 0.5T_b - t_\alpha - T_r < t < 0.5T_b - t_\alpha \\ 0, & 0.5T_b - t_\alpha < t < 0.5T_b + t_\alpha \\ -t + 0.5T_b + t_\alpha, & 0.5T_b + t_\alpha < t < 0.5T_b + t_\alpha + T_r \\ -T_r, & 0.5T_b + t_\alpha + T_r < t < T_b - T_r - t_\alpha \\ t - (T_b - t_\alpha), & T_b - T_r - t_\alpha < t < T_b - t_\alpha \end{cases} \tag{8}$$

The reference voltage $v^*_{ao}i$ is represented by (8), where N_{T_i} is the total number of SMs in the MMC arm. Finally, the output AC voltage is represented by computing the difference between (4) and (5) as follows:

$$v_{ac_i} = v_{armia} - v_{armic} = \frac{V_{dc_i}}{N_{r_i}}(n_{ia} - n_{ic}) \tag{9}$$

3. Power Circuit Analysis of the Proposed DC-DC Converter

This section presents detailed mathematical analysis of equivalent power circuit of the proposed hybrid multilevel thyristor-based DC-DC converter and the condition required to nullify the reactive power at rated power flow. The equivalent power circuit is shown in Fig. 5, where $\delta$is the phase shift between the two output AC voltages. For simplicity, the AC inductances of LCL filter are assumed equal, where $L_1 = L_2 = L$. By applying KVL in loop 1 and loop 2, the following is obtained:

$$v_{ac1} = L\frac{di_{ac1}}{dt} + v_c \tag{10}$$

$$v_{ac2} = L\frac{di_{ac2}}{dt} + v_c \tag{11}$$

where v_{ac_1}, v_{ac_2}, $i_{ac_1}$and i_{ac_2} are the instantaneous output voltages and currents of each port at the AC side. Additionally, by using KCL at node M, the following equation is obtained:

$$i_{ac1} + i_{ac2} = i_c \tag{12}$$

where, i_c is the instantaneous current of the AC link capacitor. Fundamental analysis is employed in the derivation in order to ease the calculation. Hence, Laplace transform is used in (10) and (11). Then, by substituting (12) in the later equations:

$$V_{ac1} = I_{ac1}\left(\frac{s^2LC + 1}{sC}\right) + \frac{I_{ac2}}{sC} \tag{13}$$

$$V_{ac2} = \frac{I_{ac1}}{sC} + I_{ac2}\left(\frac{s^2LC + 1}{sC}\right) \tag{14}$$

By solving (13) and (14) and using $s = j\omega$ to get the equations in the frequency domain, the fundamental component phasors of the AC currents can be obtained as follows:

$$\bar{i}_{ac1} = -j\frac{(1 - \omega^2LC)\widehat{V}_{ac1} - \widehat{V}_{ac2}\angle(-\delta)}{\omega L(2 - \omega^2LC)} \tag{15}$$

$$\bar{i}_{ac2} = -j\frac{(1 - \omega^2LC)\widehat{V}_{ac2}\angle(-\delta) - \widehat{V}_{ac1}}{\omega L(2 - \omega^2LC)} \tag{16}$$

where, $\widehat{V}_{ac1}$and $\widehat{V}_{ac2}$ are the fundamental peak components of the AC voltages. The apparent power of port 1 and port 2 are expressed generally as follows:

$$S_1 = \bar{v}_{ac1}\bar{i}^*_{ac1} \tag{17}$$

$$S_2 = \bar{v}_{ac2}\bar{i}^*_{ac2} \tag{18}$$

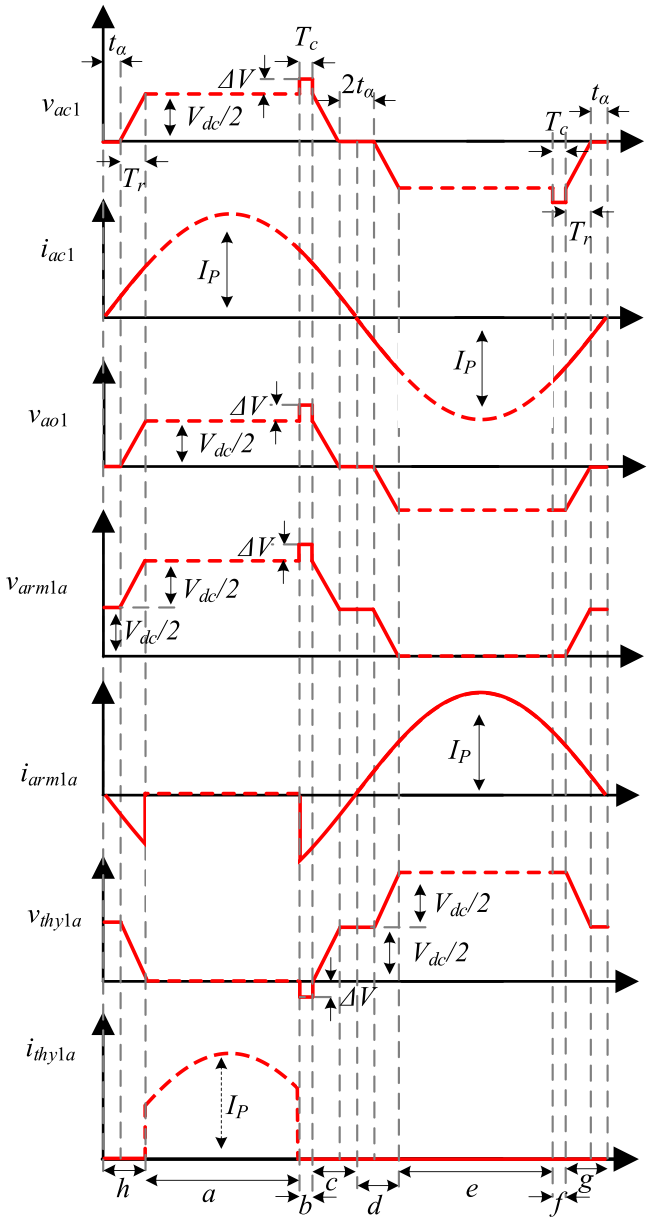

Fig. 2. Voltage and current waveforms of the proposed DC-DC converter.

where, $\bar{v}_{ac1}$, $\bar{v}_{ac2}$, $\bar{i}^*_{ac1}$ and $\bar{i}^*_{ac2}$ are the phasor fundamental components of the AC voltages and conjugate currents. Therefore, the active and reactive powers of port 1 and 2 can be calculated as follows:

$$P_1 = \frac{8V_{dc1}V_{dc2}\sin\delta\cos^2\alpha}{\pi^2\omega L(2-\omega^2 LC)} = -P_2 \tag{19}$$

$$Q_1 = Q_2 = \frac{8V_{dc}^2 1(1-\omega^2 LC) - 8V_{dc1}V_{dc2}\cos\delta}{\pi^2\omega L(2-\omega^2 LC)}\cos^2\alpha \tag{20}$$

where, $\bar{v}_{ac1} = \frac{2\sqrt{2}V_{dc1}}{\pi}\cos\alpha$, $\bar{v}_{ac2} = \frac{2\sqrt{2}V_{dc2}}{\pi}\cos\alpha$. The rated power flow is designed at phase shift (δ=90°) and firing-angle ($\alpha = 0$).

By equating the reactive power in (20) to zero at rated power angles, the condition to nullify reactive power at rated power flow is as follows:

$$1 = \omega^2 LC \tag{21}$$

Then, the power equations can be calculated as follows:

$$P_1 = \frac{8V_{dc1}V_{dc2}}{\pi^2\omega L}\sin\delta\cos^2\alpha = -P_2 \tag{22}$$

$$Q_1 = Q_2 = -\frac{8V_{dc1}V_{dc2}}{\pi^2\omega L}\cos\delta\cos^2\alpha \tag{23}$$

It is obvious that if the angle δ decrease below 90°, the reactive power will start to increase. Moreover, the AC currents are reduced to be as follows:

$$\bar{i}_{ac1} = \frac{j2\sqrt{2}V_{dc2}}{\pi\omega L}\cos\alpha\angle(-\delta) \tag{24}$$

$$\bar{i}_{ac2} = \frac{j2\sqrt{2}V_{dc1}}{\pi\omega L}\cos\alpha \tag{25}$$

4. Circuit parameter design

This section provides a detailed analysis and design of the AC filter based on zero-reactive power circulation at rated power flow, SMs' capacitors sizing, the arm inductance, and number of HB SMs, respectively.

4.1. LCL filter design

The value of the AC inductance L is calculated to achieve the required rated power (P_r) at the conditions ($\delta = 90°$ and $\alpha = 0°$), which can be calculated from (22) as follows:

$$L = \frac{8V_{dc1}V_{dc2}}{\pi^2\omega P_r} \tag{26}$$

On the other hand, the AC capacitance is determined to achieve zero reactive power at rated power conditions, which can be calculated based on (21). Hence, it can be calculated as follows:

$$C = \frac{1}{\omega^2 L} \tag{27}$$

4.2. Design of SMs' capacitance

It is required to design a suitable SM capacitance to limit the SM voltage ripple less than 10%. By studying equivalent variable capacitor model of MMC arm in Fig. 4, the arm current can be computed as follows:

$$i_{arm} = C_{arm}\frac{dv_{c_{arm}}}{dt} \tag{28}$$

Using (1), (2), and (3) in (28), the change in voltage across the capacitor can be defined as follows:

$$\Delta V_c = \frac{1}{C_{SM}}\int\frac{n(t)}{N_T}i_{arm}dt \tag{29}$$

It is worth noting that the dominant times of charging/discharging the SM capacitors are the time of thyristors commutation and the firing time. Hence, they are the main cause of capacitors voltage ripple. Hence, the change in capacitor voltage is deduced by substituting (6), (9), and (24) in (29) and solving the integration, the voltage ripple across the capacitor becomes as follows:

$$\Delta V_c = \frac{4V_{dc}}{\pi\omega^2 LC_{SM}}\cos\alpha\left(-\frac{N_r}{N_T}\sin(\delta)\cos(\alpha)+\frac{N_r}{N_T}\sin(\delta)+\sin(\alpha+\delta) - \sin(\omega(T_c)+\alpha+\delta)\right) \tag{30}$$

Assuming that the required percentage voltage ripple ratio across the capacitor is k and can be calculated as:

$$k = \frac{\Delta V_c N_r}{V_{dc}} \tag{31}$$

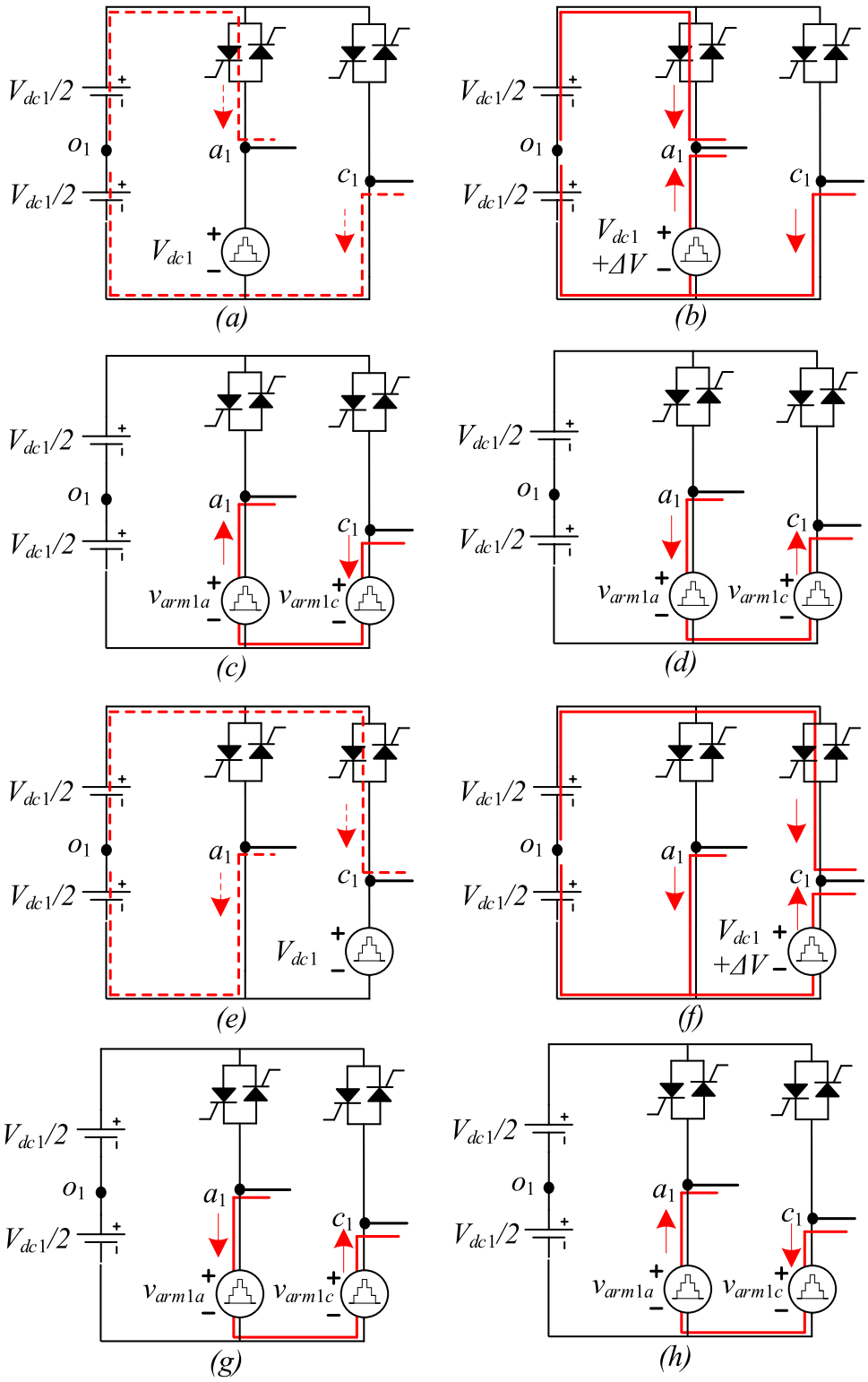

Fig. 3. Current routings of bridge 1 during the whole period: (a), (e) thyristor conduction sections, (b), (f) Thyristor commutation sections, (c), (d), (g), (h) MMC arms ramp generation sections.

Also, the number of the extra SMs is very small compared to the rated number of SMs (N_r). Therefore, the capacitance of each SM is determined as follows:

$$C_{SM} = \frac{4N_r}{\pi\omega^2 Lk}\cos\alpha(-\sin(\delta)\cos(\alpha)+\sin(\delta)+\sin(\alpha+\delta)-\sin(\omega(T_c)+\alpha+\delta)) \quad (32)$$

It is clear that the value of the SM capacitance depends on the range of operating values of αandδ. Therefore, based on the control technique utilized, the design value of the SM capacitance will be determined. Hence, the SM capacitance is investigated in more detail in the next section.

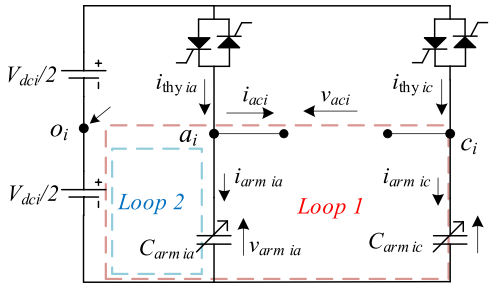

Fig. 4. The equivalent circuit of each bridge in the proposed converter.

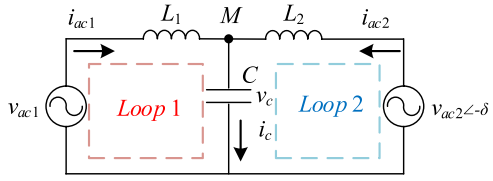

Fig. 5. The equivalent power circuit.

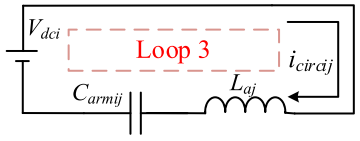

Fig. 6. Transient equivalent circuit for single leg.

4.3. Design of arm inductance

The arm inductance is burdened with the responsibility of reducing circulating current. Moreover, it is responsible to ensure that the rate of fall of current is between the thyristor's maximum ramp rate and minimum rate of fall during commutation. At the instant of the thyristor firing, a large inrush current flows in leg of H-bridge accounting for imbalance of SMs. An equivalent circuit is employed to study the transient period of circulating current which is shown in Fig. 6. By studying loop 3 using KVL, the following is obtained:

$$V_{dc} = L_a\frac{di_{circ}}{dt} + \frac{1}{C_{arm}}\int i_{circ}dt + V_{c\,initial} \tag{33}$$

By differentiating both sides with respect to time, the following is obtained:

$$\frac{L_a d^2 i_{circ}}{dt^2} + \frac{1}{C_{arm}} i_{circ} = 0 \tag{34}$$

It can be observed that (34) has natural response which is depicted as follows:

$$i_{circ} = kV_{dc}\sqrt{\frac{C_{arm}}{L_a}}\ \sin\left(\frac{t}{\sqrt{C_{arm}L_a}}\right) \tag{35}$$

Eq. (35) can be used for the arm inductance selection to limit the inrush current flowing through the thyristor, where the equation is governed by ripple factor k and arm inductance. Hence, the inductance value is calculated by solving (35) numerically across the periodic time, and selecting the largest inductance value obtained for the converter design, taking into consideration the variation of C_{arm}, which is calculated by substituting in (1), (6), and (9), and the designed circulating peak current.

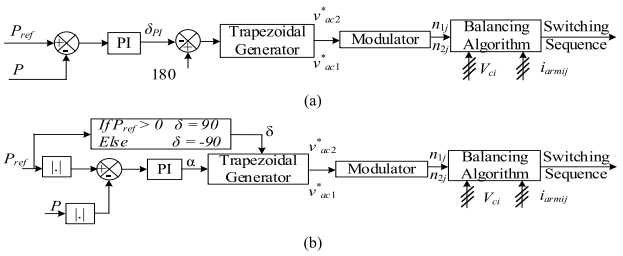

Fig. 8. Control block diagram for control techniques (a) phase shift and (b) firing-angle.

4.4. Thyristor design

The thyristor valve design is based on withstanding the full DC voltage. Hence, the number of thyristors connected in series is based on the formula shown in (36):

$$N_{thyristors} = \frac{V_{dc}}{V_{DRM}} \tag{36}$$

where V_{DRM} is the maximum off-state voltage of the thyristor. Additionally, the chosen thyristors must validate the following criteria as described in (37):

$$T_q < T_C \tag{37}$$

where, T_q is turn-off time of thyristor. Finally, it should withstand the rated current flowing through it.

4.5. Design of the total number of SMs

As mentioned earlier, the MMC arm should be able to generate $V_{dc} + \Delta V$. Therefore, extra SMs are required above the rated number (N_r) to produce ΔV which can be deduced from the criteria mentioned in [23], which governs the rate of rise/fall of current through thyristor:

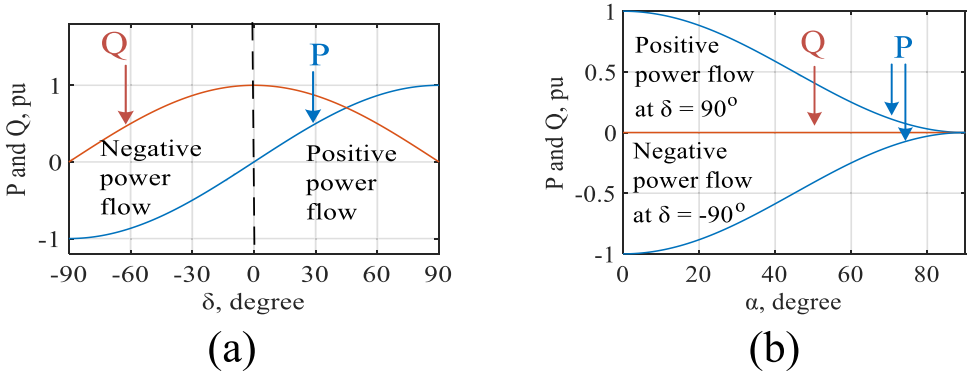

Fig. 7. The power flow variations for different control techniques are (a) phase shift control and (b) firing-angle control technique.

Table 1
Simulation model parameters.

Parameter	Description	Value
P_r	Rated power	$60MW$
V_{dc1}	DC link voltage of port 1	$\pm 30kV$
V_{dc2}	DC link voltage of port 2	$\pm 30kV$
f	Fundamental Frequency	$100Hz$
L_1	LCL Filter inductance 1	$77.4mH$
L_2	LCL Filter inductance 2	$77.4mH$
C	LCL Capacitance	$8.2\mu F$
n_t	Transformer turns ratio	1 : 1
T_r	Trapezoidal rise time	$100\mu s$
T_c	Time of commutation	$700\mu s$
N_T	Total number of SMs per MMC arm	33
N_r	Number of SMs for rated DC link voltage	30
k	Capacitor ripple voltage percentage	4%
C_{SM}	SM capacitance of converter 1 and 2	$15mF$
L_{arm}	Arm inductance of converter 1 and 2	$0.3mH$

$$\frac{I_{thy_{\max}}}{T_c - T_q} \leq \frac{(N_T - N_r)V_{dc}}{L_a N_r} \leq \zeta \tag{38}$$

where, T_q is the thyristor turn-off time and ζ is the thyristor maximum current ramp rate. Therefore, the total number of SMs can be determined with knowing the maximum thyristor current (which is equal to I_p at the worst case), the required current falling time, and the arm inductance.

5. Power flow control techniques

In this section, two different control techniques are proposed due to the presence of two control variables. The phase shift (δ) and firing-angle (α) are the two main control variables for the proposed DC-DC converter. Each one of them offers some accessibility to reduce losses during power delivery.

5.1. Phase shift control

The phase shift control technique is based on maintaining constant firing-angle $\alpha = 0$, while varying the phase shift δ between $\{-90°, 90°\}$. This control technique offers very low SM capacitance. However, it results in reactive power as the power flow deviates from the rated value. The active and reactive powers flow with respect to phase shift δ can be observed in Fig. 7 part (a). The SM sizing derived in (32) is modified by using $\alpha = 0°$ to the following:

$$C_{SM} = \frac{4N_r}{\pi\omega^2 Lk}(\sin(\delta) - \sin(\omega T_c + \delta)) \tag{39}$$

It is evident that the sizing of the capacitor in SMs is a nonlinear function as described in (39). Hence, the design must be based on maximum loading which can be found by substituting by the whole range of operation of δ from $-90°$ to $90°$. Then design based on the maximum calculated SM capacitance value. A closed-loop control of the power flow is applied, where the control block diagram is shown in Fig. 8 part (a), where the error is computed between the desired power and the actual one, then fed to a PI controller. The PI controller provides the suitable phase shift δ, which is fed to the waveform generator, where an adequate delay between both waveforms is generated. The waveforms are passed to a modulator to generate the required number of inserted SMs, which is sent to a balancing algorithm to generate the switching sequence. The balancing algorithm guarantees that all the SMs capacitors are charged and have the same voltage ripple.

5.2. Firing-angle control

The firing-angle control technique offers the advantage of active power flow with zero reactive power in the whole range. However, the required SM capacitance is higher because the conduction time of the

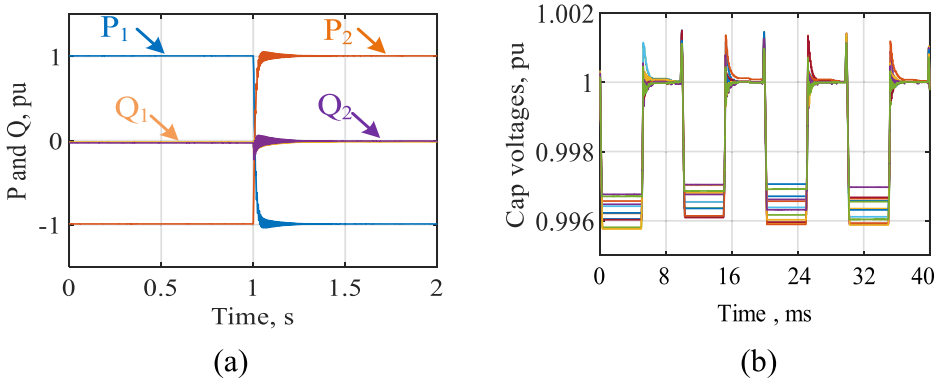

Fig. 9. Simulation results during bidirectional power flow, (a) active and reactive power flow and (b) capacitor voltage ripple.

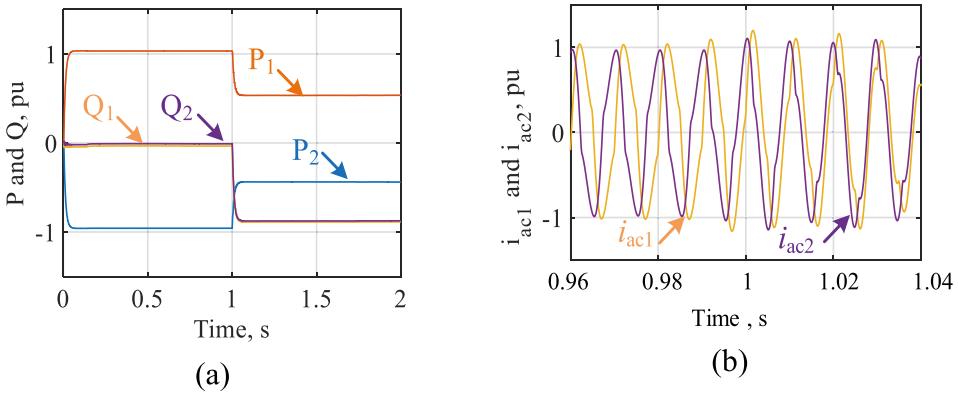

Fig. 10. Simulation results in case of phase shift control technique, (a) active and reactive power flow and (b) AC output currents.

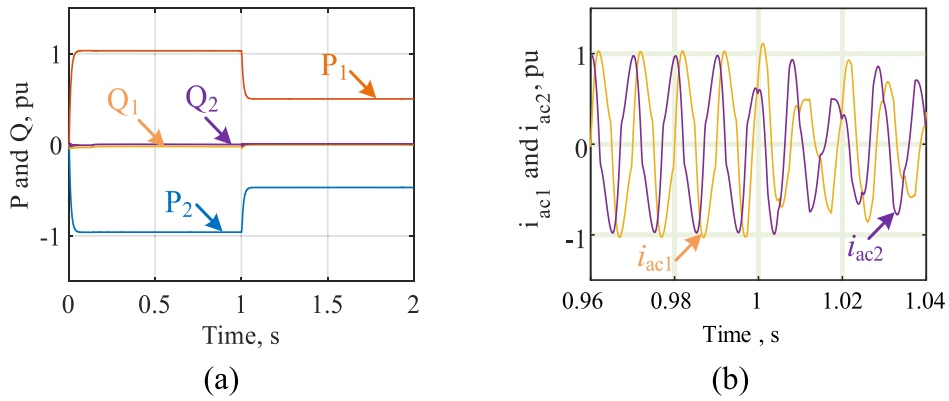

Fig. 11. Simulation results in case of firing-angle control technique, (a) active and reactive power flow and (b) AC output currents.

MMC arm is increased. The control is based on maintaining the δ phase shift to 90°and the angle α is controlled to adjust the amount of power transferred. The direction of power flow is reversed by changing the sign of the δ phase shift to $-90°$. The firing-angle α belongs to the range $\{0, 90°\}$, where the power magnitude decreases as the angle α increases.

The relation between power flow and the control variable (α) is shown in Fig. 7 part (b), where it can be observed that the power flow is proportional with $\cos^2\alpha$, which is based on (22). Moreover, the SM sizing is modified by substituting $\delta = 90°$in (32) as follows:

$$C_{SM} = \frac{4N_r}{\pi\omega^2 Lk}\cos\alpha(1-\cos(\omega T_c+\alpha)) \quad (40)$$

Similarly, the designed value of the SM capacitance can be found by substituting by the whole range of α from $-90°$ to 90° and select the maximum calculated SM capacitance. The block diagram of this control technique is shown in Fig. 8 part (b), where a closed loop is, also, applied to control the power flow. However, the PI controller generates the suitable angle α to achieve the desired power magnitude, while the power direction indicates the sign of the angle δ ($\delta = 90°$ for forward power and δ=−90° for reverse power flow).

6. Simulation results

This section validates the applicability of the proposed isolated hybrid thyristor-based DC-DC converter using MATLAB SIMULINK model. The simulation setup is based on 11-Level, where each MMC arm has 12 SMs (10 SMs for generated rated DC link voltage and 2 SMs for thyristor commutation). The parameters used in simulation are summarized in Table 1, where the SMs' capacitance is designed based on (40). Additionally, the LCL filter is based on the criteria derived in (26) and (27). Different normal operation scenarios are simulated for validation.

6.1. Bidirectional power flow

This subsection validates the uninterruptible bidirectional power flow capability of the proposed converter. The active and reactive power flow of port 1 and 2 are shown in Fig. 9 part (a). It can be observed that the power flow is from port 1 to port 2 then reversed at t = 1 s smoothly without any interruption. Moreover, the reactive power is zero before

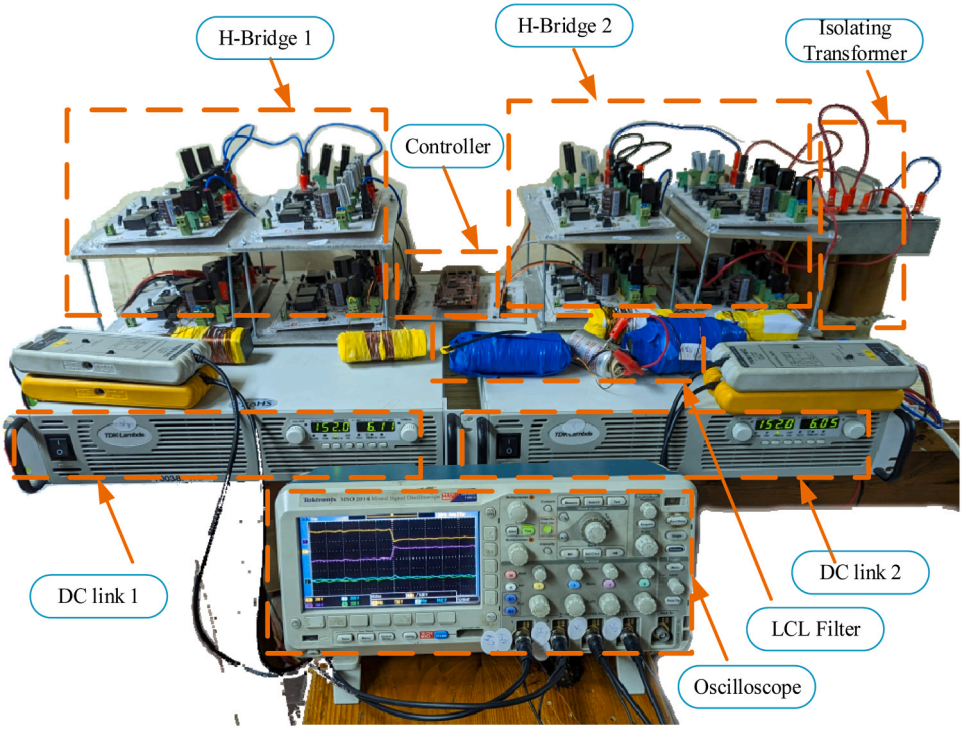

Fig. 12. Experimental test setup of the proposed converter.

Table 2
Hardware prototype parameters.

Parameter	Description	Value
P_r	Rated power	$400W$
$V_{dc1} = V_{dc2}$	DC link voltage of ports 1 and 2	$150V$
f	Fundamental Frequency	$400Hz$
$L_1 = L_2$	LCL Filter inductance 1 and 2	$18mH$
C	LCL Capacitance	$8.7\mu F$
n_t	Transformer turns ratio	$1:1$
T_r	Trapezoidal rise time	$10\mu s$
T_c	Time of commutation	$100\mu s$
N_T	Total number of SMs per MMC arm	3
N_r	Number of SMs for rated DC link voltage	2
C_{SM}	SM capacitance	$330\mu F$
L_{arm}	Arm inductance	$350\mu H$

and after power reversal due to rated power flow. Furthermore, the voltage ripple of the capacitors in SMs is shown in Fig. 9 part (b). It is evident that the ripple is less than the 4% criteria.

6.2. Power flow step change

i. *Phase shift* control

In this case, a step-change in the magnitude of the power flow from port 1 to port 2 is applied based on phase shift control technique. The amount of power flow is shown in Fig. 10 part (a).

The power flow is from port 1 to port 2, where it exhibits zero reactive power during rated power flow. On the other hand, a step-change is applied at t = 1 s, where it can be observed that the reactive power deviates from zero corresponding to deviation of the active power flow from rated value. Additionally, it is evident that the peak of the AC currents increases as a consequence to the increase in reactive power flow as shown in Fig. 10 part (b).

ii. *Firing-angle control*

In this case, the power flow is assumed from port 1 to port 2 and a step-change is applied using firing-angle control technique, where phase shift is maintained constant at $\delta = 90°$. The power flow is depicted in Fig. 11 part (a). It can be noted that as the active power deviates from rated value at t = 1 s, the reactive power is successfully maintained at zero on both ports. Moreover, the AC currents are reduced due to the reduction in the power flow with zero reactive power circulation as depicted in Fig. 11 part (b).

7. Experimental setup validation

A hardware experimental prototype is designed for the sake of further validation of the proposed DC-DC converter. The overall experimental setup is shown in Fig. 12. The hardware setup is based on 3-Level for simplicity, where each MMC arm has 3 SMs, while a single thyristor is used for the upper arm. The parameters are listed in Table 2. Moreover, the LCL filter is based on the criteria provided in (26) and (27).

7.1. Bidirectional power flow

To test the bidirectional capability of the proposed DC-DC converter, the power flow between ports 1 and 2 is reversed at the rated value. The DC link voltages, average currents, and active power of ports 1 and 2 are shown in Fig. 13 parts (a) and (b), respectively. It is evident that the current changes its polarity to change the direction of the power flow while the DC link voltage is maintained constant due to nature of VSC network. It can be observed that the power flow reversal is uninterruptible, which results in a continuous operation.

7.2. Power flow step change

In this subsection, the power flow undergoes a step change according to both control techniques of the proposed DC-DC converter as previously mentioned.

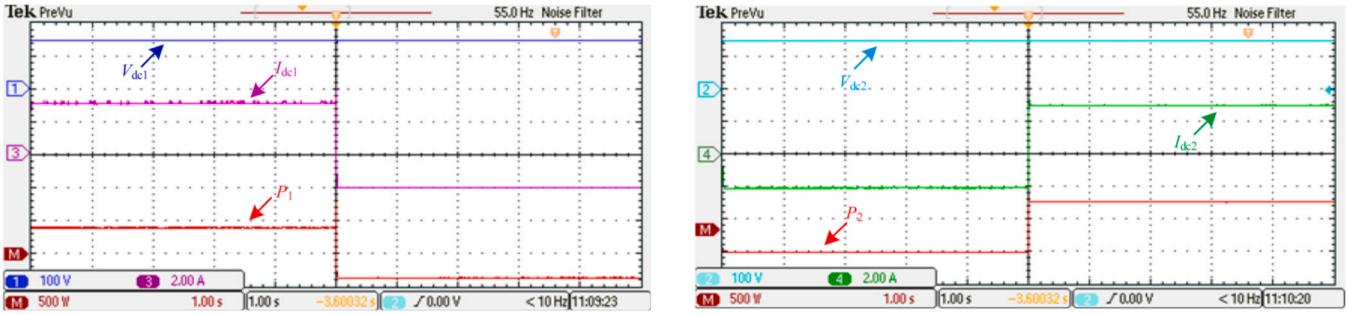

Fig. 13. Experimental results during rated power reversal: active power flow, DC link voltage and currents of (a) port 1 and (b) port 2.

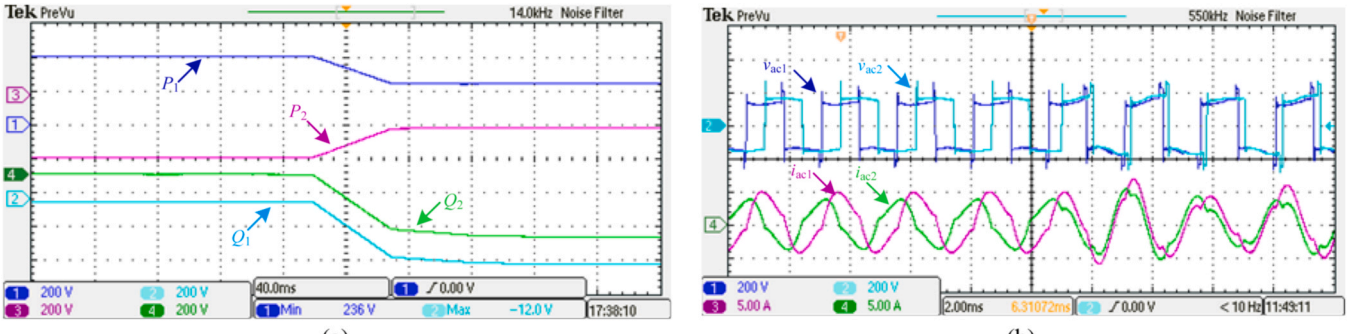

Fig. 14. Experimental results using phase shift control technique, (a) power flow and (b) AC link voltages and currents.

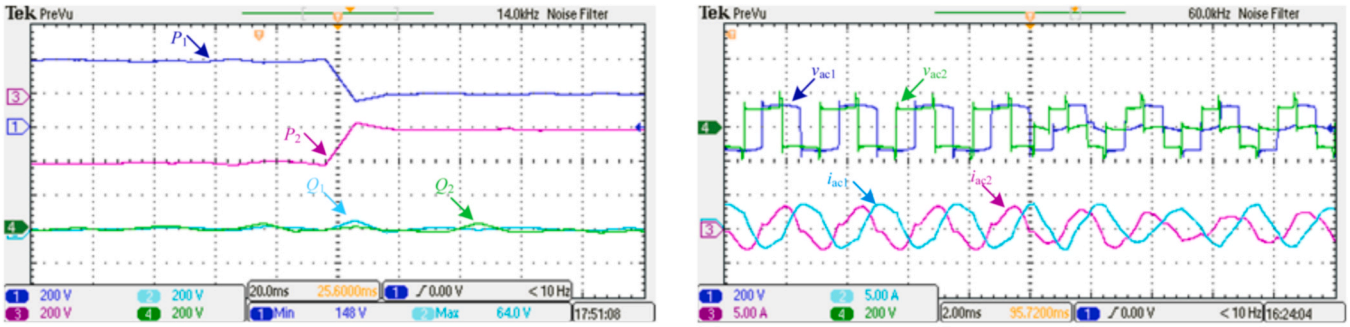

Fig. 15. Experimental results using firing-angle control technique, (a) power flow of ports, and (b) AC link voltages and currents.

Table 3
ABB semiconductors parameters.

Semiconductor type	IGBT Module5SNA 1500G450350		Bidirectional Thyristor5STB 18N4200	Phase Control Thyristor5STP 12F4200	Diode5SDF 13H4501
	IGBT	Diode			
Max voltage (V)	4500		4200	4200	4500
RMS Current (A)	1500		3020	1860	1900
On-state voltage (V) at 125^0 C at 1500 A	3.55	2.8	1.4	1.85	2.1
On-state resistance at 125^0 C (mΩ)	0.1	0.1	0.285	0.545	0.48
Cost/unit ($)	2162.41		1691.39	296.53	741.86

i. *Phase shift control*

In this scenario, a change in the magnitude of power flow is applied from port 1 to port 2 using the phase shift control technique. The active and reactive powers flow of ports 1 and 2 are shown in Fig. 14 part (a). It can be observed that during the rated power flow, the reactive power is almost zero. Additionally, as the power flow deviates from the rated value, the reactive power increases to indicate constant apparent power. Moreover, the AC voltages and currents are shown in Fig. 14 part (b), where the phase shift is $\delta = 90^\circ$ to provide the rated power flow from port 1 to port 2. The phase shift changes to $\delta = 30^\circ$ corresponding to half rated value of power flow. It is obvious that both currents are out of phase by 90° at the rated value and the phase shift changes to accommodate the change in power flow.

ii. *Firing-angle control*

To test the firing-angle control technique, a change in the magnitude of power flow is applied from port 1 to port 2. The active and reactive powers of port 1 and 2 are shown in Fig. 15 (a). It can be observed that as the power flow deviates from rated value, the amount of reactive power remains zero, which proves the paper's claims regarding this control technique. Furthermore, the AC voltages and currents are shown in Fig. 15 (b). It can be observed that the phase shift between them remains unchanged during rated and partial power flow. However, the zero level has increased during partial power flow due to the increase of the firing-angle α. Moreover, the AC currents exhibit no change in the phase shift.

8. System comparison

A comprehensive comparison is studied to show the advantages of the proposed DC-DC converter over other existing converters in terms of semiconductors count, number of capacitors, losses, and cost. Several converters are considered in the comparison including HB-MMC [13], FB-MMC [15,16], CTB [21,22], TAC /SSMMC [26–28], and TH-MMC (third embodiment of the patent) [19,20]. It is worth noting that the comparison is held assuming an H-bridge configuration for all converters. Also, the loss study is done at the rated power using the trapezoidal voltage waveform control technique with the LCL filter for all converters. Hence, the current is in phase with the voltage (zero reactive power is maintained at the rated power). Furthermore, since a trapezoidal voltage waveform control is used, the switching of the

Table 4
Key feature comparison of different converters for 60 MW system and ± 30 kV DC link.

Converter Type	HB-MMC [13]	FB-MMC [15,16]	CTB [21,22]	TAC/SSMMC [26–28]	TH-MMC [19,20]	Proposed converter
No. of SM Capacitors	30 × 4	30 × 4	15 × 2	30 × 2	15 × 4	33 × 2
Type of SWs	IGBT	IGBT	IGBT	IGBT	IGBT, SCR, Diodes	IGBT & SCR
No. of IGBTs	2×30×4 = 240	4×30×4 = 480	4×15×2 + 30 × 4 = 240	2×30×2 + 30 × 2 = 180	4×15×4 = 240	2×33×2 = 132
No. of Bidirectional Thyristors	None	None	None	None	None	30 × 2 = 60
No. of Thyristors with Antiparallel Diodes	None	None	None	None	15 × 4 = 60	None
No. of Limb Inductors	4	4	2	2	4	2
No. of DC Link Capacitors	None	None	2	None	None	None
Losses of HB-SMs	283.18 kW	None	None	141.85 kW	None	165.4 kW
Losses of FB-SMs	None	509.1 kW	0.442 kW	None	254.54 kW	None
Director Switches	None	None	282.66 kW	141.33 kW	None	None
Losses of Thyristors	None	None	None	None	103.36 kW	66.73 kW
Total Semiconductor Losses	283.18 kW 0.472%	509.1 kW0.8485%	283.1 kW 0.4718%	283.18 kW0.472%	357.91 kW0.5965%	**232.1 kW0.3869%**
Overall Semiconductor Cost	$519 k	$1.038 M	$519 k	$389.23 k	$ 581.28 k	**$386.92 k**

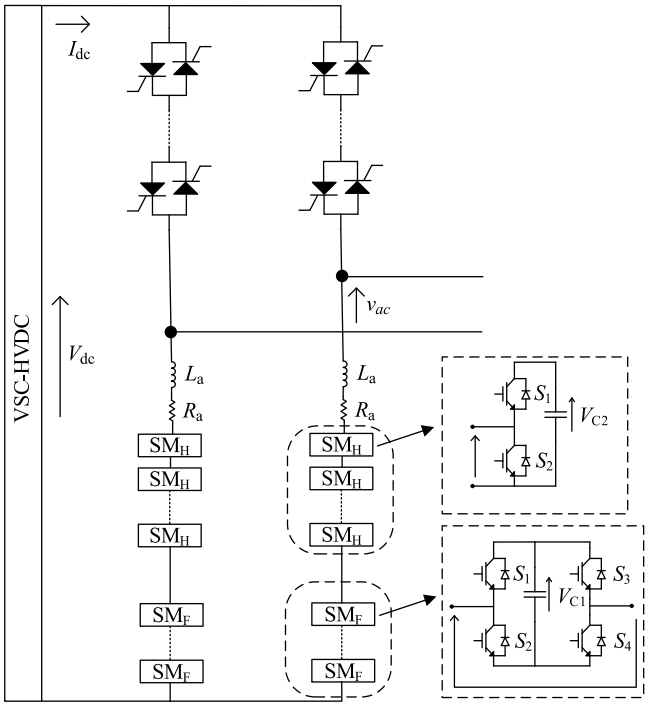

Fig. 16. A new variant of the proposed DC-DC converter intended for multiport DC-Hub.

semiconductors occurs only at the ramp time of the waveform, hence, it can be neglected for all converters. The average conduction losses calculations are based on [31] as follows:

$$P_{cond\,avg} = \frac{1}{T_b}\int_0^{T_b} p_{cond\,inst}(t)\quad dt \tag{41}$$

where, the instantaneous conduction losses of the power devices are determined as follows:

$$p_{cond\,inst}(t) = v_{cond}(i_x(t))\quad i_x(t)\quad D(t) \tag{42}$$

where, $i_x(t)$ is the instantaneous current that passes through the power devices, $D(t)$ is the duty ratio that depends on the modulation method used, and the conduction voltage (v_{cond}) is calculated as follows:

$$v_{cond}(i_x(t)) = V_{cond0}(T_{ref}) + i_x(t)\quad r_{cond}(T_{ref}) \tag{43}$$

where, V_{cond0} and r_{cond} are coefficients that can be determined from each device datasheet. T_{ref} is selected to be 125° for all devices. The comparison is based on practical ABB semiconductors as depicted in Table 3. A 60 MW system is assumed for all converters with ±30 kV DC link. The designed voltage per SM, switch, or thyristor is 2 kV. The comparison between all these converters has been summarized in Table 4.

In terms of the SM capacitors count, HB-MMC and FB-MMC require the maximum number of SM capacitors, while all the rest requires nearly half of the SM capacitor count except for the CTB topology that achieves the lowest number. However, the CTB requires two DC link capacitors which represent a major flaw Regarding the cost, the FB-MMC achieves the highest value while TAC/SSMMC and the proposed converter achieves the lowest cost. Moreover, the proposed converter achieves the lowest overall semiconductor power losses in addition to only two arm inductors per bridge are required.

9. The proposed converter in multiport DC-HUB

It is well known that the isolated two stage DC-DC converters can achieve DC fault blocking by turning off both bridges, However, in multiport DC-Hub, if a fault happens at one of the DC terminals, it is unacceptable to turn off the whole DC-Hub to block the fault. Therefore, a new variant of the proposed DC-DC converter is introduced that can block the DC-fault without turning off the other bridges. The new variant of the proposed converter only replaces the extra HB-SMs (that are used for thyristor commutation) by the same number of FB-SMs as shown in Fig. 16, therefore, the cost and losses have been slightly affected.

The fault blocking capability of the new variant is clearly illustrated in Fig. 17, where at the instant of a fault at the DC terminal, the current will flow (before any control action taken place) from the AC side through the conducting thyristor valve and MMC arm into the fault as shown in Fig. 17 (a). Therefore, to eliminate the injected current into the fault, the FB-SMs in the conducting MMC arm will generate a negative voltage to eliminate the fault current DC component (due to the SMs capacitors discharge) and the thyristors are triggered to circulate the fault current AC component as shown in Fig. 17 (b). After the thyristor valve is commutated successfully, all the gate signals to both MMC arms are prohibited as depicted in Fig. 17 (c).

10. Conclusion

This paper has introduced a new hybrid thyristor-based DC-DC converter for interconnecting VSC-based HVDC networks. Moreover, two different power flow control techniques have been developed, where each has its merits. The phase shift control technique provides smaller SM sizing at the cost of the appearance of reactive power during partial power flow, whilst the firing-angle control technique provides zero reactive power in full range of active power but with larger SM sizing. A MATLAB/SIMULINK model and a low scale experimental setup are designed and implemented to validate the concept of the proposed DC-DC converter with the new control techniques of power flow. Owing to the firing-angle control technique, the peak current in the rated power flow has been reduced from 5 A to 3.5 A. Moreover, a comprehensive comparison has been provided, which highlights the superiority of the

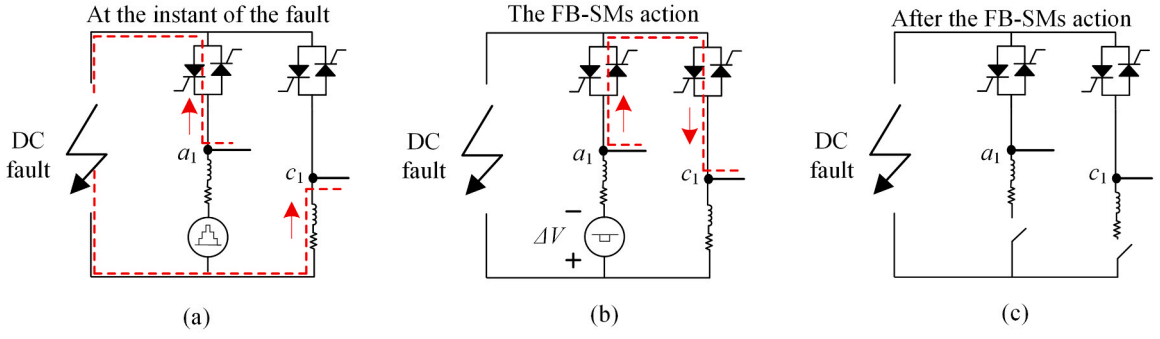

Fig. 17. Fault blocking capability illustration of the new variant of the proposed converter: (a) At the instant of DC fault (before any control action), (b) during the action of the FB-SMs in the conducting MMC arm, and (c) after the control action (fault is clearly isolated).

proposed DC-DC converter among other candidates. The proposed converter demonstrates superiority in several aspects. It has been verified that at the same ratings, it uses approximately 27% fewer IGBTs compared to the TAC. Additionally, the proposed converter exhibits an 18% reduction in overall semiconductor losses compared to the TAC, CTB, and HB-MMC. Finally, a new variant is proposed by adding extra full-bridge submodule that force turn-off the thyristor arm during DC fault in the application of DC-Hub. Thus, blackout prevention and modularity are achieved, where one the faulted port is only shutdown without affecting the healthy ports. Last but not least, further investigation is needed to determine the feasibility of using the proposed new variant as a DC hub connecting multiple ports. Additionally, the potential utilization of the converter in interconnecting LCC/VSC HVDC networks should be explored in future research.

Declaration of Competing Interest

None.

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