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New Hybrid Thyristor-based Multilevel Converter with DC Fault Blocking Capability, for HVDC Applications

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***Abstract*—HVDC systems are the most suitable solution for distant high-power transmission, where modular multilevel converters (MMCs) are now utilized due to their controllability, modularity, redundancy, and scalability. DC fault blocking capability in MMCs is normally achieved by using full-bridge submodules (FB-SMs) in the arms. However, using FB-SMs results in a high semiconductor count, which increases power losses and the overall cost. In this paper, a new hybrid thyristor-based multilevel converter (HTMC) with DC fault blocking capability is proposed that uses a low number of FB-SMs with a majority of half-bridge submodules and antiparallel thyristor valves. The theory of operation is detailed including the function of each element and thyristor valve commutation. Full parameter analysis is provided for the proposed converter. The claims of the paper are verified using a MATLAB SIMULINK model and an experimental test rig. Additionally, a detailed comparison with other viable converters is provided, which establishes that the proposed HTMC converter offers a low number of IGBTs, and lower cost and losses, with DC fault-blocking capability.**

***Index Terms*-- Modular multilevel converter (MMC), HVDC, Thyristors, Power control, Bidirectional power flow.**

I. Introduction

Interest in high-power transmission has been increasing due to the vast expansion of renewable sources, especially for long distances from the grid. The most effective method for long distances power transmission uses high voltage direct current (HVDC) rather than high voltage alternating current (HVAC) technology [1]. The line commutated converter (LCC) has been utilized since the 1960s in HVDC transmission due to the advantages of high surge current endurance, high efficiency and DC fault ride-through capability [2]. However, LCC is sensitive to AC grid disturbances because the grid voltage controls thyristor turn-on and turn-off (hence may suffer from commutation failure). Also, the LCC generates AC harmonic currents, and is unable to control reactive power independently from active power, hence needs reactive power compensation.

Using a two-level voltage source converter (VSC) can eliminate most LCC drawbacks, where the VSC can control active and reactive powers independently and can also be connected to weak AC grids [3] but at the expense of increasing cost, decreasing efficiency, and the abandonment of the DC fault blocking capability [4]. Recently, the VSC-based modular multilevel converter (MMC) has been introduced in [5], which handles some two-level VSC drawbacks. The half-bridge MMC (HB-MMC) is the most utilized MMC in the industry due to its features of controllability, redundancy, modularity, and scalability. The HB-MMC is considered to have higher efficiency due to its low frequency operation. HB-MMC modifications have been proposed to increase the efficiency and reduce the number of components [6], however, the HB-MMC cannot tolerate a DC fault [7, 8], which is a major issue in multi-terminal DC (MTDC). Hence, a DC circuit breaker (CB) should be used as a solution to block DC faults in a HB-MMCs based MTDC system [9-11]. However, a DC breaker leads to higher cost and losses. Another literature solution uses fault-tolerant converters, such as the full bridge MMC (FB-MMC). FB-MMC offers DC fault blocking capability but at the expense of doubling the number of semiconductors, which significantly increases converter cost and decreases efficiency [12]. As a development to the FB-MMC, a hybrid MMC has been introduced [13, 14], which replaces some of the full bridge submodules (FB-SMs) with half-bridge submodules (HB-SMs). Also, the converter proposed in [15], called the alternate arm converter (AAC), replaces some of the FB-SMs with a director switch, which is comprised of a series of connected IGBTs. These converters aim to decrease the overall cost and number of utilized semiconductors while maintaining DC fault-blocking capability. Subsequent AAC converter research has enhanced and improved its operation [16-18]. The extended overlap AAC (EO-AAC) is one modification to the AAC converter, where a third harmonic waveform is subtracted from the fundamental component to achieve a smoother current and a wider operational range at the expense of a higher number of FB-SMs. However, despite the replacement of some FB-SMs, the efficiency of these converters remains lower than that of standard HB-MMC and LCC converters.

Thus the concept of adding thyristors to VSC-converters in order to increase efficiency has prompted research [19]. Thyristor-bypassed SM power groups (PG)-based converters have been proposed [20-22], where antiparallel thyristors bypass the SMs that are non-blocking (at the instants of their conduction) to reduce operational losses. In the literature, PGs have been used in the FB-MMC, hybrid MMC, and EO-AAC. Even though these converters achieve lower conduction losses, their main drawback is the utilization of a large number of semiconductors (FB-SMs and antiparallel thyristors) that significantly increase the total cost. The active forced commutated (AFC) bridge-based converter in [23, 24], consists of antiparallel thyristor valves for bulk power flow and a chain

of FB-SMs for controlling the turn-off of the thyristor valves. The FB-SMs chain is also used to establish the ramp periods of the AC voltage waveform. This converter achieves low conduction losses, but it has the drawback of requiring a large filter at the AC link due to high harmonic content. In [25, 26], a converter, called the modular embedded multilevel converter (MEMC) was proposed, which utilizes antiparallel thyristor valves with SMs in a three-level structure. The thyristor valves are used to decrease the conduction losses and reduce SM storage energy requirements. However, to incorporate DC fault blocking, FB-SMs are used which increases the number of semiconductors and the overall cost. The converter in [27, 28], named the hybrid alternate common arm converter (HACC), uses antiparallel thyristor valves to connect arms in parallel to double the power capability of the converter without doubling semiconductor ratings. However, this converter suffers from discontinuous operation. Also, the turn off process of the thyristor valves limits converter power capability. In [29], an MMC of mixed cells (HB-SMs and unipolar FB-SMs) is proposed with crossing thyristor branches (CTB-MMC). The thyristor branches are used to cross-connect different arm inductors to interrupt the current during a DC fault. Since the thyristors are only fired during faults, this topology relies solely on SMs during normal operation, and as a result, does not take advantage of lower thyristor conduction losses.

From the foregoing discussion, the main issue with existing converters is the large number of FB-SMs to achieve DC fault-blocking capability, which increases the total number of semiconductors. In this paper, a new hybrid thyristor-based multilevel converter (HTMC) is proposed for HVDC applications. The proposed converter utilises antiparallel thyristors, HB-SMs, and a limited number of FB-SMs. Normally, thyristors are favoured over IGBTs due to their high overcurrent capability, lower cost, lower losses, and availability at higher voltage and current ratings.

The summarised main contributions of the paper are:

- A new hybrid multilevel thyristor-based converter with DC-fault blocking capability.
- Low number of IGBTs (minority of FB-SMs), lower overall cost, and reduced conduction losses (utilization of thyristors).
- Detailed analysis of the proposed converter during normal operation as well as during a DC fault.
- The converter's full parameter design.
- Enabling thyristor commutation time and overlap time between upper and lower arms without affecting the output AC waveform by subtracting a third harmonic from the reference voltage waveform.
- Discussion on the relationship between the third harmonic ratio and the number of FB-SMs.

These claims are validated using a MATLAB SIMULINK model and experimental results. An extensive comparison is performed using typical parameters to highlight the advantages of the proposed converter over those in the literature, in terms of semiconductor count, passive elements, current stresses, losses, cost, fault clearing time, weight, and size.

The remainder of this paper is organized as follows: Section II discusses the proposed topology architecture, operation, and analysis for normal operation and DC fault scenarios. Section III provides a complete parameter design for the proposed HTMC. Section IV presents simulation results based on a 401-level MATLAB/SIMULINK model of the proposed HTMC. Section V provides results from a scaled-down 3-phase 5-level experimental test rig of the proposed converter. Section VI, before the conclusions, presents an extensive comparison between the proposed converter and other converters in the literature.

II. Proposed Topology Description

A. Proposed Converter Architecture

The proposed 3-phase HTMC has 6 arms as shown in Fig. 1, where each arm consists of a thyristor valve (series connection of antiparallel thyristors) and an MMC stack which is comprised of HB-SMs, and a limited number of FB-SMs. Each arm element type has a specific role during converter operation. The HB-SMs are responsible for creating the output sinusoidal AC voltage waveform. The FB-SMs create an overlap period between the lower and upper arms (where both the thyristor valves in the same leg are conducting) to retain balance between SM capacitors.

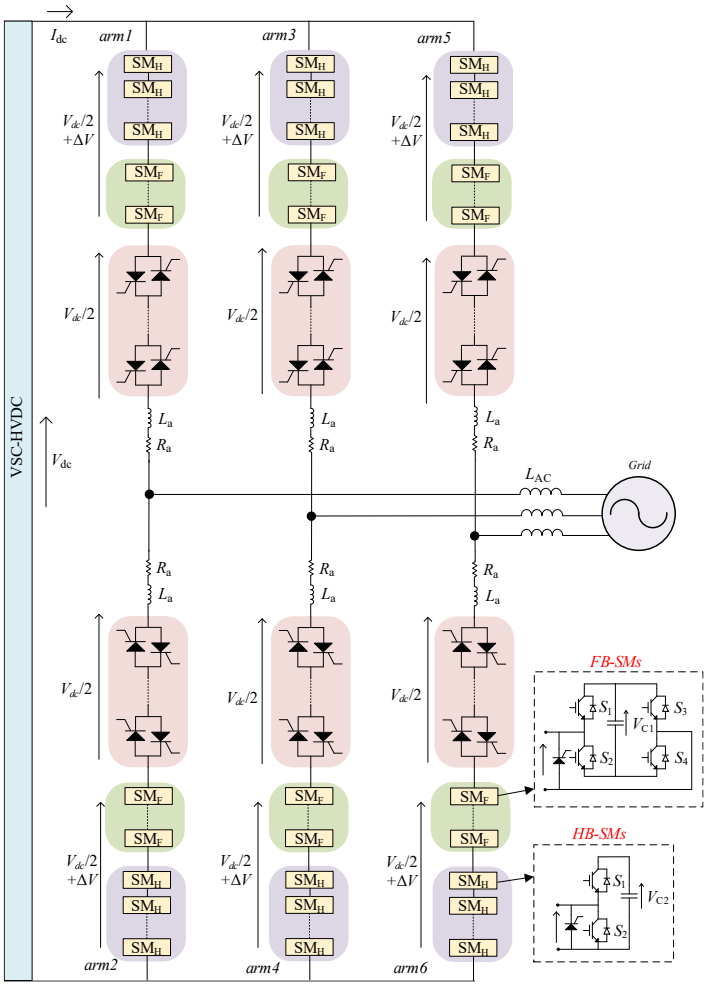


Fig. 1. Proposed converter architecture.

In addition, the FB-SMs are responsible for thyristor commutation in normal operation and DC fault cases (FB-SMs use their positive voltage state during normal operation commutation while their negative voltage state is used for commutation during faults). The thyristor valve is used to decrease the conduction losses in normal operation and block the fault current during fault scenarios. Both thyristor valves and HB-SMs in each arm are designed to endure $½V_{dc}$, while FB-SMs per arm are designed to generate $\pm \Delta V$ (to allow for the overlap and commutation times). Thus, the whole MMC stack should be able to generate from $-\Delta V$ to $½V_{dc} + \Delta V$.

Note the SMs have protection bypass thyristors as shown in Fig. 1 to bypass the AC component of the DC fault current until it is blocked by the thyristor valve (as is illustrated in detail in subsection C).

B. Proposed Converter Operation and Analysis (with Third Harmonic Subtraction)

Overlap and commutation periods are essential during operation of the proposed converter due to the utilisation of thyristors. The overlap period is important to rebalance the energy between the upper and lower SM capacitors while the commutation period is required to turn off the thyristor valves at the end of their conduction period. However, without third harmonic subtraction (only sinusoidal fundamental AC waveform) to allow even a small overlap or commutation time, a large number of FB-SMs is required, which increases the converter cost, and losses. Therefore, a third harmonic waveform is subtracted from the sinusoidal fundamental AC waveform so that the resultant waveform is characterised by a low voltage change near zero as shown in Fig. 2 (first drawing, in red) compared to the fundamental waveform (in green), hence a low number of FB-SMs is required. Therefore, subtracting a third harmonic waveform permits an increase in an arm overlap period and allow a longer time for force commutation of the thyristor valve while using fewer FB-SMs.

In addition, the FB-SMs can produce its negative state voltage to increase the overall phase peak voltage ($\hat{v}_a$) to $½V_{dc} + \Delta V$ as shown in Fig. 2. Therefore, the fundamental phase peak voltage ($\hat{v}_{a_1}$) remains at $½V_{dc}$. Hence, the fundamental phase voltage v_{a_1} is as follows:

$$v_{a_1}(t) = \hat{v}_{a_1} \sin \omega t = ½V_{dc} \sin \omega t \tag{1}$$

The injected third harmonic voltage (v_{a_3}) is:

$$v_{a_3}(t) = \Delta V \sin 3\omega t = k_3 \hat{v}_{a_1} \sin\ 3\omega t \tag{2}$$

where k_3 is the third harmonic voltage ratio. The resultant phase voltage $v_a(t)$ is:

$$v_a(t) = ½V_{dc}(\sin \omega t - k_3 \sin 3\omega t) \tag{3}$$

Since the MMC stack and thyristor valve are series connected and sharing the DC link voltage, the arm 1 voltage is:

$$v_{arm_1}(t) = v_{stack_1}(t) + v_{valve_1}(t) \tag{4}$$

In order to provide the required phase voltage, force commutating the thyristor valve, and to maintain the maximum thyristor valve voltage at $½V_{dc}$, the MMC stack 1 voltage is given as (5), while MMC stack 2 voltage is given by (6).

$$v_{stack_1}(t) = \begin{cases} ½V_{dc} - v_a(t), & -T_{ov} < t < ½T_p \\ ½V_{dc} \text{ or } ½V_{dc} + \Delta V, & ½T_p < t < ½T_p + T_c \\ ½V_{dc} + \Delta V, & ½T_p + T_c < t < T_p - T_{ov} \end{cases} \tag{5}$$

$$v_{stack_2}(t) = \begin{cases} ½V_{dc} \text{ or } ½V_{dc} + \Delta V, & 0 < t < T_c \\ ½V_{dc} + \Delta V, & T_c < t < ½T_p - T_{ov} \\ ½V_{dc} + v_a(t), & ½T_p - T_{ov} < t < T_p \end{cases} \tag{6}$$

where T_c is the overall commutation time which includes the circuit commutation turn off time of the thyristor t_q and the falling time of the current T_f. T_{ov} is the overlap time and T_p is the periodic time. The 2nd part of the v_{stack_1} equation is equal to $½V_{dc} + \Delta V$ in the case of positive arm current at the instant of commutation so that the MMC stack can provide force voltage commutation to the thyristor valve before continuing with the next part of the waveform. But in case of negative arm current, it is equal to $½V_{dc}$ so that a positive voltage can be applied to the thyristor valve for force commutation. The same applies for the first part of v_{stack_2}.

To understand the operation of the proposed converter, phase '*a*' voltage waveforms in addition to MMC stacks and thyristor valves of arms 1 and 2 voltage and current waveforms are depicted in Fig. 2, where the dashed currents are for positive power flow while the solid currents are for negative power flow. For clarity, the dashed parts of the voltage waveforms of the MMC stack and thyristor valve correspond to the dashed arm currents.

Fig. 2 is divided into 6 sections from section 'a' to section 'f', which are explained in the parts of Fig. 3, where in each section the converter operation is as follows:

Section 'a': MMC stack 2 provides force commutation to thyristor valve 2 by generating $½V_{dc} + \Delta V$ for positive arm current at the commutation instant (solid currents in Fig. 2) or by generating $½V_{dc}$ for negative arm current at the commutation instant (dashed currents in Fig. 2). Thyristor valve 1 is still conducting while MMC stack 1 is building the output phase voltage, so to be unaffected by commutation action.

Section 'b': Thyristor valve 1 is conducting. MMC stack 1 is building the output phase voltage while MMC stack 2 is maintained at $½V_{dc} + \Delta V$ to keep the maximum voltage on thyristor valve 2 at $½V_{dc}$.

Section 'c': Both thyristor valves are conducting (overlap period). MMC stack 1 continues to build the output phase voltage while MMC stack 2 produces the complementary voltage to maintain the leg voltage at V_{dc}. In this period, circulating current flows in both arms to balance the upper and lower SM capacitor voltages.

Section 'd': MMC stack 1 provides force commutation to thyristor valve 1, the same as with MMC stack 2 in section '**a**'. Thyristor valve 2 is conducting while MMC stack 2 is building the output phase voltage so as not to be affected by commutation action.

Section 'e': Thyristor valve 2 is conducting. MMC stack 2 is building the output phase voltage while MMC stack 1 is maintained at $½V_{dc} + \Delta V$ to keep the maximum voltage on thyristor valve 1 at $½V_{dc}$.

Section 'f': Both thyristor valves are conducting (overlap period). MMC stack 2 continues to build the output phase voltage while MMC stack 1 produces the complementary voltage to keep the leg voltage at V_{dc}. Like section '**c**', circulating current flows in both arms to balance voltages on the upper and lower SM capacitors.

The same procedures are applied for the other phases but with phase shifts of -120° and 120° to the second and third phases, respectively.

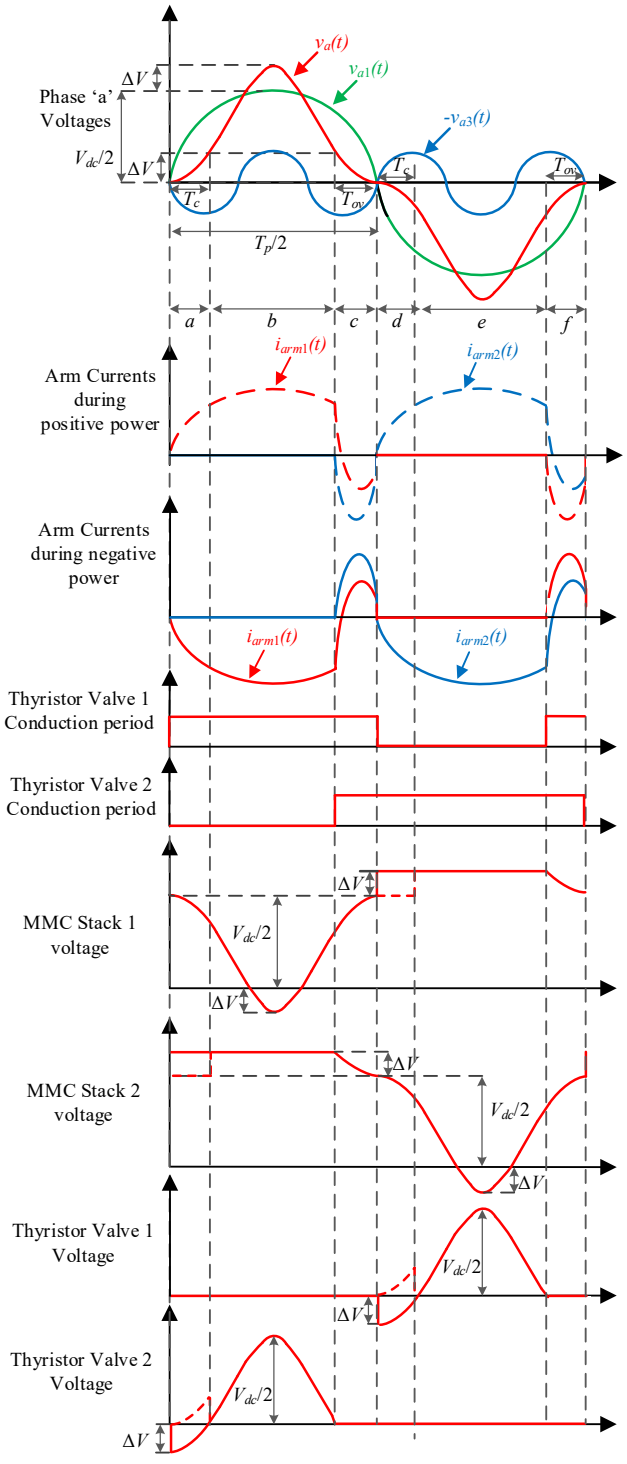


Fig. 2. Phase '*a*' voltage waveforms and related voltage and current waveforms of the MMC stack and thyristor valve of arms 1 and 2.

C. *DC-Fault Blocking Analysis*

The DC-fault current from the converter perspective can be divided into two components, namely DC component due to the SMs capacitors discharge and AC component due to the AC grid feeding the DC fault through the converter arms. The proposed converter can quickly interrupt the DC component (using the FB-SMs). On the other hand, the AC component is mainly terminated inherently by the thyristor valve. For a clearer illustration, an example is studied as shown in Fig. 4, where it is assumed that phase 'a' has a positive voltage (maximum magnitude), while phase 'b' and phase 'c' have negative voltages. In addition, phase 'b' is assumed to have the lowest voltage magnitude, near zero, hence in the overlap state. Fig. 4(a) shows the fault occurrence instance, before fault detection, where the blue line indicates the DC component of the fault current (in phase 'b' due to the overlap state), while the yellow and the red lines indicates the AC components of the DC fault. Fig. 4(b) shows the instant of fault detection, where the DC fault blocking procedures are initiated, namely; in phase 'b', all HB-SMs are bypassed while the FB-SMs inject their negative voltage to quickly block the DC component of the DC fault current. All antiparallel thyristor valve gate pulses are prohibited. Also, the conducting SMs protection thyristors are fired to conduct the AC components of the DC fault current until it is extinguished. Fig. 4(c) shows the instant where the DC component of the DC fault current is blocked. Note that if the AC component still exists in phase 'b' then it would flow in the protection thyristors in the lower arm of phase 'b' until the fault current is interrupted. Finally, Fig. 4(d) shows the instant where the fault current is completely terminated by the thyristor valve, where all the SMs are bypassed and the AC voltages are endured by the thyristor valve.

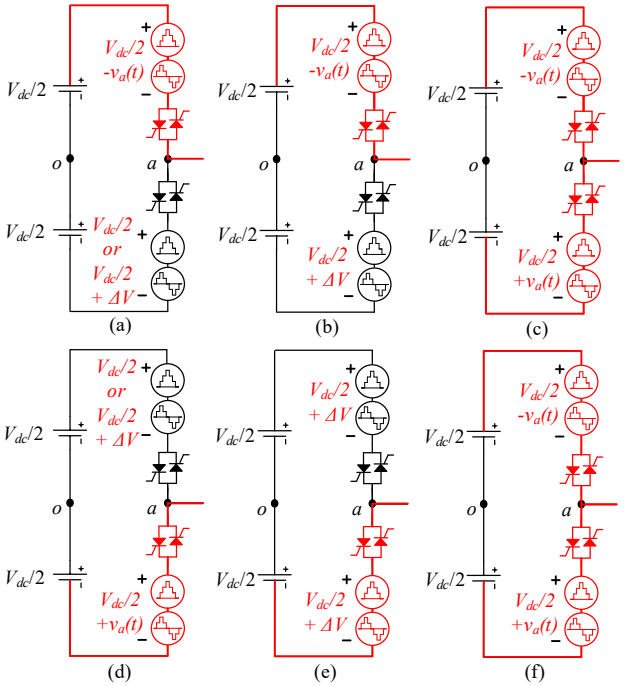


Fig. 3. Operation analysis diagrams of phase '*a*': (a) thyristor valve 2 commutation, (b) arm 1 conduction, (c) overlap period, (d) thyristor valve 1 commutation, (e) arm 2 conduction, and (f) overlap period.

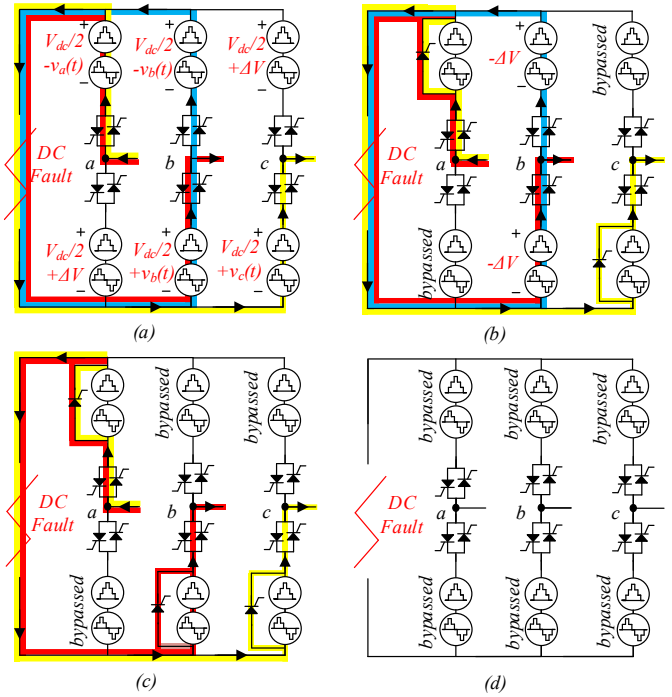


Fig. 4. Fault blocking operation diagram: (a) DC fault occurrence, (b) DC fault detection instant, where all fault blocking procedures are initiated, (c) DC component of the fault is interrupted, and (d) DC fault is completely eliminated.

III. System Design

A. Third Harmonic Ratio and SMs/Thyristors Count

In order to determine the third harmonic ratio k_3, the minimum overall commutation time T_c must be calculated. The overall commutation time T_c of the thyristor valves should be more than the fall time of the thyristor peak current T_f plus the thyristor circuit-commutation turn off time t_q, where $T_c \geq T_f + t_q$. In the analysis, it is assumed that overall commutation time T_c is equal to the overlap time T_{ov}. Since the FB-SMs are responsible for creating commutation periods, the phase voltage in (3) at T_c should be equal to ΔV (as depicted in Fig. 2) so that the MMC stack can apply negative voltage across the thyristor valve during the commutation period, as follows:

$$\frac{V_{dc}}{2}(\sin(\omega T_c) - k_3 \sin(3\omega T_c)) = \Delta V = k_3 \frac{V_{dc}}{2} \tag{7}$$

Hence, the relation between k_3 and T_c can be deduced as:

$$k_3 \geq \frac{\sin \omega T_c}{1 + \sin 3\omega T_c} \tag{8}$$

To show the effect of the third harmonic subtraction on the required ΔV (FB-SMs voltage), Fig. 5 shows the per unit value of the FB-SMs voltage ($\Delta V_{pu} = \Delta V / ½V_{dc}$) with and without third harmonic subtraction, where $\Delta V_{pu} = k_3$ in the third harmonic subtraction case. The required FB-SMs voltage is decreased dramatically with third harmonic subtraction, especially for $T_c > 1$ ms.

The number of FB-SMs can be determined as:

$$N_{FB} = \frac{\hat{v}_{a_3}}{V_{SM}} = \frac{k_3 V_{dc}}{2V_{SM}} \tag{9}$$

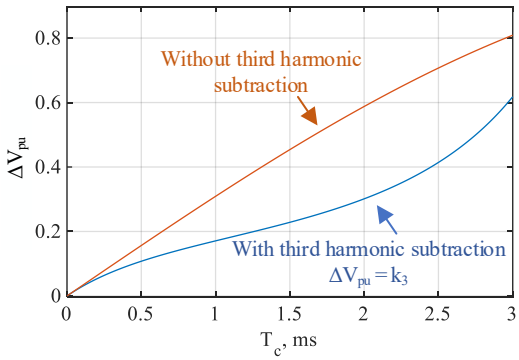


Fig. 5. The per unit value of the FB-SMs voltages with and without third harmonic subtraction.

where V_{SM} is the SM nominal voltage. On the other hand, the number of HB-SMs, N_{HB}, should be based on the fundamental waveform peak voltage $\hat{v}_{a_1}$:

$$N_{HB} = \frac{\hat{v}_{a_1}}{V_{SM}} = \frac{V_{dc}}{2V_{SM}} \tag{10}$$

For the thyristor valve, their maximum voltage is kept at $½V_{dc}$, as mentioned previously. Therefore the number of thyristors in each valve is:

$$N_{thy} = \frac{\hat{v}_{valve}}{V_{thy}} = \frac{V_{dc}}{2V_{thy}} \tag{11}$$

where V_{thy} is the nominal voltage of each thyristor. The number of thyristors can be equal to that of the HB-SMs if both have the same rated voltage.

B. Arm Inductance, L_a

The arm inductance (L_a) is selected such that during thyristor valve commutation, the falling time of the thyristor current from its peak value is equal to or less than the desired value T_f. Also, the arm inductance should limit the rate of the change of the thyristor current (di/dt) to less the maximum permitted turn-on current ramp rate of the thyristor, σ.

Assuming a positive arm current during the instant of commutation of thyristor valve 2, MMC stack 2 generates its peak voltage of $(1 + k_3)½V_{dc}$, while MMC stack 1 builds the AC waveform. Both thyristor valves are conducting before the commutation process occurs. Therefore, with two arm inductances in each leg, the voltage applied on the arm inductance[1] (v_L) is:

$$\begin{aligned} v_L(t) &= ½(V_{dc} - v_{arm_1} - v_{arm_2}) \\ &= ½(V_{dc} - v_{stack_1} - v_{stack_2}) \end{aligned} \tag{12}$$

Substituting the MMC stack voltages results in:

$$\begin{aligned} v_L(t) &= ¼V_{dc}\big(\sin \omega t - k_3(1 + \sin 3\omega t)\big) \\ &= \frac{L_a\, di_{arm}}{dt} \end{aligned} \tag{13}$$

Therefore, the rate of change of the arm currents is given by:

$$\frac{di_{arm}}{dt} = \frac{V_{dc}}{4L_a}\big(\sin \omega t - k_3(1 + \sin 3\omega t)\big) \tag{14}$$

By solving this differential equation, the arm current is:

$$\begin{aligned} i_{arm}(t) = -\frac{V_{dc}}{12\omega L_a}(k_3(3\omega t - \cos 3\omega t) \\ + 3\cos \omega t) + c \end{aligned} \tag{15}$$

Assuming that at the time of commutation ($t = 0$), the arm current equals the peak phase current ($\hat{\imath}_a$), which is the worst-case scenario, then the constant c is calculated as follows:

$$i_{arm}(0) = \hat{\imath}_a = -\frac{V_{dc}}{12\omega L_a}(3 - k_3) + c \tag{16}$$

$$c = \hat{\imath}_a + \frac{V_{dc}}{12\omega L_a}(3 - k_3) \tag{17}$$

Therefore the arm current formula during commutation is:

$$i_{arm}(t) = \hat{\imath}_a - \frac{V_{dc}}{12\omega L_a}\big(k_3(3\omega t - \cos(3\omega t) + 1) + 3(\cos(\omega t) - 1)\big) \tag{18}$$

It is desired that at $t = T_f$, the arm current be zero, therefore:

$$i_{arm}(T_f) = 0 = \hat{\imath}_a - \frac{V_{dc}}{12\omega L_a}\big(k_3(3\omega T_f - \cos(3\omega T_f) + 1) + 3(\cos(\omega T_f) - 1)\big) \tag{19}$$

Hence the arm inductance (L_a) can be calculated as (20).

$$L_a \le \frac{V_{dc}}{12\omega \hat{\imath}_a}\big(k_3(3\omega T_f - \cos(3\omega T_f) + 1) + 3(\cos(\omega T_f) - 1)\big) \tag{20}$$

Also, the inductance should consider that the maximum permitted thyristor turn-on current ramp rate σ is not exceeded. The maximum current rate of change occurs at the instant of thyristor valve commutation. Therefore, the following equation should be satisfied, which is derived by substituting t=0 in (14).

$$L_a > k_3 \frac{V_{dc}}{4\sigma} \tag{21}$$

It is worth noting that the arm inductance is selected near the maximum value calculated from (20) to limit the circulating currents during overlap periods.

C. *Capacitance in HB-SMs and FB-SMs*

In this section the capacitances of both the HB-SMs and FB-SMs are calculated, where for an accurate evaluation of their capacitance, the conduction period of the MMC stack is divided into two portions. The first portion occurs when the MMC stack generates a positive voltage where the energy deviation in the MMC stack is shared among all the SMs ($N_t = N_{HB} + N_{FB}$). The second portion occurs when the MMC stack generates a negative voltage where the energy deviation is endured only by the FB-SMs. The capacitance design of the proposed converter follows the same procedures as in [30]. However, the method is modified to calculate the energy deviation of each SM directly instead of the whole MMC stack, to accurately design both the HB-SMs and FB-SMs. The energy deviation of each SM in the MMC stack (ΔE_{SM}) can be calculated from:

$$\Delta E_{SM}(t) = \int_0^t \frac{P_{stack}(x)}{N_{SM}(x)}\,dx \tag{22}$$

where P_{stack} is the MMC stack power and N_{SM} is the number of the functionable SMs during the conducting periods of the MMC stack. N_{SM} depends on the MMC stack voltage as previously illustrated and obeys the following equation:

$$N_{SM}(t) = \begin{cases} N_{HB} + N_{FB}, & v_{stack}(t) > 0 \\ N_{FB}, & v_{stack}(t) < 0 \end{cases} \tag{23}$$

The apparent power is:

$$|\bar{S}| = \frac{3\hat{v}_{a_1}\hat{\imath}_{a_1}}{2} \tag{24}$$

where $\hat{v}_{a_1}$ and $\hat{\imath}_{a_1}$ are the fundamental phase peak voltage and current, respectively. The MMC stack power P_{stack} is:

$$P_{stack}(t) = v_{stack}(t)\big(i_{stack}(t)\big) = \frac{2}{3}|\bar{S}|U(t) \tag{25}$$

where $U(t)$ is defined as:

$$U(t) = (1 - \sin\omega t + k_3 \sin 3\omega t)(\sin(\omega t + \phi)) \tag{26}$$

where ϕ is the power factor angle. By substituting (23) and (25) into (22), the energy deviation of the HB-SM is:

$$\Delta E_{HBSM}(t) = \frac{2}{3}\frac{|\bar{S}|}{(N_{HB}+N_{FB})}\int U(x)\,dx, \quad v_{stack}(t) > 0 \tag{27}$$

The integration is valid only when the MMC stack generates a positive voltage and during the MMC stack conducting period until entering the overlap state, where energy balance occurs between the upper and lower arms.

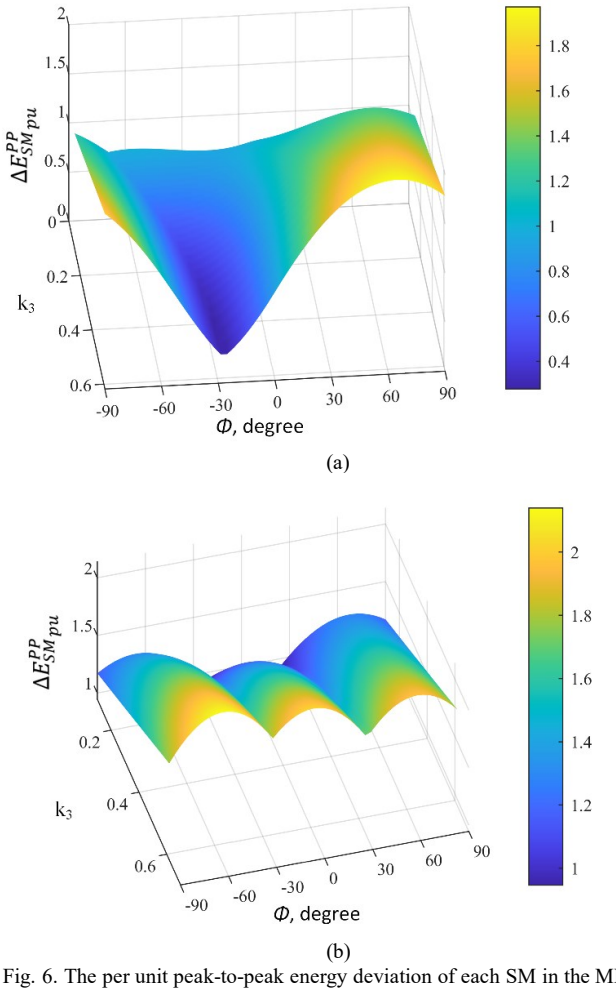


Fig. 6. The per unit peak-to-peak energy deviation of each SM in the MMC stack at different k_3 and ϕ: (a) HB-SM case and (b) FB-SM case.

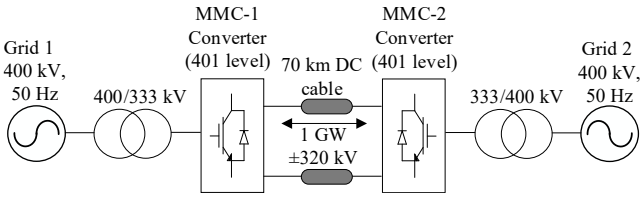


Fig. 7. Point-to-point 401-level HVDC transmission system.

Table 1: MATLAB Simulation Model Parameters

Parameter	Description	Value
P_r	Rated power	1 GW
V_{dc}	DC link voltage	±320 kV
v_g	Grid voltage	380 kV
f	Fundamental Frequency	50 Hz
L_{AC}	AC interfacing inductance	68.9 mH
T_c	Overall commutation time	1.26 ms
N_{HB}	Number of HB-SMs	200
N_{FB}	Number of FB-SMs	40
V_c	SM nominal voltage	1.6 kV
C_{HB}/C_{FB}	HB-SMs/FB-SMs capacitance	12.5 mF
L_{arm}	Arm inductance	5.5 mH

On the other hand, by doing the same substitution, observing that $N_{FB} = (N_{HB} + N_{FB})k_3/(1 + k_3)$, the energy deviation of the FB-SMs is:

$$\Delta E_{FBSM}(t) = \frac{2}{3}\frac{|\bar{S}|}{(N_{HB}+N_{FB})} \times \begin{cases} \int U(x)\,dx\ , & v_{stack}(t) > 0 \\ \frac{1+k_3}{k_3}\int U(x)\,dx, & v_{stack}(t) < 0 \end{cases} \quad (28)$$

where the factor $(1 + k_3)/k_3$ appears when the MMC stack generates a negative voltage because only the FB-SMs are burdened by the energy deviation in this section.

From (26), (27), and (28), k_3 and ϕ affect the energy deviation of the MMC stack SMs. Therefore, Fig. 6 is plotted to show the per unit peak-to-peak energy deviation ($\Delta E^{pp}_{SM\,pu}$) for different values of k_3 and ϕ, which obeys:

$$\Delta E^{pp}_{SM\,pu} = \frac{10^3 \Delta E^{PP}_{SM}(N_{HB} + N_{FB})}{|\bar{S}|} \quad (29)$$

where Fig. 6 (a) and (b) show the per unit peak-to-peak energy deviation of the HB-SMs and FB-SMs, respectively, in the MMC stack. Clearly the peak-to-peak energy deviation of both SMs increases with increasing k_3. On the other hand, the peak-to-peak energy deviation of the HB-SMs increases to a maximum value around ϕ=70° because the peak of the arm current matches a larger portion of the MMC stack voltage generation. However, the FB-SMs peak-to-peak energy deviation marginally changes with changing ϕ. The reason is that the FB-SMs, during the negative arm voltage generation (around zero ϕ), burden the energy deviation alone. Also, FB-SMs participate in the energy deviation with the HB-SMs resulting in a more flatten peak-to-peak energy deviation with ϕ. It can be deduced from the curves that the FB-SMs achieve a slightly higher maximum peak-to-peak energy deviation ($\Delta E^{pp}_{SM\,max}$) at each k_3 compared to that of the HB-SMs. Based on the maximum peak-to-peak energy deviation of the HB-SMs/FB-SMs at the desired k_3 deduced from Fig. 6 curves, and considering the desired peak-to-peak voltage ripple ratio (ΔV_r^{pp}), the SM capacitance (C_{SM}) is calculated as:

$$C_{SM} = \frac{\Delta E^{pp}_{SM\,max}}{\Delta V_r^{pp}\, V^2_{SM}} \quad (30)$$

IV. Simulation Validation

The MATLAB-SIMULINK model built for HTMC validation, is based on the 401-level system developed in [31]. The point-to-point connection of the HVDC transmission system is depicted in Fig. 7. Since the MMC stack in each arm only handles half the DC link voltage, the MMC stack is comprised of 200 HB-SMs and 40 FB-SMs. Based on the previous analysis, the converter parameters are designed and listed in Table 1. Since the thyristor turn off time t_q is typically 800µs, it is suitable to assume that the overall commutation time is 1.26ms, which corresponds to k_3=0.2 assuming $T_{ov} = T_c$. The arm inductance is selected as 5.5 mH based on (20) and (21). For capacitance evaluation, the maximum peak-to-peak energy deviation is determined for both SMs from the energy curves in Fig. 6 at $k_3 = 0.2$, where $\Delta E^{PP}_{SM\,max}$ of the HB-SM and FB-SM are found to be 5.86 kJ and 6.17 kJ, respectively. Substituting into (30) with ΔV_r^{pp}=0.2 (assuming a cell voltage ripple of ±10%), the capacitance of both HB-SM and FB-SM are selected to be 12.5 mF. A filter is used at the DC link terminal to smooth the DC current and limit the short circuit current. The simulation model is tested for normal operation as well as DC fault scenarios in order to validate the proposed converter.

A. Normal Operation

Bidirectional power flow capability is shown in Fig. 8 (a), where power is reversed successfully in 0.5 s while maintaining zero reactive power. The line voltages and phase currents are depicted in Fig. 8(b) and Fig. 8(c), respectively, where the third harmonic waveforms do not appear. Also, the commutation time does not affect the output waveforms. The arm currents in the case of grid absorbing and injecting power are shown in Fig. 8(d) and Fig. 9(a), respectively. The arm currents do not exceed the 1 pu value in both cases, hence low controlled current stresses in the proposed converter are achieved. The stack voltages are depicted in Fig. 9 (b) and Fig. 9 (c) in grid absorbing and injecting cases, respectively. In the grid absorbing case, the stack generates a voltage of 0.5pu at the time of commutation because of the negative arm current. However, in the grid injecting case, the MMC stack produces a voltage of 0.6pu due to the positive arm current at the instant of commutation. The thyristor valve voltages are shown in Fig. 9(d) and Fig. 10(a) for absorbing and injecting cases, respectively, where the thyristor valve voltage does not exceed 0.5pu. The simulation results nearly follow the deduced waveform diagrams in Fig. 6. The capacitor voltages of the HB-SMs, and FB-SMs are shown in Fig. 10(b) and Fig. 10(c) respectively, where the peak-to-peak voltage ripple does not exceed the 10% limit.

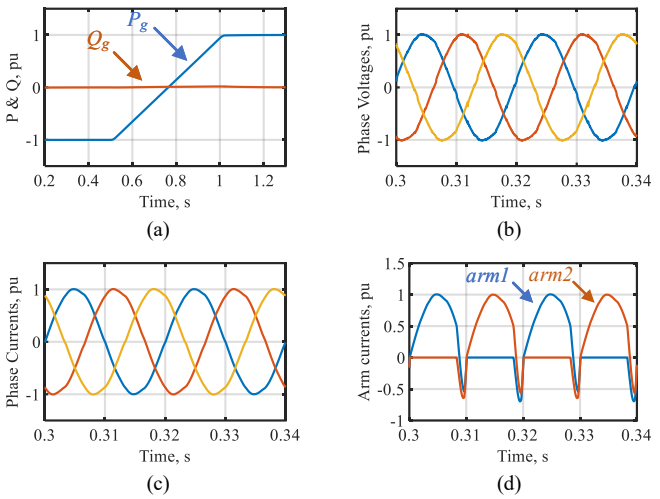


Fig. 8 Simulation - normal operation results: (a) The grid active and reactive power, (b) Phase voltages, (c) Phase currents, and (d) Arm currents in the grid absorption case.

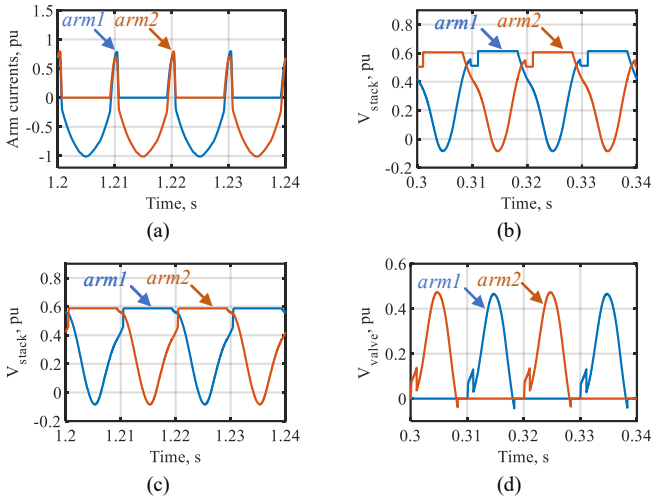


Fig. 9 Simulation - normal operation results: (a) Arm currents in the grid injection case, (b) MMC stack voltage in the grid absorption case, (c) MMC stack voltage in the grid injection case, and (d) Thyristor valve voltage in the grid absorption case.

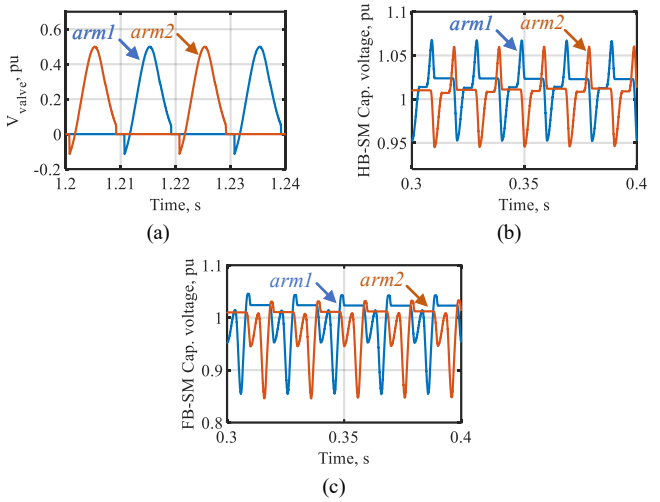


Fig. 10. Simulation - normal operation results: (a) Thyristor valve voltage in the grid injection case, (b) HB-SM capacitor voltages, and (c) FB-SM capacitor voltages.

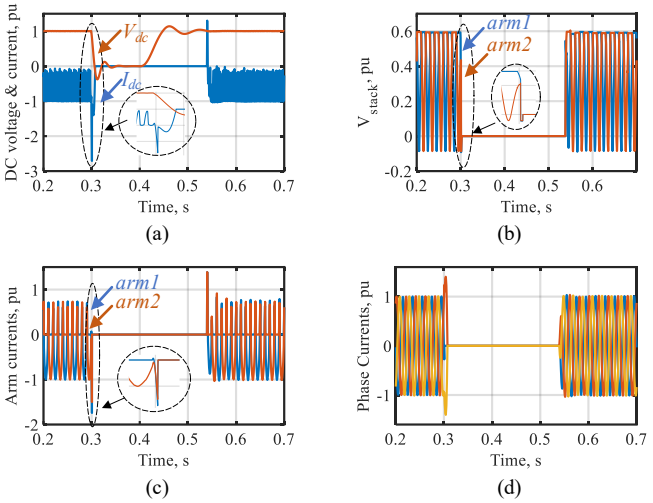


Fig. 11. Simulation - dc fault results: (a) DC link voltage and current, (b) MMC stack voltage, (c) Arm currents, and (d) Phase currents.

B. DC Fault

In this case, a dc fault is introduced at the DC link terminal at t=0.3s, where the fault persists for 100 ms. Fig. 11(a) shows the DC link voltage and current, where at the instant of DC fault occurrence, the fault current increases rapidly indicating the SMs capacitors discharge until the current is blocked by the action of the FB-SMs, as depicted in Fig. 11(b). Then, the AC component of the DC fault current starts to increase until it is blocked by the thyristor valve. Fig. 11(c) shows the arm currents of leg 1 indicating that it is in the overlap state at the instant of the fault. The phase currents depicted in Fig. 11(d) indicate successful isolation of the DC fault, thus validating the effectiveness of the proposed converter in blocking DC fault currents. Additionally, the post-fault restoration capability of the proposed converter is shown.

V. Experimental Setup

A scaled-down experimental test rig is used to assess the proposed converter, using 3-phase 5-levels as shown in Fig. 12, where each arm has 2 HB-SMs, 1 FB-SM, and 1 antiparallel thyristor. Parameters are calculated and listed in Table 2. Since the ratio between the FB-SMs and HB-SMs is 50%, k_3 can be increased to 0.5. Therefore, the overall commutation time T_c=1.6 ms is selected. Three cases are considered in the experimental study: normal operation, power reversal, and a dc fault.

A. Normal Operation

The proposed HTMC is connected to a 3-phase grid as shown in Fig. 13 (a), where the phase currents are depicted in Fig. 13 (b). The phase currents are not deformed by the third harmonic subtraction or by thyristor commutation action, which validates the proposed control. The arm currents of the proposed HTMC shown in Fig. 13 (c) indicate low currents stress on the semiconductors. The MMC stacks operate with balanced SM capacitor voltages as shown in Fig. 13 (d). The MMC stack voltages are depicted in Fig. 13 (e), where a negative voltage exists due to the third harmonic subtraction. The thyristor valve voltages are depicted in Fig. 13 (f), where a negative voltage occurs due to thyristor commutation action performed by the MMC stack.

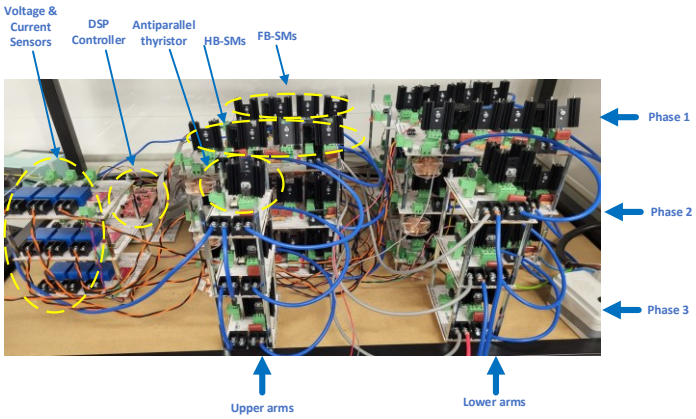


Fig. 12 The experimental test rig.

Table 2: Experimental Parameters

Parameter	Description	Value
P_r	Rated power	200 W
V_{dc}	DC link voltage	140 V
v_g	Grid voltage	52 V
f	Fundamental Frequency	50 Hz
L_{AC}	AC interfacing inductance	20 mH
T_c	Overall commutation time	1.6 ms
N_{HB}	Number of HB-SMs	2
N_{FB}	Number of FB-SMs	1
V_c	SM nominal voltage	35 V
C_{SM}	SM capacitance	8.2 mF
L_{arm}	Arm inductance	0.47 mH
R_{fault}	Fault resistance	8 Ω

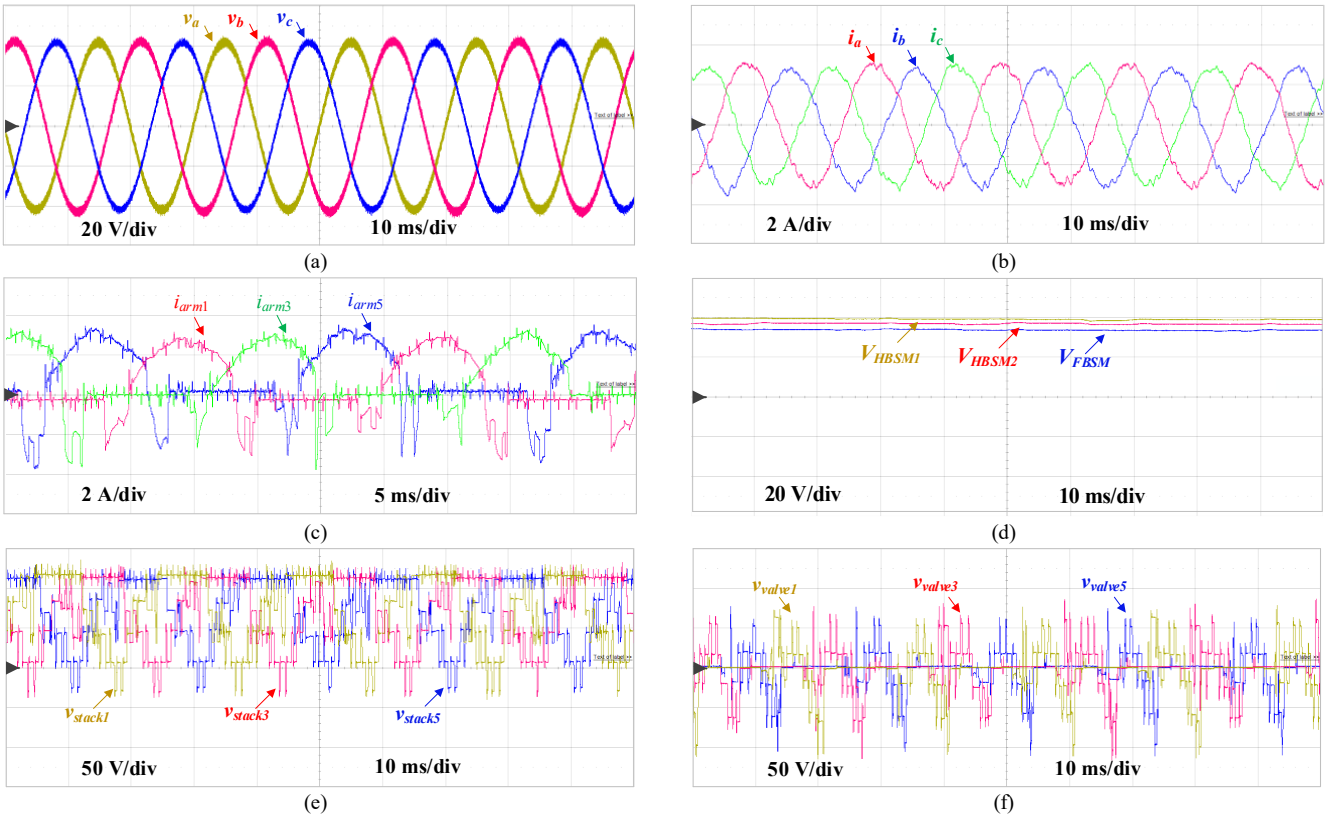


Fig. 13. Experimental - normal operation results: (a) The grid phase voltages, (b) Phase currents, (c) Arm Currents, (d) MMC stack 1 capacitor voltages, (e) MMC stack voltages, and (f) Thyristor valve voltages.

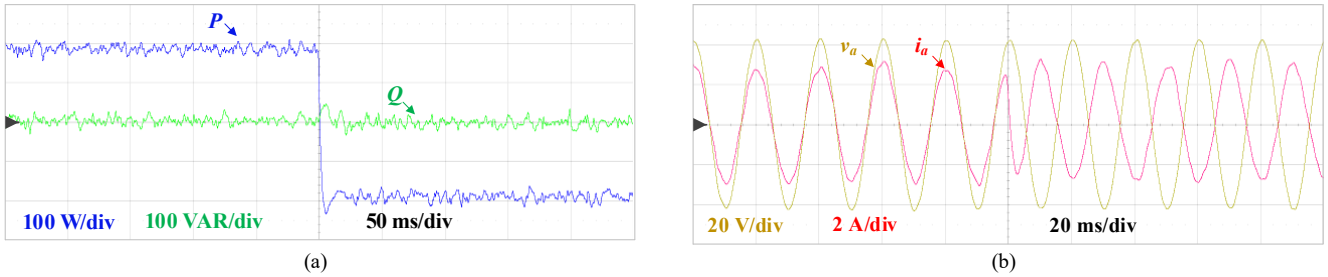
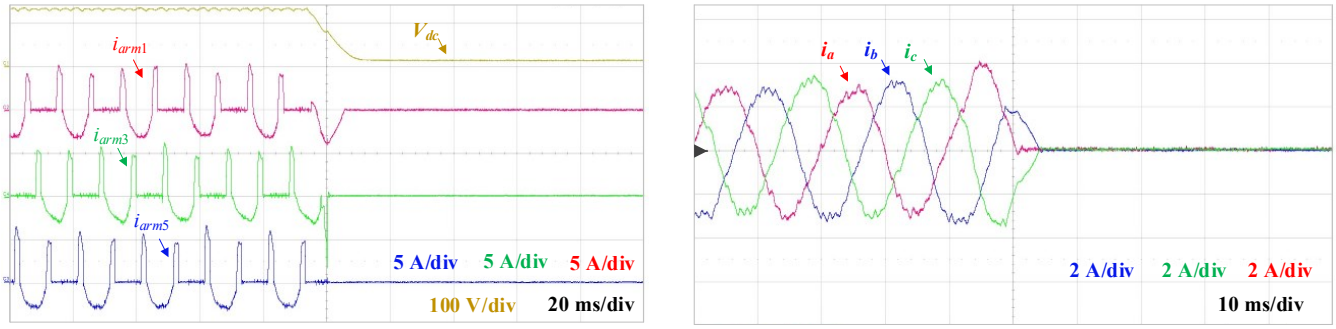


Fig. 14. Experimental - power reversal results: (a) Active power and reactive power and (b) Phase 'a' AC voltage, and phase 'a' AC current.



(a) (b)

Fig. 15. Experimental – dc fault results: (a) DC link voltage and arm currents and (b) Phase currents.

B. *Power Reversal*

To test the bidirectional capability of the proposed HTMC, the power flow is initially from the DC side to the grid at 200W then power reversal action occurs, -200W, while maintaining zero reactive power, as seen in Fig. 14(a). The phase 'a' voltage and current are shown in Fig. 14(b). where the voltage and current are in-phase at the instant of positive power and out-of-phase at the instant of negative power; indicating successful power reversal operation of the proposed HTMC.

C. *DC fault*

To further validate the DC fault blocking capability of the proposed converter, a DC fault is tested experimentally. Fig. 15(a) shows that the DC link voltage starts to collapse at the instant of fault occurrence. The upper arm current of the second leg (I_{arm_3}) clearly starts to increase rapidly indicating that this arm is in the overlap state at the fault instant. After fault detection, the arm current (I_{arm_3}) is decreased rapidly to zero by the action of the FB-SMs. On the other hand, the DC fault AC component seen in arm 1 current (I_{arm_1}) is inherently extinguished by thyristor valve action. The phase currents depicted in Fig. 15(b) indicate successful isolation of the DC fault, validating the effective blocking of DC fault currents within the proposed converter.

VI. Comparison

To highlight the features and advantages of the proposed HTMC converter and further validate the claims of the paper, an extensive comparison is performed in this section, with several converters reported in the literature, in terms of: semiconductor count and type, passive elements, current stresses, losses, cost, weight, size, and dc fault clearing time. Typical ABB switches and thyristors are used in the comparison in Table 3. Each capacitor is a combination of the capacitor labelled as C44UVGT7105M34K (1,050µF, 1,800V, 5.1kg, 5,311cm^3, $136.67) [32]. The switching and conduction losses are calculated based on [33], with an average switching frequency of 250 Hz. The arm inductor weight, size and losses are designed based on the practical approach given in [34]. All passive elements and semiconductors are considered in the size, weight, and cost calculations, where an extra 15% is assumed in the volume calculations.

The comparison is carried out between non-thyristor-based converters, such as the HB-MMC with a solid state DC CB [9, 35], FB-MMC [12], Hybrid MMC [13], and AAC [15], and thyristor-based converters such as the thyristor bypass-based MMC (TB-MMC) [11], crossing thyristor branches-based MMC (CTB-MMC) [29], power group (PG)-based FB-MMC [20, 22] and PG-based Hybrid MMC [20, 22]; as depicted in Table 4. The comparison is based on a typical 401-level MMC based HVDC system with 1 GW rated power and a ±320 kV DC link. The nominal voltage per SM is 1.6 kV while the nominal voltage per thyristor is 4 kV. The DC filter is considered in all (cost, weight, size, and losses) calculations for both the proposed and the AAC topologies. It is assumed that the DC-link filter capacitance is equivalent to a single leg as stated in [30].

From the comparison table, in terms of capacitor number, total converter weight, and size: the proposed HTMC is second after the AAC. However, considering the number of IGBTs, overall cost, and semiconductor losses: the proposed HTMC is first among all candidates, achieving the lowest number of IGBTs, cost and semiconductor losses. But, in terms of DC fault clearing time, the proposed converter achieves 15~18 ms, which is considered higher than other topologies, except the TB-MMC, due to thyristor commutation time.

Table 3: Typical ABB Semiconductors Parameters

Parameters	IGBT Module 5SNA 1800E330400		Thyristor 5STP 12K6500	SM Bypass thyristor 5STP 12F4200
	IGBT	Diode		
Max voltage	3300 V		6500 V	4200 V
RMS Current	1800 A		2250 A	1860 A
On-state voltage at 125°C	3.2 V	2.65 V	1.84 V	1.86 V
On-state resistance at 125°C	0.1 mΩ	0.1 mΩ	0.647 mΩ	0.545 mΩ
Turn on & off switching or reverse recovery energies at 125°C	4.3+4 J	2.3 J	0.3+4.2 J	0.3+0.8 J
Size	1010.8 cm^3		291.2 cm^3	117.25 cm^3
Weight	1.19 kg		1.15 kg	0.6 kg
Cost/unit	$2063		$904.96	$242.61

Table 4: Key Feature Comparison of Different Converters based on 401 level HVDC system parameters

Converter Type	HB-MMC with Solid-state DC CB [9, 10]	TB-MMC [11]	FB-MMC [12]	Hybrid MMC [13]	AAC [15]	PG-based Hybrid-MMC [20, 22]	CTB-based MMC [29]	Proposed converter (HTMC)
No. of SMs	400x6	400x6	400x6	400x6	255x6	400x6	400x6	240x6
Capacitance per SM	10.5 mF	10.5 mF	10.5 mF	10.5 mF	5.25 mF	10.5 mF	10.5 mF	12.5 mF
Total number of capacitors	10x400x6 =24000	10x400x6 =24000	10x400x6 =24000	10x400x6 =24000	5x255x8 =10200	10x400x6 =24000	10x400x6 =24000	12x240x8 =23040
No. of IGBTs	2x400x6+400 =5200	2x400x6 =4800	4x400x6 =9600	4x200x6 +2x200x6 =7200	4x255x6 +200x6 =7320	4x200x6 +2x200x6 =7200	2x344x6 +3x56x6 =5400	4x40x6 +2x200x6 =3360
No. of Thyristors	None	200x6 =1200	None	None	None	2x200x6 =2400	200x6 =1200	2x100x6 +40x6+200x6 =2640
Arm inductor	46 mH (0.1 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	5.5 mH (0.012 pu)	46 mH (0.1 pu)	46 mH (0.1 pu)	5.5 mH (0.012 pu)
RMS arm currents	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{\pi}{6}I_{dc}$	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{1}{\sqrt{3}}I_{dc}$	$\frac{2}{3}I_{dc}$
DC Fault clearing time	3~5 ms	19~24 ms	0.5~1 ms	1.5~3 ms	1~2 ms	1.5~3 ms	0~3 ms	15~18 ms
Total semiconductor losses	8.76 MW 0.876%	7.77 MW 0.777%	12.87 MW 1.287%	10.32 MW 1.032%	8.02 MW 0.802%	6.22 MW 0.622%	8.48 MW 0.848%	5.58 MW 0.558%
Overall Cost	$16.06 M	$14.26 M	$23.09 M	$18.13 M	$16.5 M	$20.31 M	$15.5 M	$11.59 M
Overall Weight	153.37 tons	155 tons	156.4 tons	153.5 tons	62.92 tons	162.2 tons	155.7 tons	134.9 tons
Overall Volume	160.82 m^3	160.89 m^3	165.33 m^3	162.54 m^3	74.83 m^3	164.8 m^3	161.58 m^3	149.97 m^3

VII. Conclusion

This paper introduced a novel Hybrid Thyristor-based Multilevel Converter (HTMC) with DC fault-blocking capability. The proposed HTMC's analysis has been illustrated in both normal operation and under DC fault scenarios. In the analysis, a third harmonic waveform has been subtracted from the fundamental waveform to take advantage of the FB-SMs negative voltage capability in normal operation. This enhances the overlapping period between the upper and lower arms and allows longer periods for thyristor commutation. Hence, at k=0.2, sufficient overlap and commutation times are achieved. The proposed converter capabilities have been validated via a 401-level MATLAB-SIMULINK model and experimentation on a scaled-down 3-phase 5-level system.

A detailed comparison with alternative converters has been provided in terms of: semiconductor count, passive elements, cost, current stresses, losses, DC fault clearing speed, size, and weight. The proposed HTMC has relatively slow fault clearing speed since it mainly depends on the thyristor valve action. However, the proposed HTMC is first in terms of a lower IGBT count (30% lower than the next best topology), lower losses due to the usage of thyristor valves (10% lower than the nearest converter), and lower cost (19% lower than the nearest). It is second in terms of the overall weight, volume, and capacitors count. Hence, the results indicate that the proposed HTMC is a worthy candidate for HVDC applications.

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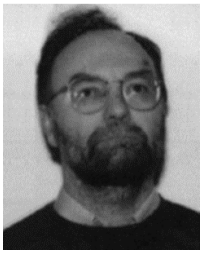

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