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The Effect of Grid-Connected Converter Control Topology on the Diagonal Dominance of Converter Output Impedance

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ABSTRACT This work investigates the effect of grid-connected converter topology on equivalent converter output impedance with a specific focus on the diagonal dominance of the impedance matrix across a frequency range. When considering multiple-input multiple-output systems most traditional stability techniques are reliant on the diagonal dominance of the studied system. Therefore, a rating of diagonal dominance is proposed based upon the correlation coefficient between row and column in the impedance matrix. This provides a scale that ranges from off-diagonally dominant (−1) through uniformly distributed (0) and up to diagonally dominant (1) across a range of frequencies. The scale is used to specify which control structures can be considered as diagonally dominant at certain frequencies and which control components have the greatest effect on the rating. A direct relation is found between system exhibiting a diagonal dominance rating of 0.7 and above and the efficacy of traditional stability margins. Traditionally strong systems with low network impedance where controllers can be tuned conservatively exhibit high degrees of diagonal dominance and can be analysed quickly with traditional margins with minimal error. For systems exhibiting a lower rating, disk margins are explored as an alternative which offer greater accuracy. Additionally, more realistic perturbations of gain and phase occurring simultaneously in multiple channels can be considered which is more applicable for the modern electricity network with a high penetration of grid-connected converters.

INDEX TERMS MIMO impedance, diagonal dominance, stability margins, impedance based stability analysis, disk margins.

I. INTRODUCTION

POWER converter interfaced generation is becoming the new norm as the network transitions from traditional fossil fuel generators to cleaner renewable energy sources [1]. This has been largely driven by worldwide policies to combat climate change [2]. While the move to renewable energy is crucial, the introduction of more power converters to the electricity network leads to new network-wide challenges on operation, control and protection [3], [4], [5]. In particular, the stability of converter dominated networks has been identified as critical [6]. Several network events that led to partial outages have been described in Britain, Texas and China [7], [8].

While some prior work has been completed investigating the stability challenges of these types of systems, see e.g. [9], model complexity is often lacking, utilising only standard grid following (GFL) current controllers with complex functions disabled to facilitate easier analysis [10], [11], [12]. With more large power sources and loads becoming converter interfaced, grid conditions can vary rapidly and it is important that the remaining converters have the robustness to stay connected. The most recent work involves the inclusion of

more complex control systems such as power and voltage control [13], [14], power synchronising control [15] and synchronous machine emulation [16]. Proper investigation of these system involves the incorporation of a frequency dependent component to the network [17]. Moreover, negative sequence control (NSC) is a component that is often overlooked but ever present in real world controllers. These systems present unique challenges in terms of analysis by reducing the symmetry of frequency responses in different reference frames and hence, require more complex analysis.

Simplified power converter models may lead to inaccurate small-signal stability assessments. In some cases, networks are modelled using SISO impedances or utilise transformations to ensure systems become diagonally dominant and can be analysed in a loop-at-a-time method [18], [19], [20], [21], [22]. In these cases, traditional stability techniques and margins can be applied with confidence. However, a proper system description requires MIMO impedances to account for channel interactions, which is a topic of current research [15], [17], [23], [24]. In some cases, these impedances can be diagonally dominant which simplifies analysis. Additionally, work has been completed in [9] to transform a system that exhibits channel interactions in the dq-frame to a diagonally dominant system in the sequence frame. Stability of these system can often produce misleading results. For example, the system may be correctly labelled as stable but at the wrong point e.g., a pole is closer to the unstable region than originally thought. The stability definition is correct but the stability margins will be significantly different which could cause issue for further analysis with more components. If a diagonally dominant system is not possible gain and phase margins can be misleading as simultaneous variations can occur, significantly reducing the safety net [25]. However, in some cases specific tunings produce a diagonally dominant (DD) system allowing the MIMO system to be accurately analysed via SISO techniques without disabling key components. This could result in significant time saving during analysis with less expertise in complex stability analysis.

This paper will demonstrate the effect of differing controller topology and tuning on the DD of the obtained equivalent converter output admittance. A novel method of rating DD based on the sample correlation coefficient between the rows and columns of the admittance matrix is proposed. Furthermore, recommendations on suitable situations where traditional stability analysis techniques are valid are provided based on the proposed method of DD rating. Modern admittance-based analysis techniques are becoming increasingly complex, time consuming and require significant experience to apply with confidence. Therefore, finding situations where this can be avoided will be beneficial.

The analysis finds that traditionally strong systems can operate under controller tunings that produce DD systems which removes the need for complex MIMO analysis techniques. The novel contribution of this work lies in the determination of where the limit of DD is for applying traditional SISO stability methods and which control components have the greatest effect on the rating. The paper extends the understanding of why conventional SISO stability margins are not applicable for advanced grid-connected converters in situations such as weak grids where more complex tunings are required to operate the system safely. Using differing controller complexity and tuning, the failures of traditional margins are illustrated. The paper observes that reduction of the DD of the admittance matrix causes SISO analysis techniques to fail with the error becoming exponentially worse when the DD rating falls below 0.7. Stability analysis based on disk margins are suggested and implemented as an alternative in this work when the D rating falls below this value and offer a more realistic approach to considering robustness in the modern network [25] despite being more complex.

II. MODELLING

The following section describes the modelling process for a GFL controller. A standard dq-frame current loop is augmented with outer-loop power and voltage control alongside negative sequence current regulation with PWM and discretisation delays. A full description of the system can be found in [26]. A diagram is provided in Fig. 1.

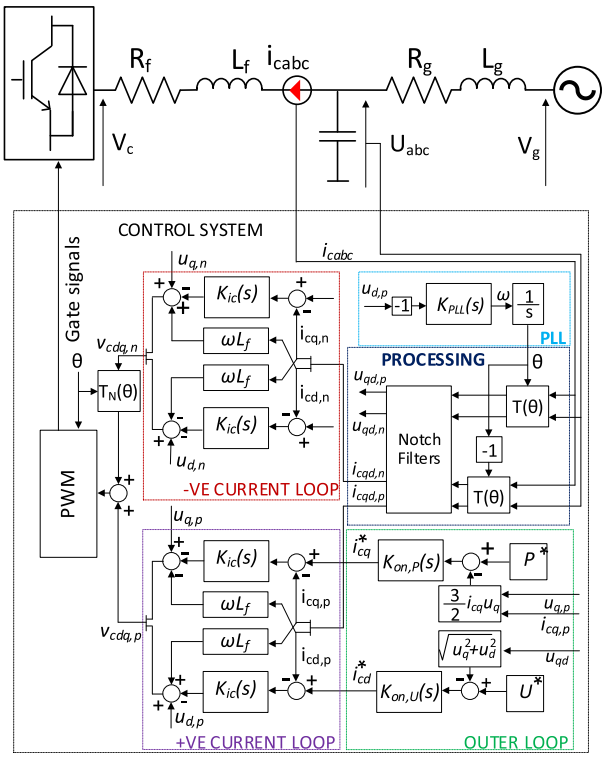

FIGURE 1. **Converter control block diagram.**

A. CONTROLLERS

The inner-loop current controllers regulate the positive and negative sequence current via PIs tuned using the internal

model control technique [27]. The positive sequence control is denoted CC with the negative sequence NSC throughout this work. The voltage command for PWM synthesis is a combination of PI output, cross coupling term ωL_f and a filtered voltage feedforward. Controller gains and time constants are the same within the same sequence but the positive and negative sequence values can vary. Outer-loop control regulates the active power (PC) and voltage (VC) in the positive sequence via two PIs while no outer-loop control is present in the negative sequence. A PLL is utilised for grid-synchronisation. The delays introduced by converter switching and discretisation are modelled using a first order Padé approximation. Notch filters tuned at 100 Hz are used to remove unwanted components in the positive and negative sequences.

B. SEQUENCE TRANSLATION

The modelling process is described in the positive-sequence dq-frame. Control components form the same transfer functions in their respective positive and negative sequences. Any negative sequence components must be transformed into the correct frame. Any components expressed in the negative sequence ($G^-_{c,qd}$) are transformed to the positive sequence via [28]:

$$G^+_{c,qd} = \begin{bmatrix} G_{qq} & G_{qd} \\ \mathrm{G_{dq}} & G_{dd} \end{bmatrix} \tag{1}$$

$$G_{qq} = \frac{1}{2}[G^-_{c,qq}\left(s - j2\omega_g\right) + G^-_{c,qq}\left(s + j2\omega_g\right)] \tag{2}$$

$$G_{qd} = \frac{1}{2}j[G^-_{c,qd}\left(s - j2\omega_g\right) - G^-_{c,qd}\left(s + j2\omega_g\right)] \tag{3}$$

$$G_{dq} = \frac{1}{2}j[G^-_{c,dq}\left(s - j2\omega_g\right) - G^-_{c,dq}\left(s + j2\omega_g\right)] \tag{4}$$

$$G_{dd} = \frac{1}{2}[G^-_{c,dd}\left(s - j2\omega_g\right) + G^-_{c,dd}\left(s + j2\omega_g\right)] \tag{5}$$

III. SMALL SIGNAL AND IMPEDANCE ANALYSIS

Considerable work exists utilising converter admittance and impedance for stability analysis [10], [11], [15], [17], [18], [19], [20], [23], [29]. The majority of work employs simplifications or approximations when representing converter components [10], [18]. The complex nature of rotations between reference frames, notch filters and delay components result in vastly different system characteristics. The combination of these aspects introduces several new poles and zeros to the system transfer functions. The new dynamics may be crucial at certain system operating points for determining stability and robustness.

A. ADMITTANCE AND IMPEDANCE GENERATION

To achieve this, the converter admittance is generated via a state-space model of the form:

$$\Delta\dot{\boldsymbol{x}} = \boldsymbol{A}\Delta\boldsymbol{x} + \boldsymbol{B}\Delta\boldsymbol{u} \tag{6}$$

$$\Delta\boldsymbol{y} = \boldsymbol{C}\Delta\boldsymbol{x} + \boldsymbol{D}\Delta\boldsymbol{u} \tag{7}$$

where $\boldsymbol{x}$, $\boldsymbol{u}$ and $\boldsymbol{y}$ are the model state, input and output vectors respectively, and $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}$ and $\boldsymbol{D}$ are the state, input, output and feedthrough matrices respectively. The system in Fig. 1, excluding the network and capacitor is linearised and modelled in synchronous reference frame to create the state-space model shown in Fig. 2.

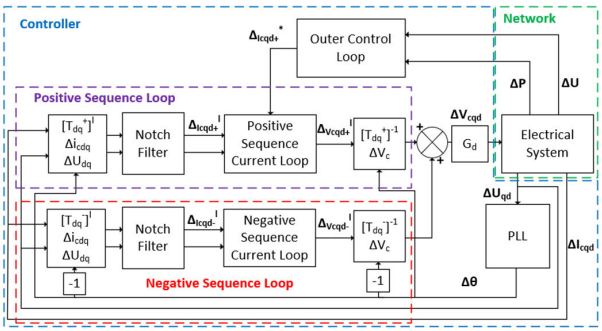

FIGURE 2. State-space model.

Once the model is linearised, the converter admittance is classified as the ratio of the response current from the converter to the voltage disturbance at the PCC:

$$Y_c = \frac{\Delta I_c}{\Delta V_{PCC}} \tag{8}$$

The converter admittance is determined by the physical filter components and the control architecture shown in Fig. 1. The capacitor is not included but can be modelled as a load effect. To generate the admittance from the state-space matrix the model inputs and outputs are selected to be:

$$\boldsymbol{u} = \begin{bmatrix} \Delta v_{q,PCC} \\ \Delta v_{d,PCC} \end{bmatrix} \tag{9}$$

$$\boldsymbol{y} = \begin{bmatrix} \Delta i_{q,c} \\ \Delta i_{dc,} \end{bmatrix} \tag{10}$$

The state-space then represents the converter admittance:

$$\begin{bmatrix} Y_{qq,c} & Y_{qd,c} \\ Y_{dq,c} & Y_{dd,c} \end{bmatrix} = \frac{\boldsymbol{y}}{\boldsymbol{u}} = \frac{\Delta \boldsymbol{i}}{\Delta \boldsymbol{v}} \tag{11}$$

The grid impedance is modelled as a Thevenin Equivalent utilising different impedances to represent various network short-circuit ratios.

B. IMPEDANCE RATIO FORMULATION

To analyse the interaction between the converter and the grid a simplified network diagram is required. The circuit in Fig. 2. is altered by considering the converter including the filter and controller as a current source with parallel admittance as described in subsection III-A. A diagram is provided in Fig. 3.

The contribution from each source to the current at the PCC can be considered via the following equation (the s-terms are omitted for clarity):

$$\boldsymbol{I}_{pcc} = \left(\boldsymbol{i}_c - \boldsymbol{v}_g\boldsymbol{Y}_c\right) \cdot \left(\frac{\boldsymbol{I}_2}{\boldsymbol{I}_2 + \boldsymbol{Z}_g\boldsymbol{Y}_c}\right) \tag{12}$$

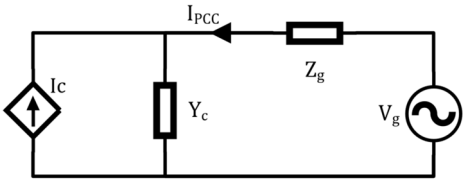

FIGURE 3. Simplified diagram of converter connected to grid.

Making the likely assumption that both the converter and grid are stable independently, the stability of the system is dependent on the minor loop gain - $Z_g Y_c$. Any properly designed converter should be stable when disconnected. Once the ratio is obtained the system can be analysed using any stability technique applicable for MIMO systems.

IV. COMPARING MODEL COMPLEXITY

This section provides an initial illustration of how different control components can affect stability definitions via Nyquist plots. The parameters applied to the system shown in Fig. 1 are provided in Table 1.

TABLE 1. Parameter table.

Parameter	Symbol	Value
Grid Voltage ($V_{L-L,RMS}$)	V_G	690 V
Converter Power	P_C	3 MW
Grid Frequency	ω_G	50 Hz
Grid Impedance	$R_g + jX_g$	0.16+j15.9 $m\Omega$
Filter Impedance	$R_f + jX_f$	1.6+j23.8 $m\Omega$
Grid Side Controller		
Current Cont. PI Gains	$\mathrm{Kp_{ig}}$, $\mathrm{Ki_{ig}}$	0.025, 0.53
PLL PI Gains	$\mathrm{Kp_{PLL}}$, $\mathrm{Ki_{PLL}}$	0.789, 175.8
Voltage Cont. PI Gains	$\mathrm{Kp_{VC}}$, $\mathrm{Ki_{VC}}$	0.5, 100
Power Cont. PI Gains	$\mathrm{Kp_{PC}}$, $\mathrm{Ki_{PC}}$	0.0029, 1

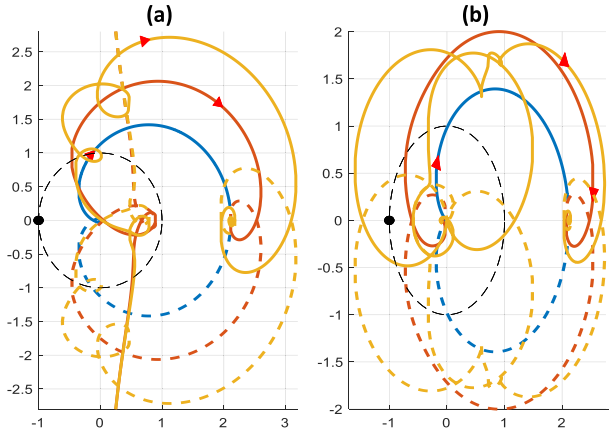

FIGURE 4. Comparison of varied control complexity – CC (blue), Full$^+$ (red), Full$^-$ (yellow) (a) 1st Eigenloci (b) 2nd Eigenloci.

The simplest topology includes only a current controller (CC), giving a simple impedance characteristic where the off-diagonal terms can be ignored and SISO methods can be applied as there is no channel interaction. The second controller enables the PLL, wraps the outer loop power and voltage controller and includes measurement filters and PWM delays (Full Control$^+$). The final controller enables the negative sequence current control (Full Control$^-$). The complete control structure for a single converter connected to the network is shown in Fig. 1. The control gains remain constant for all controller types in this case. Fig. 4 shows the first and second eigenloci in subplots (a) and (b), respectively for the three control types. When comparing the Nyquist plots in Fig. 4 (a), a large difference can be observed in the traces. Current control shows the tightest circle with the simplest trajectory which is expected. As the outer-loop control is introduced the trace becomes larger but does not encircle the critical point. However, the trace has a closer proximity to the critical point $(-1,0)$ suggesting a smaller stability margin. The yellow trace becomes more complex with multiple loops caused by the notch filters in the negative sequence control. However, when analysing Fig. 4 (b), the addition of the negative sequence control actually causes the system to become unstable, due to the encirclement of the critical point. Interestingly, this makes the system more sensitive to phase variations when NSC is included. Instabilities can occur for small regions of phase disturbances where these loops encircle the critical point. Conversely, these loops do not make the system more sensitive to gain variations as the orientation of the loops without a rotation from a phase disturbance are unlikely to pass close to the critical point. These results can be confirmed by eigenvalue analysis of the characteristic equation formed using state-space matrices. Similar to the Nyquist plots, the CC and Full$^+$ controllers are both stable due to no zeros being present in the RHP. However, when the negative sequence is added a pair of complex conjugate zeros with a positive real part appear indicating instability. These zeros represent unstable poles in the closed loop transfer function. Additionally, the extra complexity of the full controller introduces further poles and zeros closer to the imaginary axis. Only one zero is present for CC with all others much further in the LHP. This further suggests more stability and performance concerns as control complexity increases.

V. STABILITY MARGINS

As converter control becomes more complex, methods of determining robustness become increasingly vital to ensure converters remain connected. For SISO systems, this is usually achieved via gain and phase margins. Three issues arise in the case of grid-connected converters. Firstly, since the model usually forms a non-minimum phase (NMP) system the phase margin and associated design rules may not be valid as multiple crossings of 0 dB may be present throughout the frequency range. Secondly for MIMO systems, gain and phase margins can only be employed in a loop-at-a-time method. Therefore, interloop interactions are not considered. These interactions become especially important as the matrix

off-diagonal terms increase in magnitude. Therefore, traditional phase and gain margins may be applicable for simple current control that is diagonally dominant but not for a fully-functional grid-connected converter. Thirdly, phase and gain margins do not account for simultaneous changes in phase and gain which occur readily in real systems and can cause instability even if the phase and gain margins are large. This section explores how different control components effect the DD of the impedance ratio formed and the subsequent influence on stability margins.

A. ANALYSING DIAGONAL DOMINANCE

Work has been completed on applying stability analyses that are dependent on the DD of the analysed system [9]. Moreover, studies have shown that systems that are mirror frequency decoupled in the synchronous reference frame are diagonally dominant in the modified sequence domain [28]. This is the case for simple current controllers and this effect is illustrated with the mirror-frequency decoupled (MFD) system in the synchronous reference frame shown in Fig. 5 and the DD system in the sequence-frame in Fig. 5 (b). The process for transforming between reference frames is detailed in [28].

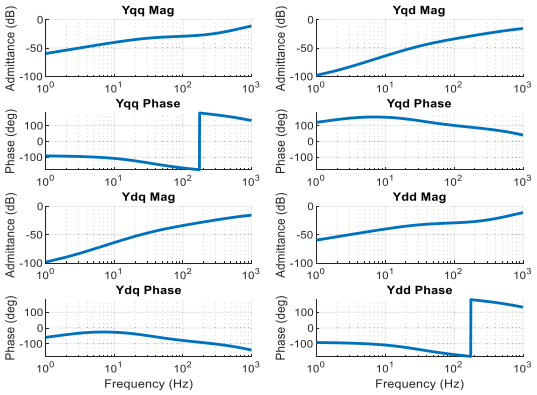

FIGURE 5. CC converter admittance ratio in the dq-frame.

From Fig. 5, the off-diagonal terms are of similar magnitude and no DD is observed. When transformed to the sequence-frame, Fig. 6 shows that the off-diagonal terms become almost zero and the system is diagonally dominant. However, as control complexity increases to include all components the sequence-frame can also become coupled. The sequence-frame admittance for the full controller without NSC and with NSC is shown in Fig. 7.

From Fig. 7, neither system retains the DD of CC when transformed to the sequence frame. Therefore, traditional margins are meaningless for both systems. The DD of the system shown in Fig. 5 (b) is apparent. However, precisely determining the DD of a system can be challenging when the off-diagonal term grows. Moreover, the DD varies with frequency. If the traditional margins are found to be at a frequency where the DD is high, then the margins are likely applicable.

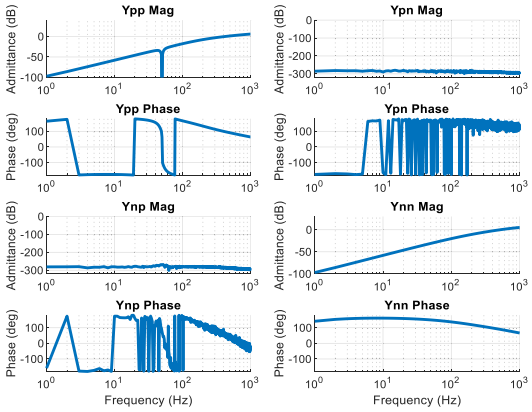

FIGURE 6. CC converter admittance ratio in the pn-frame.

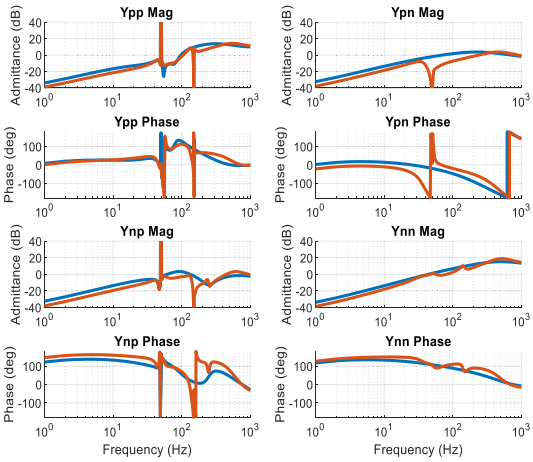

FIGURE 7. Sequence frame admittance of advanced controllers – Full^{+}(blue), Full^{-}(orange).

The converse is also true. An easily scalable rating of DD can be obtained by calculating the sample correlation coefficient between rows and columns in the same matrix to obtain an r value [30]. This process is achieved by considering a square matrix A of size t *by* t, in this study the square matrix is the impedance ratio $\boldsymbol{Z}_g\boldsymbol{Y}_c(\mathrm{s})$. The sample correlation coefficient requires paired data and the impedance ratio offers only one data set. This is where the approach differs from the traditional method, two data sets are obtained from one matrix, one based on rows and the other on columns achieved using (15) and (16). Since the coefficient requires standard deviations the squared versions of these are also required and are obtained using (17) and (18). Three vectors require specification to achieve this: $\boldsymbol{j}$, a k-long vector of ones, $\boldsymbol{r} = (\mathbf{1}, \mathbf{2}, \ldots, \boldsymbol{k})$ and $\boldsymbol{r_2} = (\mathbf{1^2}, \mathbf{2^2}, \ldots, \boldsymbol{k^2})$. The rating of diagonal dominance D can then be found via:

$$D = \left| \frac{n\Sigma xy - \Sigma x \Sigma y}{\sqrt{\left(n\Sigma x^2 - (\Sigma x)^2\right)\sqrt{n\Sigma y^2 - (\Sigma y)^2}}} \right| \tag{13}$$

$$n = \boldsymbol{jAj}^T \tag{14}$$

$$\Sigma x = \boldsymbol{rAj}^T \tag{15}$$
$$\Sigma y = \boldsymbol{jAr}^T \tag{16}$$
$$\Sigma x^2 = \boldsymbol{r_2 A j}^T \tag{17}$$
$$\Sigma y^2 = \boldsymbol{jAr}_2^T \tag{18}$$
$$\Sigma xy = \boldsymbol{rAr}^T \tag{19}$$

When the two matrices are constructed in this form, values can only be perfectly correlated on the diagonal where the value, D, would be equal to one indicated a perfectly diagonally dominant matrix. If off-diagonal terms are introduced a perfect correlation is no longer possible and D begins to decrease to around zero when the matrix is uniformly distributed and -1 when the off-diagonal terms are dominant. This can be applied to the 2×2 MIMO impedance ratio at each frequency to find a frequency dependent rating of DD. This approach is used to analyse the individual effect of each control component on the DD of the impedance ratio in both the dq and pn-frames. Literature suggests that when Pearson's correlation coefficient is greater than 0.7 the data exhibits a strong correlation [31]. For this reason, a D rating of 0.7 or higher is proposed to provide an initial indication of a diagonally dominant system. The base case is a positive sequence current controller with all other components including the PLL disabled. Each additional control component is then enabled individually alongside the positive sequence current control and the results are provided in Fig. 8.

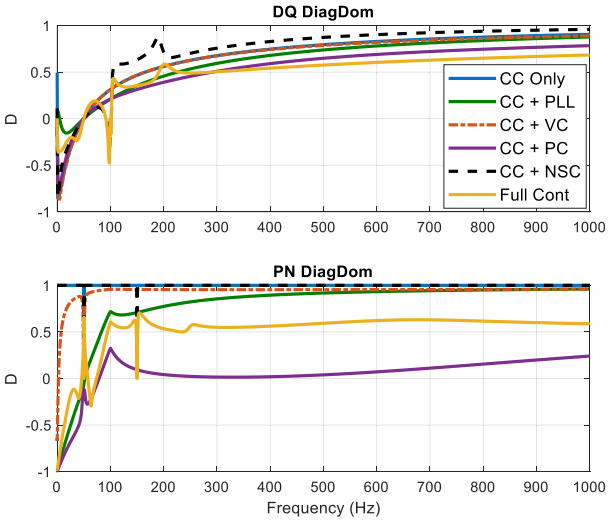

FIGURE 8. Comparison of Diagonal Dominance in dq and pn frames for differing control complexity.

From Fig. 8, no system is DD in the DQ domain below 500 Hz. Beyond this point the rating of CC, CC + VC and CC + NSC are above 0.7 and can be considered diagonally dominant. When transformed into the PN frame both the positive and negative sequence current controllers retain DD despite the increased complexity introduced from NSC. The PLL provides a significant reduction in DD in both frames and is a crucial component for inclusion in stability studies. The VC reduces the DD at low frequencies but this effect is reduced at higher frequencies. The PC individually represents the worst rating of DD in both frames across a range of frequencies. However, it is the one control configuration that provides a greater D rating in the dq-frame compared to the pn. The DD in the pn-frame for VC and PC are directly related to the bandwidths of the outer-loop control. Traditional tuning rules would suggest that the outer-loop should be around (5-10) times slower than the inner-loop to avoid interactions [32]. When this occurs the shape of the impedance ratio trace is dominated by the faster current loop and DD is maintained when the outer-loop control is enabled. However, this traditional tuning recommendation may not be sufficient for the more antagonistic grid conditions observed in the modern network. When the outer-loop control is faster the system is no longer DD.

VI. STABILITY MARGINS

This section explores how the rating of DD effects the efficacy of traditional stability margin techniques and determines an appropriate limit for their application. Beyond this disk margins are utilised for systems that do no meet the threshold specified.

A. TRADITIONAL SISO GAIN MARGIN

An acceptable rating of DD can be obtained by analysing the traditional gain and phase margins for the systems considered. The traditional SISO gain margins (GM) for each controller are provided in Table 2 alongside the GM frequency and the DD of the matrix at the GM frequency. This is due to the efficacy of the margins being dependent on the DD of the matrix at the specific frequency where the margin is obtained.

TABLE 2. Comparison of SISO gain margins for controllers.

Cont	Gain Margin (GM)		GM Freq. (Hz)		D at GM Freq.	
	dq	pn	dq	pn	dq	pn
CC	12.2	3.85	3.18	53.2	-0.844	1
CC+ PLL	3.47	3.10	57	102	0.035	0.712
CC+ VC	12.4	3.95	3.26	53.3	-0.835	0.868
CC+ PC	25.1	∞	13.1	n/a	-0.176	n/a
CC + NSC	10.0	2.07	3.17	151.7	-0.787	1
Full-	10.2	2.1	45.3	151.7	-0.116	0.638

From Table 2, the rating of DD for the DQ-frame margins is always approximately zero or lower and the gain margins are significantly larger in most cases compared to the pn-frame where the DD is larger. The margins are frame independent meaning the pn-frame margins can be applied to the dq-frame system and vice versa. This is proven in

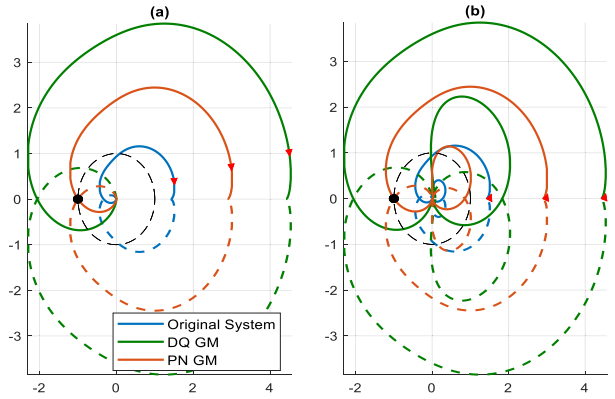

FIGURE 9. Application of SISO gain margins to CC in (a) dq-frame (b) pn-frame.

Fig. 9 which compares the application of the SISO gain margins determined in each frame via Nyquist plots of the most sensitive eigenloci. The gain margins are applied in both channels at once via:

$$\boldsymbol{M}(s)=k_{GM}\boldsymbol{I_2}\boldsymbol{Y}(s) \tag{20}$$

where k_{GM} is the gain margin determined for the original system, $\boldsymbol{Y}(s)$ and $\boldsymbol{M}(s)$ is the perturbed system assumed to be on the stabiltiy limit. From Fig. 9 (a), the dq-frame GM significantly overshoots the critical point while the pn-frame GM estimates the limits of stability correctly. This is expected from the DD ratings obtained in Table 2. Similarly, the same result is obtained when the GM is applied to the pn-frame system in Fig. 9 (b). The GMs obtained for the remaining systems have been applied to the dq-frame system and the resultant Nyquist plots of the most sensitive eigenloci are provided in Fig. 10. The percentage error measuring the minimum distance between the Nyquist plot and the critical point is shown in Table 3.

From Fig. 10 (a), the GM obtained when the PLL is included is similar in both frames with the dq-frame providing a slightly higher GM. This results in the Nyquist plot passing through the critical point when the pn-frame GM is used. The percentage error is still small for the pn-frame margin but significantly larger than the error obtained for CC when the system was completely DD. Similar results are obtained with the plots shown in Fig. 10 (b)(d)(e) with the pn-frame margin always obtaining a better rating of stability margins due to the higher DD rating. From the obtained results, a D rating of 0.7 or higher appears sufficient for the system to be considered diagonally dominant and the for the application of traditional SISO gain margins to be valid. The addition of the PC shown in Fig. 10 (c) offers some concern as a GM could not be obtained in pn-frame, likely due to reduced DD throughout the entire frequency range. While the dq-frame GM appears to provide a correct measure, the trace significantly undershoots the critical point very close to the real axis. The pn-frame margin is assumed a very large number of 100 as infinite is not possible. This overshoots the critical

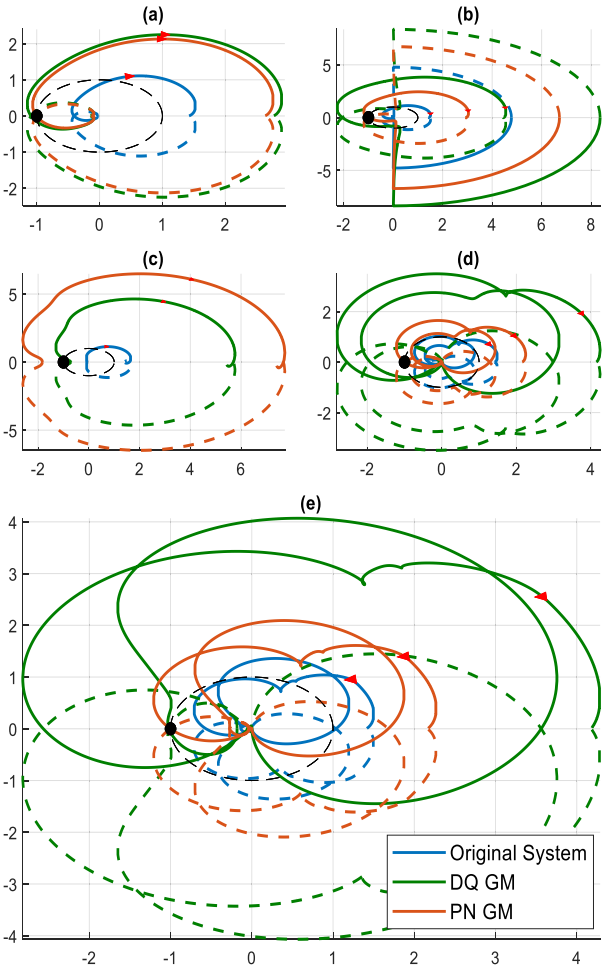

FIGURE 10. Application of SISO dq and pn gain margins to (a) CC + PLL (b) CC +VC (c) CC + PC (d) CC + NSC (e) Full$^-$ Control.

point and indicates that the original margin of infinity is clearly incorrect. The DD for the PC in pn-frame only reaches above 0.6 when singularities occur in the impedance ratio and are likely not representative of the real system at that frequency.

B. TRADITIONAL SISO PHASE MARGIN

The rating of DD can further be validated by analysing the effect of traditional SISO phase margins (PM) on the considered systems which are provided in Table 4.

TABLE 3. Percentage error for SISO gain margin.

Cont	Percentage Error (%)		D	
	dq	pn	dq	pn
CC	106	0.05	-0.844	1
CC + PLL	9	0.6	0.035	0.712
CC + VC	104	-0.03	-0.835	0.868
CC + PC	-28.65	82.7	-0.176	n/a
CC + NSC	154	0.06	-0.787	1
Full$^-$	157	0.23	-0.116	0.638

TABLE 4. Comparison of SISO phase margins for controllers.

Cont	Phase Margin (PM)		PM Freq. (Hz)		D at PM Freq.	
	dq	pn	dq	pn	dq	pn
CC	-126°	-95.0°	126	96.3	0.403	1
CC+ PLL	-108°	-100°	509	448	0.761	0.907
CC+ VC	-126°	-96.8°	127	96.8	0.408	0.956
CC+ PC	-108°	-101°	511	391	0.692	0.709
CC+ NSC	-119°	-59.5°	183	153	0.817	1
Full$^-$	-61.1°	-60.5°	254	258	0.491	0.578

From Table 4, the phase margins are generally obtained at higher frequencies where the impedance ratio is naturally more diagonally dominant as the physical inductance becomes more prevalent with increasing frequency. The DD rating in the pn-frame is large enough to be considered almost perfectly DD in most cases excluding the Full$^-$ controller. The dq-frame phase margins should be more applicable than the GM due to the increased value of D at higher frequencies. The application of the PMs is provided in Fig. 11 by rotating the Nyquist plots of the original system. Note that both eigenloci are provided for CC + PC in Fig. 11 (d)(e) and CC + NSC in Fig. 11 (f)(g) as both eigenloci were sensitive to phase variations unlike the previous applied gain variations. The percentage error indicating the maximum error in the direction of the imaginary axis is shown in Table 5.

TABLE 5. Percentage error for SISO phase margins.

Cont	Percentage Error (%)		D	
	dq	pn	dq	pn
CC	45	0.11	0.403	1
CC + PLL	14	0.3	0.761	0.907
CC + VC	43	0.3	0.408	0.956
CC + PC	-4.9	-5.9	0.692	0.709
CC + NS	9.8	0.05	0.817	1
Full$^-$	-13.1	-11.8	0.491	0.578

From Fig. 11 (a)(b)(c), similar results are obtained for PM application as for GM. The pn-frame PM provide the most accurate stability margins due to the significantly higher D rating. The percentage error for the dq-frame margins are also lower which is in agreement with the D rating obtained compared to the GM errors shown in Table 3. The only exception is when the PLL is added. For the PM, the D rating it 0.761 and an error of 14 % is obtained, which is acceptable but slightly higher than expected. The rating of DD does not have a linear relationship with the error obtained due to the complex nature of analysing the MIMO eigenloci. This is most obvious around for margins obtained around 50 Hz in the dq-frame, likely due to harmonics and control components providing singularities around these frequencies.

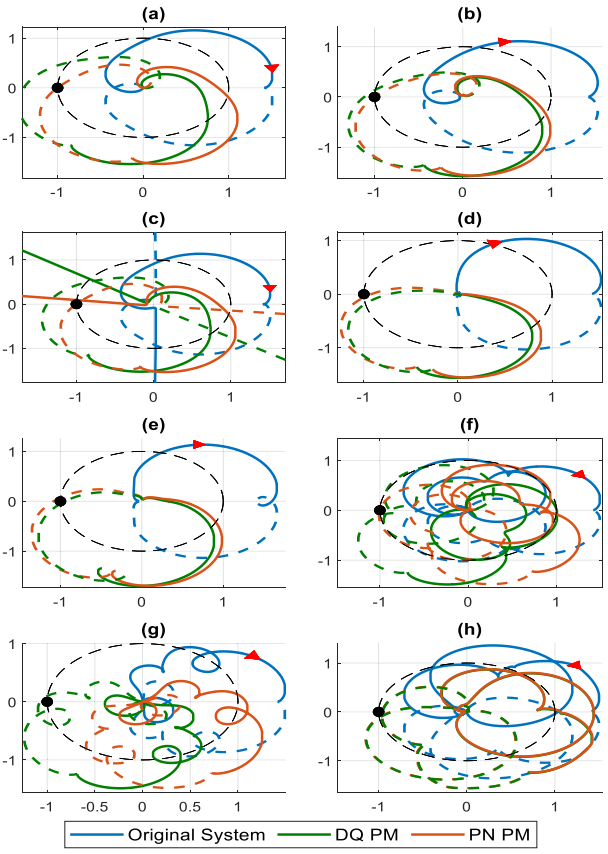

FIGURE 11. Application of dq and pn SISO phase margins to (a) CC (b) CC +PLL (c) CC + VC (d) CC + PC 1st Loci (e) CC + PC 2nd Loci (f) CC + NSC 1st Loci (g) CC + NSC 2nd Loci (h) Full$^-$.

TABLE 6. Comparison of loop at a time disk margins.

Cont.	Disk GM	Disk PM	Frequency (Hz)	D
CC	$\begin{Bmatrix}8.37\\8.37\end{Bmatrix}$	$\begin{Bmatrix}\pm76°\\\pm76°\end{Bmatrix}$	$\begin{Bmatrix}4.8\\4.8\end{Bmatrix}$	-0.792
CC + PLL	$\begin{Bmatrix}8.48\\3.29\end{Bmatrix}$	$\begin{Bmatrix}\pm76°\\\pm56°\end{Bmatrix}$	$\begin{Bmatrix}10.7\\11\end{Bmatrix}$	-0.126
CC + VC	$\begin{Bmatrix}8.53\\10.8\end{Bmatrix}$	$\begin{Bmatrix}\pm76°\\\pm79°\end{Bmatrix}$	$\begin{Bmatrix}4.8\\4.8\end{Bmatrix}$	-0.860
CC + PC	$\begin{Bmatrix}49.2\\10.8\end{Bmatrix}$	$\begin{Bmatrix}\pm88°\\\pm79°\end{Bmatrix}$	$\begin{Bmatrix}0\\103\end{Bmatrix}$	$\begin{Bmatrix}0\\0.218\end{Bmatrix}$
CC + NSC	$\begin{Bmatrix}2.36\\2.36\end{Bmatrix}$	$\begin{Bmatrix}\pm44°\\\pm44°\end{Bmatrix}$	$\begin{Bmatrix}102\\102\end{Bmatrix}$	0.070
Full$^-$	$\begin{Bmatrix}2.67\\2.27\end{Bmatrix}$	$\begin{Bmatrix}\pm49°\\\pm42°\end{Bmatrix}$	$\begin{Bmatrix}102\\102\end{Bmatrix}$	0.077

The error obtained for the margins is not only dependent on DD but the magnitude and phase of the impedance ratio at the given frequency. However, when the D rating is above 0.7 the efficacy of traditional margins is evident and independent of these other factors. When the rating is below 0.7, an error will be obtained and generally, the lower the D rating the greater the error obtained with some exceptions.

VII. SENSITIVITY ANALYSIS

Previously in literature there has been situations where complex controller structures have been analysed using SISO techniques successfully [9]. These systems are thought to have outer loop control components tuned to a low bandwidth which reduces the overall effect on the impedance shape. These tunings are viable in the modern system and the D rating can be quickly determined for systems to ascertain if simpler, SISO analysis is applicable. This section explores the DD and subsequent gain margins obtained for various tunings of the PLL, PC and VC.

For each control structure the tuning of both proportional and integral gains is altered via multiplication of the initial gains by a tuning constant, α, which is specified as a 100-step range of (1-100) for the PLL and PC and (1-25) for the VC. The initial gains are shown in Table 1. The SISO gain margin at the specific gain margin frequency is obtained alongside the rating of diagonal dominance at that frequency. If the gain margin is precise the Nyquist plot should pass directly through the critical point $(-1,0)$ and a 0.5 % error is used to obtain an appropriate rating of DD. The D rating, percentage error and gain margin are shown for the 100 tuning constant steps in Fig. 12. The magnitude of percentage error is also plotted on a logarithmic scale to better indicate the 0.5 % error threshold.

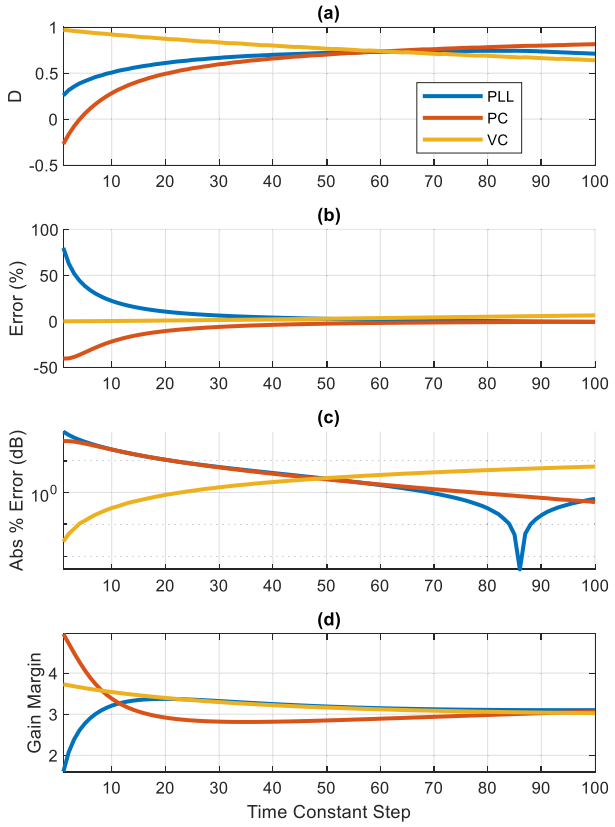

FIGURE 12. Sensitivity analysis results for 100 time constant steps (a) D rating (b) Percentage error (c) Absolute percentage error on log scale (d) Gain Margin.

From Fig. 12(a), the DD of the PLL and PC systems increases as the controller gains increases and the response time becomes faster. Conversely, the DD of the VC system decreases as the VC controller speeds up. The percentage error in Fig. 12(b) indicates a very similar relationship between D rating and error in obtaining a correct stability limit for the PLL and PC systems despite being negative of each other. Furthermore, the error for the VC increases as the DD decreases and at a slower rate. The instability of the PLL and PC systems are related to the second eigenloci while the VC is related to the first eigenloci. This explains the different sensitivities between D rating and error. The D rating analyses the entire matrix, not individual rows therefore an exact match when analysing different eigenloci cannot be expected. Using the zoomed plot in Fig. 12(c), it can be seen that the 0.5 % error is reached when the D rating is 0.742, 0.778 and 0.9, respectively for the PLL, PC and VC systems.

From this analysis is safe to assume that a D rating of 0.7 or higher is safe to consider the system DD and that traditional SISO techniques can be applied with a small factor of safety. It can also be seen that the magnitude of error increases exponentially when the D rating falls below 0.7. This may not be as visible for the VC controller as when the tuning is increased beyond the largest constant, the error for the VC exhibits a large step while the D rating continues to decay as the problematic pole appears to be removed. Since the rating is based solely on mathematical structure of the admittance matrix this rating should be applicable to further admittance matrices for differing control types.

The VC requires a higher D rating than other systems to achieve the tight error tolerance set, but when the D rating is 0.7 the error is still less than 5 %. Again, the reason for this is due to the instability for the VC being related to the first eigenloci. When the mathematical structure is analysed, the Y_{np} component is the greatest in magnitude and is the key reason for the reduced DD. The VC has less effect on Y_{np} than the PLL or PC and therefore the error exhibits a lower sensitivity. This lower sensitivity appears to require a greater D rating to obtain the 0.5 % error threshold for the VC. While the D rating is clearly not the only factor at play effecting the applicability of SISO margins, it provides a good estimate of where they can be applied.

The analysis suggest that SISO gain margins can be applied in systems where the power control and PLL are tuned quickly and the voltage control is tuned slowly. This type of tuning is viable in strong networks. These situations still occur frequently in the modern network despite most novel research focusing on weak networks. By analysing the D rating of the system before stability analysis, complicated MIMO analysis which is complicated and time consuming can be avoided.

VIII. DISK MARGINS

Disk margins have been proposed as a method to tackle these issues in MIMO systems and can be applied irrespective of DD [25]. Disk margins can consider complex perturbations

in all loops at once to give a better idea of real stability margins and are applicable to NMP systems. This is particularly important in grid-connected converters considering that 3ϕ perturbations from the network will extremely rarely result in a single channel reaction in the synchronous reference frame controller. With disk margins, gain and phase margins are considered as a complex multiplicative factor f, of the form:

$$f \in D(\alpha, \sigma) = \left\{ \frac{1 + \frac{1-\sigma}{2}\delta}{1 - \frac{1-\sigma}{2}\delta} : \delta \in C, |\delta| < \alpha \right\} \tag{21}$$

where the set $D(\alpha, \sigma)$ defines the complex set of perturbations. If the disk skew factor σ, is selected to be 0 the overall perturbation gain can increase or decrease by the same magnitude. In this case the open-loop system is the impedance ratio:

$$L = Z_g Y_c \tag{22}$$

The disk margin can then be defined as the maximum value of α that allows fL to remain stable for all $f \in D(\alpha, \sigma)$. If the set of possible system perturbations is known, the disk skew can be altered to more accurately cover the real system variations. For MIMO systems, the multiplicative factor f is applied to each channel individually for loop-at-a-time (LAT) margins or two factors $f_1, f_2 \in D(\alpha, \sigma)$ applied simultaneously to both input channels for multi-loop (ML) margins. The loop-at-a-time and all-loop disk margins for each system in the dq-frame are compared in Table 6 and Table 7, respectively. The dq-frame is used to indicate the improvement in determining stability margins in systems that are not diagonally dominant.

TABLE 7. Comparison of Multi-loop disk margins.

Controller	Disk GM	Disk PM	Frequency (Hz)	D
CC	2.85	±51°	5.6	-0.763
CC + PLL	2.78	±50°	10.8	-0.126
CC + VC	2.97	±53°	5.7	-0.821
CC + PC	8.28	±76°	95.4	0.197
CC + NSC	1.65	±28°	102	0.07
Full	1.69	±29°	102	0.077

From Table 6, the minimum LAT GM is always lower than the SISO gain margins determined in Table 2 in the dq-frame. However, in most cases the LAT GM is higher the pn-frame GM obtained. This is due to the LAT GM being designed for a single channel and will overestimate margins if applied to more than one channel simultaneously. Despite the pn-frame margins being of a similar SISO nature to LAT, the same effect is not observed due to the increased DD in the pn-frame. Hence, the gain variation is smaller and can be applied to both channels. Furthermore, the LAT PMs obtained are also significantly lower than the traditional SISO PMs found in Table 4. This effect is exacerbated for the more complex control, especially when including NSC due to the complex nature of the Nyquist trace previously discussed. This indicates that the disk margin method may offer a more realistic measure of stability irrespective of the D rating which is very low in each case with no system being considered close to DD.

From Table 7, the ML disk margins offer the most conservative measure of stability with the smallest ratings. This is expected and guarantees stability for a range of combinations of perturbation that could be possible in the electrical network. The frequencies at which the system is considered sensitive to gain and phase variations are largely in agreement with the frequencies obtained for the LAT margins and hence, the D rating is the same. The ML GMs are much lower showing that the system is far more sensitive to variation than previously thought with traditional SISO margins and LAT margins. The same is observed for the phase margins This effect increases as the complexity of the system increases and appears independent of DD. The LAT and ML disk margins are applied to the CC system in Fig. 13 via Nyquist plots of the worst case eigenloci. The remaining systems are plotted in Fig. 14. Note that both eigenloci are plotted in Fig. 14 (c)(d) for the CC + PC system due to the differing effect of the applied margins.

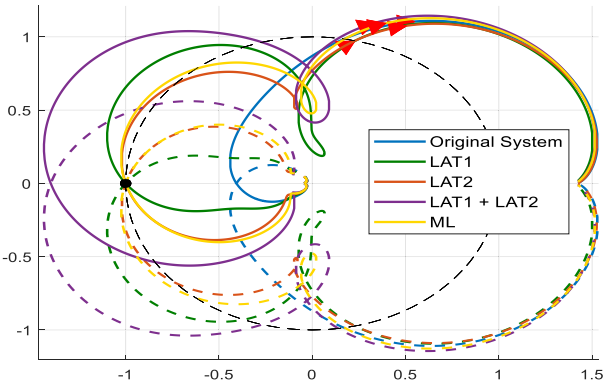

FIGURE 13. Comparison of LAT and ML disk margins for CC system.

From Fig. 13, each LAT and the ML margin predicts the stability limit exactly with simultaneous gain and phase variations. When the LAT margins are combined the stability limit is largely overestimated in the case of the CC system. The introductions of the simultaneous gain and phase variations does introduce some complicated loops in the Nyquist traces that are not previously present. A table of errors is not provided as the error is always less than 0.5 % except for the combined LAT margins where the error is very large with one exception.

From Fig. 14 (a)(b)(e)(f), the result that was observed for CC is repeated for most of the more complicated systems. The LAT disk margins provide the most accurate assessment of simultaneous gain and phase variation for a single channel perturbation. However, this very rarely occurs and

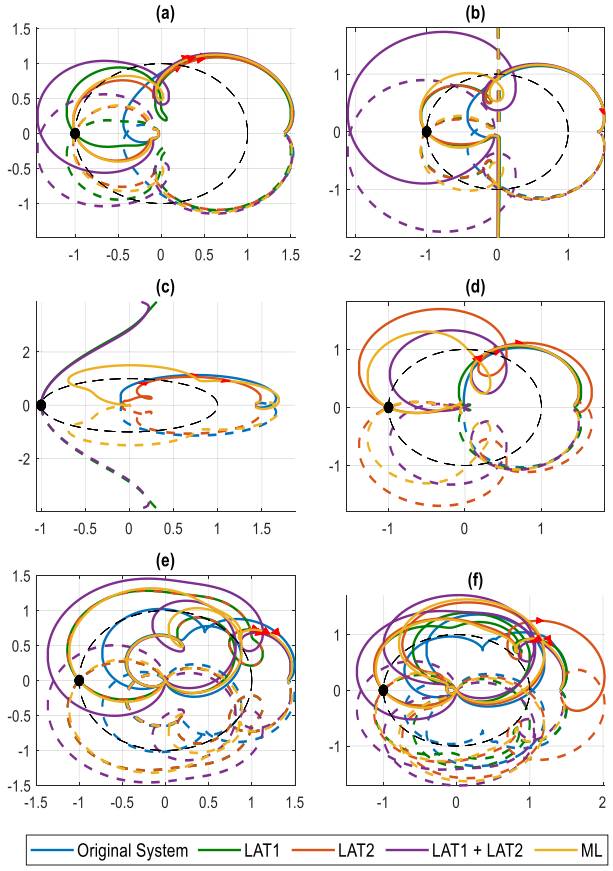

FIGURE 14. Comparison of LAT and ML disk margins for (a) CC + PLL (b) CC + VC (c) CC + PC 1st loci (d) CC + PC 2nd loci (e) CC + NSC (f) Full^{-}.

in most cases using the traditional SISO margins is likely preferable in the pn-frame where the D rating is above 0.7. The CC + PC system eigenloci shown in Fig. 14 (c)(d) provide an interesting result where the combination of the two LAT margins provide almost the same results as the ML margins. Moreover, the individual LAT margins effect the 2nd eigenloci driving it towards instability while the combined LAT and ML margins shift the 1st eigenloci toward the critical point. This is interesting as the ML margin appears much smaller than the combination of LAT margins but suggests that the axis with the large LAT margin is actually very robust to any variation. This also explains the reason for the poor measure from the traditional SISO margins which provided the greatest error.

The SISO margins are simpler and more widely recognised so should be used where applicable. However, for the real network ML disk margins offer the best approach achieving the exact stability margins envelope that the system can handle. This includes simultaneous gain and phase variations in all loops at once which is representative of the real system. This allows the control design to be more robust for the modern network with a higher penetration of converter connected generation which does not form diagonally dominant impedances across the frequency range.

IX. CONCLUSION

The effect of different grid-connected controller complexity on the DD of the obtained converter output impedance and subsequent impedance ratio for stability analysis has been identified. Only simple current control in both the positive and negative sequence can form a MFD system in the synchronous reference frame and hence DD system in the modified sequence domain across the entire frequency range. Active power control provides the greatest reduction in DD while voltage control provides the least. However, the effect of both outer-loop controllers is directly dependent on the bandwidth of the outer-loop control with a slower time constant providing greater DD.

A rating of DD based on the correlation coefficient between rows and columns in the same matrix has been proposed with a rating of -1 indicating the off-diagonal terms are dominant, 0 suggesting a uniformly distributed matrix and 1 indicative of a purely diagonally dominant matrix. Using the proposed method, a rating of 0.7 is determined as sufficient for the application of traditional SISO stability margins to grid-connected converters which should be used where applicable due to their widescale understanding and simplicity. The sequence frame is found to maintain the DD property better than the synchronous reference frame (SRF) but reduced DD is still observed as more control components are added. Interestingly, the NSC alters the SRF impedance significantly but if the PLL is disregarded, the MFD property of the matrix is maintained. Hence the NSC does not affect the DD of the matrix in the sequence frame. Impedance based stability analysis has been conducted to validate this result with margins applied to the Nyquist traces of eigenloci. Pitfalls of traditional margins in non-diagonal dominant systems have been remedied by the application of disk margins which consider gain and phase perturbations more representative of the real electrical network and provide a more conservative measure of system robustness. The multi-loop disk margins are found to offer the best results independent of DD.

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All results can be fully reproduced using the methods and data described in this article and references provided.

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