Active Distribution Networks Fault Current Limitation with Energy Recovery Based on Power Electronics in Hybrid AC-DC Systems

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***Abstract*—The active distribution networks are becoming increasingly complicated hybrid AC-DC systems constructed by massive power electronics, the magnitude and direction of power flow may change randomly at any time, making the usual protection potentially insensitive, increasing the negative impacts of single-phase-to-ground (SPG) fault which accounts for the majority of all faults that occurred in medium-voltage (MV) distribution networks in the past. The zero-sequence current in the impedance branch induced between the lines and ground will pass through the SPG fault branch as fault current. This study transfers the zero-sequence current from the SPG fault branch to the power electronic branch connected between the faulty phase and ground involved in the construction of hybrid AC-DC system, thereby limiting SPG fault branch current and reducing fault node potential. This helps to extinguish fault arc and provides engineers with safe conditions to clear faulty elements from the SPG fault branch. The power electronic bears the same fault current and fault phase voltage as SPG fault and will therefore absorb energy in the same way as SPG fault, the energy is recovered and routed back to the hybrid AC-DC system via interconnected power electronics for reuse. The proposed is verified by simulation and experiment.**

***Index Terms*—active medium-voltage distribution networks, single-phase-to-ground fault, fault current limiting, active fault arc suppression, energy recovery, hybrid AC-DC systems, power electronics transformer**

I. INTRODUCTION

WITH the penetration of distributed resources, active distribution networks may become increasingly complicated hybrid AC-DC systems constructed by a great quantity of power electronics in the future [1]. In this case, the magnitude and direction of power flow may change randomly at any time [2], which may lead to the potential insensitivity of usual protection, thereby increase the negative impacts of faults [3]. According to statistics, the majority of all faults that occurred in medium-voltage (MV) distribution networks in the past were single-phase-to-ground (SPG) faults, which may be accompanied by arcing, resulting in fires, electrocution of life, and widespread power outages, etc [4], [5]. Thus, the active MV distribution networks are urgently need to improve their capabilities of self-healing and self-recovery from SPG fault [6], [7].

SPG fault typically contains a large amount of capacitive fault current and a small amount of resistive fault current caused by the impedance induced between the lines and ground. Ref [8] provides a detailed analysis of SPG fault current via the symmetrical component method, where a phasor diagram of currents was drawn for our easy understanding, and the flow path of capacitive and resistive components of the SPG fault current was clarified. In [9], the experimental measurement of SPG fault current for various fault causes was conducted, and the real SPG fault current waveform data was collected for our analysis and comprehending. The experimental results align well with those measured by other authors in other distribution networks mentioned in this literature, even if they applied simplified measuring circuits.

If the SPG fault current is large and persistent, a series of derivative problems may be caused. For examples, when the SPG fault current increases, the electrical potential of the ground may increase due to the thermal and mechanical stresses of grounding grid, and the protection provided by the grounding grid against step and contact potential may become insufficient [10]. Based on the analysis in ref [11], the fault current distribution between grounding electrodes and cables sheaths was considered as the main factor affecting the safety of grounding grid, and a simulation model was built to further analyze the negative impacts of different factors on the fault current distribution. Temporary overvoltage is another serious problem that may arise from SPG fault, and an experiment proved that the temporary overvoltage may exceed 2.3 p.u. in MV distribution network with isolated neutral, sometimes may evolving into cross-phase faults [12]. Therefore, the SPG fault current and fault potential should be limited to a safe range, avoiding energy loss from fault in form of thermal energy and serious life-threatening electrocution [13]. Moreover, this helps to extinguish the fault arc and has a high probability of restoring the distribution network on its own, or provides engineers with safe conditions to clear faulty elements from the SPG fault

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branch in time, avoiding power outage to loads.

Among the latest applications, superconductor is considered to be one of the desired fault current limiter as it is lossless during the normal operation but an intrinsic high resistance can be induced during a fault to limit the high fault current, and it can be applied to different parts of AC and DC power systems such as power generation, power transmission, and power distribution [14]. However, the cost of superconducting fault current limiter with design, manufacture and operation is high compared to conventional current limiting solutions and a low temperature operating environment is required so that it has not been fully accepted by the power system researchers and engineers and is therefore not applied on a large scale in industry [15]. It could be a very promising application in the future after addressing these problems.

At present, in DC system, current-limiting reactors are still commonly accepted, they suppress the surge of fault current when a fault occurs and contain resistors for further current limiting, but may deteriorate the system stability and dynamic responsiveness, the rapid fault current clearing and system recovery. With the maturity of thyristor technology, fault current limiters based on power electronics have better cost performance. In [16] and [17], power electronic switches were applied to control the rapid opening and closing of reactor branch, mitigating the negative impacts of reactors on the system. However, reactors may saturate during fault current limiting and they can only limit the surge of fault current but not the peak. Consequently, ref [18] presented to provide additionally virtual reactance controlled by modular multilevel converter that interconnects AC and DC systems at the converter station to assist the reactor in limiting fault current, avoiding reactor saturation and additional current limiting devices. Ref [19] applied a stand-alone controlled voltage source converter to completely replace reactors so that the negative impacts of reactors are completely eliminated, with better current limiting performance, but it is additionally installed. Similarly, in AC system, inductive Peterson coils are still the accepted fault current limiters commonly, but they may cause negative impacts on the system such as resonance overvoltage and long transient process. Accordingly, power electronics were connected to the neutral point to work with inductive Peterson coils to regulate away from the resonance point, mitigating the negative impacts and further limiting the residual component of the SPG fault current [20], [21]. Moreover, the adjustable current-limiting coils combined with active converters were presented to reduce the capacity of inverters and improve the dynamic performance of inductive Peterson coils in [22], [23]. However, the transient process is still long and the coil may affect the stability of converters. Thus, ref [24]-[27] applied the stand-alone single-phase or three-phase converters to limit the fault current, completely eliminating the negative impacts of inductive coils, with faster dynamic response and better stability, but the converters are also additionally installed, with high costs.

In the available research reported in literature, the main research gap between fault current limiters based on power electronics in AC and DC system is that DC fault current limiters take into account the energy interaction with the fault during the fault current limiting process, i.e., the flexible fault current limiter can recover fault energy for DC system [28], [29], but the recovered energy was consumed directly, not stored or reused. Therefore, ref [30] proposed a secondary active DC fault current limiter topology which not only has excellent secondary active current limiting performance, but also can recover and store fault energy for reuse. As for AC fault current limiters, the corresponding research reported in literature in this field is deficient, and the energy recovery technology is only available in rail transit [31]-[33], where the energy is usually generated by train braking, and recovered via power electronics for reuse.

As mentioned at the beginning, active distribution networks may become complicated hybrid AC-DC systems constructed by many power electronics in the future. Depending on the voltage level, hybrid AC-DC systems can be classified as low-voltage (LV) AC-DC system [34], [35], MV AC-DC system [36], [37], and high-voltage (HV) AC-DC system [38], as well as hybrid AD-DC system with MV and LV interconnections [39], [40] and MV and HV interconnections via solid state power electronic transformers [41]. They come in a variety of topologies, but operate in a large similar way. Of these, hybrid MV and LV AC-DC systems typically carry more distributed resources penetration due to the matching of voltage levels, including photovoltaic power (PV), wind power, energy storage devices (ESD) and electric vehicles (EV) that can be considered as sources or loads, thus the power electronics that interconnect multiple AC and DC systems are also considered as energy routers [42], [43], which can simultaneously manage the voltage, current, and power flow of hybrid AC-DC system.

Given the flexibility and availability of power electronics in AC-DC system, this paper takes a hybrid AC-DC system with MV and LV interconnections based on power electronic transformer as an example, applying the power electronics in the hybrid AC-DC system to limit the SPG fault current in the MV distribution network while recovering the corresponding energy. The topology of this power electronic transformer connected between the MV distribution network and ground is cascaded H-bridge (CHB), where the DC-link of each H-bridge contains a capacitor and is connected to the ESD of the DC system via isolated DC converter. All ESD are connected to the common DC bus of the DC system in parallel via non-isolated DC converters, and the distributed resources and loads

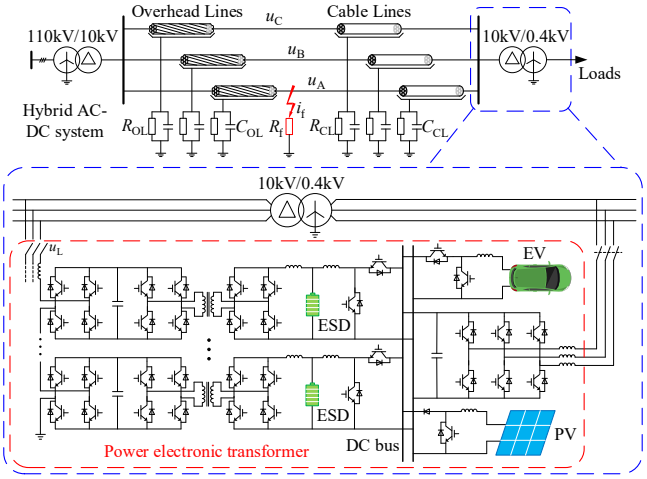

Fig. 1. Topology of hybrid AC-DC system with MV and LV interconnections based on power electronic transformer.

such as PV and EV are also connected in the common DC bus via non-isolated DC converter. The DC bus is connected to the LV distribution network via three-phase converter, building the hybrid AC-DC system with interconnection of the MV and LV distribution networks, as shown in Fig. 1.

The implementation of this topology is that when a SPG fault occurs in the MV distribution networks, the CHB connected between the faulty phase and ground is controlled as a branch of zero-sequence circuit, transferring the zero-sequence current in the impedance branch induced between the distribution networks and ground, from the SPG fault branch to the CHB branch, thereby limiting SPG fault branch current and reducing fault node potential, because this zero-sequence current is the main cause of SPG fault branch current. During this period, the CHB withstands the same fault current and fault phase voltage as a SPG fault and will therefore absorb energy from the MV distribution networks in the same way as a SPG fault. The energy is not lost but is absorbed and temporarily stored in the DC capacitors. The isolated DC converter that interconnects the DC capacitor and the ESD in the DC system provides an energy routing path for the absorbed energy so that it can be recovered and stored in the ESD for a long time or supplied directly to the LV distribution network loads via three-phase converter for reuse, while maintaining the DC capacitance voltage stable.

The advantages are that it does not cause resonant overvoltage and long transient process as inductive Peterson coil do and addresses the problem of energy interaction between the SPG fault branch and the fault current limiter branch, and that no fault current limiting devices need to be additionally installed. Moreover, during the normal operation of distribution network, it serves as a power electronic transformer that can transmit power to LV loads to share the strain on distribution transformer. Especially in the case of charging EV in clusters at night, the power can be transmitted to the EV from both paths, the distribution transformer and the power electronics, avoiding overload operation of the distribution transformer, and the ESD can profit from the difference between peak-valley price by peak-load shifting. During this period, the power electronic transformer can also convert the asymmetrical three-phase components in the MV distribution network to the DC system and then reconvert them to symmetrical three-phase components for the LV distribution networks by controlling the CHB as a negative or zero sequence circuit, which can symmetrize both the three-phase voltage and current in the MV and LV distribution networks. These are well worth studying for researchers at present and will be very useful for active distribution networks in the future.

It is worth emphasizing that the proposed method is not limited to the specific topology referred to herein. The key to power electronics for limiting SPG fault current is whether the topology has a zero potential point and can be connected to ground which can provide a path for the zero-sequence current induced between the distribution network and ground to flow, thus preventing it from passing through the SPG fault branch, otherwise the power electronics topology can be used to limit fault currents as long as they have sufficient voltage and current withstand capability and are fully four-quadrant controllable. The energy absorbed during this period can be recovered, and stored or fed back in the form of DC capacitor energy routing via interconnected power electronics. The main contributions of this article are summarized as follows.

1) The characteristics of SPG fault current caused by the zero-sequence current induced by the MV distribution network and ground are analyzed, whereby the characteristics of active power loss from the fault caused by the SPG fault current with different fault resistance is concerned and summarized and clearly shown, accordingly a solution idea to improve the fault resistance by limiting the SPG fault current is proposed.

2) Combined with the analysis of zero-sequence circuit in MV distribution network, it is proposed to transfer the zero-sequence current induced by the MV distribution network and ground from SPG fault branch to power electronics branch by control for limiting fault current. The active power interaction between the power electronics and the fault is derived through voltage-current vector analysis, and the power electronics DC energy routing is proposed to recover the active power.

3) The coordinated control for power electronics is designed. Through simulation and experiments, it has been proven that the SPG fault current can be limited in case of different fault resistance, avoiding energy loss from fault. The fault node potential is also reduced, the fault arc can be extinguished due to the combustion conditions not being met, which also meets the safe conditions for engineers to clear faulty elements at the location of SPG fault, without power outage to loads.

The remaining of this paper is organized as follows: the principles of SPG fault current limiting with energy recovery are introduced in Section II. The control and implementation are presented in Section III. The simulation and experimental results are collected and discussed in Section IV and Section V, respectively. The conclusions are elaborated in Section VI.

II. Principles of SPG Fault Current Limiting With Energy Recovery

A. Analysis of SPG Fault Current and Energy Loss

Taking the simplified 10 kV distribution network with a SPG fault in Fig. 1 as an example for analysis. The feeder types include overhead lines and cable lines. The line impedance is temporarily neglected and only the phase-to-ground impedance is considered. Assume that the three-phase-to-ground impedance is symmetrical. R_{OL} and C_{OL} are the phase-to-ground leakage resistance and capacitance of the overhead lines, respectively, and R_{CL} and C_{CL} are the phase-to-ground leakage resistance and capacitance of the cable lines, respectively, which are induced between the distribution network and ground and can be measured [5], [20]. u_{A}, u_{B}, and u_{C} are the three-phase-to-ground voltages, respectively. The grid frequency f is 50 Hz. The initial phase angle of the phase A voltage is assumed to be zero. The SPG fault occurs in the phase A, and the fault resistance is R_{f}, and the fault current is i_{f}.

According to Kirchhoff's current law (KCL), the SPG fault current can be expressed as

$$-i_{\mathrm{f}}=u_{\mathrm{A}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right)+u_{\mathrm{B}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right)+u_{\mathrm{C}}\left(\frac{1}{R_{\mathrm{OL}}}+\mathrm{j}\omega C_{\mathrm{OL}}+\frac{1}{R_{\mathrm{CL}}}+\mathrm{j}\omega C_{\mathrm{CL}}\right). \quad (1)$$

Let

$$R_0=\frac{R_{\mathrm{OL}}R_{\mathrm{CL}}}{3\left(R_{\mathrm{OL}}+R_{\mathrm{CL}}\right)}, \quad (2)$$

$$C_0=3\left(C_{\mathrm{OL}}+C_{\mathrm{CL}}\right). \quad (3)$$

The fault current i_{f} can be rewritten as

$$i_{\mathrm{f}}=\frac{u_{\mathrm{A}}}{R_{\mathrm{f}}}=\frac{e_{\mathrm{A}}+u_0}{R_{\mathrm{f}}}=-u_0\left(\frac{1}{R_0}+\mathrm{j}\omega C_0\right). \quad (4)$$

Where e_{A} is the line-to-neutral voltage of the phase A; u_0 is the zero-sequence voltage. Therefore, u_0 can be expressed as

$$u_0=\frac{-R_0e_{\mathrm{A}}}{R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0}. \quad (5)$$

Replacing (5) into (4), the fault current can be restated as

$$i_{\mathrm{f}}=\frac{e_{\mathrm{A}}\left(1+\mathrm{j}\omega R_0C_0\right)}{R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0}. \quad (6)$$

The active power p_{L} consumed by the SPG fault can be expressed as

$$p_{\mathrm{L}}=i_{\mathrm{f}}^2R_{\mathrm{f}}=\frac{\left|e_{\mathrm{A}}\right|^2\left|1+\mathrm{j}\omega R_0C_0\right|^2R_{\mathrm{f}}}{\left|R_{\mathrm{f}}+R_0+\mathrm{j}\omega R_{\mathrm{f}}R_0C_0\right|^2}. \quad (7)$$

From (7), the active power loss p_{L} is related to the fault resistance R_{f}, and the order of R_{f} in the denominator is higher than that in the numerator. The other parameters are constants. Take a medium-sized MV distribution network in a suburb of China as an example, the typical constant parameters are $\left|e_{\mathrm{A}}\right|=10/\sqrt{3}$ kV, $R_0=2000\ \Omega$, $C_0=19.5\ \mu\mathrm{F}$, accordingly, the relationship between the active power loss p_{L} and the fault resistance R_{f} can be shown in Fig. 2.

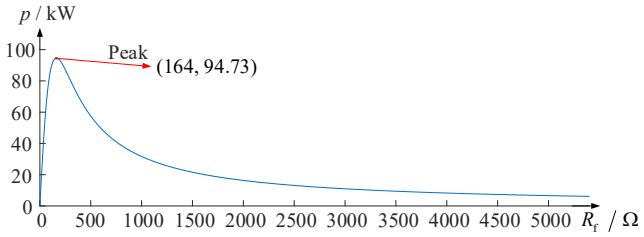

Fig. 2. Active power loss from fault branch under different fault resistances.

When R_{f} is between 17 Ω and 1612 Ω, the active power loss exceeds 20 kW. In this case, the temperature of the fault branch will rise with time, resulting in serious heating, which may cause serious accidents such as fires and electrocution of life. When $R_{\mathrm{f}}=164\ \Omega$, the active power loss is the largest, which is 94.73 kW. If the fault current i_{f} can be rapidly reduced to zero, the fault branch can be equivalent to an open circuit, and R_{f} is equivalent to an infinite resistance. In this case, $p_{\mathrm{L}}=0$ according to (7), and the fault energy loss and corresponding negative impacts can be avoided.

B. Principles of SPG Fault Current Limiting with Energy Recovery via Power Electronics

As shown in Fig. 1, when a SPG fault occurs, the current of the CHB branch connected to the fault phase is regulated to bypass the SPG fault branch. The fault phase can be identified via the fault phase selection algorithm that has been studied to identify SPG fault phase for fault current limiters to adapt to Asymmetric distribution networks [24]. In this case, the zero-sequence equivalent circuit of the MV distribution network can be drawn, as shown in Fig. 3.

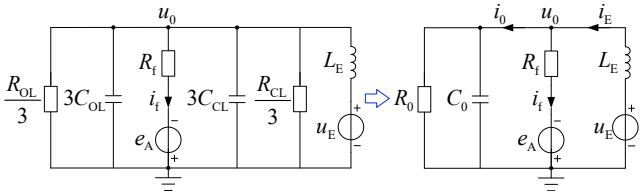

Fig. 3. Equivalent zero-sequence circuit of active MV distribution network during a SPG fault.

Where u_{E} and i_{E} are the output voltage and current of the CHB, respectively; L_{E} is the filter inductance. From Fig. 4, if $i_{\mathrm{E}}=i_0$, $i_{\mathrm{f}}=0$ according to KCL, and $u_0=-e_{\mathrm{A}}$ according to Kirchhoff voltage law (KVL). The output current i_{E} is described as

$$i_{\mathrm{E}}=i_0=u_0\left(\frac{1}{R_0}+\mathrm{j}\omega C_0\right)=-e_{\mathrm{A}}\left(\frac{1}{R_0}+\mathrm{j}\omega C_0\right). \quad (8)$$

The parameters R_0 and C_0 can be obtained in many ways [5], [20], so the reference current of CHB can be calculated by (8). In this way, i_{f} is transferred from the fault branch to the CHB branch, so that the fault branch current is regulated to zero and R_{f} is equivalent to an infinite resistance, $p_{\mathrm{L}}=0$ according to the analysis in Part A above, avoiding energy loss from fault, and there are no additional current limiting devices that need to be installed.

During this process, since i_{f} is transferred from the fault branch to the CHB branch, there is energy interaction between the fault and the CHB converter, the active power output by CHB converter p_{O} can be expressed as

$$p_{\mathrm{O}}=\left|u_{\mathrm{L}}\cdot i_{\mathrm{E}}\right|=\left|u_{\mathrm{A}}\cdot i_{\mathrm{E}}\right|=\left|u_{\mathrm{A}}\right|\cdot\left|i_{\mathrm{E}}\right|\cos\alpha. \quad (9)$$

Where u_{L} is the voltage at the connection point between the CHB branch and MV distribution networks, α is the phase angle difference between u_{L} and i_{E}. The active power output by the CHB converter should ideally be zero because the fault phase voltage is reduced to $u_{\mathrm{A}}=u_0+e_{\mathrm{A}}=0$. Consequently, the fault arc can be extinguished due to the combustion conditions not being met, which also meets the safe conditions for engineers to clear faulty elements at the location of SPG fault, without power outage to loads, and other negative impacts can also be avoided.

However, u_{L} is different from u_{A} due to the existence of line impedance in practice, so the active power output by the CHB converter is typically not zero. The vectors u_{L} and i_{E} before and after the SPG fault current is limited are drawn in Fig. 4.

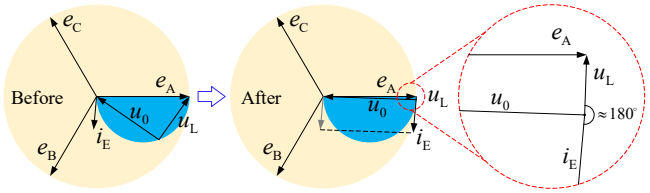

Fig. 4. Vector diagram of grid-connected voltage and output current of CHB in active MV distribution networks.

From Fig. 4, although the amplitude of u_L is not very large after the SPG fault current is limited, the phase angle difference α between u_L and i_E is close to 180°. Therefore, $cos\,\alpha \approx -1$, and (9) can be represented as

$$p_O = |u_L \cdot i_E| \approx -|u_L| \cdot |i_E|. \quad (10)$$

It can be seen that the CHB withstands the same fault phase voltage and zero-sequence current induced by the distribution network and ground that is the main cause of SPG fault current as a SPG fault and will therefore absorb active power from the MV distribution network in the same way as a SPG fault. Which indicated that the CHB converter absorbs the energy that would otherwise be consumed by the SPG fault branch. The energy absorbed by the CHB converter will be stored in the DC capacitors, resulting in the DC-link voltages of the CHB to rise, affecting the CHB performance. With the help of isolated DC converter, the energy absorbed by the CHB converter is recovered via DC capacitor energy routing, it can be stored in the distributed ESD for a long time or supplied directly to the LV loads via the three-phase converter for reuse, keeping the DC-link voltages of the CHB stable. Thus, the problem of energy interaction between the SPG fault and the fault current limiter can be addressed.

III. Control and Implementation

A. Coordinated Control

The key objective of CHB converter control is the output branch current i_E, whose reference value is calculated using (8), but the key to the calculation is to obtain accurate e_A which cannot be measured directly but is obtained by subtracting u_A and u_0 that can be measured directly, i.e. $e_A = u_A - u_0$. To accurately extract e_A, a second-order generalized integral and a phase locked loop (SOGI-PLL) are designed, as shown in Fig. 5. Where u_r is the input signal whose amplitude and phase angle at the fundamental frequency need to be extracted; u_α and u_β are quadrature signals decomposed from u_r. k_s is the gain coefficient of the SOGI; ω is the fundamental angular frequency; u_{amp} is the amplitude obtained at the fundamental frequency; α is the phase angle obtained at the fundamental frequency. u_t is the output signal composed of u_{amp} and α. After the reference current i_0 is calculated by (8), a proportional integral (PI) controller is used to regulate the output current of the CHB i_E.

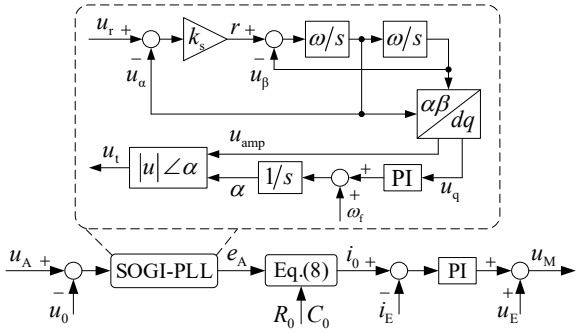

Fig. 5. Schematic diagram of reference value extraction and control for CHB.

The key objective of the isolated DC converter is the DC-link capacitor voltage of CHB for routing the energy absorbed by the CHB converter and keeping the DC-link voltage of the CHB stable. To regulate the size and direction of energy routing, a single phase-shift control method is applied. The two H-bridges of each isolated DC converter are respectively given a square wave with a frequency of 1000 Hz and a pulse width of 50 %. The phase angle of the H-bridge square wave on the DC-link capacitor side is 0°, and that on the other side is shifted to θ which is adjusted by a PI controller, as shown in Fig. 6 (a). Where u_{Hdcn} and θ_n are the DC-link voltage and phase shift angle of the nth H-bridge module, respectively, n=1, 2, 3…; $u_{Hdc\text{-}ref}$ is the reference voltage of the DC-links of the CHB.

The key objective of ESD control is the common DC bus voltage u_{dc} for supporting its stability, as shown in Fig. 6 (b). Where $u_{dc\text{-}ref}$ is the reference voltage of the DC bus; i_{batn} and D_n are the output current from the ESD to the DC bus and duty cycle signal of the nth ESD, respectively, n=1, 2, 3…; The two PI controllers in series are adopted to manage u_{dc} and i_{batn}, respectively.

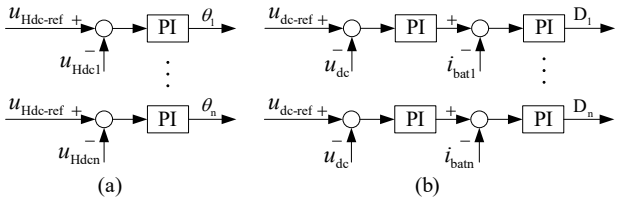

Fig. 6. Control schematic diagram of isolated DC converter and non-isolated DC converter of ESD: (a) isolated DC converter for maintaining DC voltages of CHB; (b) non-isolated DC converter for supporting DC bus voltage.

The key objective of three-phase converter is active power and reactive power. The control system for the three-phase converter is shown in Fig. 7. Where p_{ref} and q_{ref} are the reference active and reactive power, respectively; i_d and i_q are the output currents on the d-axis and q-axis, respectively; u_d and u_q are the output voltage on the d-axis and q-axis, respectively. The modulated voltage u_{abcM} of the three-phase converter can be obtained by Park inverse transformation.

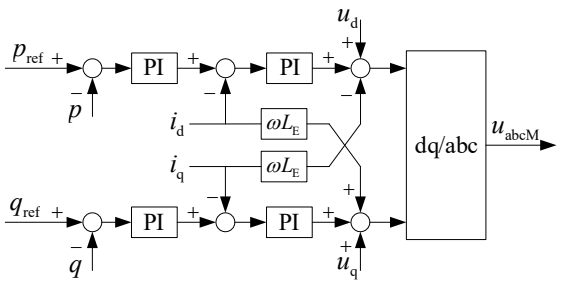

Fig. 7. Control schematic diagram of three-phase converter for suppling active and reactive power to LV distribution networks.

B. Implementation Process

The implementation flowchart of the coordinated control is shown in Fig. 8. During the normal operation of distribution network, the insulation parameters can be measured in real-time [5], [20]. When a SPG fault occurs, the fault phase can be identified rapidly [24], and then the fault phase voltage and zero-sequence voltage are sample and the difference between them is calculated in real-time. Through the control system shown in Fig. 5, the line-to-neutral voltage of the fault phase can be extracted from the difference by means of SOGI-PLL so that the reference current of the CHB can be calculated by (8). Then, the output current of CHB branch connected to the faulty phase is control as the reference current value to limit the SPG fault branch current and absorb corresponding energy. Meanwhile, by using the control system shown in Fig. 6, the isolated DC converters are control to maintain the DC-link voltage of CHB so that the energy absorbed by the CHB is routed to ESD for long-term storage or provided directly to support common DC bus voltage and to loads for reuse. Until the SPG fault is cleared and the distribution network return to normal operation, this process is terminated.

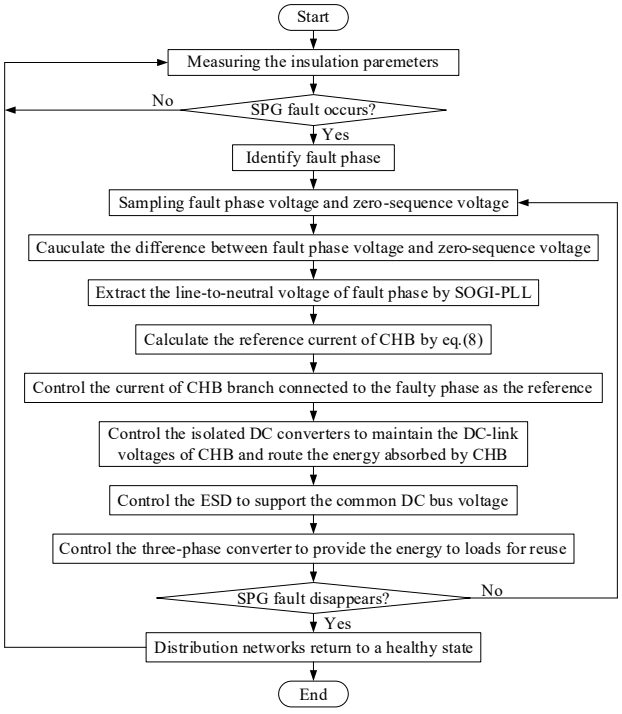

Fig. 8. Implementation flowchart of SPG fault limiting with energy recovery based on power electronics in hybrid AC-DC system.

IV. Simulation and Discussion

A. Simulation Parameters

A simulation model was built on the Simulink platform of Matlab-2017b. The simulation type is discrete, and the solver type is variable-step, and the max step size is 100 μs . The line type is three-phase PI section with overhead lines and cable lines. The battery type is lithium-ion, and the module type of PV array is 1STH-230-P, with ten series-connected modules per string and twenty parallel strings. The parameters in the simulation model are shown in Table I.

TABLE I
Simulation Parameters

Parameters	Value
Sample time	100 [μs]
Phase-to-phase voltage	10 [kV]
Capacitance to ground C_0	19.5 [μF]
Resistance to ground R_0	2 [kΩ]
Number of H-bridges in CHB N	10
DC-link voltage of H-bridge u_{Hdc}	1000 [V]
DC-link capacitor of H-bridge	4700 [μF]
Filter inductance of CHB L_E	0.05 [H]
Frequency of DC isolated transformer	1000 [Hz]
Winding ratio of DC isolated transformer	4:1
Nominal ESD voltage	300 [V]
Rated ESD capacity	500 [Ah]
Initial state-of-charge (SOC)	50 [%]
DC bus voltage u_{dc}	380 [V]
Sun irradiance of PV system	1000 [W/m^2]
Cell temperature of PV system	25 [˚C]
Maximum output voltage of PV system	300 [V]
Maximum output power of PV system	45.75 [kW]

B. Performance of Fault Current Limiting

Assuming a SPG fault occurs at $t = 0.1$ s . To compare the situation before and after the fault current regulation, the CHB connected to the fault phase is control to transfer i_f from the fault branch to the CHB branch only 0.4 s after the fault occurred. Fig. 9 shows the performance, including the active power loss from the fault p_L and the fault current i_f , in the case of $R_f = 1\ \Omega$ and $R_f = 50\ \Omega$, respectively.

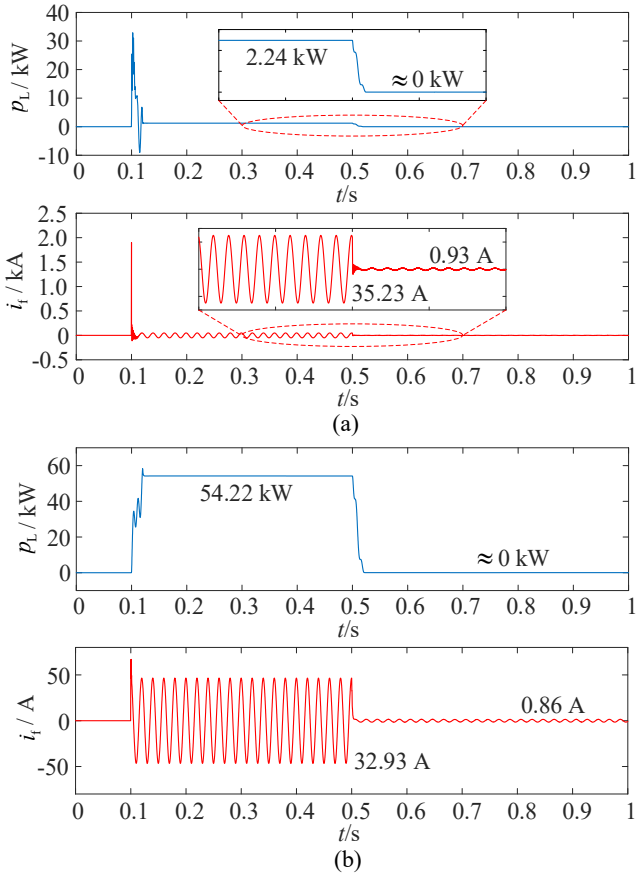

Fig. 9. Simulation waveforms of active power loss p_L and fault current i_f in the cases of different fault resistances: (a) $R_f = 1\ \Omega$; (b) $R_f = 50\ \Omega$.

At the initial period of the SPG fault, the fault current has a large impulse. The maximum impulse current reaches 1913 A in the case of $R_f = 1\ \Omega$, accordingly, the active power loss from the fault has a large impulse. The impulse decreases as the fault resistance increases. The maximum impulse current is 74 A in the case of $R_f = 50\ \Omega$. Before the fault currents are limited, although the fault currents in steady state 35.23 A and 32.93 A are very close when $R_f = 1\ \Omega$ and $R_f = 50\ \Omega$, respectively, the active power losses 2.24 kW and 54.22 kW are very different. Because p_L is related to R_f according to (7), and the slope in Fig. 2 is large when R_f is small. After the fault currents are limited, the fault currents decrease to 0.93 A and 0.86 A when $R_f = 1\ \Omega$ and $R_f = 50\ \Omega$, respectively. Meanwhile, the active power losses drop to near 0 kW.

When $R_f = 164\ \Omega$, the performances of the active power loss from the fault p_L and fault current i_f are shown in Fig. 10. They have not the current impulse and active power loss impulse at the initial period of the SPG fault. The active power loss in steady state almost reaches the maximum value 94.26 kW, which aligns well with the consequence shown in Fig. 2. After the fault current is limited, the residual fault current is 0.67 A, and the active power loss is close to zero.

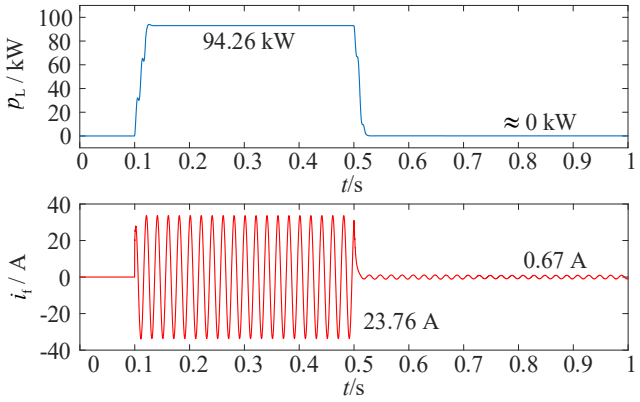

Fig. 10. Simulation waveforms of active power loss p_L and fault current i_f in the case of $R_f = 164\ \Omega$.

When R_f is greater than 164 Ω, the active power loss decreases. Fig. 11 shows the performances in the cases of $R_f = 500\ \Omega$ and $R_f = 2000\ \Omega$, respectively. Because R_f is large enough, they have not the current impulse and active power loss impulse. Moreover, although the fault currents in steady state 10.64 A and 2.83 A are relatively small, the active power losses reach 56.34 kW and 16.02 kW, respectively, which align well with the theoretical analysis conclusion of (7) and Fig. 2. After the fault currents are limited, the residual fault currents are 0.35 A and 0.09 A, respectively, and the active power losses reduce to zero.

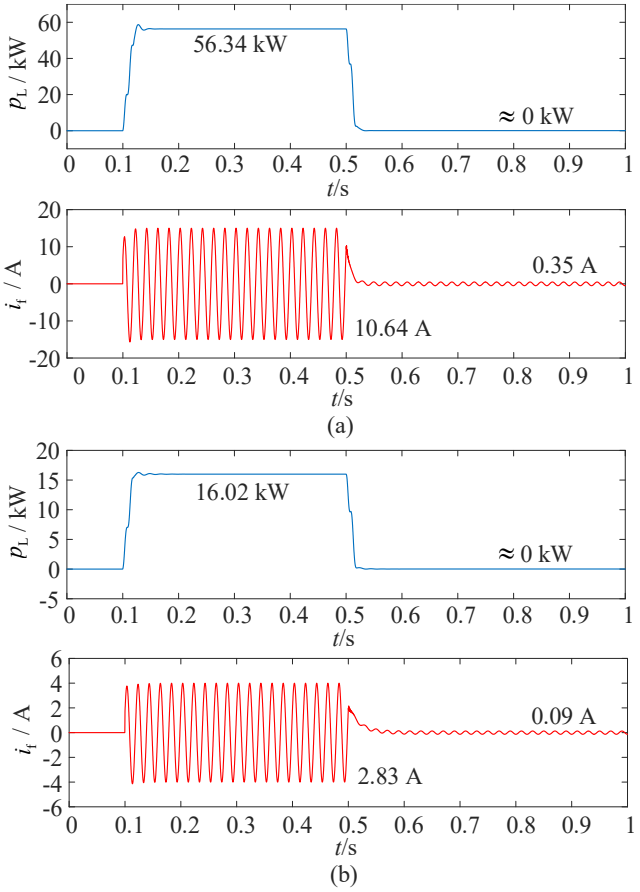

Fig. 11. Simulation waveforms of active power loss p_L and fault current i_f in the cases of different fault resistances: (a) $R_f = 500\ \Omega$; (b) $R_f = 2000\ \Omega$.

The active power curves are fitted in Fig. 12 by discrete points under different fault resistance conditions, including the

active power loss from the SPG fault branch and the active power absorbed by CHB branch. The results show that the active power curve of the fault is consistent with Fig. 2. The active power absorbed by the CHB is large when R_f is small, but it becomes small when R_f is large. Because the active power loss after the fault current limitation does not exceed 0.1 W from Fig. 9 – Fig. 11, while the recovered active power exceeds 1 kW from Fig. 12, thus the percentage of active power loss is no more than 0.1/1000 = 0.01% of the total, i.e., the recovered active power can reach over 99.99%.

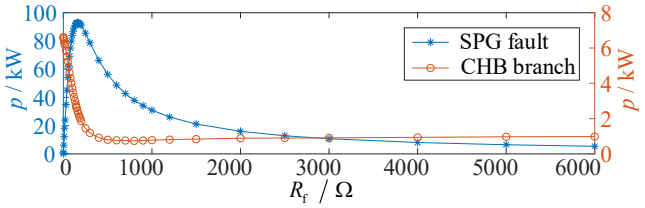

Fig. 12. Active power lost by the SPG fault and active power absorbed by the CHB under different fault resistance conditions.

Through CHB converter, for a wide range of R_f that has been tested, the fault current can be limited effectively, and the active power loss can be minimized, i.e., close to 0 kW. After the fault current is transferred to the CHB branch, the negative impacts of the SPG fault are eliminated, which prompts the distribution network to return to normal operation. Meanwhile, the active power absorbed by the CHB can be stored in the ESD for a long time or supplied directly to load for reuse, the following shows their simulation performances.

C. Performance of Energy Recovery

Fig. 13 shows the performances, including the DC-link voltages of the CHB and the SOC of ESD, when $R_f = 10\ \Omega$ and $R_f = 100\ \Omega$, respectively. At the beginning, the SOC is 50 %, and the DC-link voltages of the CHB are 1000 V. Before $t = 0.5$ s, the isolated DC converters do not work, and the DC-link voltages of the CHB drop slightly due to DC-link loss. After $t = 0.5$ s, the SPG fault current is transferred to the CHB branch, and only the energy absorbed by the CHB during this period is stored in the ESD. The DC-link voltages of the CHB are restored and maintained at 1000 V. The SOC rise from 50 %, and the rising speed in the case of $R_f = 10\ \Omega$ is about twice that in the case of $R_f = 100\ \Omega$, because the active power absorbed by the CHB in the case of $R_f = 10\ \Omega$ is twice as much as that in the case of $R_f = 100\ \Omega$ according to Fig. 2 and Fig. 12. In the cases, although the SOC of the ESD are unbalanced, they can be rebalanced via the common DC bus.

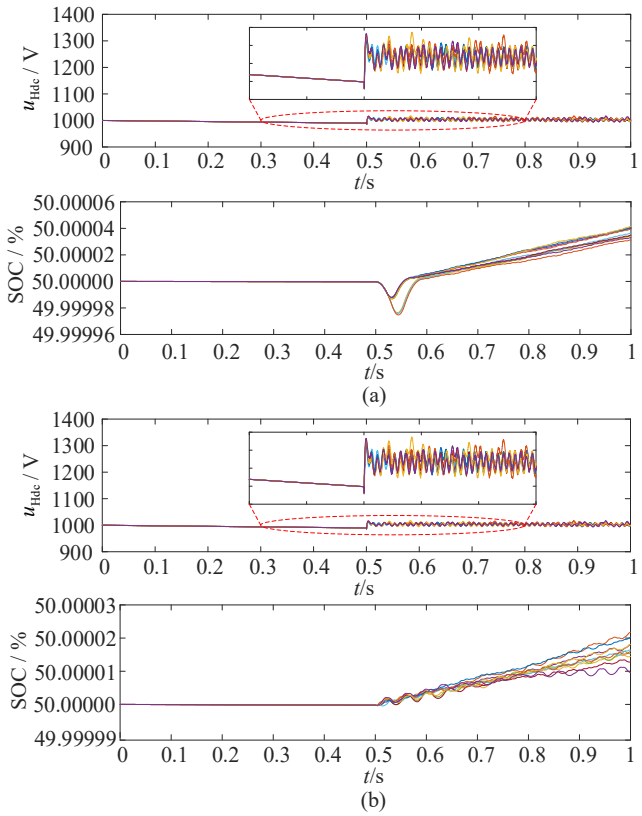

Fig. 13. DC-link voltages of CHB and SOC of ESD in the cases of different fault resistances: (a) $R_f = 10\ \Omega$; (b) $R_f = 100\ \Omega$.

The ESD is used to support the DC bus voltage u_{dc}, and the three-phase converter is responsible for transferring the energy of PV system and the ESD to LV loads for reuse, their performance is shown in Fig. 14 and Fig. 15. Because the LV distribution networks only need the three-phase converter to provide active power 20 kW, but the active power generated by the PV system is close to the maximum. Therefore, without DC load power, the ESD will store the surplus active power 25.37 kW to maintain the DC bus voltage at 380 V. When the active power generated by the PV system is insufficient, the ESD can be used as backup energy.

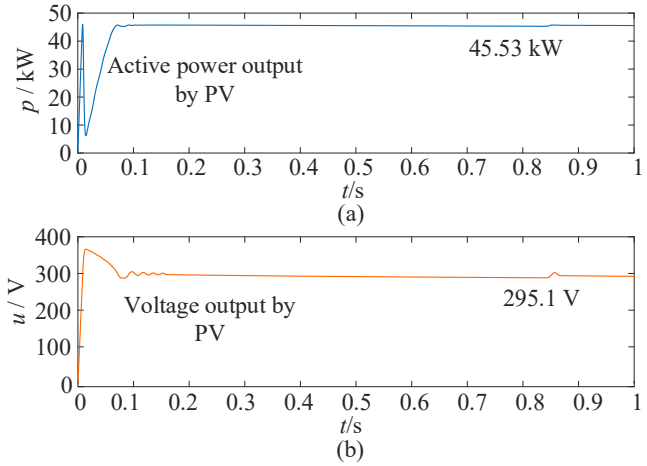

Fig. 14. Simulation waveforms of PV system: (a) Active power output by PV; (b) Voltage output by PV;

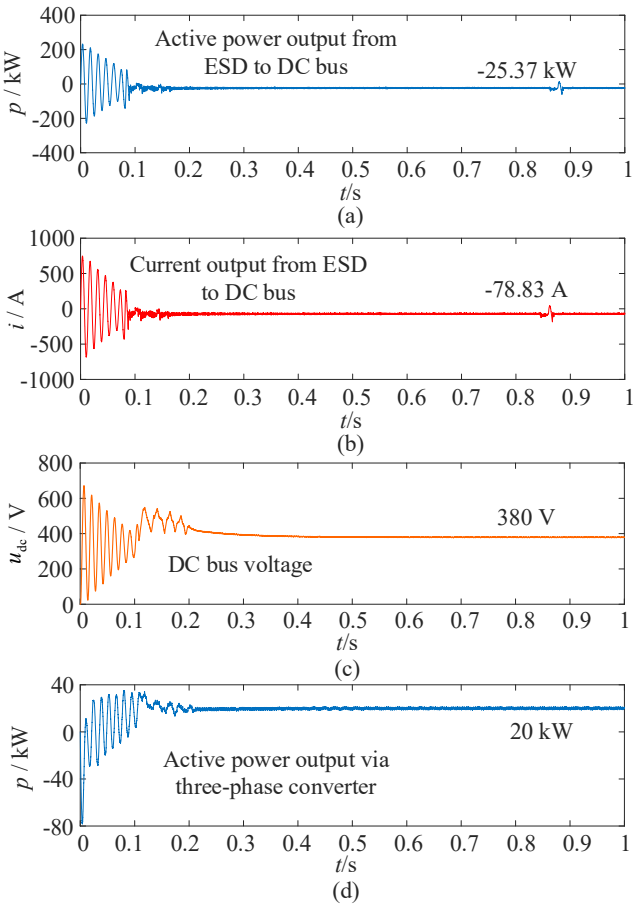

Fig. 15. Simulation waveforms of DC system: (a) Active power output from ESD to DC bus; (b) Current output from ESD to DC bus; (c) DC bus voltage; (d) Active power output via three-phase converter.

V. Experiment and Discussion

A. Experimental prototype

The proposed SPG fault current limitation with energy recovery is verified on a physical experimental system, as shown in Fig. 16. Where the specifications of distribution network cabinets and CHB industrial prototype are shown in Table II. The separate FPGA in each H-bridge module is used to receive switch drive signals from the master CPU with operation system, control the output of H-bridge module, and collect and provide feedback on operation information about the H-bridge module to the master CPU which communicates with the FPGA via optical fiber. The output current and voltage of CHB, and the three-phase voltage and current of distribution networks are sampled by Hall sensors as feedback signals of the master CPU, the specifications of sensors are shown in Table III, and the hardware working schematic is shown in Fig. 17. The CHB is connected to the distribution networks via contactor controlled by the master CPU with fault phase selection algorithm [24], the specifications of contactor are shown in Table IV. The fault generator contains resistors with different resistance values (10, 50, 100, 200, 500, 1000, 2000, 5000 Ω) which are opened and closed by silicon-controlled rectifier (SCR) controlled via MCU to simulate different fault resistors, and the schematic is drawn in Fig. 18. The type of ESD is lithium iron phosphate battery with operational protection, and its specifications are shown in Table V. In addition, the module type of PV system is TP660P polycrystalline solar module with 60 cell series, and the specifications are shown in Table II.

Fig. 16. Photos of physical prototype of hybrid AC-DC system.

TABLE II
SPECIFICATIONS OF DISTRIBUTION NETWORK CABINETS AND CHB INDUSTRIAL PROTOTYPE

Parameters	Value
Sample frequency	6 [kHz]
Phase to phase voltage	380/380 [V]
Phase to ground capacitance	13.92 [μF]
Phase to ground resistance	800 [Ω]
DC-link voltage of H-bridge u_{Hdc}	40 [V]
DC-link capacitor of H-bridge	600 [μF]
Filter inductance of CHB L_E	58.33 [mH]
DC bus voltage u_{dc}	120 [V]
Number of H-bridges	12

TABLE III
SPECIFICATIONS OF SENSORS

Parameters	Value
Rated input of voltage sensor	400 [V]
Measuring range of voltage sensor	0-±480 [V]
Measuring resistance of voltage sensor	>10 [kΩ]
Rated output of voltage sensor	5 [V]
Accuracy of voltage sensor	±1.0 [%]
Supply voltage of voltage sensor	±12 [VDC]
Frequency range of voltage sensor	0-20 [kHz]
Rated input of current sensor	15 [A]
Measuring range of current sensor	0-±48 [A]
Rated output of current sensor	2.5±0.625 [V]
Accuracy of current sensor	±0.7 [%]
Supply voltage of current sensor	+5 [VDC]
Frequency range of voltage sensor	0-100 [kHz]

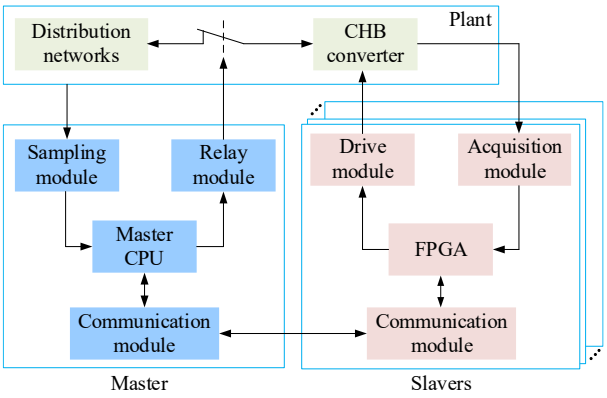

Fig. 17. Hardware working schematic of distribution networks and CHB.

TABLE IV
SPECIFICATIONS OF CONTACTOR

Parameters	Value
Thermal stability current	125 [A]
Rated insulation voltage	690 [V]
Utilization category	AC-3
Rated voltage at single-phase	220/230 [V]
Rated power at single-phase	25 [kW]
Rated voltage at three-phase	380/660 [V]
Rated power at three-phase	45 [kW]

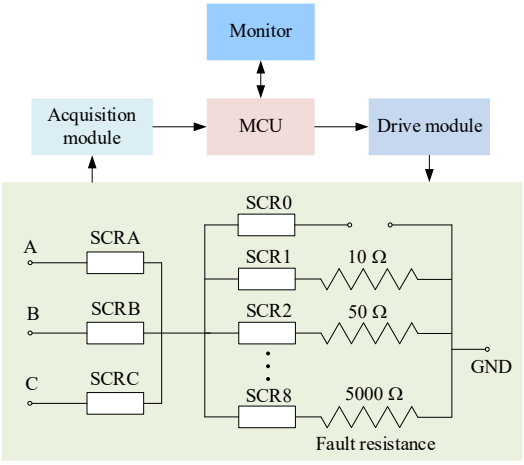

Fig. 18. Fault generator schematic.

TABLE V
SPECIFICATIONS OF ESD

Parameters	Value
Normal voltage per battery	48 [V]
Rated capacity per battery	50 [Ah]
Operating voltage range per battery	40-56.4 [V]
Maximum charging voltage per battery	60.4 [V]
Maximum charging current per battery	10 [A]
Maximum discharge voltage per battery	55 [V]
Maximum discharge current per battery	50 [A]
Discharge cut-off voltage	40 [V]
Number of batteries	12

TABLE VI
SPECIFICATIONS OF PV SYSTEM

Parameters	Value
Maximum power per module	275 [W]
Operating voltage per module	31.7 [V]
Operating current per module	8.69 [A]
Open-circuit voltage per module	38.7 [V]
Short-circuit current per module	9.17 [A]
Module efficiency	16.8 [%]
Number of modules in PV system	6
Number of series-connected modules per string	3
Number of parallel strings	2
Number of series-connected PV module	3
Maximum power of PV system	1.65 [kW]
Maximum voltage of PV system	95.1 [V]

B. Performance of Fault Current Limiting

Fig. 19 – Fig. 21 show the experimental results of SPG fault current limiting, including the CHB voltage waveform, the fault current waveform, and the CHB branch current waveform, in the cases of different fault resistances ($R_f = 10\ \Omega$, $50\ \Omega$, $100\ \Omega$, $500\ \Omega$, $2000\ \Omega$, and $5000\ \Omega$).

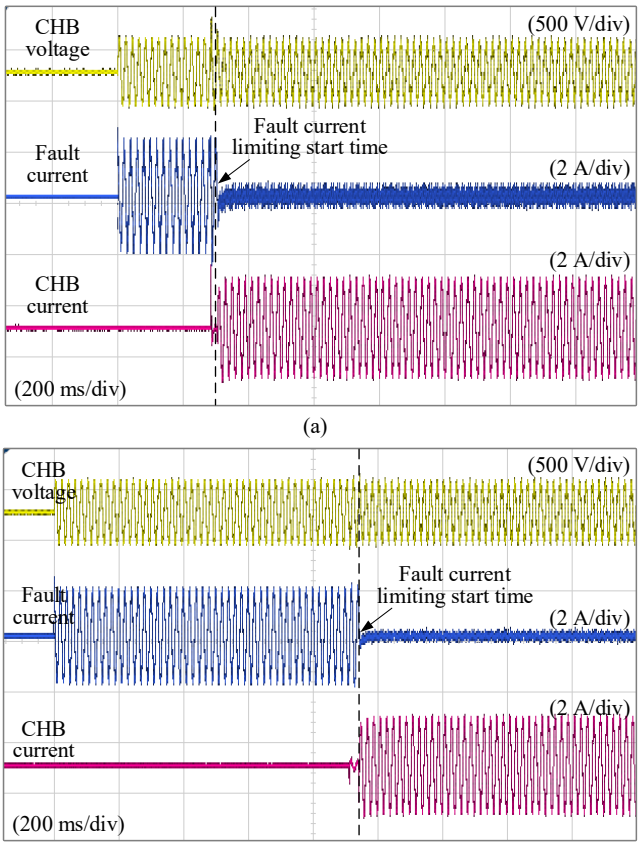

Fig. 19. Experimental waveforms of SPG fault current limiting in the cases of different fault resistances: (a) $R_f = 10\ \Omega$; (b) $R_f = 50\ \Omega$.

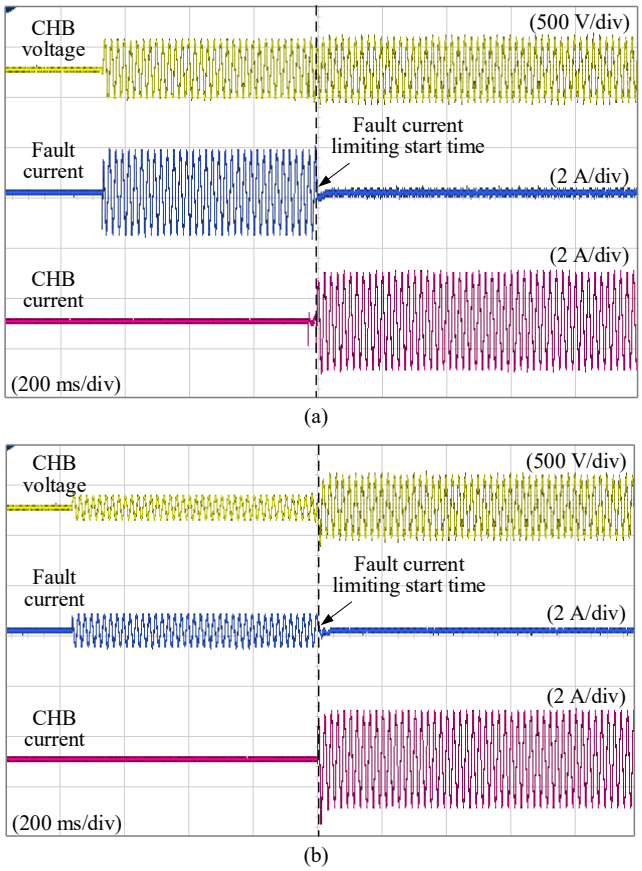

Fig. 20. Experimental waveforms of SPG fault current limiting in the cases of different fault resistances: (a) $R_f = 100\ \Omega$; (b) $R_f = 500\ \Omega$.

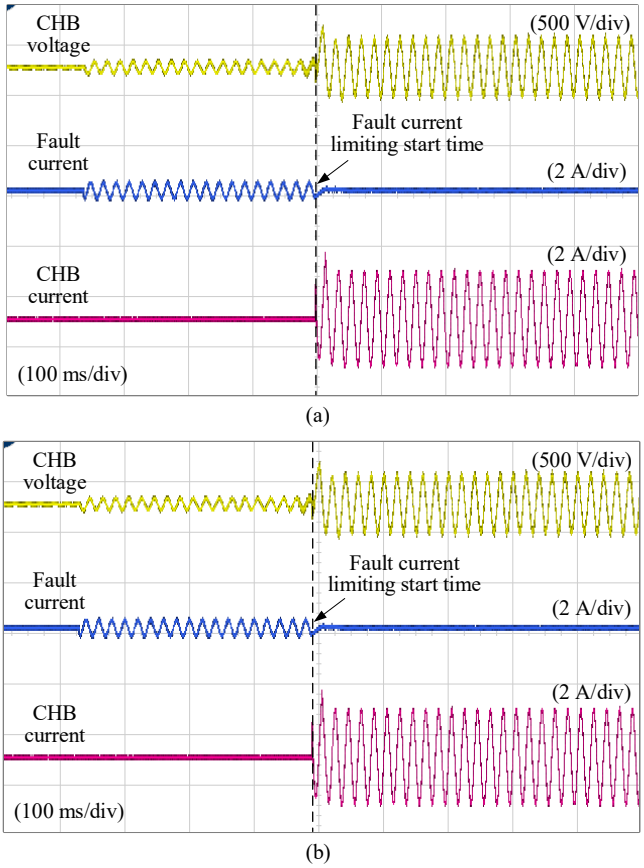

Fig. 21. Experimental waveforms of SPG fault current limiting in the cases of different fault resistances: (a) $R_f = 2000\ \Omega$; (b) $R_f = 5000\ \Omega$.

As shown in Fig. 19, when R_f is small, because the fault phase voltage drops to near zero, u_0 is close to $-e_A$, so the fault current is large which is consistent with (4). After the fault current is transferred to the CHB branch successfully, the residual fault current is close to zero, thus, the active power loss from the fault can be reduced. From Fig. 20 and Fig. 21, when R_f is large, the fault current is small because the fault phase voltage is not close to zero. However, the current transferred to the CHB branch is large, which is due to that after the fault current is transferred, the fault phase voltage is reduced to near zero and u_0 increases to near $-e_A$ according to (8) and Fig. 4. When R_f is large enough, the fault current is small enough, and the residual fault current is closer to zero. The CHB branch current is always large after the fault current is transferred, and is always the same value calculated by (8).

C. Performance of Energy Recovery

The experimental results of storing the active power absorbed by the CHB are shown in Fig. 22, including the DC-link voltage of a H-bridge module, the voltage and current of an ESD. For a clear analysis, only the active power absorbed by the CHB is stored in the ESD. In the cases of $R_f = 100\ \Omega$ and $R_f = 500\ \Omega$, respectively, the currents of the ESD are different due to the different active power absorbed by the CHB, but the DC-link voltages can be maintained at 40 V.

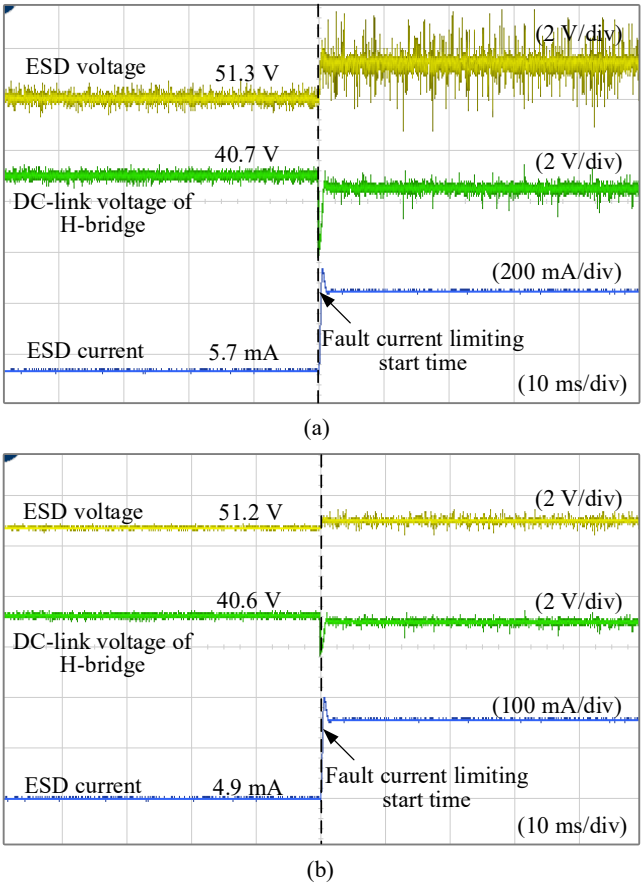

Fig. 22. Experimental waveforms of ESD for storing active power absorbed by CHB under different fault resistances: (a) $R_f = 100\ \Omega$; (b) $R_f = 500\ \Omega$.

Fig. 23 shows the experimental results of the DC system,

including a PV system voltage, the DC bus voltage, the current output from the ESD to the DC bus, and the active power output by three-phase converter. The PV system is close to the maximum output point. According to Fig. 21 (a), when the active power generated by the PV system is insufficient, the ESD provides active power to support the DC bus voltage at 120 V, accordingly, the energy absorbed by the CHB is fed back to the distribution network via the three-phase converter for reuse. On the contrary, when the active power generated by the PV system is surplus, the ESD stores the residual active power to keep the DC bus voltage.

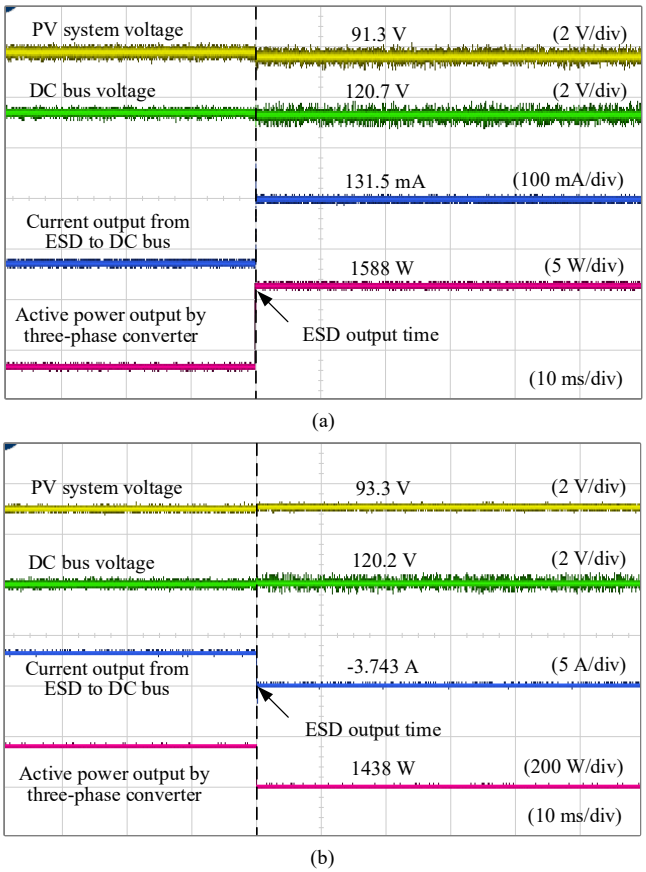

Fig. 23. Experimental waveforms of DC system in different cases: (a) Active power output by PV system is surplus; (b) Active power output by PV system is not enough.

V. Conclusion

To improve the self-healing and self-recovery capabilities of MV active distribution networks from SPG fault, and avoid the potential negative impact of SPG fault, this paper has analyzed the characteristics of SPG fault current caused by the zero-sequence current induced between the MV distribution networks and ground, and has summarized that the active power loss from the fault caused by the SPG fault current is different and the variation follows a certain pattern in the case of different fault resistance. Accordingly, a solution idea to improve the fault resistance by limiting the SPG fault current is proposed. Considering that active distribution networks may become complicated hybrid AC-DC systems constructed by many power electronics in the future, it is proposed to use the power electronic in AC-DC system to transfer the zero-sequence current induced between the MV distribution networks and ground from SPG fault branch to power electronic branch by current control for limiting fault current. During this period, the power electronic will bear the same fault current and fault phase voltage as a SPG fault and will therefore absorb energy from the MV distribution networks in the same way as a SPG fault. By voltage-current vector analysis, the active power interaction between the power electronic and the fault is derived, and the power electronic DC energy routing is proposed to recover the active power. The coordinated control for the power electronics is designed. Through simulation and experiments, it has been proven that the SPG fault current can be limited to less than 3% of the original in case of different fault resistance, avoiding energy loss from fault, and the recovered active power is supplied to LV loads for reuse. The fault node potential is also reduced, the fault arc can be extinguished due to the combustion conditions not being met, which also meets the safe conditions for engineers to clear faulty elements from the SPG fault branch, without power outage to loads.

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