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Grid integration of multiple PV inverters with reduced number of interfacing transformers— A dedicated controller for elimination of DC current injection

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Abstract

The injection of dc current offset into ac networks may impacted the lifespan of the distribution system equipment including isolation transformers and measurement devices and in serious event may cause equipment's malfunction. This paper intents to eliminate dc current offsets in the output currents using a combinational of proportional-integral (PI) and proportional resonance (PR) controls embedded in one inverter unit. Resultant output currents of this method are sinusoidal and clean from dc offset before entering the point of common coupling. This method gives advantages for transformerless option for group of interfacing inverters in the medium-scale solar farm or in arrangement of inverters restricted in a small locale. Moreover, the use of expensive and high-accuracy measurement sensor nor complex transformer can be omitted, whilst indirectly give positive impact to the operational cost of the farm. The simulation verifications proved the usefulness of the proposed method by introducing varying unknown dc offset levels in the phase currents, and a dedicated dc offset suppressor inverter able to successfully eliminate the dc offset to zero. The validity of the proposed method is demonstrated in simulation using MATLAB/Simulink.

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Keywords: DC offset; DC current suppression method; Grid interfacing inverter; PR control

1. Introduction

Power quality is a significant concern for the grid interfacing inverters. The research in the power quality area tends to focus on active harmonic filtering techniques using active power filters and voltage sag compensation using

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series compensators such as the dynamic voltage restorer. The power quality issue associated with the injection of dc current offset into the distributed generation-based inverter is often omitted, regardless the worrying concerns on the negative consequences on the equipment linked to the distribution system. The detrimental effects caused by the injection of dc current into ac system are saturation of distribution transformer's core, the addition of even harmonics along with harmful odd harmonics and extra heating suffer by the equipment. These effects resulted in a reduction of transformer's lifespan, rotating machines and electromagnetic devices. Furthermore, it may compromise the accuracy of the measurements and operation of protective relays; thus, increasing the risk of systems malfunction [1–4].

To tackle the presence of injected dc current into ac distribution network, several methods have been proposed in the literature. An isolation transformer is placed at the output of the inverter to stop the dc current from entering the ac network by electrical isolation [1,5]. However, this transformer is bulky, heavy and expensive. This approach is unpopular to be applied for grid-interfacing inverter in large solar farm. Therefore, the alternative of opted transformerless systems become desirable. From [5], the transformerless photovoltaic inverter system is claimed to reduce the overall system costs by 25% and improve system efficiency by 2% as compared to that with a transformer. Another passive method is using dc/ac capacitors to block dc current from entering the ac grid. For instance, the authors in [6] present a transformerless single-phase half-bridge inverter with the neutral connected to the supply mid-point (dc node formed by connection of two dc side capacitors in series). However, this approach is not readily extendable to three-phase inverter systems. Alternatively in [5], an ac capacitor is placed in series with the grid to serve similar function. However, this passive method may prone to excite the resonance at the ac grid and may possibly magnify the harmonic current. This significantly affect the output waveform quality and deteriorate overall system stability.

The authors in [7,8] proposes an active method that enable two functions which are to detect and minimize the dc current offset in an H-bridge inverter. This method assumes a voltage transformer with 1:1 turn ratio, and the dc offset appears across an RC capacitor circuit as shown in Fig. 1(a). The dc offset is fed into a PI controller where this controller eliminates the amount of dc offset in the circuit. Although simulation results have shown that the dc offset is eliminated, no experimentation is presented to substantiate this method. Refs. [4] studied and verified the method introduced in [8], and a mathematical model-based controller with experimental validation is presented. Another active method was introduced in [2,8–12] for a transformerless full-bridge inverter that compensates the dc voltage in the inverter output, presuming it to be proportional to the dc current offsets appears in the inverter output currents is shown in Fig. 1(b). A magnetic circuit using a low power toroidal transformer is acted as the dc offset sensor connected across the inverter terminals. When a dc voltage exists at the inverter output and detect by the dc sensor, a distortion is resulted in the reactor current and the dc compensation strategy is activated to eliminate the amount of dc offset. The experimental results show that this proposed strategy excellent in minimizing dc current to less than 5 mA for an injected grid current of 8 A_{rms}, which is within IEEE standard limit [2,13].

Ref. [6] proposes an auto-calibrating dc compensation technique, where a current transducer is inserted between the dc link capacitor and inverter phase legs to measure and limit the dc current. This calibration technique is based on the switching state of the inverter. The experimental results show this proposed technique is able to limit the dc current component to less than 8.6 mA for a 10 A_{rms} fundamental current in the inverter output. However, the reliance of this method on measurement of discontinuous input dc current may raise questions regarding its credibility, and bandwidth of the current measurements employed. In [1,6], Fig. 1(c) uses two dc-link current sensors to minimize dc offset components in three-level half-bridge inverter circuit. From this method, the dc current offset is successfully being limited to 7 mA in 5 A_{rms} output current. Nonetheless, the claimed success of the discussed methods is restricted due to the problematic discontinuous currents current sensors may experience during the inverter operation.

In this work, an active and simple dc current offset suppression method using PI control is embedded in a designated inverter (at least one inverter) to perform such function. The level of dc offsets are canceled and eliminated using the proposed control system. The key highlight of the proposed method is to reduce the dependency of high-accuracy measurement equipment which are very costly nor the use of complex transformer. It also allows transformerless option of group of interfacing inverters and only uses one power transformer for galvanic isolation at point of common coupling (PCC).

2. DC offset suppression method of grid-interfacing inverters

A dc offset suppression method for grid-interfacing inverters features a simple and viable approach to be applied in medium-scale solar farms or inverters restricted in a small locale [14]. Fig. 2 shows the typical connection

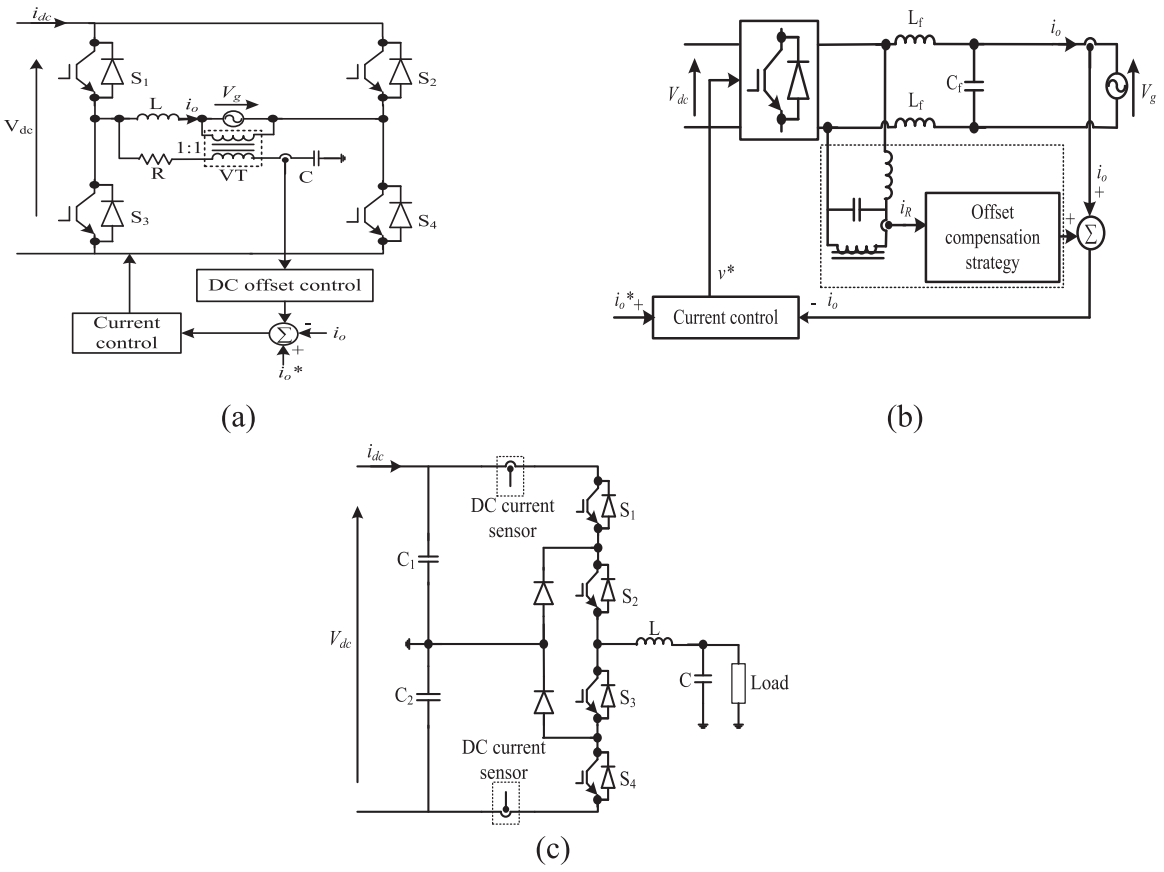


Fig. 1. (a) DC offset current minimizing loop with a voltage transformer (VT) [3,4,13], (b) DC compensation strategy with dc sensor (low power toroidal transformer) [2,10] and (c) dc offset compensation using two dc current sensors for three-level inverter [1,6].

between grid-interfacing inverters with one inverter that acted as the dc offset suppression unit in a solar farm. In this method, a minimum of one inverter unit is dedicated to perform the suppression of dc current offset along with its basic active power injection to ac network. The dedicated unit is functioned to suppress the net dc offset that may exist in the whole connection system to almost zero upon entering the isolation transformer, thus avoiding saturation possibility of the ac transformer as shown in Fig. 2.

Referring to Fig. 2, let say the phase current 'a' with amount of dc offsets in inverter unit 1 is displayed:

$$i_a = I_{dc} + I_m \sin(\omega t + \varphi) \tag{1}$$

where I_{dc} is the level of dc offsets, I_m represents mean current per phase; φ is phase angle (radians); and ω is the frequency measured in radian/seconds.

Mean phase 'a' current can be expanded as:

$$\tilde{i}_a = \frac{1}{T}\sum_{k=0}^{N} i_a(k\omega T_s) = \frac{1}{T}\int_0^T i_a(\omega t)dt = \frac{1}{2\pi}\int_0^{2\pi} [I_{dc} + I_m \sin(\omega t + \varphi)]\, d\omega t = I_{dc} \tag{2}$$

In Eq. (2), T_s is the sampling period and N is the number of samples per fundamental period, T. The mean phase current is computed separately. To create the opposite dc current that oppose the present amount of offsets in Eq. (1), the dc offset with same magnitude yet opposite polarity is injected into the individual modulating signal

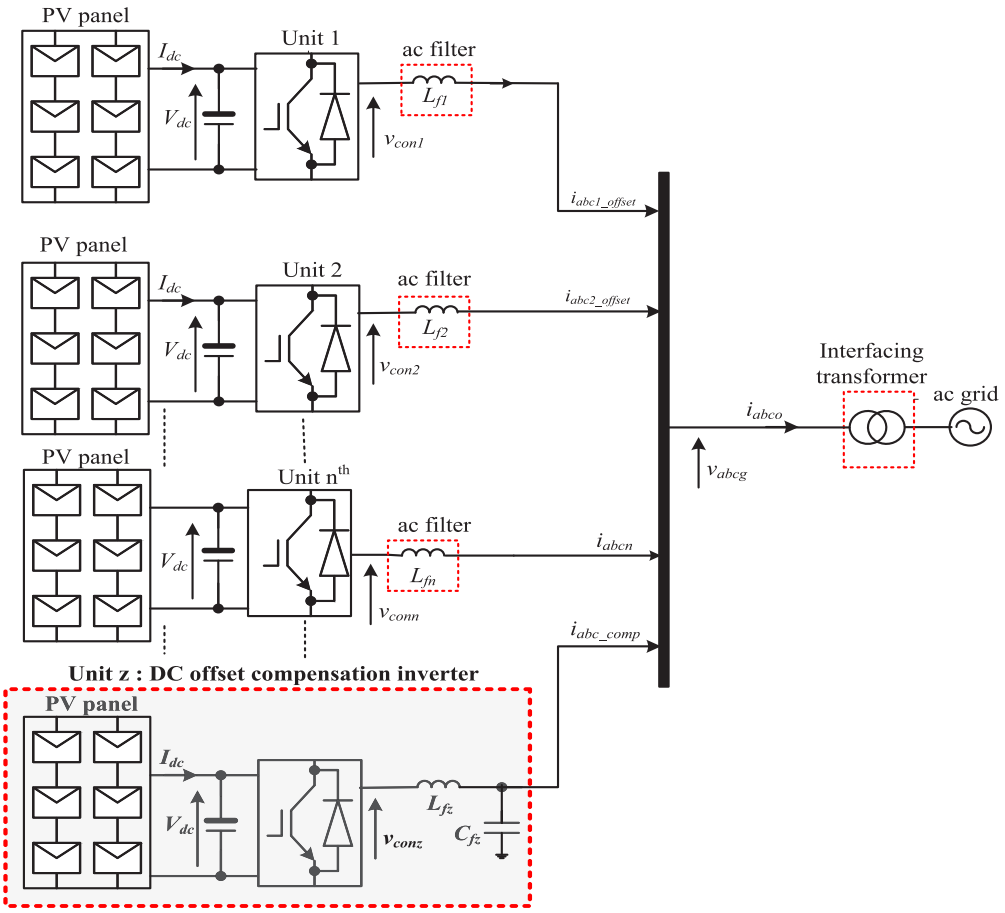


Fig. 2. Connection of grid-interfacing system with one dedicated dc offset inverter unit (Unit z).

of unit z. This is attained from the PI control as in (3):

$$u_{dc\_abc} = k_{pdc}\left(I^*_{dc} - I_{dc\_abc}\right) + k_{idc}\int\left(I^*_{dc} - I_{dc\_abc}\right)dt \tag{3}$$

where I_{dc_abc} is a three-phases dc offset vectors.

The PR control in dedicated inverter (Unit z) is controlling the fundamental current used for the output power transfer into the ac network. The transfer function of PR control is expressed as:

$$y = k_p e + k_i \frac{es}{s^2 + \omega_o^2} \tag{4}$$

where k_p is the proportional gain, k_i is the integral gain, $e = \tilde{i}^*_{abc} - \tilde{i}_{abc}$ is the error signal between the measured ac currents and the corresponding references. ω_o defined as angular frequency.

Forward Euler method is used to discretize the transfer function of PR control in Eq. (4). The state-space equations for the inverter are as follows:

$$\tilde{y}(s) = \tilde{y}_1(s) + \tilde{y}_2(s) \tag{5}$$

$$\tilde{y}_1(s) = k_p e(s) = k_p\left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s)\right) \tag{6}$$

$$\tilde{y}_2(s) = k_i \frac{s}{s^2 + \omega_0^2} e(s) = k_i \frac{1}{s + \frac{\omega_0^2}{s}} \left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s) \right) \tag{7}$$

Rewrite Eq. (7) becomes:

$$s\tilde{y}_2(s) + \frac{1}{s}\omega_0^2 \tilde{y}_2(s) = k_i \left(\tilde{i}^*_{abc}(s) - \tilde{i}_{abc}(s) \right) \tag{8}$$

With change of variable, $\tilde{y}_3(s) = \frac{1}{s}\tilde{y}_2(s)$, the first-order differential equations (9) to (11) explain the PR control is suitable to be integrated in the state-space model for control function. (12) describes the resultant when Eq. (9) + $\tilde{y}_2$ is substituted into inverter ac-side dynamic equation considering only fundamental voltages and currents.

$$\tilde{y}_1(t) = k_p \left(\tilde{i}^*_{abc}(t) - \tilde{i}_{abc}(t) \right) \tag{9}$$

$$\frac{d\tilde{y}_2(t)}{dt} + \tilde{y}_3(t) = k_i \left(\tilde{i}^*_{abc}(t) - \tilde{i}_{abc}(t) \right) \tag{10}$$

$$\frac{d\tilde{y}_3(t)}{dt} = \omega_0^2 \tilde{y}_2(t) \tag{11}$$

$$\frac{d\tilde{i}_{abc}}{dt} = -\frac{(R_f + k_p)}{L_f}\tilde{i}_{abc} + \frac{1}{L_f}\tilde{y}_2 + \frac{k_p}{L_f}\tilde{i}^*_{abc} \tag{12}$$

Differential equations (10), (11) and (12) are combined into a state space equation for PR controller gain selections. The inverter internal dynamics are treated by the passive components:

$$\frac{d}{dt}\begin{bmatrix} \tilde{i}_{abc} \\ \tilde{y}_2 \\ \tilde{y}_3 \end{bmatrix} = \begin{bmatrix} -\frac{(R_f + k_p)}{L_f} & \frac{1}{L_f} & 0 \\ -k_i & 0 & -1 \\ 0 & \omega_0^2 & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_{abc} \\ \tilde{y}_2 \\ \tilde{y}_3 \end{bmatrix} + \begin{bmatrix} \frac{k_p}{L_f} \\ k_i \\ 0 \end{bmatrix} \tilde{i}^*_{abc} \tag{13}$$

Fig. 3 presents the overall control system of the dedicated inverter (Unit z) that acted as dc offset suppression inverter. The fundamental current and dc offset are controlled independently as described and shown in Fig. 3.

3. Result verification of the proposed DC current suppression method

A test system of two grid-interfacing inverters, namely inverter 1 (unit 1) and inverter 2 (unit z) as shown in Fig. 3 are exploited in validating the feasibility of the dc offset suppression method. Inverter 1 (unit 1) is injecting power into the ac grid and contain certain level of dc offset in its output currents whilst inverter 2 (unit z) serves as the dc offset suppressor. The unknown amount of dc offset is injected in the phase current of unit 1 is achieved by inserting the offset current into the modulating signals generated in PR control as represented in Fig. 3. The offset current are then extricated as the feedback signal to inverter 2 (unit z)'s dc offset suppression control system. The dc control suppresses the offset components in the output currents to zero, leaving a relatively clean output currents entering the ac network. Table 1 lists the parameter used in this test system where inverter 1 is injecting power into the grid with certain level of polluted (dc offset) current while inverter 2 is functioned to eliminate the polluted current injected by inverter 1.

The simulation waveforms of the proposed method are presented in Fig. 4 where the reference current of inverter 1 (unit 1), i^*_{abc1} fixed at 2 A_{peak}. Using MATLAB/Simulink as the simulation tool for verification, Fig. 4(a) shows the amount of offsets being added to the modulating signals of unit 1 output phase currents (*abc)* are 5% (offset A), 10% (offset B) and −15% (offset C) respectively. The modulating signals in unit 1 with the addition of the offsets as in Fig. 4(a) is shown in Fig. 4(b). The superimposed waveforms of phase currents a, b, and c of unit 1 and unit z can be viewed in Fig. 4(c) to (e). The proposed dc suppressor inverter (unit z) contradicts the dc offset in i_{abc1} by generating similar magnitude yet opposite displacement angle as in i_{bac2}. The modulating signals of unit z(opposite counter magnitude as in Fig. 4(b)) are shown in Fig. 4(f). By adding these signals ($i_{abco} = i_{abc1} + i_{abc2}$) of Fig. 4(b) and (f), Fig. 4(g) shows the resultant phase currents which are clean from dc offsets, contain only the sinusoidal fundamental currents and follows the IEEE 929–2000 limit before entering the PCC. Finally, the grid phase voltages of 155 V_{peak} (110 V_{rms}) maintained sinusoidal with no dc offsets are represented in Fig. 4(g).

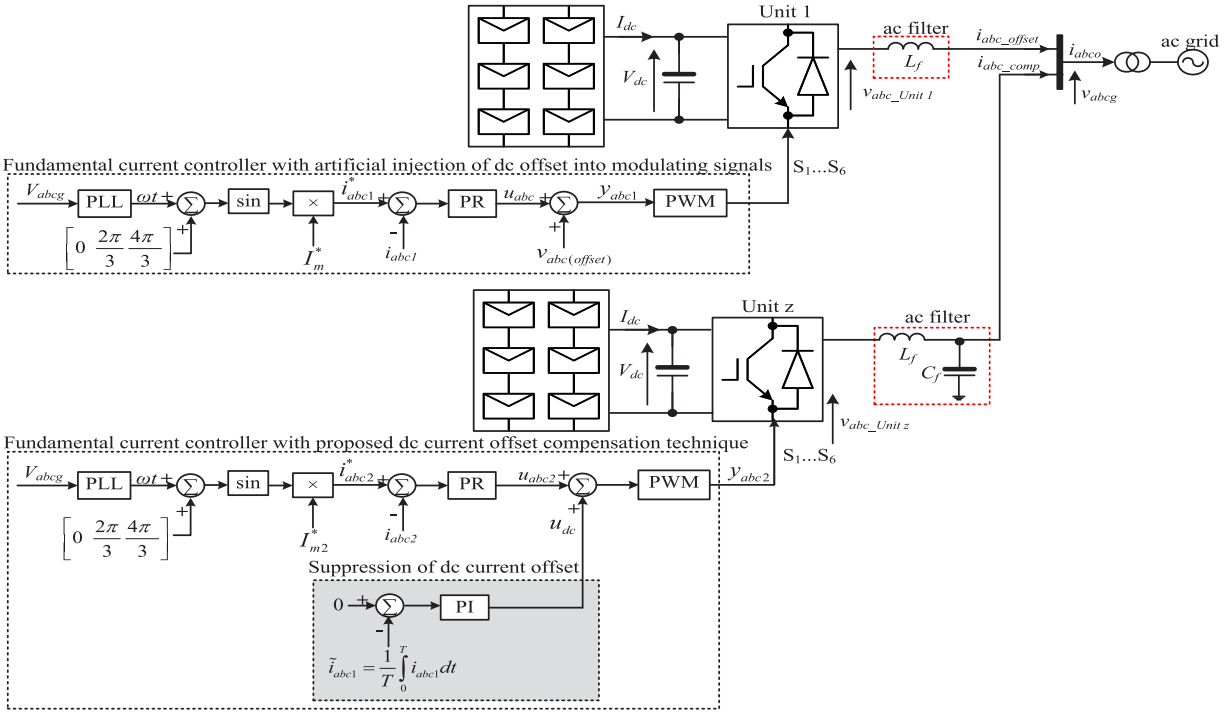


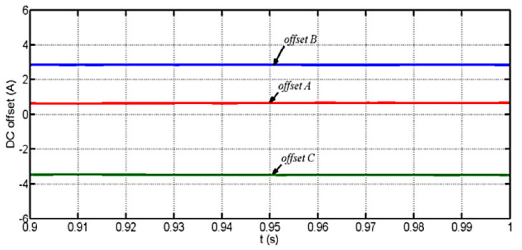
Fig. 3. Control system of the proposed dc current offset method consisting of inverter 1 (Unit 1) with certain level of dc offset and inverter 2 (Unit z) as dc offset suppression inverter.

Table 1. List of parameters used in the test system.

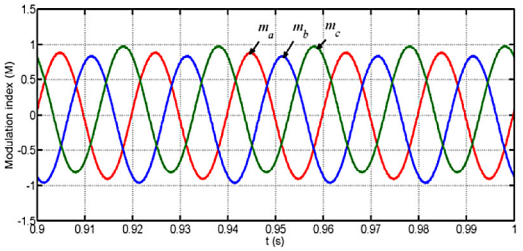
Parameters	Inverter 1	Inverter 2
	Values	
DC-link voltage, V_{dc}	200 V	200 V
Rated power, S	1000 VA	1000 VA
Switching frequency, f_{sw}	2100 Hz	2100 Hz
Filter inductor, L_f	20 mH	10 mH
Filter capacitor, C_f	–	70 μF
Proportional gain of PR control, K_p	4	4
Integral gain of PR control, K_i	1200	900
Proportional gain of PI (inverter 2), K_p		0.8
Integral gain of PI (inverter 2), K_i		120

4. Conclusion

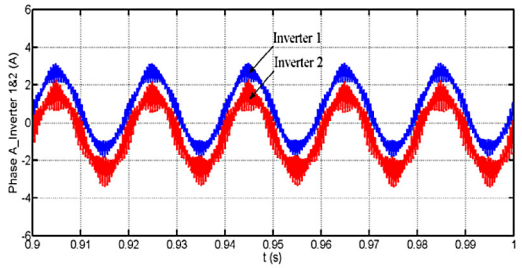
This paper presents a simple and viable dc current offset suppression method that employed PR control to eliminate dc offset to zero while PI control is used to perform the basic function of exchanging active and reactive powers into the ac grid. A minimum of one inverter unit is capable in performing the dedicated function in eliminating the dc offset components by introducing counter modulating signals with similar magnitude to cancel out the polluted output currents suffers by the grid-interfacing inverters in PR control mode. The simulation results proved the feasibility of the proposed method with injection of unknown magnitude of dc offsets. The features



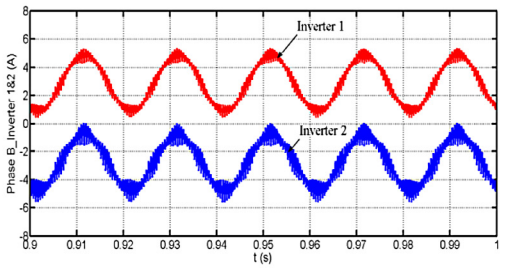
(a) DC offset components (offset A, offset B and offset C) in unit 1



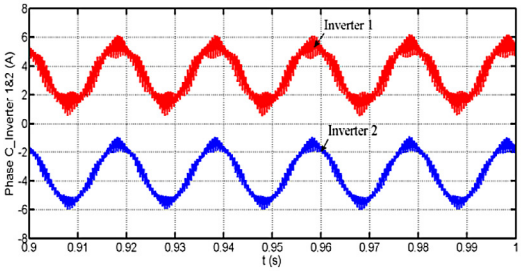
(b) Signals from modulator of unit 1 with the injected offsets (m_a, m_b and m_c)



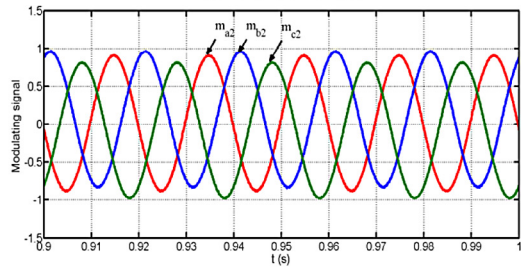
(c) Superimpose of phase current for inverter 1(unit 1) and inverter 2(unit z) with offset A



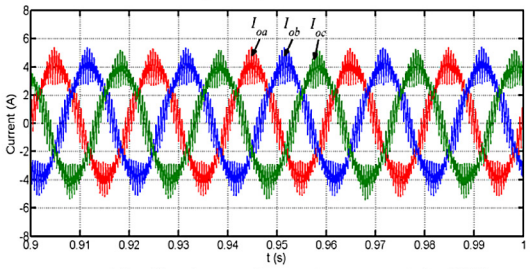
(d) Superimposed of phase current for inverter 1(unit 1) and inverter 2(unit z) with offset B



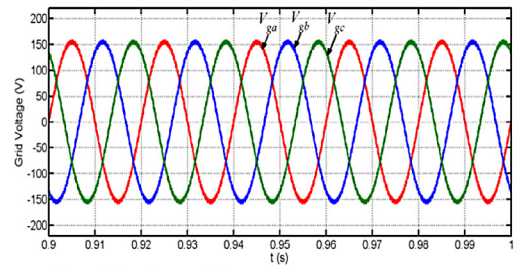
(e) Superimpose of phase current for inverter 1(unit 1) and inverter 2 (unit z) with offset C



(f) Opposite magnitude counter of signals from modulator of unit z



(g) Fundamental output currents at the PCC



(h) AC voltage at the grid

Fig. 4. Verification results display inverter 1 (unit 1) with certain level of dc current offset in the output currents whilst inverter 2 (unit z) suppress the offsets using the designated control system.

of this method are independence on the expensive and high-precision current measurement sensors nor complex transformers being installed in each individual grid-interfacing inverters in the solar farm. In addition, this method allows transformerless option of interfacing inverters in medium-scale solar farms. MATLAB/Simulink is used to confirm the validity of the dc offset suppression method.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Syahrul Ashikin Azmi reports financial support was provided by Malaysia Ministry of Higher Education.

Data availability

No data was used for the research described in the article.

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References

[1] Omar Ahmed, El-Rfaey Adel, Moussa Mona Fouad, Dessouky Yasser Gaber. Review of DC offset compensation techniques for grid connected inverters. Int J Power Electron Drive Syst (IJPEDS) 2018;9(2):478–94.
[2] Buticchi G, Lorenzani E, Franceschini G. A DC offset current compensation strategy in transformerless grid-connected power converters. IEEE Trans Power Deliv 2011;26(4):2743–51.
[3] Liu B, et al. A simple approach to reject DC offset for single-phase synchronous reference frame PLL in grid-tied converters. IEEE Access 2020;8:112297–308. http://dx.doi.org/10.1109/ACCESS.2020.3003009.
[4] Berba F, Atkinson D, Armstrong M. A new approach of prevention of DC current component in transformerless grid-connected PV inverter application. In: Power electronics for distributed generation systems (PEDG), 2014 IEEE 5th international symposium on. 2014, p. 1–7.
[5] Berba F, Atkinson D, Armstrong M. A review of minimisation of output DC current component methods in single-phase grid-connected inverters PV applications. In: 2nd int. symp. environ. friendly energies appl. EFEA 2012. 2012, p. 296–301.
[6] Armstrong M, Atkinson DJ, Johnson CM, Abeyasekera TD. Auto-calibrating dc link current sensing technique for transformerless, grid connected, H-bridge inverter systems. IEEE Trans Power Electron 2006;21(5):1385–93.
[7] Lee JS, Hwang S-H. DC offset error compensation algorithm for PR current control of a single-phase grid-tied inverter. Energies 2018;11(9):2308. http://dx.doi.org/10.3390/en11092308.
[8] Kerekes T, Teodorescu R, Rodríguez P, Vázquez G, Aldabas E. A new high-efficiency single-phase transformerless PV inverter topology. IEEE Trans Ind Electron 2011;58(1):184–91.
[9] Hui Nanmu, Feng Yingying, Han Xiaowei. DC offset elimination method of phase-locked loop based on novel generalized integrator. Energy Rep 2021;7(Supplement 1):30–5.
[10] Blewitt WM, et al. Approach to low-cost prevention of DC injection in transformerless grid connected inverters. IET Power Electron 2010;3(1):111.
[11] Li Yunlu, Wang Dazhi, Ning Yi, Hui Nanmu. DC-offset elimination method for grid synchronisation. Electron Lett 2017;53(5):335–7.
[12] He G, Xu D, Chen M. A novel control strategy of suppressing DC current injection to the grid for single-phase PV inverter. IEEE Trans Power Electron 2015;30(3):1266–74.
[13] Buticchi G, Consolini L, Lorenzani E. Active filter for the removal of the DC current component for single-phase power lines. IEEE Trans Ind Electron 2013;60(10):4403–14.
[14] Azmi SA, Roslan MA, Adam GP, Williams BW. DC current offset compensation technique in grid connected inverters. In: Power electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th international conference on. 2015, p. 617–23.

Further reading

[1] Bowtell L, Ahfock A. Direct current offset controller for transformerless single-phase photovoltaic grid-connected inverters. IET Renew Power Gener 2010;4(5):428–37. http://dx.doi.org/10.1049/iet-rpg.2009.0043.