This is a peer-reviewed, accepted author manuscript of the following research article:
Alassi, A., Feng, Z., Ahmed, K., Syed, M., Egea-Alvarez, A., & Foote, C. (2023). Grid-forming VSM control for black-start applications with experimental PHiL validation. International Journal of Electrical Power & Energy Systems, 151, [109119]. https://doi.org/10.1016/j.ijepes.2023.109119

Grid-forming VSM Control for Black-Start Applications with Experimental PHiL Validation

Abdulrahman Alassi[1,2,*], Zhiwang Feng[2], Khaled Ahmed[2], Mazheruddin Syed[2], Agusti Egea-Alvarez[2], Colin Foote[3]
[1] Iberdrola Innovation Middle East, Doha 210177, Qatar.
[2] Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow G1 1XW, UK.
[3]ScottishPower Energy Networks, Glasgow G2 5AD, UK.
*aalassi@iberdrola.com.

Abstract: The rising penetration of power converters interfaced generation into the electrical grid is leading to a paradigm shift where distributed resources are expected to provide ancillary services. The voltage-source behavior of grid-forming converter (GFC) makes it an attractive black-start provision alternative. This paper thus proposes a modified grid-forming virtual synchronous machine (VSM) control that is tailored for black-start applications. Voltage and power loops in the proposed controller are modified to provide soft energization to mitigate transformers inrush current, in addition to improved voltage support for the restored AC network and a smooth synchronization with neighboring islands or the main grid after a black-start event. The VSM control performance is first validated through simulations. Then, Power Hardware-in-the-Loop (PHiL) technique is used to validate the ability of a hardware GFC equipped with the modified VSM controller to restore a simulated network in a digital real-time simulator (DRTS) platform. Current-type Ideal Transformer Model (I-ITM) interface technique is successfully used in the experiment with time-delay impact compensation in the synchronous dq0 frame. The novel presented PHiL demonstration in this paper paves the way for similar testing of industrial GFCs for black-start and ancillary services provision under flexible network restoration conditions and complexity.

Keywords: Grid-Forming Converter, Virtual Synchronous Machine, Black-Start, Power Hardware-in-the-Loop, Grid Synchronization.

1. Introduction

Black-start is an ancillary service that has been long associated with conventional synchronous generators (SGs) in power networks. The ongoing sharp increment in distributed energy resources (DER) and renewable energy sources (RES) grid integration is requiring a shift in the classical network operation paradigm as the rising penetration of these resources gradually offsets SGs [1]. For instance, solar PV, Type IV wind turbines and battery storage are grid-connected through power electronics-based Voltage Source Converters (VSCs). In the classical grid-following control mode, VSCs rely on following the external grid voltage, which does not exist when the network is blacked out. Instead, the control alternative that is attracting high research and industrial interest is to operate VSCs as grid-forming converters (GFCs), allowing them to establish independent voltage reference, and enabling them to act as anchor sources in black-start [2, 3]. AC networks restoration often involves energizing transformers and cable segments, which may lead to high-magnitude inrush currents. Uncontrolled transformer energization can result into inrush currents of up to 6-10 times the rating [4], whereas VSCs are known to have very limited overcurrent capability [5].

Thus, combining grid-forming control and inrush current mitigation techniques for black-start from GFCs is a necessity. A feasible energization technique that exploits GFCs voltage control flexibility is soft energization, which applies a ramping voltage to mitigate inrush current amplitude, and has recently been proposed and utilized in different works in the literature [6-8]. Applying soft energization should utilize an adequate voltage ramp-duration, which is influenced by factors such as network impedance and transformers residual flux [9].

Establishing an electrical island during black-start may also involve load pick-up between the GFC and the point of common coupling (PCC). Distant loads pickup in island mode can lead to measurable voltage drops. Voltage support capability at the PCC is thus important to sustain the rated voltage. When present, transformers On-Load-Tap-Changers (OLTC) can participate in the required voltage support [10, 11]. That said, the grid-forming control may also be adjusted to provide voltage support through reactive power injection. Finally, synchronizing the restored island is also an important black-start step to group different neighboring electrical islands and/or to achieve synchronized operation with the main grid. This can be implemented through setting a reference frequency that is slightly above or below the nominal grid frequency, creating a phase drift between both voltage phases and leading to eventual crossing between the phases. However, this technique is classically prone to delays and mismatches that may lead to measurable variations at the closing instant [12]. Thus, considering techniques that achieve steady-state phase error elimination prior to synchronization facilitates the seamless grid-connection process, especially when the synchronizing voltage measurements are available.

Several grid-forming control techniques are introduced in the literature, with different levels of complexity and industrial implementation maturity. Droop control is a commonly used technique with grid-forming capabilities [13], and shares many similarities with the power synchronizing control (PSC) [14]. Droop is widely used in research papers tackling grid-forming control due to its simplicity and effectiveness. Matching GFC control is another emerging technique that aims to control the converter frequency through DC link voltage variations [15]. That said, this technique is in the research stages. Virtual Synchronous Machine (VSM) control is gaining more traction in research and industry as it mimics synchronous generators capabilities through relatable parameters such as virtual inertia and virtual damping [16]. Different variations of VSM exist in the literature, including the synchronverter reported in [17]. Other GFC controllers also exist in the literature such as the inducverter [18], where the basic implementation of this controller is based on power reference tracking rather than flexible voltage. GFC controllers have been compared in literature in terms of frequency stability (droop, VSM, dispatchable Virtual Oscillator Control (dVOC) and matching

control) [19], transient stability and inertia impact (droop (with and without power measurement low-pass filters), PSC and VSM) [20], as well as the disturbance performance and soft energization compatibility (droop, PSC, VSM and matching) [21]. The different controllers are observed to be capable of successfully achieving the key functionalities with stability margins that depend on factors such as tuning. Taking this into consideration, the VSM control is selected in this paper as the basis for the modified GFC control for black-start, given its satisfactory performance in the literature, compatibility to soft energization, and the tunable inertia and damping parameters that are relatable to synchronous machines analogy. Overall, the presented overview thus far has identified three key possible improvements to classical grid-forming control that are relevant to black-start, being the incorporation of soft energization for inrush current mitigation, voltage support and grid-synchronization capabilities. These three aspects are investigated in this paper and a modified VSM grid-forming control is proposed.

On the other hand, large-scale testing of grid-forming converters in distribution networks is a challenging task that requires lengthy planning for live trials and disruption of normal services. An attractive alternative to bridge simulations and practical deployments is Power Hardware-in-the-Loop (PHiL). PHiL has been a commonly used technique for testing relays, protection equipment, flywheels, VSCs, and many other use cases [22-26]. Though, applications where the external hardware is used to energize a network simulated in a Digital-Real-Time-Simulator (DRTS) platform have been quite limited. Applying PHiL for black-start use cases implies utilizing a hardware GFC that can be interfaced to a DRTS platform with simulated model of the target network to be energized. PHiL testing configuration exposes the hardware converter to real-world measurement mismatches and delays, while allowing it to interact in real-time with flexible (scaled) real-time simulated networks through a power interface. This allows for testing to be dynamically performed under a wide range of simulated network configurations and power ratings. The power interface in PHiL interconnects between the hardware GFC and the simulated network in the DRTS. Various PHiL power interface techniques are presented in the literature, with the ideal transformer model (ITM) technique being used widely for different applications [27]. Partial-Circuit Duplication (PCD) has also been presented recently for grid-forming converters PHiL in [28]. However, this technique requires installing a physical impedance between the converter and the power interface, which should be precisely replicated inside the DRTS platform. Mismatches in impedance measurement can lead to deviations in PHiL accuracy [29]. This paper thus considers ITM methods for power converters testing.

The objective of this paper is to propose modifications to classical grid-forming controllers that aim to enable the power converters utilization for complete black-start scenarios under different operating conditions. The modified control is an upgrade of an earlier version presented in [30] with expanded capabilities. Then, novel testing alternatives based on PHiL are studied and proposed to validate the technology before field deployment. This enables testing of multiple practical scenarios, such as evaluating the replacement of conventional generation by grid-forming converters in existing network models, and the impact of this replacement on the black-start feasibility. Finally, the contributions of this paper are summarized as below.

- Proposing a modified grid-forming VSM control for black-start applications, with functionalities supporting soft energization, PCC voltage support and smooth grid-synchronization.
- Proposing current-type (I-ITM) interface for PHiL black-start testing of grid-forming converters with time-delay impact compensation, and validating the interface through a practical black-start testing scenario.

The remaining of this paper is structured as follows: Section 2 presents the modified VSM control with the highlighted functionalities. The PHiL analysis is then presented in Section 3, followed by a comprehensive PHiL validation case study in Section 4. A summary of the paper content and recommendations for practical applications are highlighted in the paper conclusions in Section 5.

2. Modified VSM Control

The system configuration for black-start testing relies on several factors such as the number of compatible present DERs and circuits routing. In this paper, it is assumed that a single GFC is connected to an energizing DER (e.g., battery storage) to energize a connected network consisting of transformers, loads and grid synchronization point. The three VSM modifications presented in this paper are: ramping voltage reference tracking (soft-energization), PCC voltage support and grid-synchronization. Classically, VSM is implemented using $P-f$ and $Q-V$ loops as illustrated in Figure 1 [17]. $P-f$ loop is responsible for generating the synchronizing angle, whereas the $Q-V$ loop generates the voltage amplitude reference tracked by the converter. Equation (1) demonstrates the VSM swing equation emulation.

$$J\frac{d\omega}{dt} = \frac{1}{\omega_{ref}}(P_{ref} - P) + D_p(\omega_{ref} - \omega) \quad (1)$$

where J is the virtual inertia, D_p is the virtual damping, ω_{ref} and ω refer to the reference and measured angular frequency, with similar analogy for P. The classical $Q-V$ loop equation for VSM control is shown in (2).

$$|V| = \frac{\omega}{sK_v}(D_q\,\Delta|V_{GFC}| + \Delta Q) \tag{2}$$

where $1/K_v$ is the integrator gain, D_q is the voltage damping, $\Delta|V|$ and ΔQ are voltage and reactive power errors, respectively. In the following subsections, the modified VSM loops for black-start applications are presented.

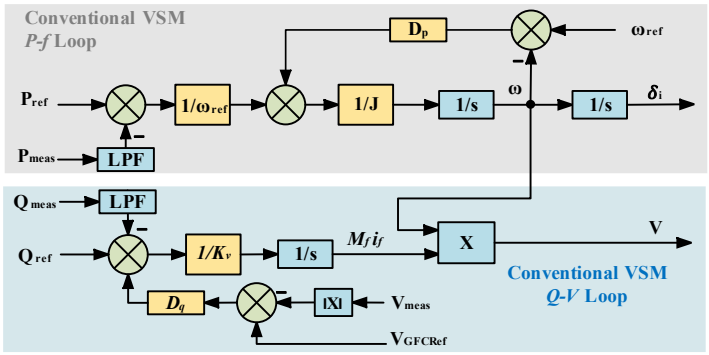


Figure 1: Classical grid-forming VSM control implementation.

2.1. Modified $Q - V$ Loop

The VSM voltage loop is first modified to adjust the constant voltage reference to a ramping value for soft energization compatibility. Although several transformer energization techniques exist in the literature such as the use controlled switching and pre-insertion resistors (PIRs) [31, 32], the application of these techniques requires additional equipment such as point-on-wave relays and breakers with PIRs , unlike soft energization which exploits the VSCs voltage control flexibility without necessarily requiring additional hardware. Soft energization can be applied to a grid-forming converter by defining the control voltage reference as in equation (3).

$$|V_{ref}| = \begin{cases} \frac{t}{T_{ramp}}|V_{nom}| : t \le T_{ramp} \\ |V_{nom}| \quad : t > T_{ramp} \end{cases} \tag{3}$$

where V_{ref} is the VSM reference voltage, V_{nom} is the nominal peak converter voltage in steady-state, t denotes time and T_{ramp} is the ramping time from 0 to 1 pu voltage. Gradual voltage ramp helps mitigating the impact of transformers core saturation and consequently reduces the peak inrush current as a function of the applied ramp-rate. The energized transformer state plays a significant role in the inrush build-up, mainly through the core characteristics and residual flux (ϕ_r). Proper ramp-rate selection is essential for effective inrush current mitigation in the energized network. The authors quantify in [33] the key inrush current influencing factors for soft energization as: a) energizing network impedance, b) transformers residual flux (ϕ_r), c) transformer saturation characteristics and d) ramp-up time (T_{ramp}). The authors also note in [33] that incorporating inner current control loops to the outer grid-forming converter control

is observed to accelerate inrush current mitigation. This also helps mitigating the voltage transients resulting from hard energization with current loops.

On the other hand, the voltage loop can also be modified to support the PCC voltage (e.g., under high load conditions). This can be achieved through integrating an additional control path in the voltage loop with a PI compensator. In case the PCC voltage measurement is not available due to the lack of implemented communication equipment between the converter and the PCC, then local measurements and knowledge of the circuit parameters may be used to produce an approximated value (e.g., through Thevenin's equivalent of the network between the GFC and the PCC) as demonstrated in Section 2.4. The incorporation of voltage compensation path helps in achieving smooth grid-synchronization when the PCC voltage drop is significant such that it may violate voltage amplitude synchronization requirements at the grid-connection point. The additional PI compensating path can be activated only when required (e.g., if the steady-state voltage drop is significant). This compensation is recommended to be used in island mode since voltage control is influenced by the grid after synchronization. This is achieved by the proposed S_{grid} and $S_{V_{comp}}$ switching logic and is combined with simultaneous PI control reset to avoid uncontrolled behavior after disconnection. S_{grid} is 1 in grid-connected mode and 0 otherwise, whereas $S_{V_{comp}}$ is set to 1 when the PCC voltage-support is enabled. Equation (4) illustrates the mathematical expression of the modified VSM voltage loop with unsaturated output. Overvoltage protection is added to provide a limit on the GFC voltage rise due to compensation as illustrated in equation (5).

$$V_{uns} = \frac{\omega}{sK_v}\left(D_q\left(\Delta|V_{GFC}| + S_{V_{comp}}\Delta|V_{PCC}|\left(K_{p_{pcc}} + \frac{K_{i_{pcc}}}{s}\right)\right) + S_{grid}\Delta Q\right) \tag{4}$$

$$V = \begin{cases} V_{sat} & : \quad V_{uns} \geq V_{sat} \\ V_{uns} & : \quad V_{uns} < V_{sat} \end{cases} \tag{5}$$

The voltage saturation aims to protect the converter from steady-state overvoltage that violates its protection limits, and to also avoid overvoltage that may exceed knee-point of connected transformers, which could lead to sustained high magnetizing current. That is, if a significant voltage drop exists in the network due to excessive loading or long, lossy, cables, then VSM voltage compensation may still be provided, but up to a limit that does not violate steady-state energization constraints. The modified VSM voltage loop is illustrated in Figure 2. Severe voltage drops may result in voltage levels below those allowed by the grid code even after VSM compensation. In such scenarios, additional equipment should be considered such as reactive power (VAR) compensators.

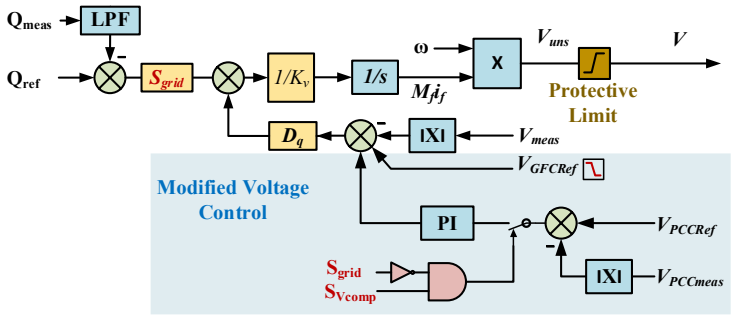


Figure 2: Modified VSM $Q-V$ loop with soft energization and PCC voltage compensation capabilities.

2.2. Modified $P-f$ Loop

Practically, if synchronizing requirements in terms of voltage amplitude $|V|$, frequency (f) and phase angle (δ) are not satisfied and two voltage sources are connected at random points, then large spikes in voltage and current could occur. The worst possible scenario is to synchronize two sources that are 180 degrees out of sync. Typical synchronization requirements based on IEEE standard as reported in [18] are summarized in Table 1.

Table 1: IEEE Grid synchronization requirements in distribution systems.

DER Rating	Δf (Hz)	$\Delta\|V\|$ (%)	$\Delta\delta°$
0 – 500 kVA	0.3	10	20
>500 – 1500 kVA	0.2	5	15
>1500 – 10000 kVA	0.1	3	10

The proposed $P-f$ loop modification can either drive the power loop angle directly [34], or adjust the converter power reference [35]. The latter configuration is used here. In terms of the required inputs to the modified controller, the grid and PCC voltage angles δ_g and δ_{PCC} can be extracted from voltage signals using phase-locked loops (PLLs) as shown in Figure 3. Since synchronization takes place at the PCC, the grid and PCC voltage measurements are required to operate the modified controller, or at least, the error signal between the synchronizing voltage phase angles. The phase angle error can be measured locally at the synchronization point and transmitted to the converter control module. Remote wireless sensing and signals transmission of the voltage measurement may be involved for successful technique implementation, depending on how far the PCC is from the converter. Measurements from the closing relay side can be monitored by the operator to validate the phase error elimination before sending the breaker closing command. The aim is to drive the phase difference between both angles ($\Delta\delta_{g\_PCC}=\delta_g-\delta_{PCC}$) to zero through a controller that outputs a temporary VSM power reference adjustment in island mode. Mathematically, the VSM power loop equation is modified to include a temporary power term P_{sync} that is only activated when synchronization is required to influence δ_i in Figure *3* and match it to the grid angle, resulting in equation (6).

$$J\frac{d\omega}{dt} = \frac{1}{\omega_{ref}}(P_{ref} - P + S_{sync}P_{sync}) + D_p(\omega_{ref} - \omega) \quad (6)$$

S_{sync} is set to 1 only when synchronizing sequence is initiated and remains as 0 otherwise. P_{sync} is a temporary power term, and is the output of synchronizing control that drives δ and f errors to zero through a PI control as in (7).

$$P_{sync} = \frac{\Delta\delta_{g\_pcc}}{2\pi}(k_{psync} + \frac{k_{isync}}{s}) \quad (7)$$

A rate-limiter is used to extract the effective phase difference between both angles to avoid the continuous scatter between -2π and 2π resulting from the PLLs. In addition, a PI integrator reset is activated when the synchronizing control is activated to avoid violent initial P_{sync} variations. The PI output may be limited to the rated converter power value, to avoid the impact of $P_{sync} + P_{ref}$ exceeding the converter rating and leading to higher frequency deviations than the design value. Figure 3 illustrates the modified VSM power loop, showing the P_{sync} estimation steps.

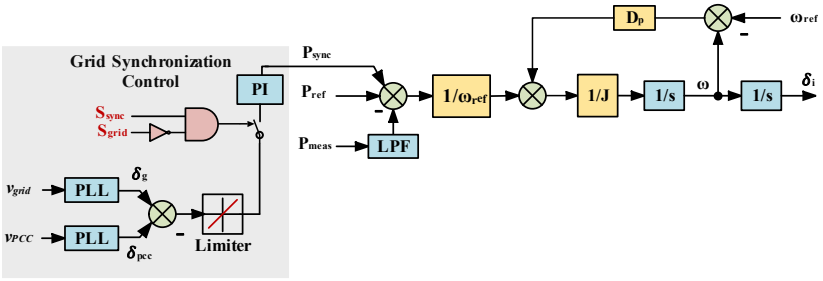


Figure 3: Modified VSM $P-f$ loop with smooth grid-synchronization capabilities.

2.3. Modified VSM Testing

The performance of both voltage and power loops is first validated through the test network presented in Figure 4. The network consists of a GFC (40 MVA, 11 kV), LC filter, a three-phase transformer (11/33 kV, 53 MVA), and a

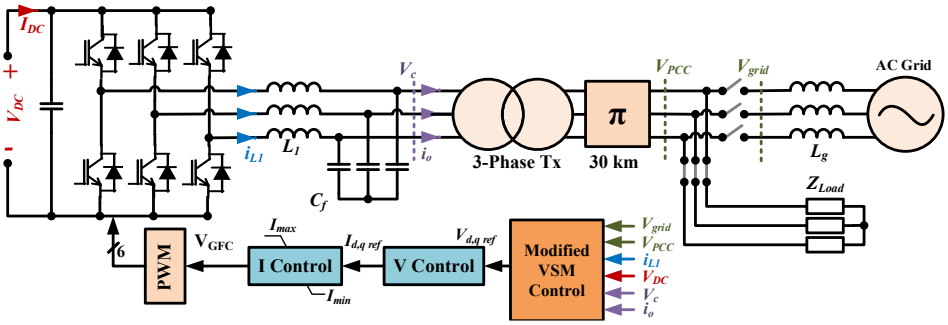


Figure 4: Test network for modified grid-forming VSM testing.

30 km $\pi-section$ with the default MATLAB/Simulink parameters scaled to introduce conditions that allow for voltage controller testing (2.5 times the default resistive impedance and 1.5 times the default inductive impedance).

2.3.1. Soft Energization

The impact of incorporating ramping voltage reference for transformer energization into the modified VSM is demonstrated through an example where the energization of the three-phase transformer with $\phi_r = [0.3, 0, -0.3]$ pu is carried out first through hard (uncontrolled) energization, then by applying a gradual voltage ramp in $T_{ramp} = 3\ s$. The used transformer saturation characteristics are inherited from the default MATLAB/Simulink three-phase transformer model with the saturation-curve knee-point define at $\phi_{sat} = 1.2\ pu$. The VSM control output in this test is used to drive inner voltage and current control loops as shown in the high-level block diagram in Figure *4*. Applying hard energization results into instantaneous high magnitude inrush current exceeding the transformer rating, whereas the gradual voltage ramp results into a significantly less peak inrush value as in Figure 5. This demonstrates the positive impact of applying soft energization, by utilizing the flexible voltage control of grid-forming converters.

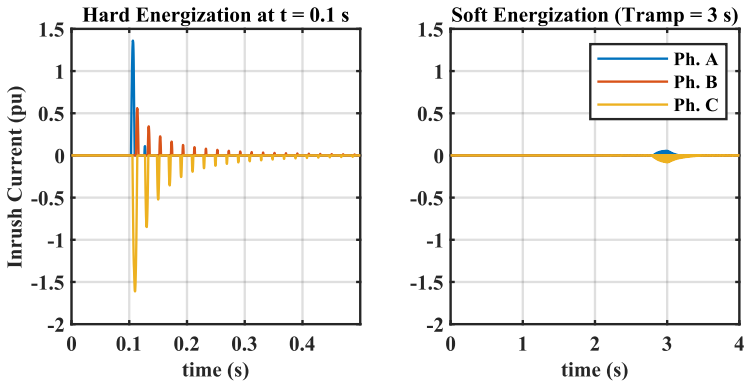


Figure 5: Demonstration of Hard vs. soft transformer energization impact on inrush current.

2.3.2. PCC Voltage Support

In this test, the system initially operates in island mode, and an active 0.5 pu load is connected at the PCC at $t = 2\ s$ as illustrated in Figure 6. This leads to an increase in GFC power output. Evidently, the power falls short of the rated load power due to the reduced voltage at the PCC (0.94 pu). Then, at $t = 2.5\ s$, the PCC voltage compensation path is activated in the VSM voltage loop, leading the PCC voltage to be driven to 1 pu while increasing the internal GFC terminal voltage to 1.07 pu (below the pre-set voltage saturation limit which is set here to 1.1 pu). After voltage compensation, the active power is pumped to its target value around $0.5\ pu$ (plus resistive line and transformer losses). The additional VAR consumption is minimal, and depends on the line reactive impedance and the compensation required to overcome its voltage drop impact and drive the PCC voltage to 1 pu. This example shows the compensation technique effectiveness in correcting PCC voltage deviations, while maintaining transformer and converter limits.

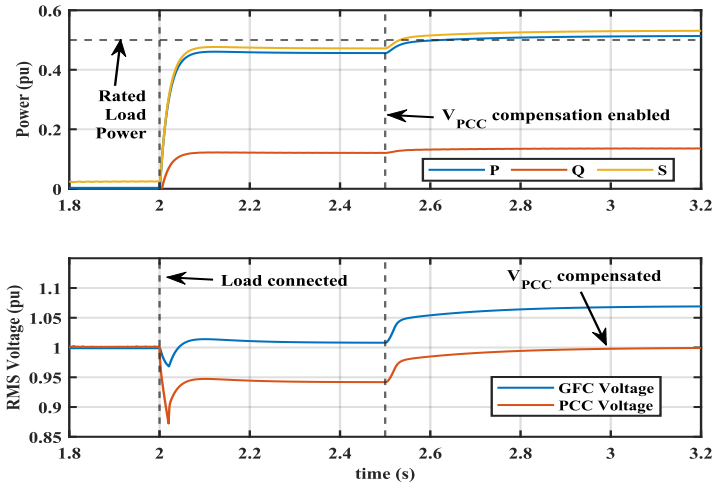


Figure 6: Modified VSM with PCC voltage compensation – test case results with impact on P,Q,S and voltage across the converter output and PCC.

2.3.3. VSM Power Synchronization

The proposed synchronizing control is tested in this subsection to validate its operation. Given the higher power rating of the tested converter (40 MVA) compared to the ratings reported in Table 1, stricter synchronization requirements are adopted. Namely: $\Delta f < 0.1\ Hz$, $\Delta|V|$ (%) < 1%, and $\Delta\delta < 5°$ at the PCC. Synchronizing control PI gains are set to $k_{psync} = 0 \rightarrow 1000$ (in 2 seconds for smooth operation), and $k_{isync} = 1000$. In practice, more relaxed synchronization gains can be used since the control settling time is of a reduced priority. Figure 7 illustrates the synchronizing control simulation results. In this test, the synchronizing control activation signal is received at $t = 4\ s$, but the control is not activated until the next angle error zero crossing. Although this step is not mandatory, it helps minimizing the synchronizing power overshoot. The power reference is set to 20 MW (0.5 pu), and no load is connected in the island mode. Thus, the power loop initially has an error that manifests itself into a continuously changing angle deviation between the converter output voltage and the grid voltage until synchronizing control is activated, as in Figure 7(a). Then, P_{sync} acts to push $\sum P$ in the VSM power loop to zero such that the phase output is constant. This requires that P_{sync} settles at -20 MW (-0.5 pu) to cancel the pre-set reference since the connected load is zero, the closed-loop controller ensures that the steady-state P_{sync} is combined with the instant where the phase error is zero. This is observed in Figure 7(b), and snapshots of phase A grid and PCC voltages at the instant of receiving the synchronizing command, and the instant of grid synchronization at $t = 8\ s$ are shown in Figure 7(c) and Figure 7(d) . Thus, clearly demonstrating the matching phase angle at the synchronization instant.

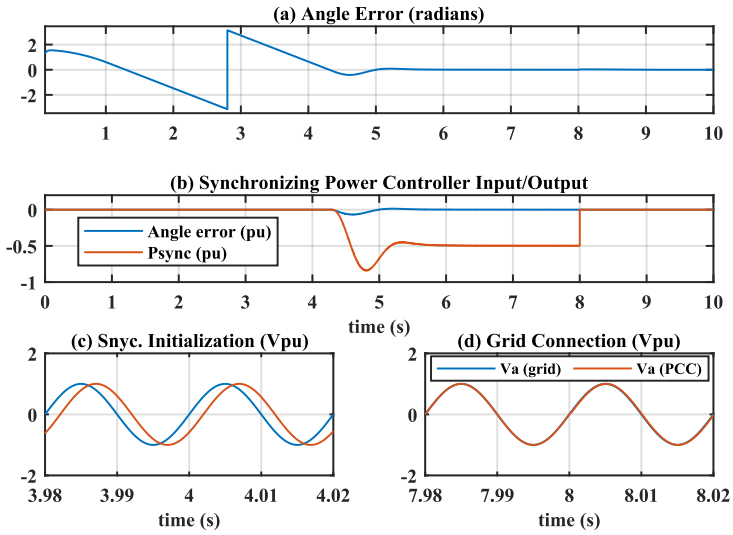
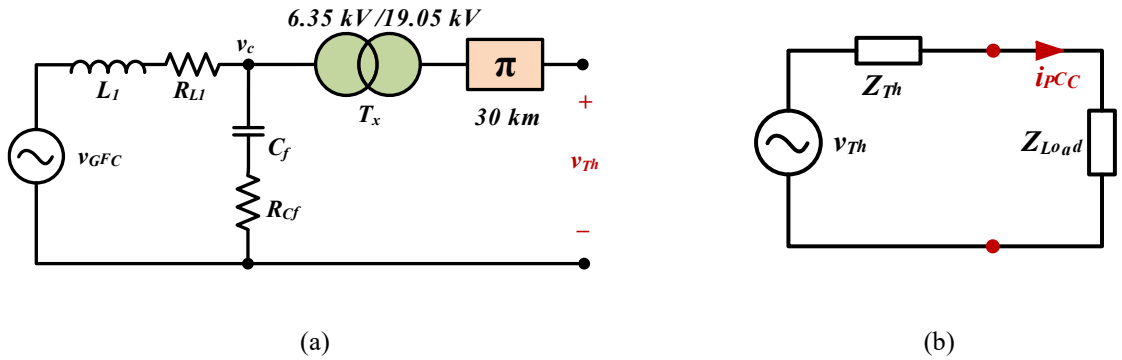


Figure 7: Synchronizing control testing: (a) angle error, (b) synchronizing PI control input/output, (c) phase difference at synchronization command point, (d) phase difference at synchronization.

2.4. Thevenin's based PCC Voltage Estimation Technique

The use of the proposed modified VSM voltage control loop with direct PCC voltage measurement is subject to the availability of this reading. If this is not the case, then an estimation method is proposed for PCC voltage based on local measurements at the converter terminal, in addition to knowledge of the distribution circuit topology between the GFC and the PCC. Such information is assumed to be accurately available for many Distribution System Operators (DSOs). The idea is to calculate the GFC network Thevenin's circuit as seen from the PCC when such calculation is feasible by the network topology, and to estimate the voltage from this equivalent circuit. As an example, the network circuit in Figure 4 can be simplified on a per-phase basis as illustrated in Figure 8a, consisting of the filter, transformer (Tx) and $\pi -$ section line/cable. The Thevenin voltage (v_{Th}) and impedance ($Z_{Th} = R_{Th} + jX_{Th}$) are estimated at the PCC terminals from the equivalent circuit shown in Figure 8b.



(a) (b)

Figure 8: (a) Per-phase simplified circuit of the test network, (b) Thevenin's equivalent circuit.

Then, the PCC current (i_{PCC}) is approximated through multiplying converter output current by the inverse transformer turns ratio (Tx_{ratio}), with similar analogy to (v_{Th}) estimation as below.

$$i_{PCC} \approx \frac{i_{L1}}{Tx_{ratio}} \tag{8}$$

$$v_{Th} \approx v_{GFC}\, Tx_{ratio} \tag{9}$$

Consequently, solving for the PCC voltage from the Thevenin's equivalent circuit in Figure 8b yields the following.

$$v_{PCC} = v_{Th} - i_{pcc}(R_{Th} + jX_{Th}) \tag{10}$$

Equations (8)-(9) are specific the used test network, whereas equation (10) is generic and can be applied to different topologies as it is based on the Thevenin's equivalent voltage and impedance. The estimated voltage can eventually be used to drive the VSM PCC voltage compensator. For instance, the voltage estimation implemented within the controller is depicted in Figure 9 for the used test network. PLLs are used in the voltage estimation method control implementation to extract the angle of voltage and current, which are subtracted to obtain the impedance phase angle.

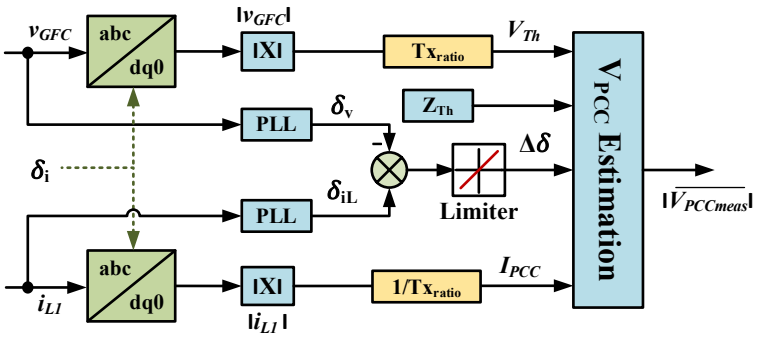


Figure 9: PCC voltage estimation algorithm based on Thevenin's circuit for the used GFC test network.

Finally, the PCC voltage estimation technique for the islanded operation mode is validated through a VSM voltage compensation scenario. As demonstrated in Figure 10, the PCC voltage is compensated to 1 pu in a nearly identical fashion to that obtained through direct voltage measurement.

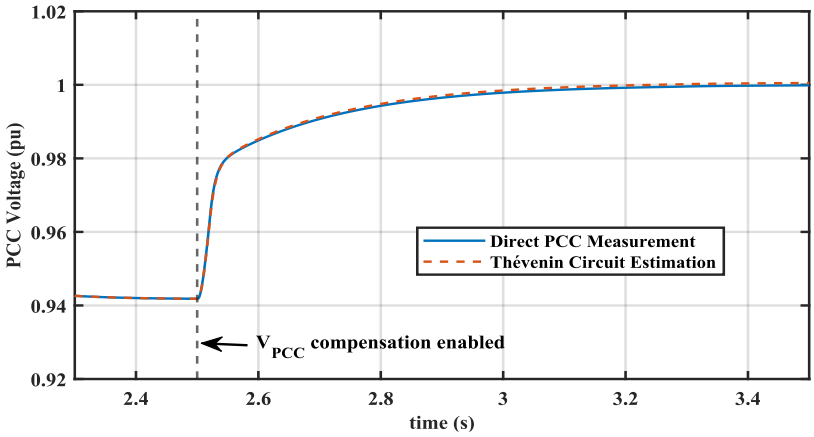


Figure 10: Validation of the Thevenin-based PCC voltage estimation technique.

3. PHiL for GFCs Black-Start Testing

PHiL allows for evaluating the dynamic performance of hardware converters under realistic conditions and in a scaled environment. The physical rating of PHiL experiments is limited by the rating of the physical GFC, in addition to the power amplifier (PA) used to interface the Hardware-under-Test (HuT) to simulated network. ITM interface techniques for PHiL are mainly classified into voltage (V-ITM) and current (I-ITM) types [36]. V-ITM is typically used for grid-following power converters testing [37]. In this configuration, the converter (HuT) acts as a current source and synchronizes to the voltage received from DRTS (grid). However, applying this method in grid-forming converter operating mode implies connecting two devices operating in voltage source mode with potentially unsynchronized voltages. This is more likely to lead to unstable operation as the authors reported in [38]. Instead, using I-ITM bypasses this requirement since the hardware power interface essentially operates as a current source following the hardware GFC voltage signal, and is thus used in this paper as it is deemed more suitable for black-start applications due to its simplicity while maintaining the high accuracy requirement. Figure 11 demonstrates the PA variation between V-ITM and I-ITM for GFC testing.

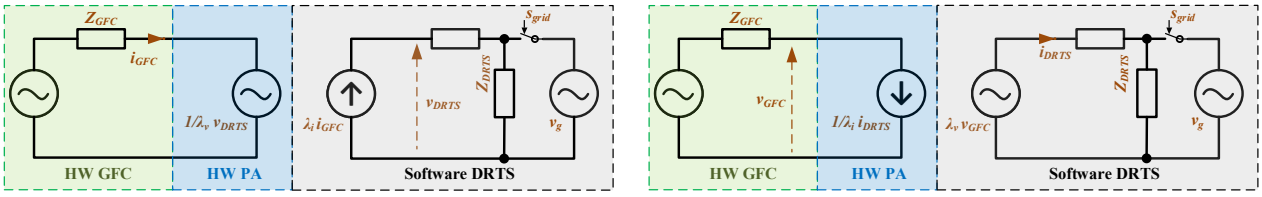


Figure 11: ITM generic implementation for grid-forming converters testing: (a) V-ITM, (b) I-ITM.

3.1. PHiL Scaling Ratios

In the experiments presented in this paper, the VSM control is implemented into a Triphase 90 kVA converter (TP90kVA). Though, the experiments are restricted to 15 kVA since the used switched-mode interface power amplifier (TP15kVA) is rated at this limit. In principle, hardware converters rating is not a restrictive factor to PHiL testing involving MVA-scale simulated networks, and the HuT-PA pair are used to build a proof-of-concept experiment and investigate the feasibility of using hardware GFCs to demonstrate black-start provision through PHiL. To achieve high accuracy, appropriate scaling factors λ should be used for voltage, current and power between the hardware and real-time software domains as shown in equations (11)-(13).

$$\lambda_v = V_{DRTS}/V_{GFC} \tag{11}$$

$$\lambda_i = I_{DRTS}/I_{GFC} \tag{12}$$

$$\lambda_{pq} = \lambda_v \lambda_i \tag{13}$$

The recommended steady-state per-phase voltage for the used hardware is $230\ V_{rms}(325\ V_{peak})$, whereas the simulated network GFC is connected at 11 kV level ($8981\ V_{peak}$). The ratio thus translates to $\lambda_v \approx 27.5$. As a result, the hardware GFC output sent to the DRTS side is multiplied by λ_v before being fed to the simulated network in real-time. On the other hand, the peak TP15kVA current is recommended to be less than 20 A to comply with protection requirements. The peak simulated network power in the DRTS platform has been set to 35 MW, and thus the DRTS current is scaled down by a factor $\lambda_i = 150$.

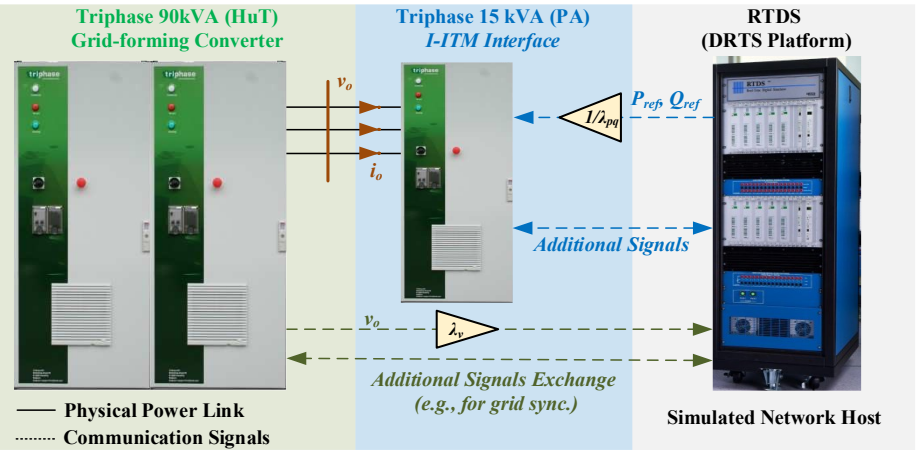


Figure 12: Experimental layout used for PHiL validation of GFCs black-start testing.

Consequently, the power scaling ratio is calculated as 4125 between the hardware HuT-PA pair, and the DRTS simulated network. Figure 12 demonstrates the experimental setup for the conducted PHiL tests. In addition to the

main exchanged parameters (voltage and current/power references), additional signals can be exchanged between hardware and software domains as required by the control. For instance, the synchronizing voltages phase error is sent from the DRTS to the HuT for the modified VSM control operation. The DRTS used in the experiment is the Real-Time Digital Simulator (RTDS) platform, with PB5 cards and RSCAD v5 software.

3.2. Time Delay Impact Compensation

Time delay exists in the HuT-DRTS path when sending the output voltage measurement from the hardware grid-forming converter side to the DRTS platform. Delays also occur in the DRTS-PA path through the exchange of power or current reference from the DRTS to the hardware power amplifier. This also applies to any additional signals required for the control operation (e.g., the synchronization angles error being fed back from the DRTS to the hardware grid-forming converter VSM control). The i_{DRTS} feedback signal from DRTS to PA in I-ITM can be sent as a three-phase sinusoid, which is more sensitive to time-delays and prone to higher accuracy deviations [39]. Alternatively, power references can be shared as scaled P_{ref} and Q_{ref} to the power amplifier, which can then be converted to currents within the PA with minimized delay impact since power references are essentially sent as constants. Additional sources of delay may still exist in the system such as the ones arising from the HuT-DRTS path. Thus, an aggregate delay impact compensation framework is proposed and applied to the DRTS-PA path, with the objective that the scaled active and reactive power measurements in hardware closely match those measured within the DRTS in real-time.

The time delay impact compensation adopted is implemented in the synchronous dq0 frame through manipulating the inverse transformation angle for the measured output voltage as illustrated in Figure 13. The physical GFC output voltage is measured by the power amplifier, operating in I-ITM as a grid-following converter tracking the reference generated by the GFC, as the voltage to be followed. This voltage (v_o), shown in Figure 12, is passed through a PLL to extract its phase angle δ_v, which is used to drive the synchronous frame controller.

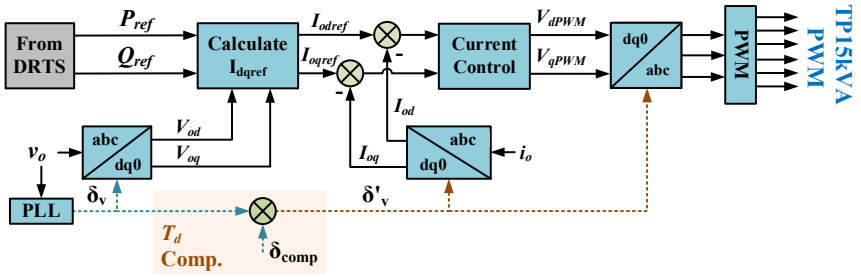


Figure 13: Implemented PHiL time delay compensation for the power amplifier (TP15kVA).

Simultaneously, the active and reactive power references P_{ref} and Q_{ref} are received through the DRTS platform. The GFC output voltage and power references are used to calculate the synchronous frame current references for the PA control as in equations (14)-(15).

$$I_{odref} = \frac{2}{3}\frac{(V_{od}P_{ref}+V_{oq}Q_{ref})}{V_{od}^2+V_{oq}^2} \tag{14}$$

$$I_{oqref} = \frac{2}{3}\frac{(V_{oq}P_{ref}-V_{od}Q_{ref})}{V_{od}^2+V_{oq}^2} \tag{15}$$

These reference currents are then compared to the measured input currents at the PA terminal (GFC output current). Inverse synchronous frame conversion for i_o is driven by the compensated angle δ_v', which is calculated as in (16).

$$\delta_v' = \delta_v + \delta_{comp} \tag{16}$$

where, δ_{comp} is a delay compensating value between 0 and 2π, which is used to adjust the accuracy of the scaled PHiL hardware measured power and to maintain it within acceptable limits against the DRTS power measurements. The PA current direction is recommended to follow the convention illustrated in Figure 12, such that the current entering PA results into positive power (consumed), since the reference P and Q received from the DRTS side follow similar convention. This way, the scaled physical power is injected from the GFC to the PA when P_{ref} is positive.

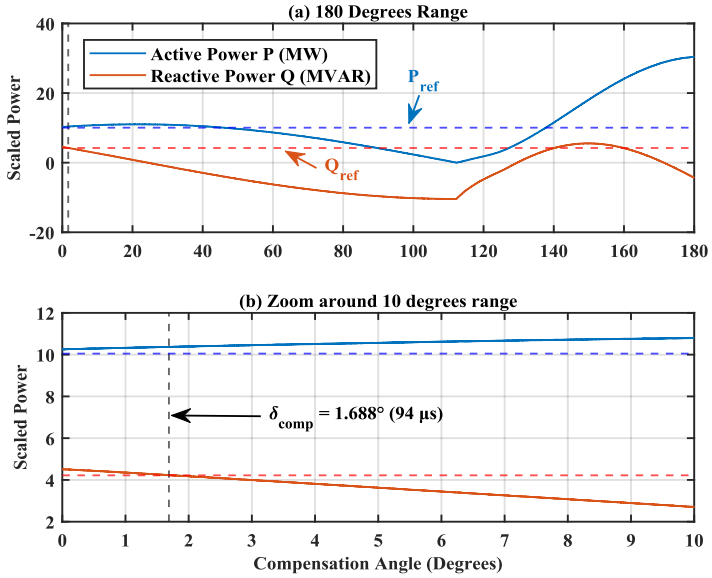


Figure 14: Time delay compensation impact showing: (a) 180-degree compensation range, (b) reduced scale to illustrate the chosen compensating angle.

To demonstrate the impact of time delay and its compensation, an experiment is carried out where δ_{comp} is varied between 0 and 180°. The angle is changed gradually over a period of 360 seconds (i.e., with a slope of 0.5 °/s). The

power references sent from the DRTS side is fixed at $P_{ref} = 10.05\,MW$ and $Q_{ref} = 4.22\,MVAR$. The hardware power (P and Q) are measured from the PA side (multiplied by $\lambda_P = 4125$), and recorded over the full testing range. The experiment results are summarized in Figure 14. For the presented power references, a common compensation point that is in the vicinity of these references is found at $\delta_{comp} = 1.688°$ $(0.0295\,rad)$ which amounts to 94 μs compensation according to (17). This value is thus used for the remaining of the experiments conducted in this paper.

$$T_{d(PA)} = \frac{\delta_{comp(rad)}}{2\pi f} \tag{17}$$

4. PHiL Case Study

The presented case study and the test scenarios in this section aim to validate the modified VSM control use for a complete black-start scenario testing under PHiL configuration using a test simulated network. This includes soft transformer energization, load pickup and grid synchronization. Extension to different network configurations is feasible through the flexibility provided by the simulated nature of the network implemented into the DRTS platform.

4.1. Test Network Definition

The main difference between the PHiL test network and the one presented in Figure 4 is the load connection at the secondary transformer terminals to expand the testing scenarios spectrum. The simulated transformer parameters in the DRTS platform are modified to be closely correlated to reported data in a Scottish distribution network [40]. The network loads here are divided into a main (initially closed) 20 MW load, and a 10 MW disturbance load that is connected post-synchronization to test the control response robustness. The test network is illustrated in Figure 15, showing the external hardware (GFC), power interface and the test network in the DRTS platform (RSCAD/RTDS).

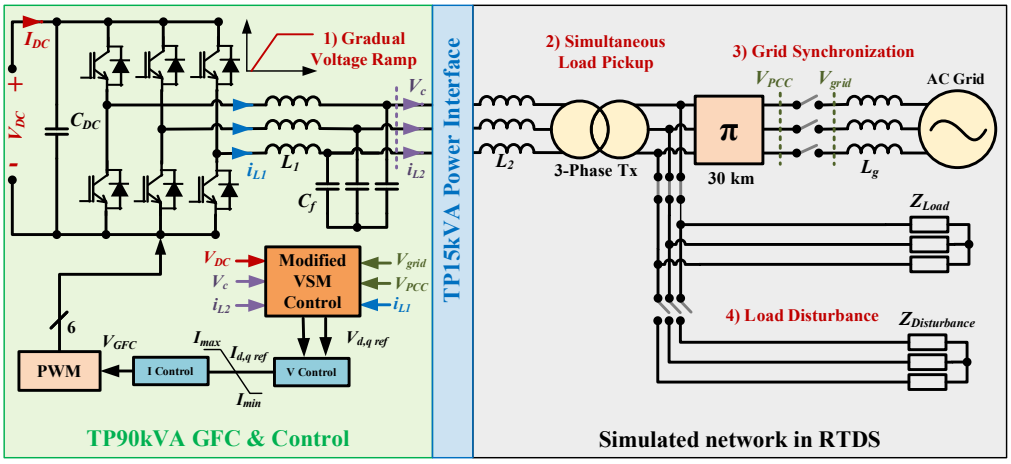


Figure 15: Test network block-diagram used for PHiL black-start experiments.

The modified VSM control utilizes inertia and damping factors that maintain minimum frequency variations at rated power disturbances. The voltage scale $\lambda_v = 27.5$ is applied for the network simulated in RSCAD. The simulation real-time input voltage is scaled up to a base value of 11 kV_{LL} from 400 V_{LL}. An additional inductance is added after the emulated voltage source in the RSCAD model to represent L_2 of an LCL filter, which is considered to improve the PHiL system performance, and its value is calculated as 1 mH (0.1 pu in RTDS/RSCAD). Soft energization technique is used for transformer inrush current mitigation with a ramp duration of 10 seconds. The VSM outer $P-f$ and $Q-V$ loops are interfaced to inner voltage and current control loops in synchronous dq frame for improved current protection. The peak absolute residual flux (ϕ_r) for the energized transformer is 0.25 pu, and thus negligible inrush current is expected against the selected voltage ramp duration, given that the saturation flux $\phi_{sat} = 1.2\ pu$ for the transformer saturation curve [33]. The soft network energization is simultaneous to the main 20 MW load pickup. Key test system parameters are summarized in Table 2. Grid synchronization is then performed using the modified VSM. The PCC voltage phase error is sent from RSCAD/RTDS to Triphase90kVA in real time to drive P_{sync} to the value resulting in zero phase error. Beyond synchronization, the grid-forming VSM continues to operate in voltage-control mode and is capable of reactive power injection/absorption as potential ancillary services.

Table 2: Key test network parameters for PHiL Black-start experiments.

PHiL Interface Parameters			
λ_v	27.5	λ_i	150
Hardware GFC Parameters (TP90kVA)			
DC Voltage	700 V	Switching Frequency	16 kHz
LCL Filter L_1	0.5 mH @ 400 V	LCL Filter C_f	47 µF @ 400 V
AC Voltage	230 V_{rms}	Sampling Time	62.5 µs
GFC Control Parameters (in TP90kVA)			
VSM Loop			
Power Loop D_p	14.28	Virtual Inertia J	0.028
Voltage Loop D_q	306	k_v	5771
Inner Loops PI gains			
k_{pv}	0.2	k_{iv}	1
k_{pi}	0.2	k_{ii}	10
DRTS Simulated Network Parameters			
LCL Filter L_2	1 mH @ 11 kV	Power Base	40 MVA
Transformer Parameters ($\Delta - Y$)			
Power Rating	53 MVA	Voltage Ratio V_o/V_i	33/11 kv
Knee-Voltage	1.25 pu	L_{sat}	0.265 pu
Leakage Inductance	0.1 pu	ϕ_r	[0.25, -0.1, -0.15] pu
Transmission Line Parameters ($\pi - model$)			
(R, L, C) per km	12.73 $m\Omega$, 1.07 mH, 9.95 nF	Length	30 km
Network Loads			
Main Load	20 MW	Disturbance Load	10 MW
Grid Parameters (33 kV_{LL})			
Short-Circuit Power	500 MVA	X/R Ratio	14.5

4.2. Experimental Test Results

The results presented in this section show a combination of hardware and software results obtained from the black-start experiment to showcase the synergy between both domains, which leads to the hardware GFC being tested under similar dynamic conditions to those present in the real-time simulation. The main events in the simulated black-start scenario are summarized in Table 3.

Table 3: Key test network parameters for PHiL black-start experiments.

Event	time (s)	Event	time (s)
$t = T_{ramp}$	10	P_{ref} change (35 to 10 MW)	36.75
Grid-synchronization	22.75	P_{ref} change (10 to 20 MW)	43.75
P_{ref} change (20 to 35 MW)	29.75	Load Disturbance (20 to 30 MW)	48.75

Initially, the grid-forming VSM implemented in TP90kVA unit is activated with a 10 seconds voltage ramp between 0 and 325 V_{peak}. This voltage is sensed and sent to RTDS and scaled up by 27.5 to represent 8981 V_{peak} (11 kV V_{LL} equivalent) in real-time. The scaled-up voltage is fed into the simulation network to energize the 53 MVA transformer, line and 20 MW load. Then the restored island is synchronized to the grid after the angle error is driven to zero, followed by power reference variation and a load disturbance. Figure 16 demonstrates the matching trends between the simulation in RSCAD/RTDS and the scaled down version in TP90kVA (GFC).

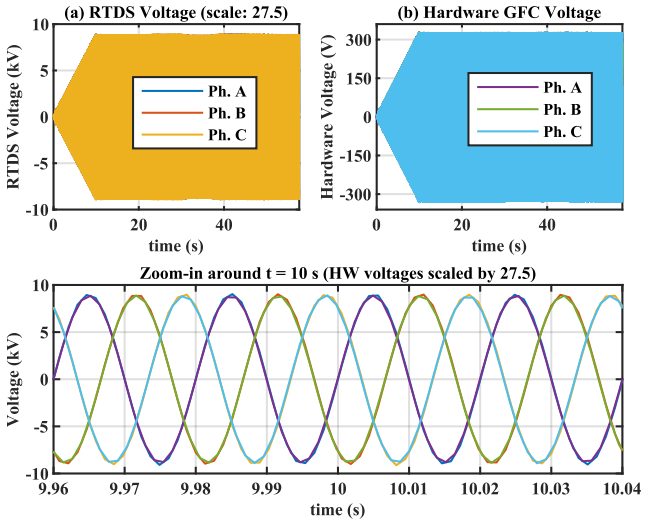


Figure 16: Simulated (RTDS) and hardware (GFC) output voltage measurements: (a) RTDS voltage, (b) Hardware GFC output voltage, (c) RTDS and scaled-up hardware voltages around $t = 10\ s$.

The transformer energization is also observed to result into minimal inrush. The peak transformer $\phi_r = 0.25\ pu$, combined with the soft ramp duration of 10 seconds, lead to nearly complete inrush current elimination. That said, higher residual flux combination would have generated a higher peak inrush that could still be mitigated by adapting

the ramp-up time T_{ramp} through soft energization. The flux and inrush currents for the studied scenario from RSCAD/RTDS are demonstrated in Figure 17.

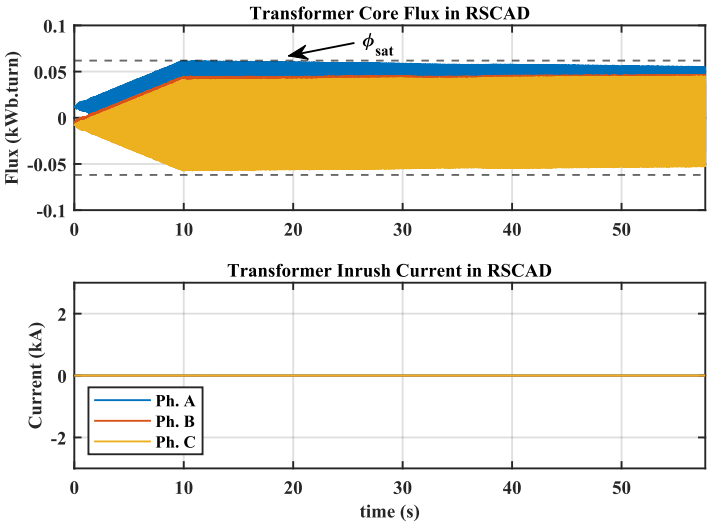


Figure 17: Transformer flux and magnetizing current during PHiL simulated network energization.

As for the grid-synchronization, the control is activated during the ramp to accelerate the convergence for improved results visualization. Initially, a variable phase-shift is observed, and as the synchronizing PI control tracks the zero-angle point error, the phase-angle between PCC and grid voltages in the simulated DRTS network approaches zero as shown in Figure 18. Phase A voltages at both sides of the synchronizing circuit breaker are shown in Figure 18(b) around the moment of synchronization $t = 22.75\ s$.

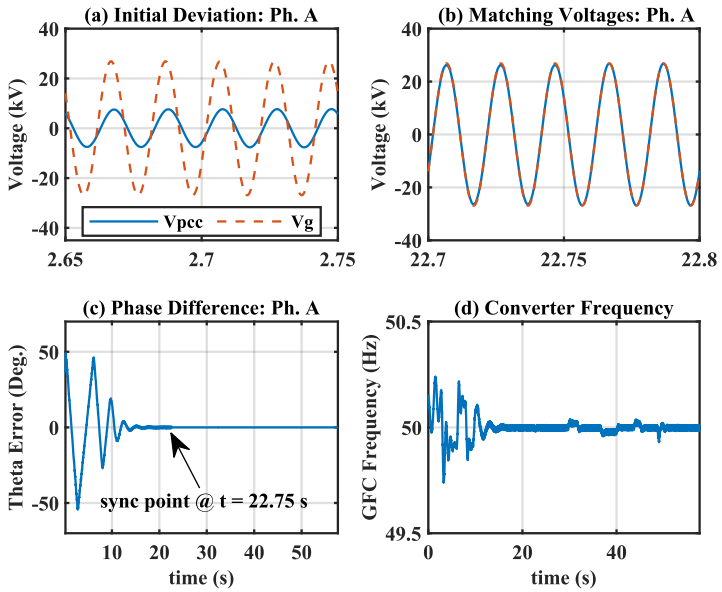


Figure 18: Modified VSM synchronizing control operation: (a) initial phase deviation, (b) sync. voltages at the synchronization instant, (c) instantaneous phase error, (d) GFC frequency.

The phase error between both voltages throughout the synchronization process is demonstrated in Figure 18(c). The converter frequency trace is shown in Figure 18(d), showing slight variations around the steady 50 Hz points during the ramp and synchronizing control action, and small changes as a result of the power reference adjustments. The converter output frequency remains within an acceptable band throughout the experiment.

After synchronization, the VSM control power reference tracking mode is activated. Initially, the VSM power reference is set to 20 MW, leading to minimum active power setpoint variation compared to the pre-synchronization status. After a 7 seconds period, the power reference is ramped from 20 MW to 35 MW with a 7.5 MW/s slope. The control tracks the new setpoint smoothly by changing the export current as illustrated in Figure 19. To further demonstrate the setpoint tracking capability in PHiL, two additional events are simulated: first, by ramping down the power reference to 10 MW with a similar slope, then by increasing it again to 20 MW, with 7 s time interval between each variation. Finally, a load disturbance is applied at t = 48.75 s where an additional 10 MW load is connected. The aggregate impact of the post-synchronization setpoint variations and the load disturbance is shown in Figure 19, demonstrating the real-time synergy between the system behavior in software and hardware GFC.

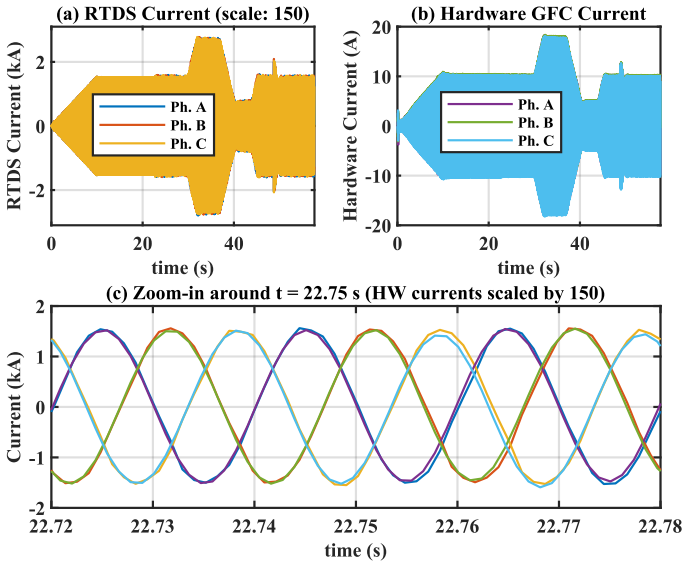


Figure 19: Simulated (RTDS) and hardware (GFC) output current measurements: (a) RSCAD/RTDS current, (b) Hardware GFC current, (c) RTDS and scaled-up hardware current.

The software vs. hardware active and reactive power tracking performance is also benchmarked for the PHiL application as illustrated in Figure 20. For this comparison, the hardware power, measured from TP90kVA side, is scaled up by $\lambda_{pq} = 4125$ to match the network power scale simulated in RSCAD. Filtered power measurements are used in both hardware and software sides for noise reduction using low-pass filters. The active and reactive power

reference tracking performance is satisfactory between hardware and software, with the applied time-delay compensation of around 94 μs as identified in section 3.2. The hardware converter reacts successfully in real-time to the local reference adjustments. For instance, adjusting the reference from 20 MW to 35 MW at $t = 29.75\ s$, which corresponds to a hardware power ramp from 4.85 kW to 8.48 kW that is fed to the power interface amplifier. The VSM control reactive power tracking path is not prioritized in this experiment compared to GFC voltage control. Reactive power consumption or injection between TP90kVA and TP15kVA follow the requirement to maintain the voltage signal to its control setpoint, with a peak, filtered, value that does not exceed 1 MVAR (in its scaled-up form) as shown in Figure 20(b).

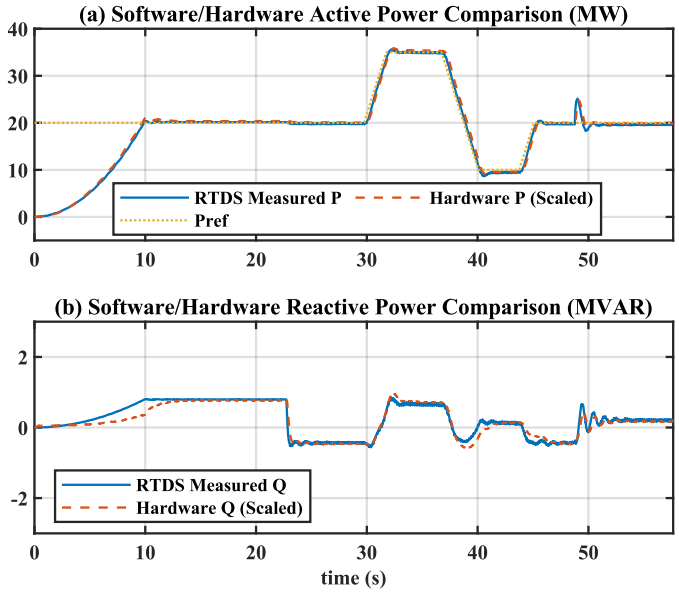


Figure 20: PHiL active and reactive power tracking throughout the experiment (simulated network vs. hardware GFC)

Finally, the current exported to the grid in RSCAD/RTDS, and the grid active power and reactive power measurements during the PHiL experiment are presented in Figure 21. Between $t = 22.75\ s$ and $t = 29.75\ s$, the grid current and power are close to zero. This is because the GFC power reference is set to 4.85 kW (which is scaled to 20 MW in RSCAD/RTDS). In the next stage, the grid imports 15 MW as illustrated in Figure 21(c) after the GFC export in RSCAD/RTDS is increased to 35 MW. The remaining segments follow similar behavior where the grid absorbs or supplies the surplus power in response to the hardware GFC reference power variations and the connected loads in RSCAD/RTDS. Meanwhile, the VAR exchange is adjusted as required to maintain the system demand and voltage.

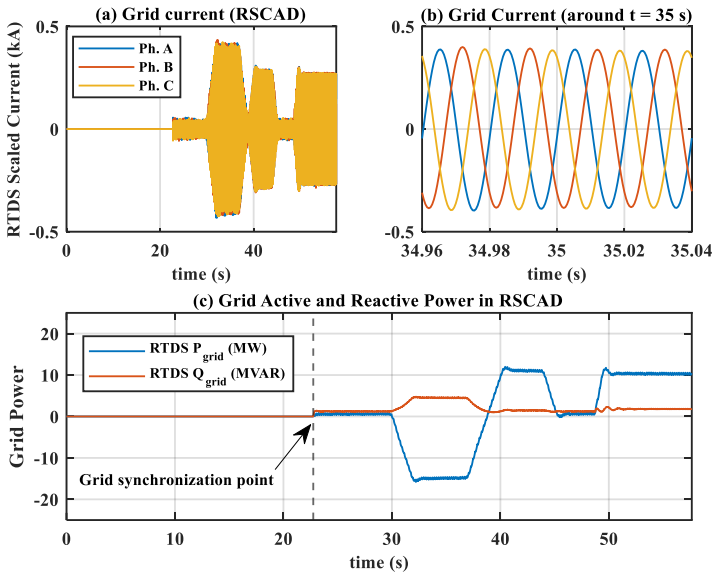


Figure 21: Grid current and power monitoring throughout the experimental PHiL scenario: (a) grid current (overall), (b) grid current around t = 35 s, (c) grid export active and reactive power throughout the test scenario.

5. Discussion on Results Generalization

The black-start test scenarios presented in this paper are based on a single power converter energizing a network with relatively high X/R ratio that enables effective decoupling between active and reactive power control. In practice, networks could consist of several converter units operating in different combinations (e.g., grid-forming or grid-following), and the X/R ratio could also be reduced especially in lower voltage distribution networks. Thus, a discussion is presented in this section on these two aspects to highlight typical approaches in literature and link them to the modified VSM design within the context of black-start.

5.1. Black-Start from Multiple DERs

The existence of multiple converters is typical in wind and solar PV farms, and the converters can be controlled either in grid-forming or grid-following mode, or a mix of both techniques. In a black-start scenario, it has been established that a grid-forming unit must exist to create the electrical island. The work presented in [41] demonstrates the black-start of a wind farm consisting of 50 wind turbines equipped with a droop-based converter control with inner current loops. All converters are controlled in grid-forming mode, and the successful restoration is illustrated under different modes including soft and one-by-one energization. The reported results demonstrate simultaneous soft energization of all the converters from 0.2 pu to 1 pu voltage, whereas another scenario shows sequential energization starting with a single wind turbines string, with the remaining strings synchronizing to it in grid-forming mode. Such

synchronization should in principle be feasible using the proposed synchronization technique in the present paper. The mixed operation between grid-forming and grid-following converters for a wind farm black-start has also been reported in [42], showcasing the feasibility of this option (e.g., when the control of some converters is pre-set to grid-following mode). This is achieved by first creating the island through grid-forming unit(s), followed by synchronizing the grid-following wind turbine strings to the established island. On the other hand, the interactions between grid-forming and grid-following converters operating in proximity are analyzed in [43]. Stability analysis demonstrate for a test network consisting of two converters and a grid connection point, that operating at least one converter in grid-forming VSM mode improves the system's robust stability as compared to converters operation in PLL-based grid-following mode. This summary shows the feasibility of achieving black-start from multiple grid-forming converters (or a mix of grid-forming and grid-following), while also highlighting that grid-forming operation based on VSM can benefit the system stability.

5.1.1. Operation of parallel VSMs for black-start and grid-synchronization

The highlighted successful multi-DER utilization for black-start in grid-forming mode in the literature is also validated by testing the modified VSM parallel operation and power sharing during a black-start event, including synchronization between different converters, and between the converters cluster and the grid. In this test scenario, two DERs are connected to two grid-forming converters equipped with the modified VSM control. The test network is illustrated in Figure *22*, showing each converter connected to a step-up transformer, followed by a π − section cable. The synchronization point between both converters is set before the load at the PCC. The objective here is to energize the network, synchronize both DERs and to finally synchronize the two converters cluster to the grid.

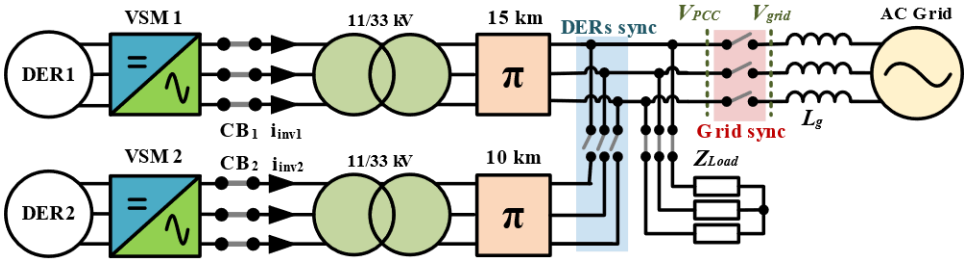


Figure 22: Block-diagram of parallel VSM Converters operation used for multi-DER control validation.

The first converter is initially connected to the load, and the second converter should synchronize at the DERs sync point after the transformer and cable energization is done. The voltages at both ends of the DERs sync circuit breaker

should match prior to the synchronization. Hence, VSM_2 control loop should contain an additional synchronization path as illustrated in Figure 23 to bring the DERs voltages (v_{VSM1} & v_{VSM2}) to a match before closing the switch, in a similar manner to that of the main grid-synchronization path in the results reported earlier (Figure 7). The DER synchronization path is activated through the (S_{sync_VSM}) switch, and is disconnected after synchronization is achieved through changing (S_{ps_VSM}) to 1. The main grid-synchronization control is recommended to remain connected to both VSM controllers such that P_{sync_g} is added simultaneously to their $P-f$ loops without impacting their power sharing proportion throughout the synchronization process. Thus, this path is also maintained in Figure 23.

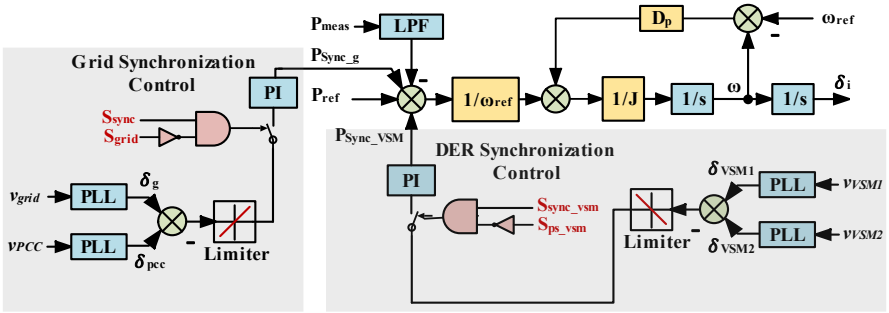


Figure 23: Modified VSM P-f loop for VSM2.

The test scenario to energize the network in Figure 22 starts with VSM_1 connected to a 0.5 pu load, and simultaneously energizing the transformer and cable segment. Soft energization is used with $T_{ramp} = 5\ s$, leading to power supply from the first converter of 0.5 pu at $t = 5\ s$. The power reference VSM_2 is energized separately with the same ramp-rate, and is initially not connected to the load. At $t = 5\ s$, the DER synchronization path in VSM_2 control is also activated, and successful synchronization is achieved at $t = 10\ s$ after the angle error between both voltages is driven to zero. Consequently, power sharing is achieved between the converters, and is proportional to their power references and control damping factors (D_p). In this scenario, the power references of both converters are set to 0.5 pu with similar damping factors, leading to equal power sharing with each converter supplying 0.25 pu for the load power (see Figure 24). If D_p is different for the converters, then it is observed that power sharing through power references is influenced proportionally, with the same observation applied to the synchronizing power (P_{sync_g}). Finally, grid-synchronization control is activated at $t = 11\ s$, driving (P_{sync_g}) equally to both converters with negligible impact on power sharing during the process. The synchronization is achieved at $t = 15\ s$, and the converters track their power references from this point onward (going back to 0.5 pu each). At $t = 20\ s$, the VSM_2 reference is

updated to 0.25 pu, which is reflected on the converter power output while VSM_1 output remains constant. Figure 24 summarizes the results and shows the reactive power output of each converter and their output frequency operating within acceptable bounds. As expected, both converters frequencies nearly match their behavior following the DERs synchronization step.

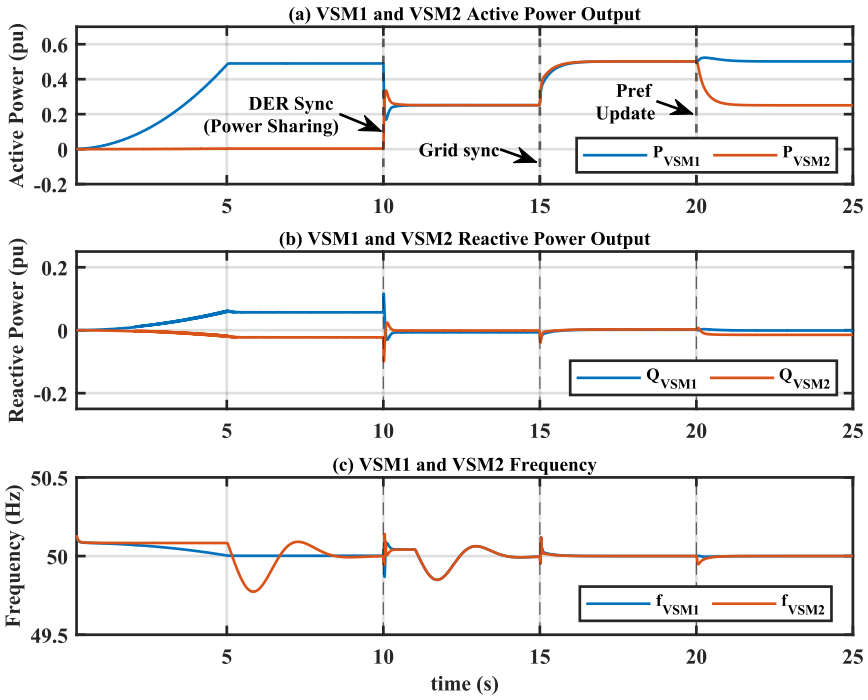


Figure 24: Simulation test results for parallel-connected VSM network energization and synchronization scenario.

5.2. Impact of X/R Ratio

The $P-f$ and $Q-V$ grid-forming loops control operation is based on the common assumption of high X/R ratio which enables effective decoupling between active and reactive power control. Namely, the approximations in (18)-(19) for power transfer between two voltage sources over an impedance (Z_{Li}) are valid if Z_{Li} is highly inductive.

$$P = \frac{V_i V_g}{Z_{Li}} \sin(\delta_i - \delta_g) \approx \frac{V_i V_g}{Z_{Li}} (\delta_i - \delta_g) \tag{18}$$

$$Q = \frac{V_i^2}{Z_{Li}} - \frac{V_i V_g}{Z_{Li}} \cos(\delta_i - \delta_g) \approx \frac{V_i^2}{Z_{Li}} - \frac{V_i V_g}{Z_{Li}} \tag{19}$$

where V_i and V_g are the converter and grid voltages, respectively, while δ_i and δ_g are their voltage angles, and $Z_{Li} = R_{Li} + jX_{Li}$. In the case that X/R ratio is low, the cross coupling between $P-V$ and $Q-f$ increases as demonstrated in [44]. This in turn impacts the control performance. Several remedies are proposed in the literature to mitigate the impact on the control tracking accuracy, such as the use of virtual impedance, feedforward compensation [45] and

dynamic decoupling [46]. The virtual impedance may include a virtual reactance to increase the effective X/R ratio and decouple active and reactive power quantities, whereas virtual resistance could be used to damp virtual oscillations [47]. Power decoupling techniques incorporation into the control should thus be considered when the system X/R ratio is low to improve its performance.

A power decoupling example is presented here for the modified VSM operation within a network with low X/R ratio for illustration. The used compensation technique is based on the virtual inductance L_v. This classical power decoupling method, also presented in reference [45], is shown in Figure 25, where the dq axes currents are scaled by the virtual reactance and used to correct the reference voltages generated by the outer grid-forming VSM control loop in the highly resistive network.

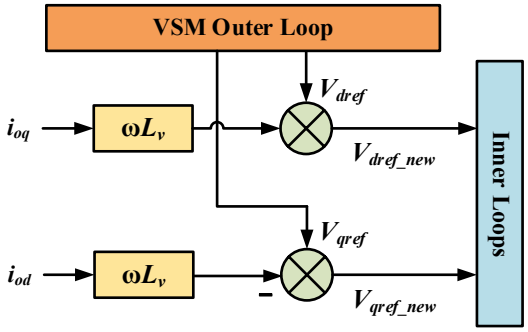


Figure 25: Static virtual inductance implementation for power decoupling.

In grid-connected mode, the control is tested under two scenarios. First, with L_v set to zero, showing a significant coupling and oscillatory behavior between active and reactive power against a step in Q_{ref}. In Figure 26(a), Q_{ref} is stepped from 10 MVAR to 15 MVAR at $t = 15\ s$, and back to 10 MVAR at $t = 20\ s$. Clearly, power coupling is highly present between both quantities and the active power is oscillatory against the applied reactive power step. In the second scenario, L_v decoupling path is activated, and the same step change in Q reference is observed to result in highly reduced decoupling between active and reactive power, leading to smoother transition for reactive power, and a mitigated impact on the active power as shown in Figure 26(b). Overall, the presented case demonstrates a simplified example of the power coupling impact in networks with low X/R ratio using a classical compensation method combined with the proposed VSM to showcase compatibility. Extension to dynamic decoupling methods is also recommended to achieve robust decoupling with improved performance.

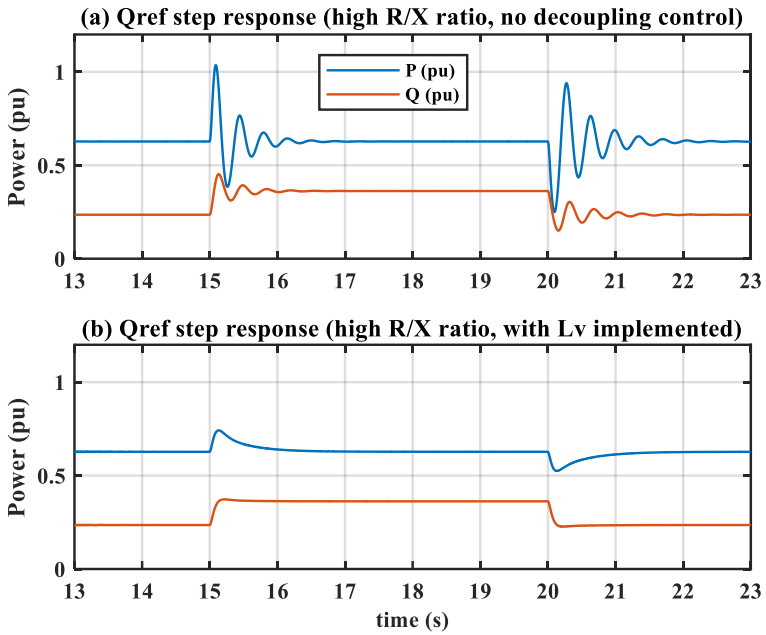


Figure 26: Impact of L_v on power decoupling against reactive power reference step: (a) before adding L_v, (b) after adding L_v.

6. Conclusions

This paper presented a modified VSM control for black-start applications, with validated soft energization, voltage support and grid-synchronization capabilities. The proposed synchronization technique relies on driving the phase angle error at the synchronizing point to zero before closing the circuit breaker to avoid the impact of classical synchronizing breakers closing-time mismatch. Power Hardware-in-the-Loop testing has been presented in this paper (with I-ITM interface) to experimentally test the modified controller implemented in a hardware GFC under flexible real-time simulated network configuration. I-ITM interface enabled the connection between the hardware GFC and PHiL power amplifier without prior synchronization requirement, and the setup has been used to successfully demonstrate the modified VSM capabilities in a complete black-start scenario, consisting of soft transformer energization for inrush current mitigation, load pickup and grid-synchronization. A time-delay impact compensation technique has also been proposed whereby power references are used to drive the power amplifier to mitigate the delay impact, while also providing aggregate compensation in synchronous dq0 frame to match active and reactive power between software and hardware domains.

The PHiL testing resulted in a successful tracking of voltage and current references in real-time between the hardware and the scaled-up simulated network. In addition, synchronizing between the hardware GFC and an internal grid simulated in RSCAD/RTDS has been achieved by relaying the required measurements from within the simulated

network to the external hardware GFC control, closing the control and synchronization loop. The presented configuration thus paves the way for testing extended networks in a controlled and non-destructive environment. That is, different network topologies can in principle be similarly tested for black-start under the novel proposed configuration with industrial converter models and compatible power interfaces in a non-destructive and controlled PHiL environment to assess and validate their control capabilities for black-start and network support applications, where the dynamic network behavior is reflected on the hardware GFC in real-time through the established power interface. This requires the use of compatible DRTS platform with sufficient computation capabilities to handle real-time complex network simulations (e.g., through using advanced simulators generation or multiple legacy simulators to increase the computation capability).

7. Acknowledgment

This publication is supported by Iberdrola S.A. as part of its innovation department research activities. Its contents are solely the responsibility of the authors and do not necessarily represent the official views of Iberdrola Group. The experimental work is funded by ScottishPower Energy Networks as part of the Distributed ReStart project.

8. References

[1] J. Matevosyan *et al.*, "Grid-Forming Inverters: Are They the Key for High Renewable Penetration?," *IEEE Power and Energy Magazine,* vol. 17, no. 6, pp. 89-98, 2019.

[2] J. L. Rodríguez-Amenedo, S. A. Gómez, J. C. Martínez, and J. Alonso-Martinez, "Black-Start Capability of DFIG Wind Turbines Through a Grid-Forming Control Based on the Rotor Flux Orientation," *IEEE Access,* vol. 9, pp. 142910-142924, 2021.

[3] R. H. Lasseter, Z. Chen, and D. Pattabiraman, "Grid-Forming Inverters: A Critical Asset for the Power Grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 925-935, 2020.

[4] Y. Pan, X. Yin, Z. Zhang, B. Liu, M. Wang, and X. Yin, "Three-Phase Transformer Inrush Current Reduction Strategy Based on Prefluxing and Controlled Switching," *IEEE Access,* vol. 9, pp. 38961-38978, 2021.

[5] R. Ierna *et al.*, "Dispatching parameters, strategies and associated algorithm for VSM (virtual synchronous machines) and HGFC (hybrid grid forming convertors)," 2019.

[6] C. P. J. Jansen, J. G. Slootweg, and R. A. C. T. d. Groot, "Calculation of Transformer Inrush Currents occurring during the Energizing of the Public Grid after a major Black Out," in *2005 IEEE Russia Power Tech*, 27-30 June 2005 2005, pp. 1-7.

[7] A. Roscoe *et al.*, "Practical Experience of Providing Enhanced Grid Forming Services from an Onshore Wind Park," 2019.

[8] J. Glassmire, S. Cherevatskiy, G. Antonova, and A. Fretwell, "Using Virtual Synchronous Generators to Resolve Microgrid Protection Challenges," in *2021 74th Conference for Protective Relay Engineers (CPRE)*, 22-25 March 2021 2021, pp. 1-7.

[9] A. Alassi, K. Ahmed, A. Egea-Alvarez, and C. Foote, "Soft Transformer Energization: Ramping Time Estimation Method for Inrush Current Mitigation," in *56th UPEC Conference*, 31 Aug.-3 Sept. 2021, pp. 1-6.

[10] J. Liu *et al.*, "An OLTC-inverter coordinated voltage regulation method for distribution network with high penetration of PV generations," *International Journal of Electrical Power & Energy Systems,* vol. 113, pp. 991-1001, 2019.

[11] H. A. Khan, M. Zuhaib, and M. Rihan, "Voltage fluctuation mitigation with coordinated OLTC and energy storage control in high PV penetrating distribution network," *Electric Power Systems Research,* vol. 208, p. 107924, 2022.

[12] A. Vukojevic and S. Lukic, "Microgrid Protection and Control Schemes for Seamless Transition to Island and Grid Synchronization," *IEEE Transactions on Smart Grid,* vol. 11, no. 4, pp. 2845-2855, 2020.

[13] W. Du *et al.*, "A Comparative Study of Two Widely Used Grid-Forming Droop Controls on Microgrid Small-Signal Stability," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 963-975, 2020.

[14] L. Zhang, L. Harnefors, and H. Nee, "Power-Synchronization Control of Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Systems,* vol. 25, no. 2, pp. 809-820, 2010.

[15] C. Arghir, T. Jouini, and F. Dörfler, "Grid-forming control for power converters based on matching of synchronous machines," *Automatica,* vol. 95, pp. 273-282, 2018.

[16] U. Tamrakar, D. Shrestha, M. Maharjan, P. B. Bhattarai, M. T. Hansen, and R. Tonkoski, "Virtual Inertia: Current Trends and Future Directions," *Applied Sciences,* vol. 7, no. 7, 2017.

[17] Q. Zhong and G. Weiss, "Synchronverters: Inverters That Mimic Synchronous Generators," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 4, pp. 1259-1267, 2011.

[18] M. Ashabani, F. D. Freijedo, S. Golestan, and J. M. Guerrero, "Inducverters: PLL-Less Converters With Auto-Synchronization and Emulated Inertia Capability," *IEEE Transactions on Smart Grid,* vol. 7, no. 3, pp. 1660-1674, 2016.

[19] A. Tayyebi, D. Groß, A. Anta, F. Kupzog, and F. Dörfler, "Frequency Stability of Synchronous Machines and Grid-Forming Power Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 1004-1018, 2020.

[20] D. Pan, X. Wang, F. Liu, and R. Shi, "Transient Stability of Voltage-Source Converters With Grid-Forming Control: A Design-Oriented Study," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 1019-1033, 2020.

[21] A. Alassi, K. Ahmed, A. Egea-Alvarez, and O. Ellabban, "Performance Evaluation of Four Grid-Forming Control Techniques with Soft Black-Start Capabilities," in *2020 9th International Conference on Renewable Energy Research and Application (ICRERA)*, 27-30 Sept. 2020 2020, pp. 221-226.

[22] G. Li *et al.*, "An improved DIM interface algorithm for the MMC-HVDC power hardware-in-the-loop simulation system," *International Journal of Electrical Power & Energy Systems,* vol. 99, pp. 69-78, 2018.

[23] S. Karrari, G. De Carne, and M. Noe, "Adaptive droop control strategy for Flywheel Energy Storage Systems: A Power Hardware-in-the-Loop validation," *Electric Power Systems Research,* vol. 212, p. 108300, 2022.

[24] E. García-Martínez, J. F. Sanz, J. Muñoz-Cruzado, and J. M. Perié, "Online database of Power Hardware In-the-Loop tests," *Data in Brief,* vol. 29, p. 105128, 2020.

[25] E. García-Martínez, J. F. Sanz, J. Muñoz-Cruzado, and J. M. Perié, "A Review of PHIL Testing for Smart Grids—Selection Guide, Classification and Online Database Analysis," *Electronics,* vol. 9, no. 3, p. 382, 2020.

[26] B. Li, Z. Xu, S. Wang, L. Han, and D. Xu, "Interface Algorithm Design for Power Hardware-in-the-loop Emulation of Modular Multilevel Converter Within High-Voltage Direct Current Systems," *IEEE Transactions on Industrial Electronics,* vol. 68, no. 12, pp. 12206-12217, 2021.

[27] M. Bokal, I. Papič, and B. Blažič, "Stabilization of Hardware-in-the-Loop Ideal Transformer Model Interfacing Algorithm by Using Spectrum Assignment," *IEEE Transactions on Power Delivery,* vol. 34, no. 5, pp. 1865-1873, 2019.

[28] J. Hernandez-Alvidrez, N. S. Gurule, M. J. Reno, J. D. Flicker, A. Summers, and A. Ellis, "Method to Interface Grid-Forming Inverters into Power Hardware in the Loop Setups," in *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)*, 15 June-21 Aug. 2020 2020, pp. 1804-1810.

[29] S. Resch, J. Friedrich, T. Wagner, G. Mehlmann, and M. Luther, "Stability Analysis of Power Hardware-in-the-Loop Simulations for Grid Applications," *Electronics,* vol. 11, no. 1, p. 7, 2022.

[30] A. Alassi, K. Ahmed, A. Egea-Alvarez, and C. Foote, "Modified Grid-forming Converter Control for Black-Start and Grid-Synchronization Applications," in *56th UPEC Conference*, 31 Aug.-3 Sept. 2021 2021, pp. 1-5.

[31] D. Bejmert, M. Kereit, and K. Boehme, "Controlled energization procedures of power transformers," *International Journal of Electrical Power & Energy Systems,* vol. 135, p. 107555, 2022.

[32] C. Yu, S. G. Abdulsalam, C. Shiuming, and X. Wilsun, "A sequential phase energization technique for transformer inrush current reduction - Part I: Simulation and experimental results," *IEEE Transactions on Power Delivery,* vol. 20, no. 2, pp. 943-949, 2005.

[33] A. Alassi, K. H. Ahmed, A. Egea-Alvarez, and C. Foote, "Transformer Inrush Current Mitigation Techniques for Grid-Forming Inverters Dominated Grids," *IEEE Transactions on Power Delivery,* pp. 1-11, 2022.

[34] J. Wang, A. Pratt, and M. Baggu, "Integrated Synchronization Control of Grid-Forming Inverters for Smooth Microgrid Transition," in *2019 IEEE Power & Energy Society General Meeting (PESGM)*, 4-8 Aug. 2019, pp. 1-5.

[35] C. Lee, R. Jiang, and P. Cheng, "A Grid Synchronization Method for Droop-Controlled Distributed Energy Resource Converters," *IEEE Transactions on Industry Applications,* vol. 49, no. 2, pp. 954-962, 2013.

[36] G. Lauss *et al.*, "A Framework for Sensitivity Analysis of Real-Time Power Hardware-in-the-Loop (PHIL) Systems," *IEEE Access,* vol. 10, pp. 101305-101318, 2022.

[37] B. Lundstrom and M. V. Salapaka, "Optimal Power Hardware-in-the-Loop Interfacing: Applying Modern Control for Design and Verification of High-Accuracy Interfaces," *IEEE Transactions on Industrial Electronics,* vol. 68, no. 11, pp. 10388-10399, 2021.

[38] Z. Feng, A. Alassi, M. Syed, R. Peña-Alzola, K. Ahmed, and G. Burt, "Current-Type Power Hardware-in-the-Loop Interface for Black-Start Testing of Grid-Forming Converter," in *IECON 2022*, Brussels, 17-20 2022.

[39] Z. Feng *et al.*, "Interface Compensation for More Accurate Power Transfer and Signal Synchronization within Power Hardware-in-the-Loop Simulation," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, 13-16 Oct. 2021 2021, pp. 1-8..

[40] "Distributed ReStart: Power Engineering and Trials - Demonstration of Black Start from DERs Part 1," National Grid ESO, UK, 2021.

[41] M. Aten, R. Shanahan, F. Mosallat, and S. Wijesinghe, "Dynamic Simulations of a Black Starting Offshore Wind Farm Using Grid Forming Converters," presented at the 18th Wind Integration Workshop, Dublin, 2019.

[42] J. M. Turégano, "Grid Forming Wind Power Plants: Black start operation for HVAC grids and Diode Rectifier-based Wind Power Plant integration," PhD, Polytechnic University of Valencia, 2021.

[43] R. Rosso, S. Engelken, and M. Liserre, "Robust Stability Investigation of the Interactions Among Grid-Forming and Grid-Following Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 991-1003, 2020.

[44] M. Ahmed, L. Meegahapola, A. Vahidnia, and M. Datta, "Analyzing the Effect of X/R ratio on Dynamic Performance of Microgrids," in *2019 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe)*, 29 Sept.-2 Oct. 2019 2019, pp. 1-5.

[45] Y. Laba, A. Bruyère, F. Colas, and X. Guillaud, "PQ Decoupling on Grid-Forming Converter Connected to a Distribution Network," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 26-29 June 2022 2022, pp. 1-6.

[46] F. Zhao, X. Wang, and T. Zhu, "Power Dynamic Decoupling Control of Grid-Forming Converter in Stiff Grid," *IEEE Transactions on Power Electronics,* vol. 37, no. 8, pp. 9073-9088, 2022.

[47] Y. Li, Y. Gu, Y. Zhu, A. Junyent-Ferré, X. Xiang, and T. C. Green, "Impedance Circuit Model of Grid-Forming Inverter: Visualizing Control Algorithms as Circuit Elements," *IEEE Transactions on Power Electronics,* vol. 36, no. 3, pp. 3377-3395, 2021.