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Hybrid integration of chipscale photonic devices using accurate transfer printing methods

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ABSTRACT

Transfer printing is becoming widely adopted as a back-end process for the hybrid integration of photonic and electronic devices. Integration of membrane components, with micrometer-scale footprints and sub-micron waveguide dimensions, imposes strict performance requirements on the process. In this review, we present an overview of transfer printing for integrated photonics applications, covering materials and fabrication process considerations, methods for efficient optical coupling, and high-accuracy inter-layer alignment. We present state-of-the-art integration demonstrations covering optical sources and detectors, quantum emitters, sensors, and opto-mechanical devices. Finally, we look toward future developments in the technology that will be required for dense multi-materials integration at wafer scales.

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I. INTRODUCTION

Photonic integrated circuit (PIC) technologies have rapidly transitioned from device-level research demonstrations to large-scale circuits on a chip, enabled by electronic foundries[1,2] and focused startups.[3–5] The deployment of PICs for applications, including telecommunications transceivers, sensors, and LiDAR, has necessitated the development of advanced packaging solutions in tandem to wafer scale fabrication of the monolithic photonic chips. Fiber coupling, electronic ASIC control and co-packaging, free-space coupling optics, and thermal stabilization elements can all be integrated at a carrier level with PICs in a variety of geometries.[6–10] Additionally, it is clear that the full functionality of optical systems-on-a-chip cannot be delivered by single material platforms alone. The development of community programs, such as the IEEE Heterogeneous Integration Roadmap[11] and IPSRI,[12] demonstrates the wide recognition of the requirement for hybrid and heterogeneous integration in PIC-based systems manufacturing, and the need to develop standards in this area.

The integration of different material platforms together into a single package can be achieved by a range of means depending on the density of integration required,[13–16] and a few examples of which are shown in Fig. 1. For example, co-packaging of laser diode or amplifier device bars with PICs at a chip-to-chip level is sufficient for cases where only a few active devices are required and interconnects are not limited by the available chip perimeter. However, as the number of non-native material devices required on the base-PIC increases, the density and spatial distribution of these require surface-to-surface integration schemes. Flip-chip bonding technology allows for chip-to-chip alignment in the sub-micron range[17] and offers a similar level of integration to edge-coupled schemes,[18] though it is particularly useful for the direct integration of photonic and electronic chips.[19] However, in order to fully exploit the micrometer-scale dimensions of photonic devices for heterogeneous integration, a more intimate connection between materials platforms is required at a device level, and removing the need for the secondary substrate layer that is retained in schemes, such as flip-chip bonding and co-packaging. Again, there are a number of ways that this can be achieved, including regrowth of material onto fabricated PICs[20] or wafer-bonding schemes.[21] The latter method is particularly suited to the realization of photonic devices that can be coupled to existing PIC substrates. In this method, wafer sections or dies of a complementary material are directly bonded onto the host PIC with the substrate side facing up. The substrate can then be selectively removed using mechanical and chemical etching processes. The remaining device layers are then processed *in situ* on the PIC, allowing for high-accuracy layer-to-layer alignment by using pre-fabricated registration markers on the host PIC chip.[22] However, if more than one material is required to be integrated onto the PIC, then the wafer bonding and processing methods become challenging to produce new devices in close proximity to existing structures without damaging them, or compromising the quality of the wafer bonding process. The ability to integrate fully fabricated devices from a range of material platforms onto large-scale PICs is a particular challenge in areas, such as neuromorphic optical computing and on-chip quantum photonics.[23,24] In the case of PICs for quantum photonic applications, the requirements for low-loss material-to-material transitions and a wide range of required functionality (optical sources, detectors, low noise phase-shifters, cryogenic compatibility) present significant challenges for PIC integration from materials growth to advanced manufacturing methods for large-scale yield and systems complexity.

In this work, we focus on a form of back-end integration, commonly referred to as transfer printing.[25–29] The main benefits of this technique are (1) that it allows for full fabrication of devices to be transferred before integration with the host PIC; (2) it operates at a device level, allowing for dense integration of components across the PIC surface; (3) it is compatible with the integration of multiple materials on a single chip; (4) it allows for the transfer of device layers independently from their growth substrate, minimizing material waste and decoupling the layout designs required by the native and receiver substrates. A basic schematic of the transfer printing integration process is presented in Fig. 2. In this review of transfer printing integration for PIC applications, we first present the basic methodology and device requirements for transfer printing integration of thin film photonic

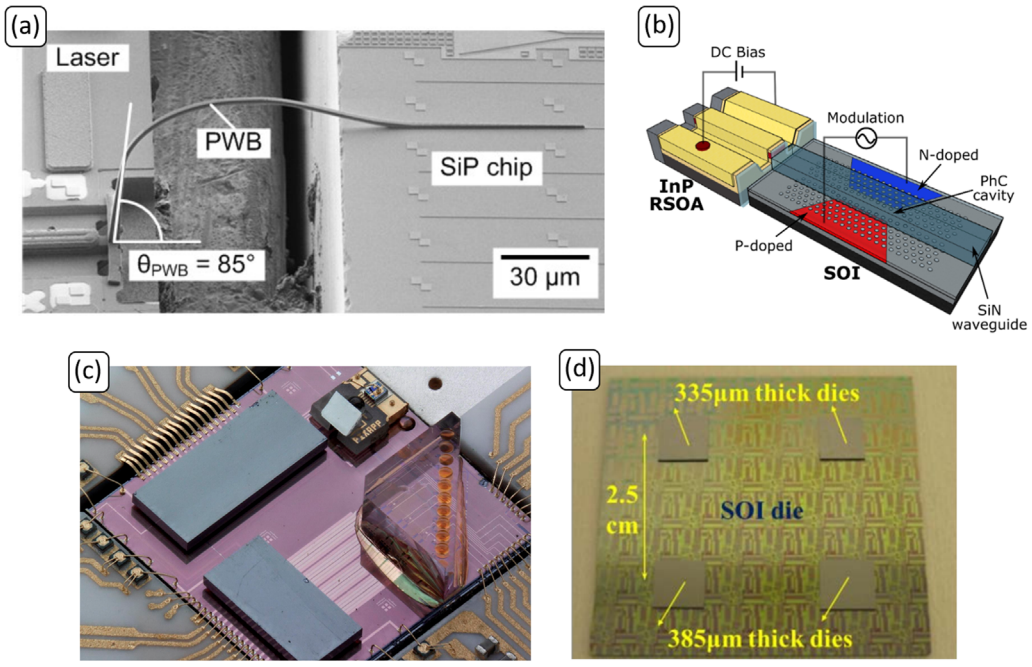

FIG. 1. Exemplar chip-scale integration schemes. (a) An InP laser integrated via photonic wire bonds to passive Si PICs. Reproduced with permission from Billah *et al.*, Optica **5**, 876 (2018). Copyright 2018 The Optical Society.[9] (b) Butt-coupling InP reflective semiconductor optical amplifier (RSOA) laser scheme. Butler *et al.*, Optics Express **27**, 11312 (2019). Copyright 2019 Authors, licensed under a Creative Commons Attribution (CC BY) license.[30] (c) The integration and packaging of several on-PIC components. Reprinted from Ref. 31. (d) InP dies wafer bonded to a Si PIC. Reproduced with permission from Keyvaninia *et al.*, Opt. Mater. Express **3**, 35 (2013). Copyright 2013 The Optical Society.[7]

devices. We discuss the case of waveguide-to-waveguide integration, in particular, highlighting the required spatial accuracy, methods for alignment of membrane waveguides to host PICs and the optical coupling geometries that have been developed. A review of the various base-PIC platforms and heterogeneously integrated materials is detailed, followed by examples of key prototype systems and applications demonstrations achieved using this technology. Finally, we discuss the future challenges and opportunities for transfer printing-based PIC integration that will be crucial in enabling new systems-on-a-chip applications.

II. TRANSFER PRINTING OF MEMBRANE PHOTONIC DEVICES: DEVICE REQUIREMENTS AND PROCESS

A. Transfer printing process

As shown in Fig. 2, transfer printing is essentially a form of pick-and-place integration, where devices from one material system are removed from their native substrate and placed in position on a host substrate. The features that distinguish this technique from mature industrial pick-and-place technologies are the small scale of devices that can be handled (in the μm range), the transfer of only a thin membrane layer (100 nm–μm) and the spatial accuracy of placement and density of devices that can be achieved. Therefore, the preparation of the devices to be transferred is crucial to the success and scalability of this method and places some key requirements on their physical format.

For membrane format photonic waveguide device transfer printing, the basic process follows the schematic in Fig. 2. First, a membrane device is fabricated on its donor substrate by lithography and etching of the waveguide devices. A receiver substrate is fabricated in parallel and both samples typically include registration marks fabricated for spatially referencing the donor and receiver optical structures. The donor membrane is suspended over its substrate layers using a sacrificial layer etch and mechanical tethering to supporting areas. A soft polymer stamp head, typically PolyDiMethylSiloxane (PDMS), is then positioned over the membrane device on the donor substrate and brought into contact. The retraction of the stamp breaks the mechanical tethers, leaving the membrane attached to the PDMS stamp. The stamp is then aligned over the receiver substrate and the membrane brought into contact. Slow retraction of the PDMS stamp leaves the membrane printed onto the receiver substrate.[32] The details of each of these stages are presented in Secs. II B, II C, III, and IV with particular reference to the fabrication of waveguide membrane devices. It is worth noting that there are other forms of transfer printing presented in the literature,[33] for example, roller printing for mass-transfer,[34] though these have thus far not been used for the realization of high spatial accuracy waveguide-waveguide device printing. Methods for the active control of the adhesive properties of stamp heads have also been studied;[35] including using shape memory polymers[27,36] or electrically actuated cantilever structures.[37] Metallic probes have also been used,[38,39] sometimes tipped with PDMS.[40]

B. Epilayer design and sacrificial membrane release

Most photonic integrated chips are designed to use only a thin layer of material grown on top of a thick substrate wafer. This may be only a few hundred nanometers of material in the case of silicon photonic devices, or a few micrometers for compound semiconductor devices. The thick substrate material is necessary to allow wafer handling during fabrication processes, including growth, lithography,

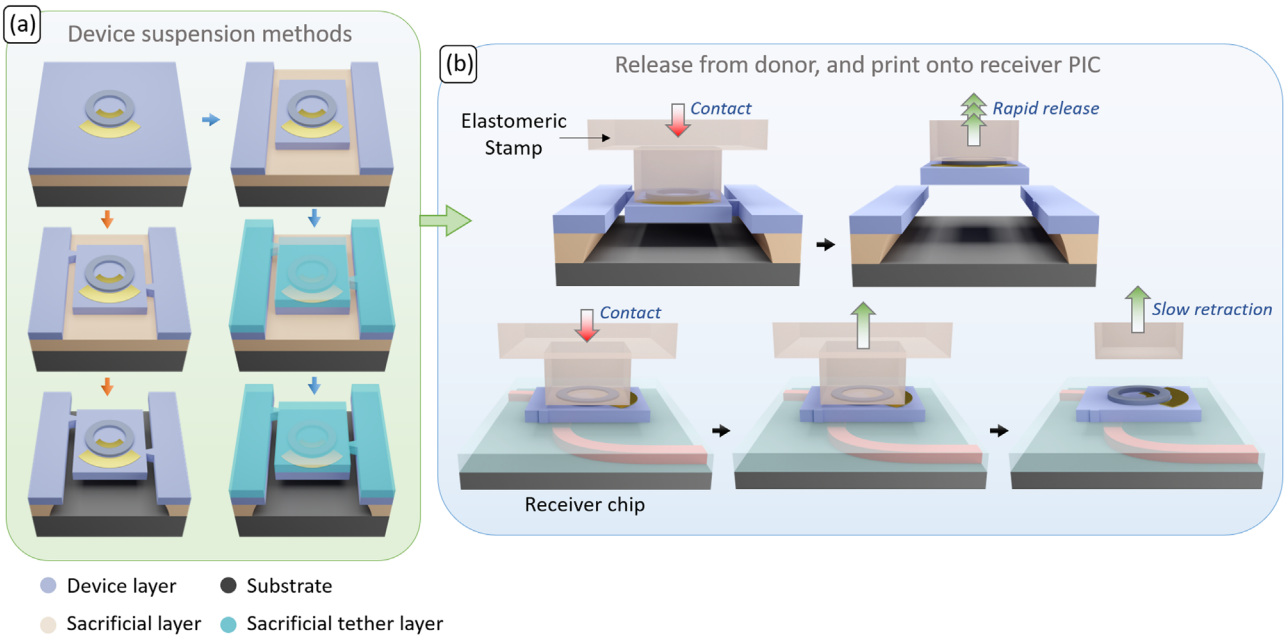

FIG. 2. Generalized schematic of the transfer-printing of membrane photonic devices. (a) Two processes by which suspended membranes may be fabricated, with tethers either monolithically fabricated in the same layer as the devices, or patterned in a sacrificial resist layer to which the top surface of the membrane adheres after the under-etch of the substrate. (b) Simplified demonstration of the process of retrieving from the donor and printing onto the receiver PIC, using an elastomeric stamp.

etching, metal, and dielectric deposition. However, if the devices can be released after these mechanically demanding stages, then the substrate can be salvaged and re-used for future wafer growth runs. The transfer printing process only uses the active device layers for integration and, therefore, requires consideration from the materials growth stage to enable membrane layers balancing their optical, electronic, mechanical, and chemical etch selectivity properties. Figure 2(a) shows that prior to printing, the optical layers are released from their substrate, typically using a wet etch or vapor etch process. To enable this release process, the membrane layers of interest must be grown onto a sacrificial layer that presents a high chemical reactivity to an etchant that the membrane layers are robust to. Typically, the substrate is also designed to be resistant to the wet etch, either chemically[41] or by a self-limiting effect, for example in the case of KOH etching of silicon layers.[42] The sacrificial layer must also be designed so that there is sufficient clearance between the membrane layers and the substrate after removal, to avoid the membrane collapsing onto the substrate, an effect often exacerbated by capillary effects when the sample is dried. The mechanical deformation of the membranes is related to the stiffness of the material, in-built stress due to crystal lattice mismatch of multi-layer structures, and the geometry of the membrane.[25]

In the simplest case, where device membranes are composed of a single material layer, the material does not typically carry in-built stress and so does not exhibit substantial bowing on release. Figure 3(a) shows an example of single crystal silicon membranes after they have been transfer printed to a host substrate, where the flatness of the membranes allows them to be vertically stacked.[25] Nevertheless, although single crystalline materials do not typically present intrinsic stress and bowing when released from their growth substrate, often these thin materials can be deformed due to near surface effects and deformations induced during fabrication or printing processes. If the sacrificial layer is not thick enough to suspend the devices from the rigid side tethers, see Fig. 3(b), then the membranes can deform and make contact with the substrate during the release process, especially for thin membrane geometries which can be extremely mechanically flexible.[43] Once bonded to the substrate, these membranes can be difficult to remove, and flat contact with the printing pickup head becomes challenging, something that is important for the high spatial accuracy integration stages. The mechanical flexibility of thin membranes in single crystalline material is clear when they are transferred to surfaces with protruding features, as shown for silicon Fig. 3(c) (Ref. 43) and diamond Fig. 3(d).[44]

Single material layers are often straightforward to produce for transfer printing integration, where the device layer can be fabricated directly onto the sacrificial layer by growth, or wafer bonding. Semiconductor layers on a silica sacrificial layer are particularly useful and allow use of a hydrofluoric acid (HF) based etch to selectively underetch the membrane devices. This method is commonly used for silicon,[45–47] diamond,[48] and lithium niobate.[49]

For compound semiconductor materials, the membrane layer is typically grown with a sacrificial semiconductor layer, where the material composition is tailored to produce chemical etch selectivity. For single optical layer membranes, such as $Al_xGa_{(1-x)}As$, this can be achieved by varying the aluminum content of the epitaxial layers.[50–52] A high aluminum content layer will be etched effectively by an HF based solution, allowing for under-etching of a low aluminum content

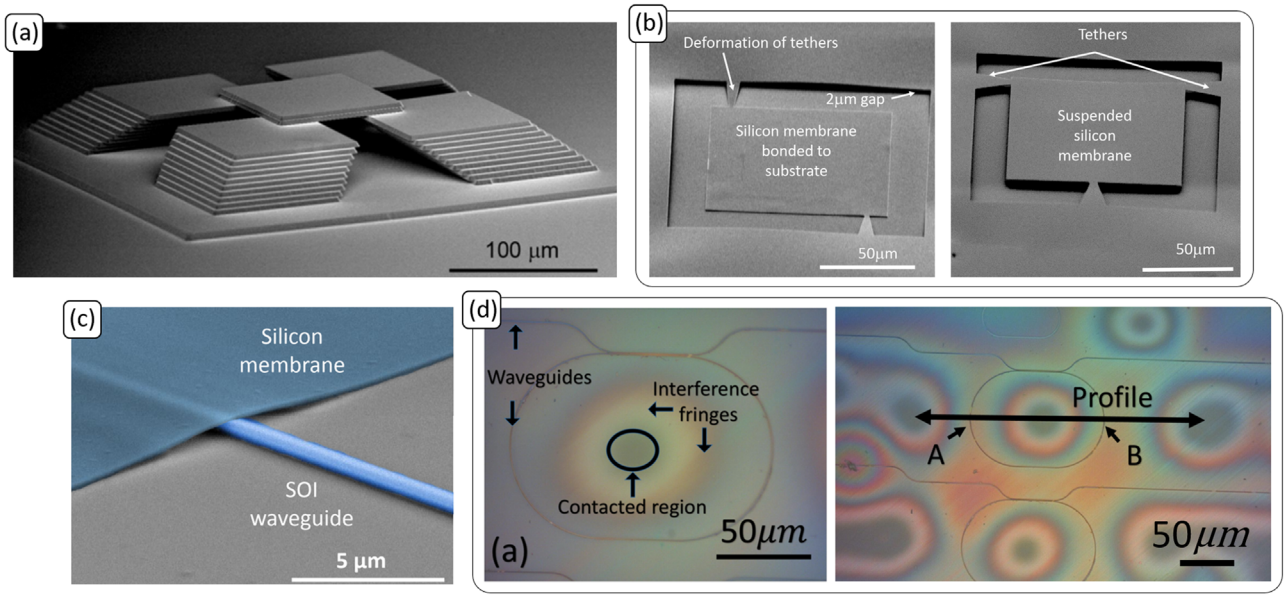

FIG. 3. (a) Stacking of several flat Si membranes. Reproduced with permission from Kim *et al.*, Proc. Natl. Acad. Sci. U. S. A. **107**, 17095 (2010). Copyright 2010 Proceedings of the National Academy of Sciences.[32] (b) Left: a collapsed Si membrane. Right: A fully suspended Si membrane. From McPhillimy *et al. 2018 British and Irish Conference on Optics and Photonics.* Copyright 2018 IEEE. Reproduced with permission from IEEE.[43] (c) Thin film silicon (150 nm thick), deforming around a Si waveguide. From McPhillimy *et al. 2018 British and Irish Conference on Optics and Photonics.* Copyright 2018 IEEE. Reproduced with permission IEEE.[43] (d) Newton's rings in a diamond membrane integrated with Si racetrack resonator chip, indicating deformation in the diamond. Hill *et al.*, Diamond Relat. Mater. **88**, 215 (2018). Copyright 2019 Authors, licensed under a Creative Commons Attribution (CC BY) License.[44]

layer or simple GaAs. The close matching of lattice constants of the growth layers results in membranes with low in-built stress and that can therefore be transfer printed easily.[47,51,53,54] The high quality, low defect, growth available for III-V compound semiconductors means that multi-layer structures with thicknesses into the few micrometer range can be fabricated with negligible bowing in membrane format.[26,55,56] For example, InP-based laser materials with complex layer stacks containing quantum well gain regions, highly doped p^+ and n^- contact layers, and sacrificial layers have been produced. For these devices, an InGaAs sacrificial layer can be used in conjunction with an $FeCl_3$-based etch.[41,57,58]

In the case of III-N semiconductors, the in-built stress of the epistructure can be significant, especially when the material is grown on a silicon substrate. Growth on silicon is useful both for wafer scale production and to provide the necessary etch selectivity of the device layers over the substrate.[59] Silicon can be etched using a KOH based solution that does not significantly etch the III-N layers. The silicon etch has two added benefits. First, it is highly anisotropic, aiding design of tether structures discussed below. Second, it is a self-limiting process, and therefore the substrate itself can act as the sacrificial layer, with the etch depth below the device layers being defined by the etched area with respect to the crystallographic etch directions. However, the significant lattice constant mismatch between silicon and the III-N layers can induce substantial wafer bowing, and in turn membrane bowing upon release.[60,61] Figure 4(a) shows an example of a III-N membrane after release and printing, showing visible Newton's rings

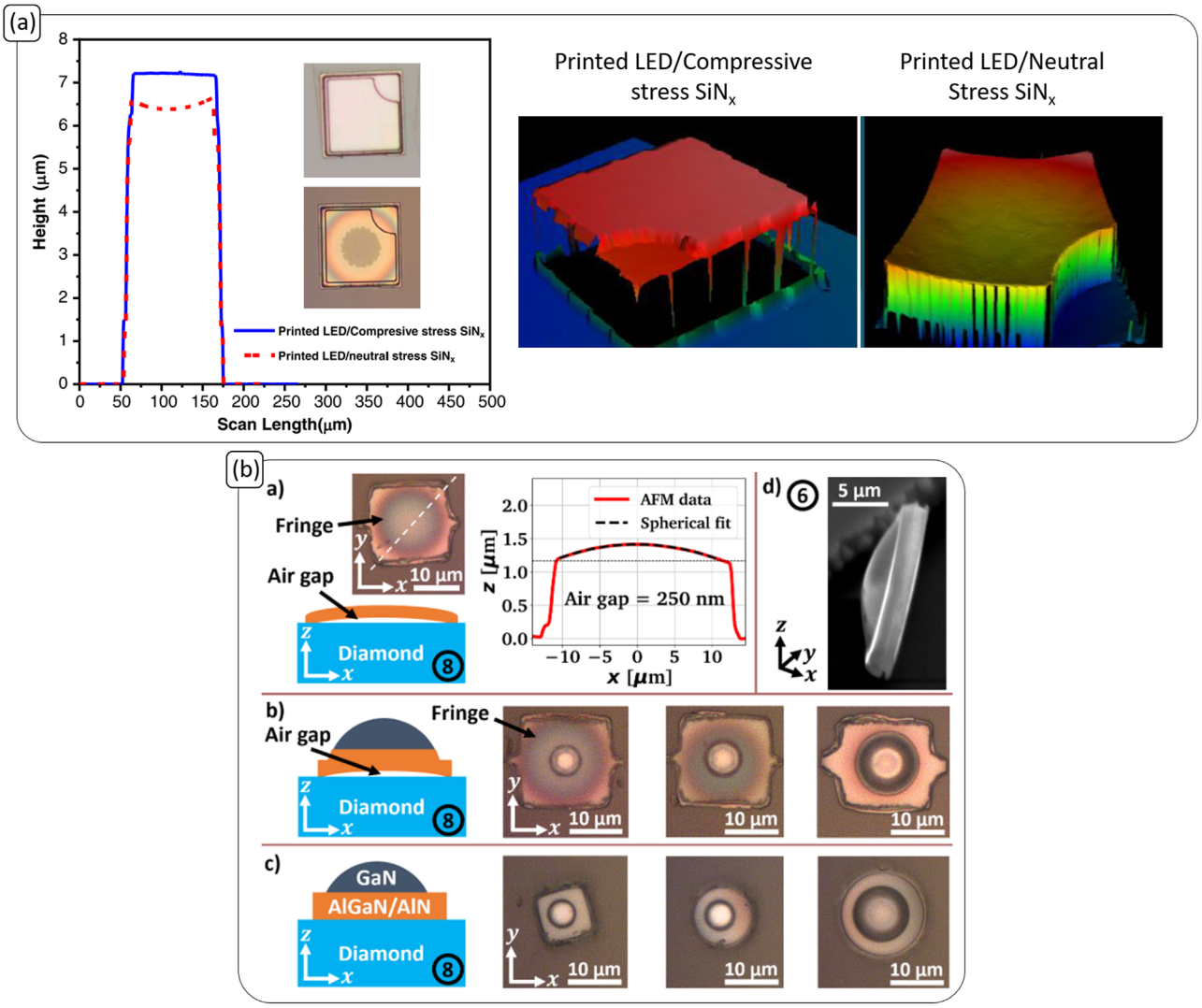

FIG. 4. (a) Demonstration of how intrinsic stress often leads to significant bowing upon release, and how additional growth layers (in this case, SiN) can be utilized to manage the membrane stress. Shaban *et al.*, Adv. Photonics Res. **3**, 2100312 (2022). Copyright 2022 Authors, licensed under a Creative Commons (CC BY) License.[60] (b) GaN membranes and microlenses, with and without bowing, after transfer printing onto diamond substrates. Reproduced with permission from Wessling *et al.*, Opt. Mater. Express **12**, 4606 (2022). Copyright 2022 The Optical Society.[64]

indicating the membrane bow. There are a number of ways that this membrane bow can be counteracted. One possibility is to use an adhesion layer on the host substrate.[25,62,63] This increases the bonding force between the membrane and the host substrate, and can also provide some in-filling under the membrane structure. Optimized material growth can be employed to tailor the inter-layer stresses to produce a balanced layer stack and, hence, flat membrane,[61] as shown in Fig. 4. In this case, if the membranes are to be etched to include waveguide structures for example, then the removal of layers during etching should be taken account of for the final membrane bow design. Additional layers can also be added to the material post-growth to counteract the membrane bow, for example using SiN upper-cladding layers.[60] In this case, the stress of the dielectric layer is tuned to act in the opposite sense to the in-built stress of the III-N layers, producing an overall neutral membrane bow.

C. Membrane tether design

The second important consideration in the design of releasable membrane layers is the geometrical design of the membrane tethers, or mechanical supports. During the sacrificial layer etch process, the membrane is, in most cases, rigidly connected to the substrate to preserve its location on the wafer and to suspend it over the substrate, see the schematic in Fig. 5(a). For thin membranes with thickness in the few hundred nanometers range, these mechanical tethers are usually fabricated in the same layer as the device membrane, presenting a mechanical link between the membrane and surrounding material. The tethers are typically designed to present a small cross-sectional area to promote mechanical cleaving during the printing process, but to be robust enough to suspend the membrane during the sacrificial etch process and drying. As noted above, the mechanical properties of the membrane also inform the required geometry of the membrane tethers. Important factors include the breaking force required to cleave the tethers, the mechanical flexibility of the membrane and crystallographic structure of the membrane material. Various geometries of tethers have been used and often include a mechanical "neck" point to locally promote the cleaving of the material.[65] Furthermore, for isotropic sacrificial layer etches, the support structures surrounding the membrane will also be under-etched, leading to flexible membrane areas surrounding the device area targeted for release. Care must be taken to avoid initiating cleaving of these areas that could be removed with the device, or collapsing the membrane onto the donor substrate, see Fig. 3(b).[43] For membranes with a thickness in the 1–3 μm range, the material structure is generally stiff enough to retain its shape after under-etching and monolithic tapers will cleave during printing. For material structures thicker than this, cleaving of the tethers can be challenging and the tethers can then be etched to a reduced thickness in a secondary reactive ion etching process, Fig. 5(b), to aid cleaving. In an-isotropic sacrificial etch processes the tether geometry can be important in seeding etch planes, and care has to be taken to avoid alignment of the structures with unwanted etch propagation planes, or processes that will self-terminate before membrane release. Figure 5(c) shows a GaN-on-silicon membrane process where the angle of the tether features to the silicon etch plane has resulted in defect features

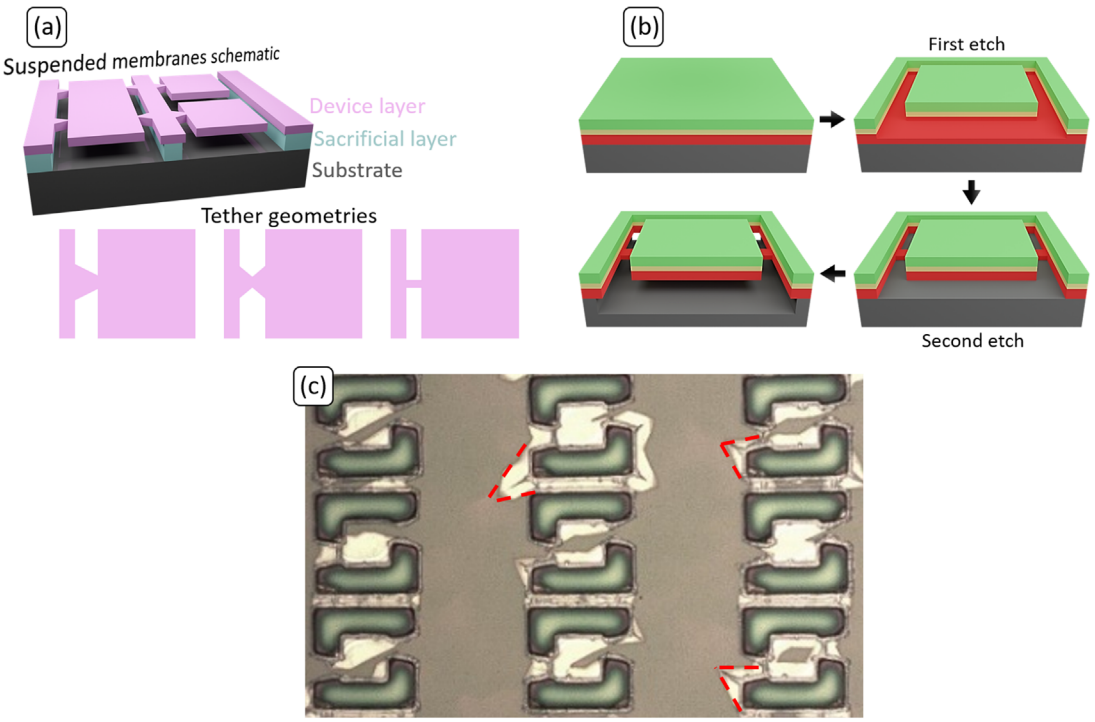

FIG. 5. (a) Perspective schematic of under-etched platelets, with some commonly used tether geometries. (b) A two-stepped membrane tether etch, useful for reducing the mechanical strength of monolithically realized tethers when the device layer is too thick. (c) Deleterious etch directions in anisotropic KOH under-etches, seeded by improperly designed tether geometries.

propagating under the support areas of the chip and destroying the membranes.

Alternatively, a sacrificial tether layer can be used,[66] as shown in the schematic of Fig. 2(a). In this process, a resist layer is applied to the donor chip after fabrication of the membrane pattern which does not include monolithic tethers. The resist layer is then patterned to protect the membrane and supporting areas and includes mechanical tethers joining the two. A sacrificial layer etch leaves the membranes suspended above the substrate, held in place by the resist tethers. The resist layer is relatively easily broken during transfer print pickup and removed via a reactive ion etch stage post-printing.

III. TRANSFER PRINTING FOR WAVEGUIDES AND PICS

Waveguide dimensions for integrated photonics are typically in the sub-μm range, making integration by transfer printing particularly challenging in terms of absolute spatial positioning. The transfer printing process flow detailed in Sec. II uses a fully post-fabrication method where waveguides must be aligned with high accuracy during the print stage. There are in fact a number of methods that can be employed to either relax the required spatial accuracy of the printing stage, or reorder the fabrication flow to avoid the high-accuracy printing stage completely. A summary of the various process flows and their particular tradeoffs are presented below.

A. Membrane transfer and post processing

To remove the necessity for high-accuracy printing altogether, the definition of waveguide devices on the membrane structure can either be avoided, or fabricated after the printing stage. This methodology strongly resembles wafer bonding techniques, but with the added benefit of only transferring small membranes, or coupons, of material, avoiding the issues of wafer bonding related to substrate removal and dense integration of multiple materials. In the most basic case, no waveguide structures are defined at any stage on the donor material, as in Fig. 6(a). Instead, a donor material, typically of lower refractive index than the receiver, is bonded onto the receiver waveguide platform with low spatial accuracy. The composite material structure is designed to allow waveguide modes that are either overlapped weakly with the printed material, or that are guided through an effective index guiding mechanism.[49,67] In the case of effective index guiding, the material benefit of the top layer is reduced due to the reduced optical field overlap.

More effective modal confinement can be achieved by processing the membrane material after transfer. In this method, alignment accuracy between the two layers can be extremely good as it is limited only by the lithography process, which uses a common set of registration marks fabricated on the receiver substrate.[70] This method does, however, require the processing of the membrane materials *in situ* on the receiver PIC and may require multiple stages of processing for the integration of more than one membrane material.

B. Recessed butt-coupling to end-facets

Similar to the co-packaging of waveguide chips detailed in the introduction, waveguides on different materials can be directly integrated using butt-coupling at their facets. In a transfer printing

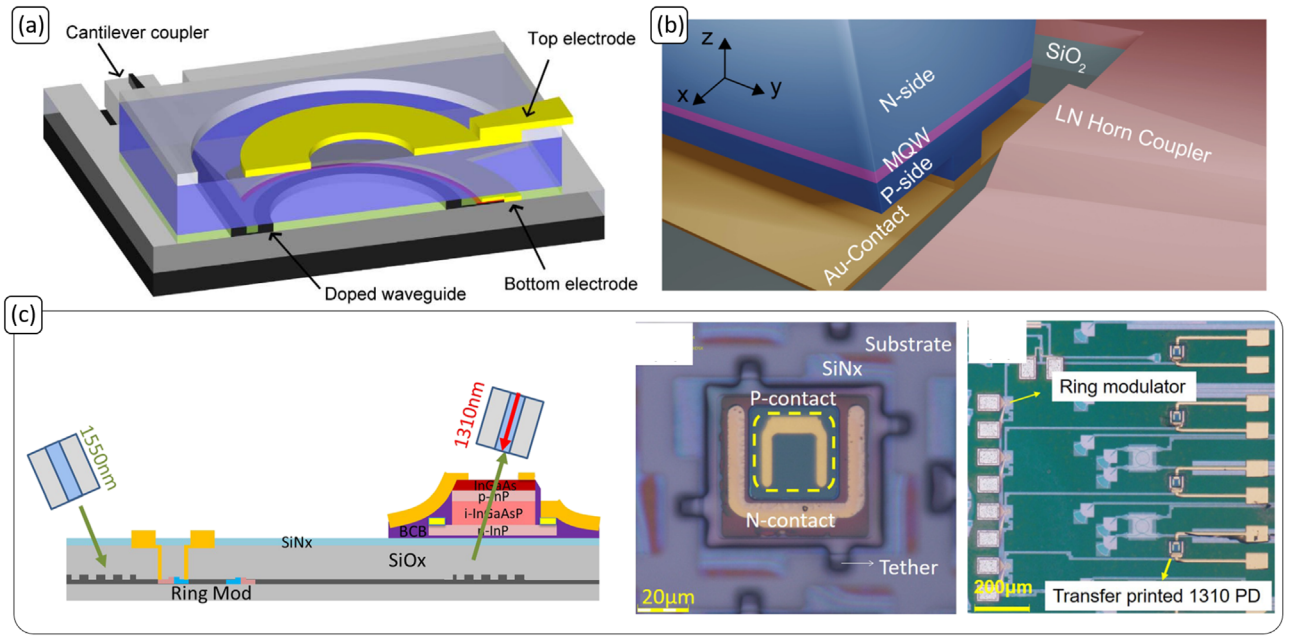

FIG. 6. (a) Lithium niobate membrane, integrated and post-processed on a Si PIC, giving the Si waveguide mode an effective second-order nonlinearity. Reproduced with permission from Chen *et al.*, Optica **1**, 112 (2014), Copyright 2014 The Optical Society.[67] (b) Recessed end facet coupling of a flip-chip bonded DFB laser for thin film lithium niobate PICs. Reproduced with permission from Shams-Ansari *et al.*, Optica **9**, 408 (2022). Copyright 2022 The Optical Society.[68] (c) Photodetectors transfer-printed onto grating couplers in the host silicon PIC, forming a four-channel transceiver. Zhang *et al.*, APL Photonics **4**, 110803 (2019).Copyright 2019 Authors, licensed under a Creative Commons Attribution (CC BY) License.[69]

process, this involves local etching of the receiver PIC to allow access to a waveguide facet. Importantly, this method requires alignment of not only the waveguides in the surface plane (designated x, y from here on), but also in depth (designated z). Matching of the waveguide z axes can be achieved by designing the material structure of the donor membrane to match the receiver PIC, as shown in Fig. 6(b). Placement accuracy in the xy plane will be discussed in Sec. IV. On the receiver PIC, a trench is etched into the material to allow placement of the donor device. Typically, the depth of the trench is defined by the thickness of a sacrificial layer in the receiver PIC that allows formation of a flat surface at a well-defined depth. For example, in silicon-on-insulator (SOI) receivers, the buried oxide layer forms a convenient etch layer, and the wet chemical selectivity to the underlying silicon substrate forms a flat platform for printing.[55,68] If the height of the trench requires trimming to match the donor material stack, then conformal deposition layers of metal or dielectric can be added to the receiver trench.[68] Using a metal layer on the receiver substrate also enables the possibility for direct electrical contacting of the printed surfaces.[71] Although waveguide ridges can be aligned, and, for materials with similar refractive index, cross-sectional geometries may be similar, there will a mode mismatch at the material transition, which can lead to point reflections and mode coupling losses.

C. Vertical coupling

Vertical grating couplers are a widely used component in PIC design, allowing for wafer scale testing, dense integration of components on compact dies and direct coupling to fiber arrays. Grating couplers have a footprint on the order of a few μm^2 and allow coupling between guided modes on-chip and free-space propagation, a convenient geometry for the integration for membrane devices at terminal ends of a PIC, either for light generation or detection, see Fig. 6(c). The spatial geometry of the grating coupler presents a suitable platform for printing membrane devices onto and is tolerant to some misalignment.[56] Other waveguides to vertical emission couplers are available on PIC platforms, including direct write polymer total internal reflection[72] and surface mirrors.[73] These are already being deployed in chip-to-chip integration platforms and may be useful for future transfer printing integration applications.

D. Directional waveguide coupling

Both facet and grating coupler structures detailed above terminate the waveguide devices in the transfer printed material. Semiconductor optical amplifiers can be deployed in a facet coupling scheme, but as previously noted, will still present a mode junction between the material platforms. An alternative coupling mechanism can be realized by using evanescent field coupling between the material layers.[74] Evanescent field couplers are commonly used in monolithic PICs, especially where precise control over the coupling fraction between coupled waveguides is required, for example in ring resonators.[75] The fractional power coupling between two co-propagating waveguides is determined by the relative modal effective indices of the guides, their physical separation and the length of the coupling section. Waveguide couplers are extremely sensitive to their separation due to the exponential decay of the evanescent waveguide mode field overlap, necessitating very high spatial accuracy transfer printing integration. One way to achieve the necessary alignment accuracy is to post-fabricate waveguides on the printed material as detailed above. However, for fully back-end compatible integration, alignment of the waveguide structures on the receiver PIC and donor membrane layer must be achieved. The various alignment schemes presented in the literature are detailed in Sec. IV.

Evanescent field coupling between printed layers avoids abrupt material transitions and allows for adiabatic mode transfer between layers. This in turn minimizes point reflections from device transitions and interface losses. It also enables the integration of multiple printed devices on a single host waveguide without terminating the transmission line, necessary for phase modulators, resonators, sensors, etc. Since the couplers are sensitive to geometrical separation of the waveguides, there are two degrees of freedom enabled by the printing scheme, first in the xy plane and second in the vertical separation of the waveguide layers, as shown in Fig. 7.

IV. HIGH-ACCURACY ALIGNMENT FOR DIRECTIONAL WAVEGUIDE TO WAVEGUIDE COUPLING

Evanescent field coupling between host PICs and transfer printed devices represents a flexible integration format, but for typical PIC waveguide geometries, requires spatial printing accuracy in the range of $\approx$100 nm. This constraint has been addressed in two main approaches: (1) design of misalignment tolerant layer-layer coupling schemes and (2) development of high-accuracy spatial registration methods. The details of a few variations on such schemes are presented below, and a comparison of their essential features is given in Table I.

A. Tapers and alignment tolerant couplers

The most straightforward way to deal with the alignment issue in evanescently coupled devices is to design optical structures that are tolerant to misalignment in the micrometer range, compatible with low-resolution alignment schemes.[47,65,76,80,82,83] By increasing the width of waveguides in the PIC and membrane device layers, the spatial overlap area for evanescent field coupling can be enhanced as shown in Fig. 8(a). The broader spatial mode of the waveguide devices results in a mode overlap integral that varies slowly as a function of misalignment in the xy plane and therefore a power coupling fraction that is tolerant to variations in the range of $\approx$1 μm. The tradeoff in this scheme is that the wider waveguides support multiple transverse modes. Minimal modal coupling in the single-mode to multi-mode sections can be achieved by using adiabatic mode tapers,[84] though this requires extra propagation length. Modal perturbations induced by the printed device material, and the vertical mode-transition region, can lead to excitation of higher order modes in the broad waveguide regions. Light in higher order modes will be seen as loss to the system as the underlying PIC transitions back to single-mode operation. These transitions have been demonstrated to work effectively for coupling between optical gain materials and passive PICs,[83] but the extended geometry and multi-mode coupling regions are not particularly well suited to compact device geometries, such as micro-resonators or point-emitters.

Another alignment tolerant coupling scheme has been proposed in the literature,[81] where the single-mode waveguide condition is maintained for both the host PIC and donor membrane layer devices. In this case, rather than tapering waveguides up to a broader area, the spatial overlap between the waveguide layers is varied as a function of

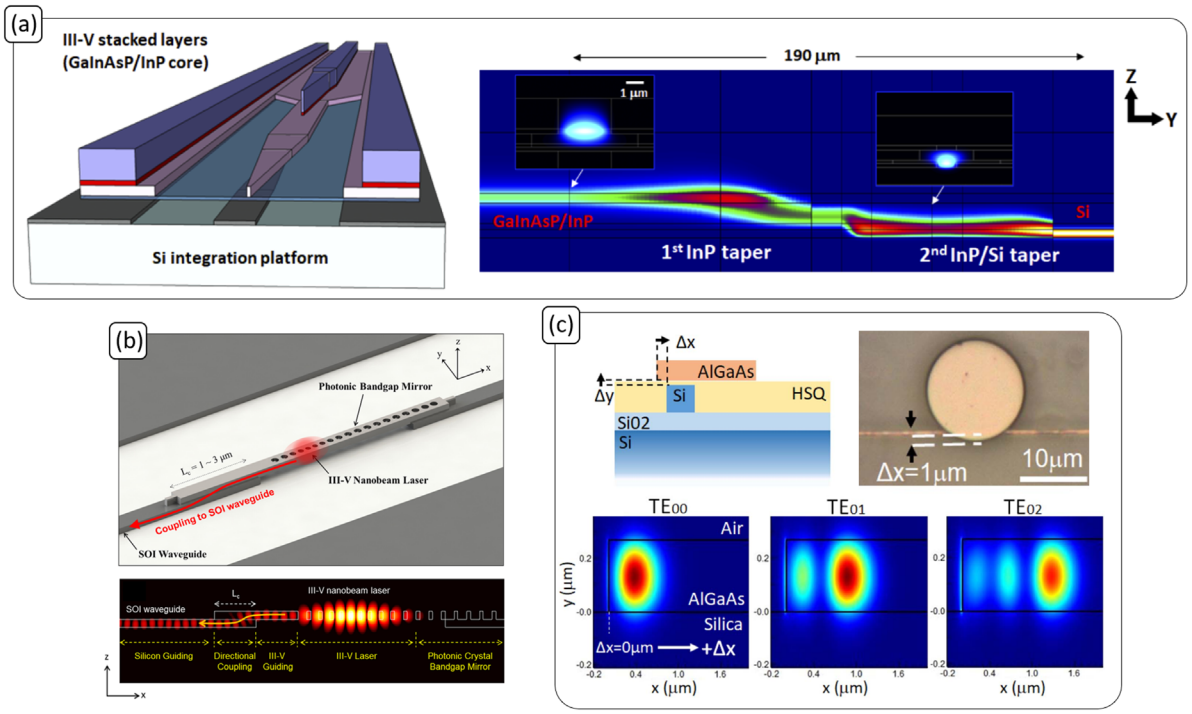

FIG. 7. (a) Coupling from host PIC to transfer-printed device, achieved with sequential adiabatic mode transitions in two taper sections. Reproduced with permission from Kou *et al.*, Opt. Express **28**, 19772 (2020). Copyright 2020 The Optical Society.[76] (b) Vertical directional coupling between a host Si waveguide, and printed III–V nanolaser. Reproduced with permission from Lee *et al.*, ACS Photonics **4**, 2117 (2017). Copyright 2017 American Chemical Society.[77] (c) Vertical coupling to a printed AlGaAs microdisk whispering gallery mode resonator. Reproduced with permission from McPhillimy *et al.*, Opt. Lett. **45**, 881 (2020). Copyright 2020 The Optical Society.[53]

TABLE I. Comparison of alignment techniques and technologies.

Alignment technique (or device design)	Alignment accuracy (or required accuracy)	Automation potential	Footprint	Scalability
In situ SEM[38]	Nanometric imaging, accuracy instead limited by printing process (100 nm)	Low, since user-feedback is continuously required	10 μm	Low, relying on SEM imaging and the serial printing of devices
Edge detection marker alignment[46,78]	<1 μm	High, requiring only simple optics and image processing software	10–100μm	High, parallel printing possible
In-situ structure overlap[39,77]	<500nm, based on width of waveguides	Low, typically requiring user-feedback control	Set by device footprint, typically 10 μm	Medium, serial device-by-device printing, though chips can feature multiple overlapped waveguides
Marker cross correlation[79]	<500nm	High, requiring only simple optics and image processing software	10–100μm	High, parallel printing possible
Tapered directional couplers[80]	Tolerant to micrometer-scale lateral misalignment	High, since micrometer-scale tolerances well within edge detection resolution limits	Large, adiabatic transitions 100 μm	High, limited only by relatively large footprint
Translationally invariant couplers[81]	Invariant to lateral misalignment, sensitive to rotational misalignment	High, rotational alignment sensitivity within traditional optical alignment techniques	Smaller than the above, though no experimental demonstrations have been made	High, given high alignment tolerances

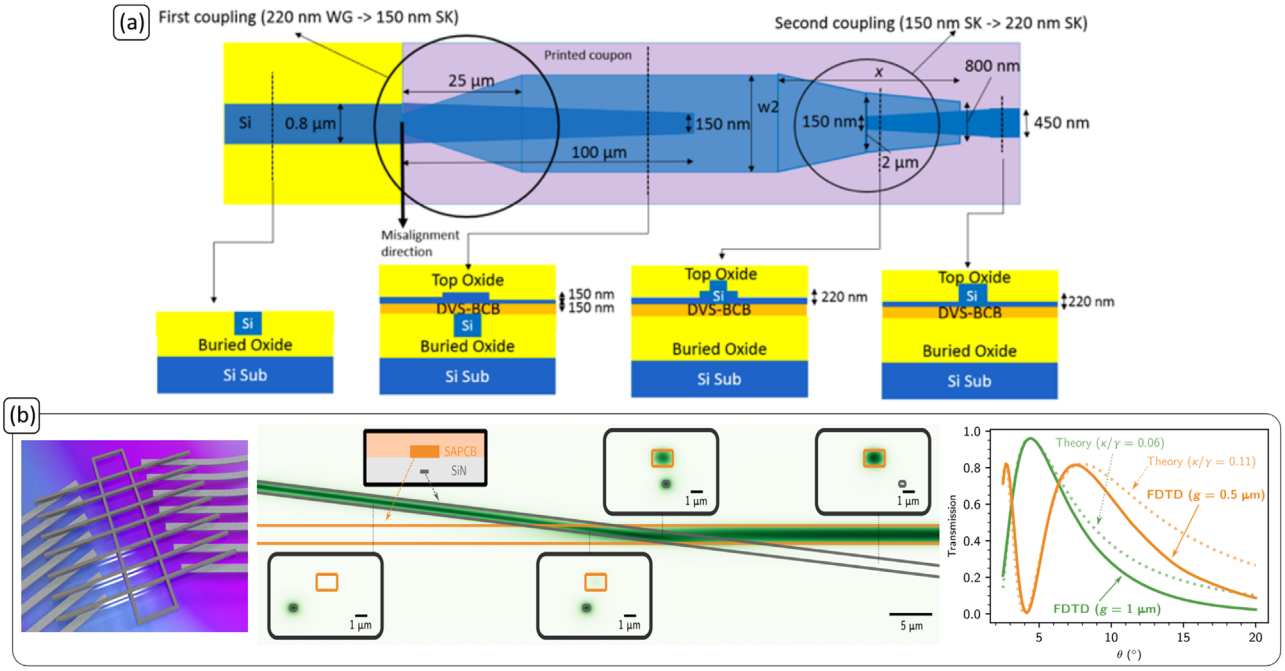

FIG. 8. (a) Broadband and alignment-tolerant adiabatic taper design. Reproduced with permission from Ye *et al.*, Opt. Express **26**, 2023 (2018). Copyright 2018 The Optical Society.[80] (b) Coupling scheme with translational symmetry between the printed device waveguides and angled host PIC waveguides.

propagation length, as shown in Fig. 8(b). This concept works similarly to the commonly employed dual material waveguide facet couplers where a high index waveguide is embedded in a larger cross section, lower refractive index waveguide. The high index waveguide is tapered from single mode guiding condition to a sub-guiding cross-sectional area, expanding the guided mode profile into the low index guide region. Efficient coupling between the structures occurs in the region where the effective modal index of the two waveguides are matched. In the transfer printed geometry, a lateral offset of the waveguide on the membrane with respect to the host PIC waveguide is used to vary the spatial overlap of the waveguide modes as a function of propagation length, producing efficient energy transfer within a compact footprint. The misalignment tolerance is significantly relaxed since a translation of the membrane device layer in the xy plane does not change the geometry of the overlap region. However, the coupler is sensitive to the relative rotational alignment of the two waveguides, as shown in Fig. 8(b). At a low relative angle, changes of a fraction of a degree can result in coupling fraction variations of up to 10%. Targeting near full energy transfer between waveguides, this rotational tolerance is achievable with conventional optical alignment techniques. The angular sensitivity also provides a potential route to precise power fraction design when using high-accuracy transfer printing systems.

B. High-resolution scanning electron microscope (SEM) imaging and transfer

To achieve very high-accuracy alignment of membrane photonic devices, the transfer printing stage can be realized using nano-probes *in situ* in a scanning electron microscope (SEM).[38,85,86] The direct imaging of the layers during the print process, along with the high precision control of the nano-manipulators, allows for nanometric accuracy in alignment, though the printing mechanics may limit this in practice. Although of very high precision, this method is serial in nature, requires direct user control, and is not compatible with the table-top transfer printing process flow detailed above. The nanoprobe pickup heads are typically needle designs that make deterministic pickup and deposition of materials particularly challenging.

C. Edge detection marker alignment

The most common form of alignment in transfer printing integration demonstrations makes use of on-chip fiducial markers or structures on the membrane devices that can act as registration markers. The general scheme for aligning structures during transfer printing using on-chip markers is presented in Ref. 46 and is shown schematically in Fig. 9(a). The donor and receiver chips are fabricated with fiducial marks that are located with lithographic precision relative to the on-chip waveguide structures. During the transfer printing process, the stamp head and the microscope imaging system are typically held in a constant location and the chips are manipulated below the stamp using high-accuracy translation and rotation stages. To align structures on the two chips to one another, first the chips are located and referenced relative to the motion control system coordinate system. Once the chips are registered in this basis, then motions between the two systems can be achieved using the common stage coordinate system. There are two crucial factors then that inform the accuracy with a transfer print process can be achieved. First is the positional accuracy of the stage system, that with current technologies can reach nanometric relative precision. The second limitation is the accuracy with which the fiducial marker can be registered with respect to the

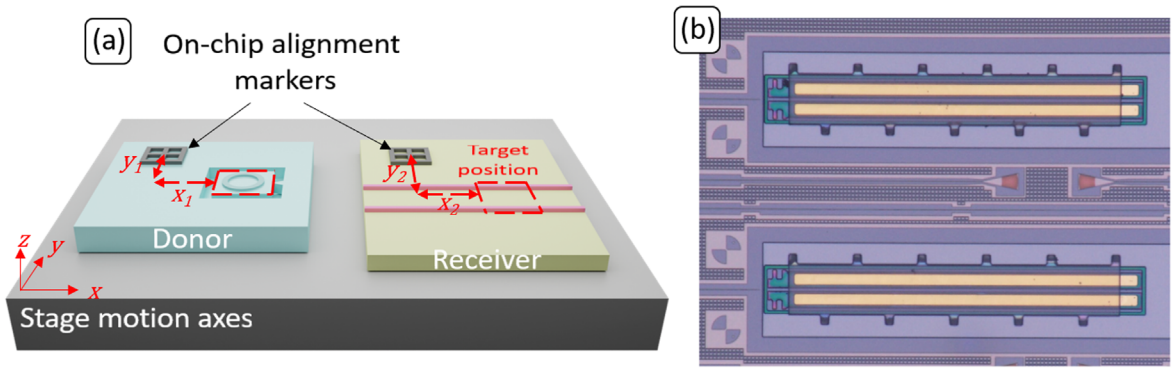

FIG. 9. (a) Transfer printing alignment schematic, with alignment markers patterned on donor and receiver chips. (b) Transfer printed InP lasers on an SOI PIC, with bowtie features on the SOI host and alignment features on the printed coupon. Reproduced with permission from Juvert *et al.*, Opt. Express **26**, 21443 (2018). Copyright 2018 The Optical Society.[55]

microscope field of view. By using high NA objectives and large pixel count camera systems, the effective pixel resolution of the imaging system can be in the sub-100 nm range, resulting in feature resolution effectively limited by the imaging optics. Effective fiducial registration can be achieved using a variety of image processing methods, which are variations on edge-detection. Image processing-based shape recognition is a well-established technology and can be carried out quickly and efficiently using minimal computational resources. The accuracy of the method is, however, limited by how well the position of a minimum feature, a line, can be located within an image. Although effective pixel resolution can be extremely good, other factors limit how well such marks can be imaged. Lithographically defined lines may have width variation in the few percent range due to fabrication tolerances and any asymmetry in a feature can affect its registered location. The quality of the imaging optics, typically using visible light, also limit the resolution with which a line can be defined to the few hundred nanometers range. As a result, the accuracy of automated edge detection-based alignment is limited to just sub-micron levels.[78] Improvements can be achieved using user feedback control but significant variance can be expected from device to device.

D. Local structure correlation and *in situ* monitoring

Substantial improvements in positional accuracy of printing can be achieved by employing local registration guide structures on the donor and receiver close to the device area. By incorporating these structures within the field of view of the imaging microscope during the printing process, a feedback mechanism can be employed to correct for any local misalignments. This technique has been used in particular, with fully suspended nanobeam waveguides, where the geometry of the guide and its support structure allow for spatial overlap registration with the receiver chip structures.[39,77,87–92] In Ref. 87, and shown in Fig. 10(a), the authors use the structure of the nanobeam and the surrounding material as a mechanical guide during printing. By imaging the membrane and receiver PIC in close proximity, their relative positions can be inferred by using either the broadening of the imaged overlap region, or local features such as line-space gaps, to measure when features are visible on the PIC through the membrane layer. Since the membrane nanobeam features are on the order of a few hundred nanometers in width, this mechanical overlap allows for positional accuracy in this range.

In Ref. 39, the authors print arrays of nanobeam waveguides in a single frame arrangement, which has the dual benefit of allowing transfer of multiple waveguides in a single shot, and provides a convenient alignment structure for print alignment, as shown in Fig. 10(b). By using a regular array of nanobeams and receiver waveguides, averaging of the mechanical overlap estimation can be carried out, with sensitivity both to the translational alignment in the xy plane and the rotational misalignment by simultaneous monitoring of both ends of the array. The authors demonstrate the effectiveness of this method through replication of the process on 16 arrays on a single chip. Nevertheless, direct automation of this process can be challenging and it is typically operated with user feedback control.

E. Marker cross correlation referencing

As noted above, a limitation of standard fiducial mark registration is imposed by edge detection resolution, mainly as a result of the optical imaging of line features. Marker registration recognition can be improved beyond this limit by making use of methods that rely on feature characteristics based on features other than the edges and shapes of fiducial marks. The use of non-periodic structures for object registration has been successfully developed in electron based imaging systems.[93] By employing the relative position of objects, which are more robust to fabrication variance than linewidth, the position of a marker can be more accurately determined. The center of a pattern can be estimated to below the pixel resolution by using multiple features for 2D pattern analysis if arranged appropriately. In Ref. 79, we presented a method for the automatic referencing of aperiodic grid fiducial markers using a 2D spatial cross correlation technique, shown in Fig. 11. In this method, aperiodic grids are lithographically defined on the donor and receiver substrates and captured using the optical microscope imaging system in the transfer print tool. The numerical cross correlation of the captured image, and an idealized grid is carried out to extract the center position of the marker within the image field of view. The field of view is related to the coordinates of the translation stage system and so local references on the donor and receiver can be referenced in the stage coordinate system. This allows for sub-100 nm accuracy referencing of structures on the two chips in a common

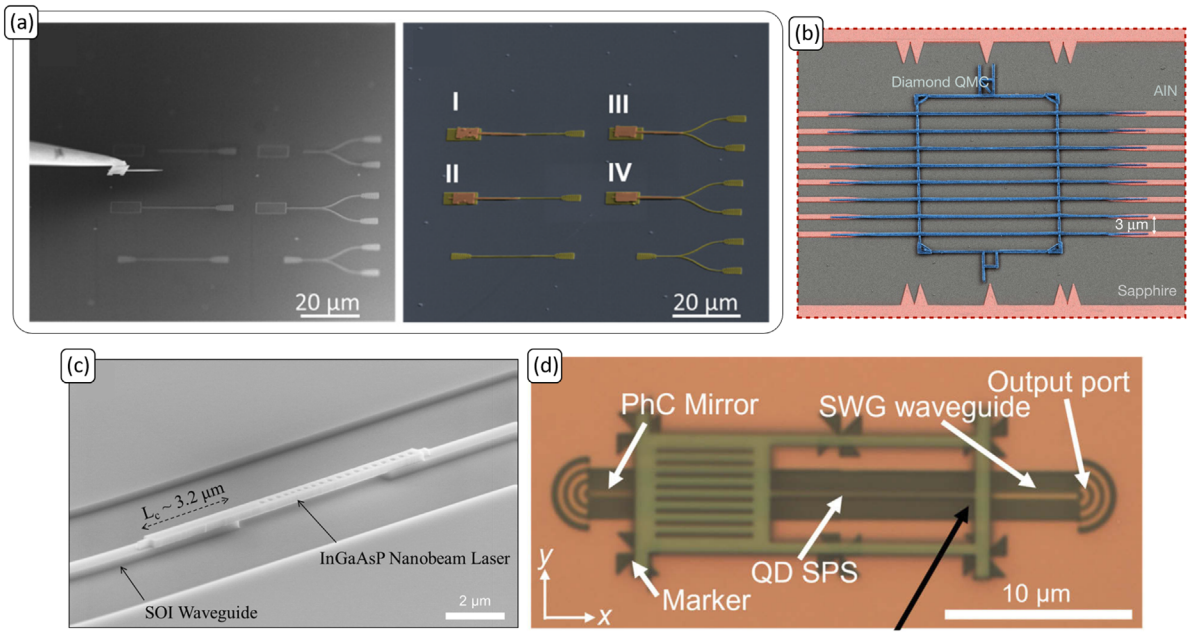

FIG. 10. (a) Nanobeam waveguides whose alignment is guided simply by the overlap of mechanical features. Reproduced with permission from Kim *et al.*, Nano Lett. **17**, 7394 (2017). Copyright 2017 American Chemical Society.[38] (b) Array of suspended diamond waveguides, printed onto an AlN PIC. Reprinted by permission from Wan *et al.*, Nature **583**, 226 (2020). Copyright 2020 Springer Nature.[39] (c) A printed nanobeam laser, aligned as above. Reproduced with permission from Lee *et al.*, ACS Photonics **4**, 2117 (2017). Copyright 2017 American Chemical Society.[77] (d) Unidirectional single photon collection from a QD, contained in a nanobeam waveguide, transfer printed with mechanical alignment onto a Si waveguide. Reproduced with permission from Katsumi *et al.*, Opt. Express **29**, 37117 (2021). Copyright 2021 The Optical Society.[88]

coordinate system that is then used to define stage motion to carry out the transfer printing stage. Measurements of calibration membrane printing were carried out for sets of devices in serial transfer and for multiple devices in a single shot. Figure 11(b) shows an SEM image of one of the test membranes after transfer, within a receiver grid. The results of the spatial alignment measurements are shown in Fig. 11(c). Finally, using a correlation image with the object to be transferred allows for this form of registration to be used where devices are randomly distributed on-chip with no rigid relationship to lithographically defined fiducial markers, e.g., in the case of populations of nanowire (NW) lasers. Figure 11(d) shows an SEM image of a transferred NW laser aligned with a lithographically defined silicon-on-insulator grating structure.

V. HYBRID PIC APPLICATIONS/DEMOS USING TP INTEGRATION

The fabrication processes detailed Secs. II–IV have enabled a range of remarkable demonstrations in heterogeneously integrated photonic chips. We cover a number of highlights in this section.

A. Optical sources and laser devices

One of the major applications drivers motivating work into heterogeneous integration for PIC chips is the demonstration of high-speed lasers, telecommunication channels, and transceivers.[69,94] Passive platforms, including silicon and silicon nitride, require integration of external optical sources, and a substantial amount of work has been carried out in this area and incorporates many of the coupling geometries detailed above. Demonstrations of the integration of vertical cavity surface emitting lasers (VCSELs) onto a SiN PIC platform, as shown in Fig. 12(a), have been made.[56] VCSEL devices were fully fabricated on their native substrate in array format and then directly printed onto vertical grating coupler sections of the SiN chip. The active aperture of the VCSEL, in the few micrometer diameter range, matches the area of the grating coupler well and is tolerant to misalignment between the structures of a few hundred nanometers, with an efficiency of around 25% to each of the in-plane output waveguides at either side of the grating.

In contrast with the VCSEL designs where the full laser cavity is realized in the III-V material and then vertically coupled into the host PIC, laser cavities can also be achieved in a dual material format. In Ref. 83, the authors demonstrate an integrated laser device where the III-V gain section is evanescently coupled to a passive silicon PIC and a Bragg grating waveguide acts as a distributed feedback element. The resultant distributed feedback laser (DFB) is then directly coupled to the silicon PIC. To mitigate misalignment of the post-processed III-V laser ridge with the silicon waveguide, the silicon ridge is tapered up to 6.3 μm for the gain region, and both the III-V and silicon ridges are tapered down to around a micrometer in the mode transfer region.

Recently, exciting advances have been made in the development of lithium niobate on insulator (LNOI) as a PIC platform,[95,96] presenting low propagation loss and useful $\chi^{(2)}$ and $\chi^{(3)}$ optical nonlinearities, though again, for full systems-on-a-chip integration, this platform requires external optical sources.[97] In Ref. 68, the authors present the integration of an InP based, edge emitting DFB laser with a LNOI photonic chip. The DFB is printed with its p-doped side onto the PIC substrate, making direct contact with a metal conductor layer

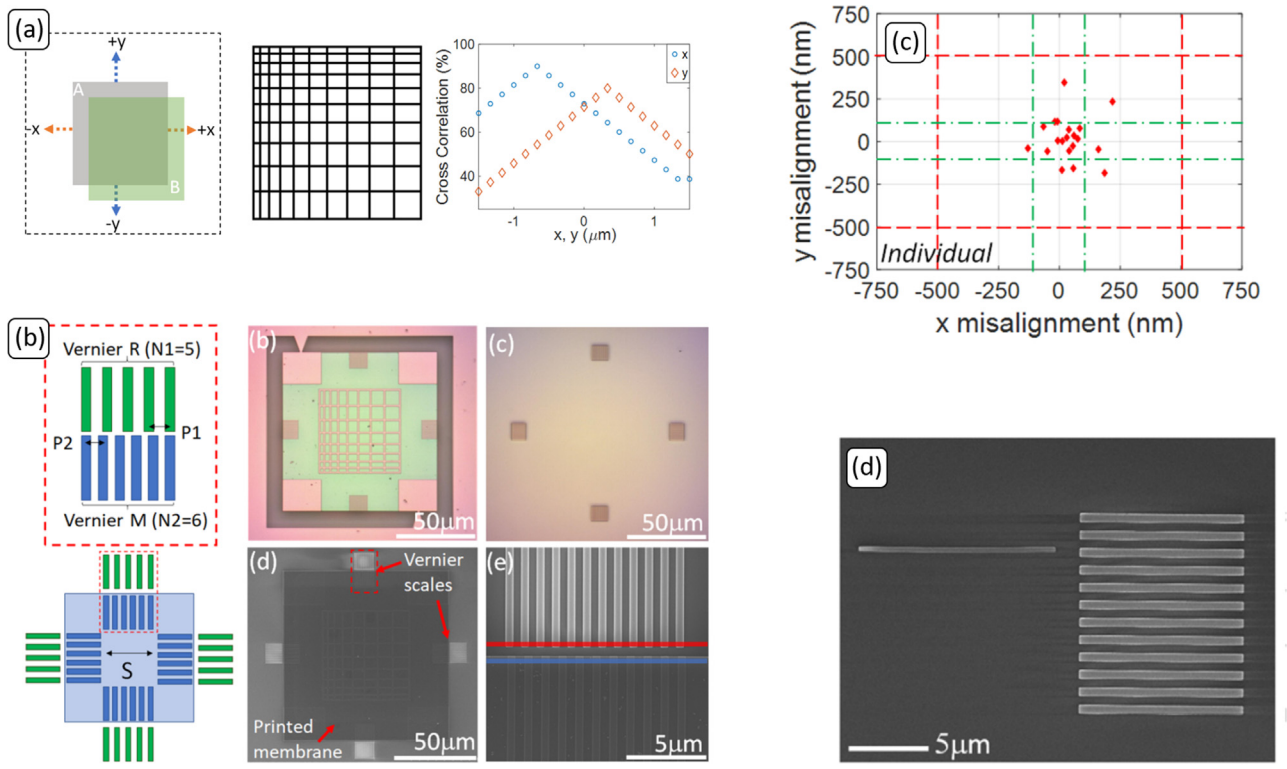

FIG. 11. (a) Schematic of alignment process using the cross correlation of aperiodic grid markers. (b) Definition of donor and receiver Vernier grids, with (bottom right) SEM of printed membrane (c) Resulting spatial alignment statistics. (d) Alignment of a nanowire laser with a monolithic Vernier scale. All adapted from McPhillimy *et al.*, ACS Appl. Nano Mater. **3**, 10326 (2020). Copyright 2020 Authors licensed under a Creative Commons Attribution (CC BY) License.[79]

for current injection, see Fig. 12(b). The waveguide modes in both materials are designed for efficient spatial overlap. The lateral dimensions are tapered up to a few micrometers in width to minimize misalignment coupling loss and the vertical heights are matched through control of the gold contact layer deposition on the LNOI chip.

The thermal heat sinking of active laser and gain sections on host PICs is an important consideration to control emission wavelength and avoid parasitic heating effects in nearby passive PIC elements. In Ref. 58, the authors present a study of the thermal behavior of InP based edge emitting laser diodes printed onto a variety of substrates, including commonly employed adhesion layers, e.g., BCB polymer. In this study, the authors used mesa etching of the laser structures to allow for top-side electrical access to both p and n contacts. This also allows study of printing onto a metal substrate layer without using this layer as an electrical injection point. As expected, integration onto thermally insulating layers such as BCB and silica leads to degraded thermal performance of the lasers and spatially extended heating around the printed laser. Direct printing onto silicon and metal layers allows for more efficient thermal transport and suggests that where this is a primary concern, edge coupled lasers in a PIC trench provide a significant improvement over evanescently coupled devices printed onto PIC uppercladding or adhesion layers.

Using the mechanical structure correlation alignment method detailed above, single-mode, optically pumped, nanobeam photonic crystal cavity lasers have been integrated with waveguide PICs.[77,89,98,99] In Ref. 89, these devices exhibit distributed feedback laser cavity action in the III-V nanobeam layer that is then efficiently coupled in one direction into the silicon PIC, making use of asymmetric design of the photonic crystal cavity, see Fig. 12. In direct contact couplers, the directional coupling is more similar to a multi-mode interference device (with two modes) than an evanescent field coupler, and therefore, optical beat lengths can be on the order of micrometers.[77] Direct contact nanobeam devices are, therefore, sensitive not only to lateral misalignment, but also axial overlap of the two waveguiding layers that defines the optical coupling fraction, requiring alignment to within a few hundred nanometers to allow for full modal power transfer. III-V micro-disk lasers have also been demonstrated, transferred onto silicon micro-pillars, though these were not coupled with on-chip waveguide devices.[54] Finally, beyond the telecommunications band, mid-IR quantum cascade laser devices have been successfully transfer printed onto silicon-on-sapphire waveguides using a tapered coupling region for mode transfer.[100]

B. Optical detectors

Photodetectors are available on foundry accessible PIC platforms, making use of Germanium layers for example.[101] Nevertheless, it can be advantageous to add active photodetector layers as a post-growth stage via transfer printing. For example, high-speed germanium-on-silicon photodetectors have been successfully integrated onto an SOI

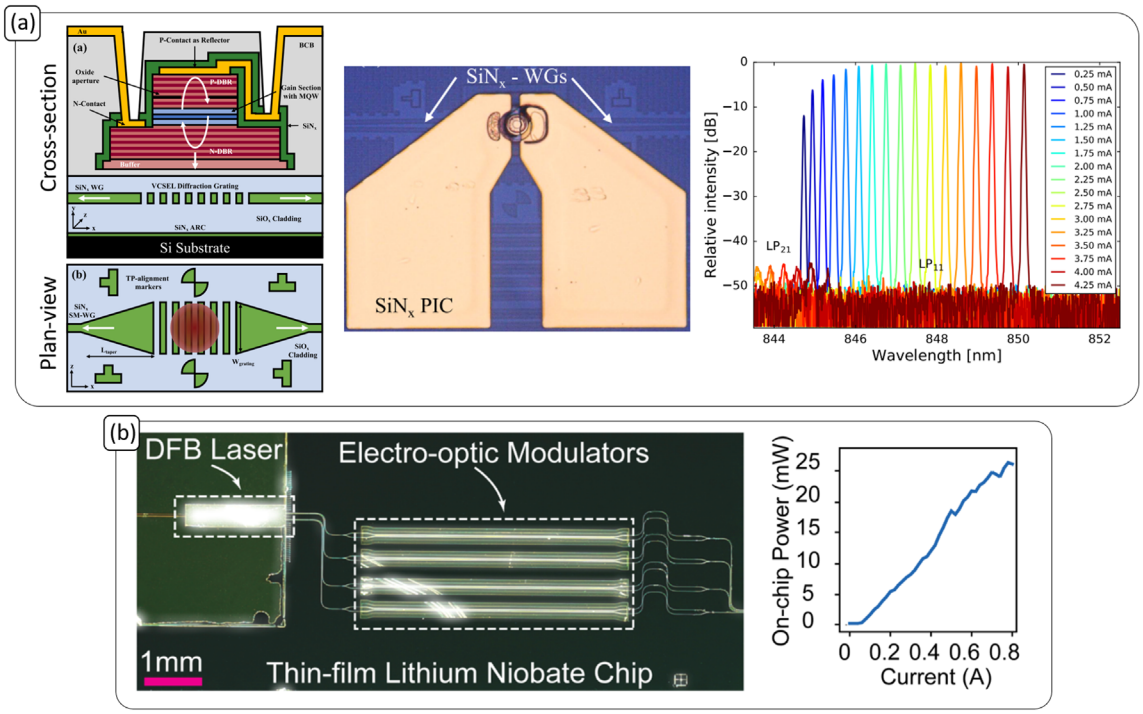

FIG. 12. (a) Cross-section, optical micrograph, and output spectrum of a transfer-printed bottom-emitting VCSEL, coupling via a diffraction grating into SiN waveguides. Reproduced with permission from Goyvaerts *et al.*, Optica **8**, 1573 (2021). Copyright 2021 The Optical Society.[56] (b) DFB laser integrated with thin film LNOI chip, combining on chip generation and electro-optic modulation. Reproduced with permission from Shams-Ansari *et al.*, Optica **9**, 408 (2022). Copyright 2022 The Optical Society.[68]

waveguide platform demonstrating 40 G/s operation, using an alignment tolerant layer to layer trident-taper coupling section, Fig. 13. Vertically coupled III-V photodetectors have also been realized by printing devices directly onto grating coupling regions,[70] Fig. 13. Furthermore, the choice of active material absorbing in the 1310 nm wavelength range allows for transparency of the photodetector to signals coupling out of the chip in the 1550 nm range and therefore use of a common fiber connector for upstream and downstream signals. Large arrays of GaAs based photodetectors were integrated onto SiN PICs and wavelength selective arrayed waveguide gratings for coarse spectrometry measurements;[102] see Fig. 13.

Integration of optical sources, waveguides, and detectors on a single chip has been realized in a III-N platform, where the waveguide channel was implemented as a multi-mode waveguide fabricated post printing of the active optical elements.[103]

C. Nanoscale quantum emitters

The integration of single photon emitters embedded in guided wave structures with large scale PICs is an outstanding challenge particularly as the properties of these nanoscale devices vary significantly across a population. A variety of geometries have been proposed for such systems, including quantum-dot-in-wire,[105] nanobeam cavities,[38,88,106–108] quantum dot containing monolayers[109] and waveguide arrays.[39] The integration of quantum-dot-in-wire devices with SiN waveguide PICs was achieved using a post-fabrication stage to ensure accurate alignment of the wires with the SiN waveguides,[105] though deterministic integration of nanowire based devices has been demonstrated by a number of groups.[24]

Integration of single nanobeam waveguides incorporating quantum dot emitters has been achieved on silicon[106] and LNOI,[107] as in Fig. 14(a). Single nanobeam cavities, that can incorporate a back reflector[88] for unidirectional coupling to the PIC, are directly vertically integrated with the underlying waveguide platform, and efficient power transfer enabled by tapering of the nanobeam waveguide, see Fig. 14. Coupling of single photon emission from the nanobeam to the PIC has been demonstrated[90] with a two cavity system presented in Ref. 87. In these devices, the use of supporting structures around the nanobeam allow for mechanical robustness of the ultra-small devices and improved alignment through mechanical structure monitoring.

The authors in Ref. 39 present an impressive scaling of the integration of nanobeam cavities containing quantum emitters, germanium, and silicon-based color centers in this case. As noted previously, by using arrays of diamond waveguides for integration with a host AlN PIC, the authors make use of distributed mechanical features to allow the precise alignment required for this geometry, see Fig. 10(b). Furthermore, each individual waveguide contains a number of color center emitters that can be optically pumped from an off-chip vertically coupled source to enable single photon emission into the guided wave structures. Each waveguide array is formed of eight waveguides, and the authors demonstrate successful integration of 16 arrays onto a single receiver chip, totaling 128 coupled waveguide devices. Serial measurements of each channel shows single photon emission into the waveguide channel from a color center emitter in the associated

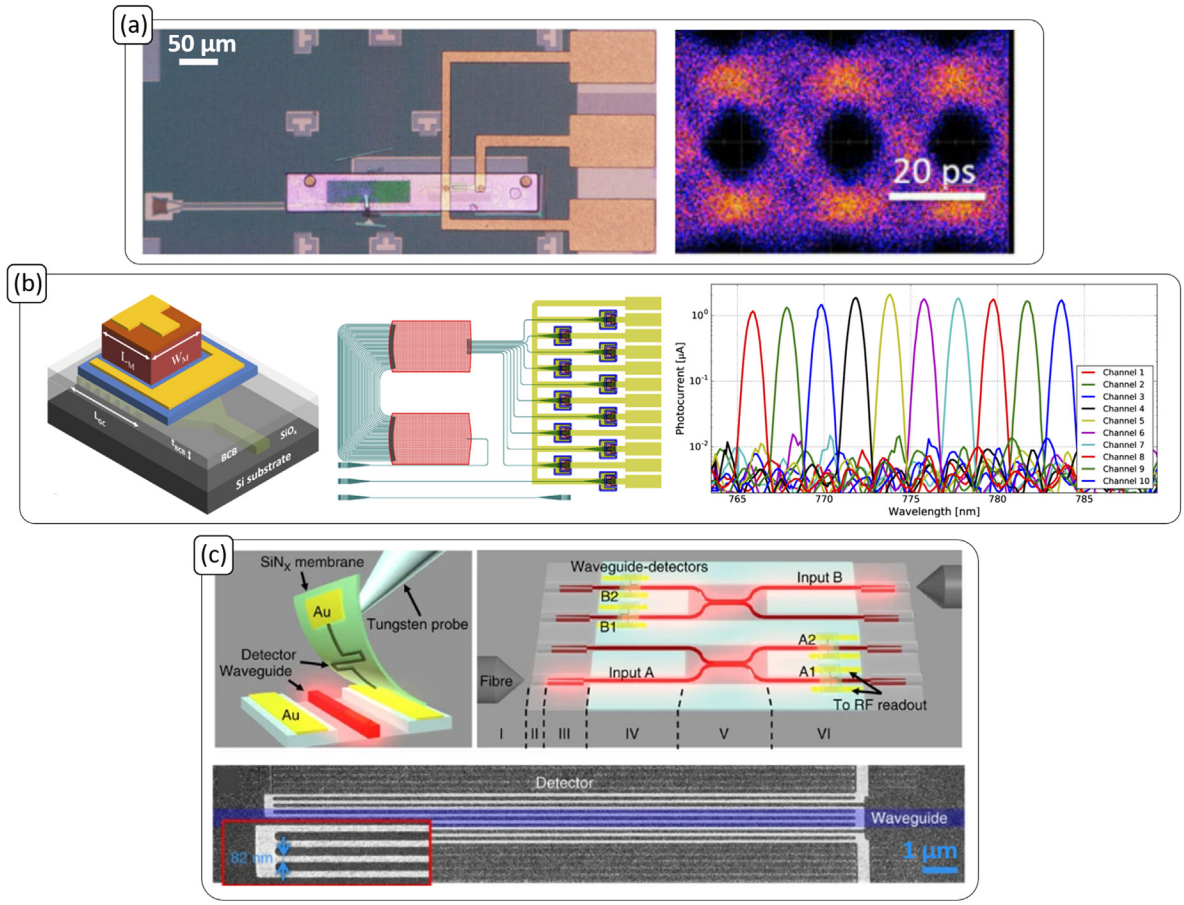

FIG. 13. (a) Ge photodiode printed onto Si waveguides, with eye diagram at 40 Gbit/s. Reproduced with permission from Ye *et al.*, J. Lightwave Technol. **36**, 1249 (2018). Copyright 2018 IEEE.[101] (b) GaAs p-i-n photodiode, forming part of an on-chip AWG spectrometer (middle), with the photocurrent response of each channel shown (right). Reproduced with permission from Goyvaerts *et al.*, Opt. Express **28**, 21275 (2020). Copyright 2020 The Optical Society.[102] (c) A single-photon detector, formed by superconducting nanowires on a transferred membrane, integrated with AlN waveguides. Najafi *et al.*, Nat. Commun. **6**, 5873 (2015). Copyright 2015 Authors, licensed under a Creative Commons Attribution (CC BY) License.[104]

diamond channel, see Fig. 14(b). From an integration point of view, the scaling in this demonstration represents a major milestone in the field, though the performance is still some way from the production of a large array of indistinguishable single emitters in individual channels. The authors present one possibility for tuning emitter wavelengths using mechanical strain, and note the challenge in fabricating single color centers in each channel.

D. Non-linear optics and sensing

Important applications for hybrid material integrated photonic chips include optical signal processing, non-linear optics and opto-mechanics. For example, integration of materials with a second-order optical non-linearity on silicon allows for electro-optic modulation that is not possible in silicon alone. Lithium niobate modulators have been realized on both silicon[67] and silicon nitride platforms as evanescently coupled layers on the host PIC platforms. Better modulation performance can be achieved by coupling the full optical mode into the lithium niobate material, requiring fabrication of waveguide structures in the transfer printed layer and accurate alignment of the process. The alternative is to use the maturing lithium niobate-on-insulator platform as the base PIC and integrate laser sources and other components via transfer printing.[68]

Third order optical non-linearities in integrated waveguides are commonly used for classical and quantum signal generation through stimulated and spontaneous four wave mixing, respectively. The selection of platform usually takes into account tradeoffs between waveguide propagation losses, transparency window, non-linear generation efficiency, and non-linear loss. Each material platform provides a particular mix of these performance metrics, and the highest efficiency non-linear generation does not necessarily align with platform maturity for scale and complexity of host PICs.[112] For example, the Kerr non-linear coefficient of silicon nitride is relatively low, while silicon presents significant two photon absorption losses in the telecommunications wavelength range. By integrating III-V materials onto passive PIC platforms, enhanced non-linear performance in resonator devices

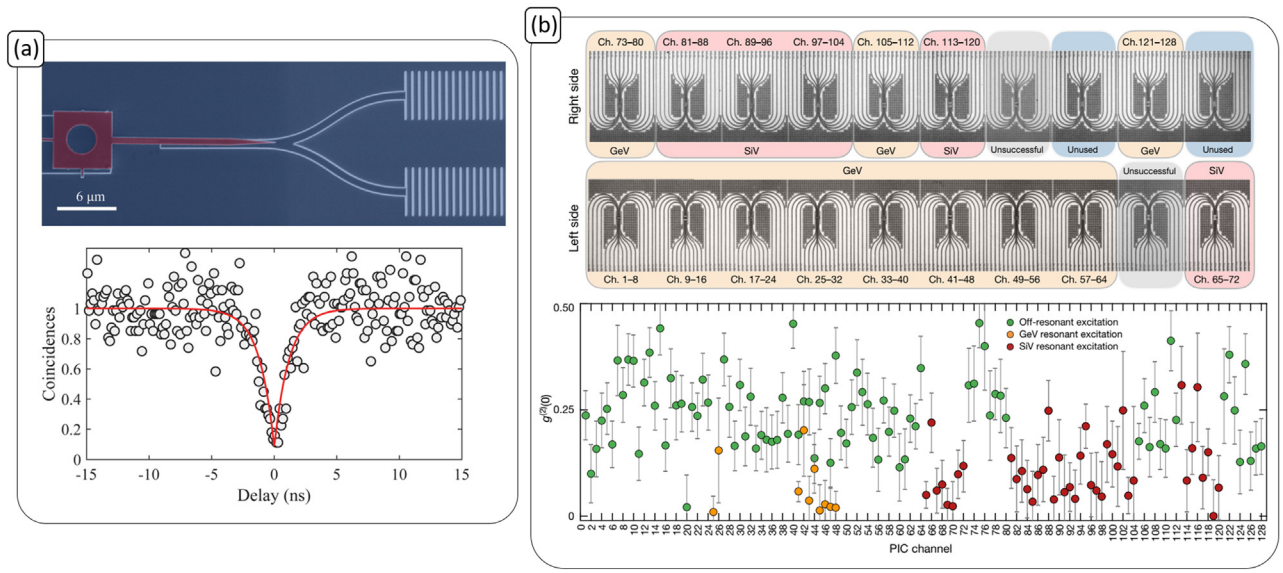

FIG. 14. (a) An InAs quantum dot, embedded in an InP nanobeam waveguide and transferred to a lithium niobate y-branch waveguide, with (bottom) second-order photon correlation showing single-photon emission. Reproduced from Aghaeimeibodi *et al.*, Appl. Phys. Lett. **113**, 221102 (2018) with the permission of AIP Publishing LLC.[107] (b) Top: An array of 16 quantum diamond micro-chiplets transferred onto an AlN PIC, each containing single-photon emitting color center defects. Bottom: Autocorrelation measurements, showing single photon emission from 128 transferred devices. Reprinted by permission from Wan *et al.*, Nature **583**, 226 (2020). Copyright 2020 Springer Nature.[39]

can be achieved whilst making use of the low loss, scalable PICs for signal routing and modulation. As shown in Fig. 7(c), AlGaAs microdisks have been directly printed onto a silicon platform for four wave mixing applications.[53] AlGaAs has a higher non-linear coefficient than silicon and minimal two photon absorption losses around a pump wavelength of 1550 nm.

Hybrid materials integration has been used to realize optomechanical structures, where lithium niobate is used as a base layer for its piezo-electric properties and a silicon optical cavity is integrated as a microwave-optical wavelength transducer.[45] Figure 15(a) shows a false color image of the hybrid integrated microwave-optical transducer with the silicon photonic cavity in blue. The resonance spectrum under microwave excitation of the lithium niobate layer is shown in Fig. 15(a).

In Ref. 111, a photonic thermometry device is presented, integrating a GaN-on-sapphire micro-resonator and a diamond microdisk, on a single bus waveguide. By using wide-bandgap materials for this application, a common issue of self-heating from the optical signal, common in silicon PIC devices, can be avoided. Furthermore, the integration of GaN and diamond micro-resonators within a few tens of μm chip footprint, see Fig. 15(b), enabled simultaneous measurement of the thermal resonance shift of both devices on a single waveguide, reducing measurement errors compared with single resonance techniques. Figure 15(c) shows a section of the transmission spectrum of the hybrid device with environmental temperature as a parameter. The difference in temperature dependent shift between the diamond and GaN resonances is due to their material dependent thermo-optic coefficients. The near unity correlation of these shifts as a function of temperature, and the fact that the resonators are so closely spaced, means that any wavelength shift can be attributed only to temperature variation. The integrated device produced a measurement error of 9 mK, representing a nearly fivefold improvement over monolithic silicon devices.

VI. DENSE INTEGRATION AND SCALING

Most of the results presented in this review concern the integration of a single printed device type onto a host PIC. One of the most promising aspects of transfer printing as an integration process is that it allows for multiple material integration with high density on-chip. In Refs. 89 and 87 the authors show serial printing of two photonic crystal nano-beam cavities within a few micrometers of one another. In the former case, these are two nanolaser devices and in the latter, the nanobeams contain single photon emitters, see Fig. 16. Figure 15(b) shows integration of microdisk resonators in AlGaAs and diamond materials onto a GaN-on-sapphire PIC.[110] The multiple materials are spaced within a few tens of micrometers of one another and show the potential for multi-device integration in a serial transfer printing process.

For devices with footprints larger than 10×10 μm^2, the microfabrication of the polymer stamp head can be defined to avoid contact with adjacent devices during the print release stage. The transfer and dense integration of micrometer scale devices in compact areas is more challenging as the stamp head will make contact with already placed devices in multi-stage assembly jobs. In Ref. 110, serial printing of nanowire devices from different donor substrates was demonstrated with inter-device spacing in the micrometer regime, see Fig. 16(a). In this work, a multi-stage transfer process was employed using polymer stamps with different levels of adhesion to allow deterministic transfer to the target substrate. The deterministic integration of nanowire devices for on-chip systems is the subject of recent work[113,114] and allows for 3D stacked geometries in dense arrangements.[115]

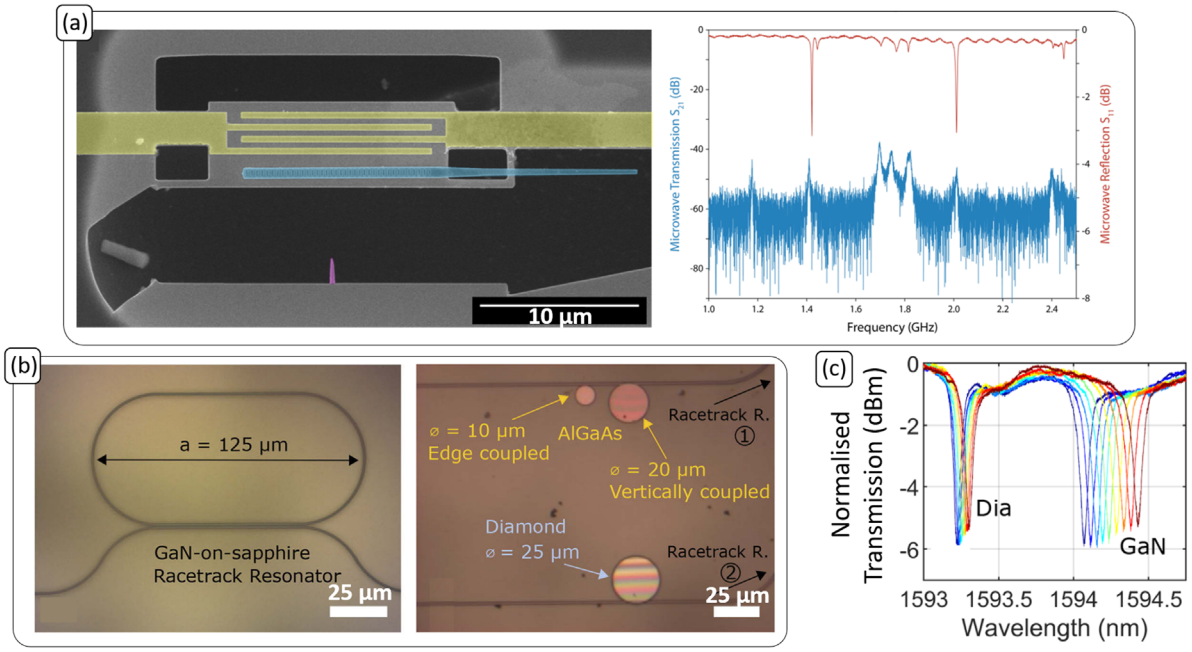

FIG. 15. (a) Micro-assembled Si photonic crystal nanobeam (in blue), on a suspended lithium niobate acoustic resonator, forming a hybrid optomechanical device, with microwave spectrum shown (right). Reproduced with permission from Marinkovic *et al.* Nano Lett. **21**, 529 (2021). Copyright 2021 Authors, licensed under a Creative Commons Attribution (CC BY) License.[45] (b) Monolithic GaN on sapphire racetrack resonator, integrated with both AlGaAs and diamond microdisks in an area commensurate with the PDMS stamp dimensions. Reproduced with permission from Jevtics *et al.*, Opt. Mater. Express **11**, 3567 (2021). Copyright 2021 The Optical Society.[110] (c) Thermal tuning of the hybrid diamond-GaN chip, showing the red-shifting of each material's resonances. Reproduced with permission from Smith *et al.*, Opt. Express **29**, 29095 (2021). Copyright 2021 The Optical Society.[111]

Large regular arrays of planar devices have been achieved where relative placement precision in the micrometer range is acceptable.[116] To demonstrate similar wafer scale integration for PICs will require rapid precision automated alignment processes, *in situ* device metrology and process development for high yield[117] and high throughput integration. Furthermore, to enable arbitrary device layouts on receiver PICs that may differ from efficient fabrication layouts on donor wafers, active device selection and printing will be

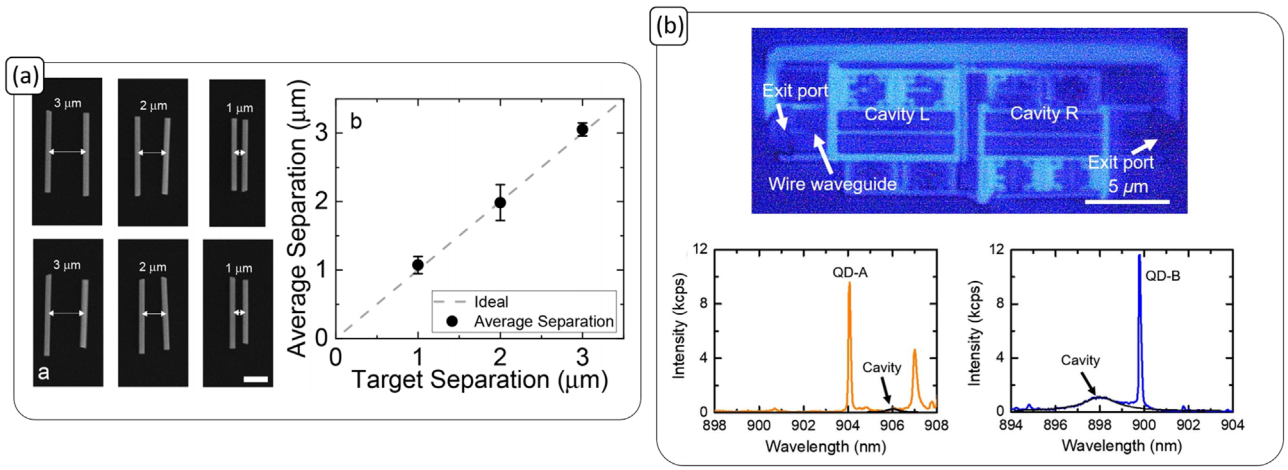

FIG. 16. (a) Deterministic transfer of serially printed nanowires, whose minimum separation of 1 μm is well within the area of the PDMS stamp. Reproduced with permission from Jevtics *et al.*, Opt. Mater. Express **11**, 3567 (2021). Copyright 2021 The Optical Society.[110] (b) Two nanobeam cavities, integrated by transfer-printing onto the same waveguide. The cavities contain QDs, whose respective emission spectra are also shown. Reproduced with permission from Katsumi *et al.*, Optica **5**, 691 (2018). Copyright 2018 The Optical Society.[87]

required[36,118] to allow large scale print on demand with throughput compatible with manufacturing technologies.

VII. CONCLUSIONS

The field of transfer printing enabled PIC technologies is evolving rapidly and key demonstrations in passive PICs with augmented functionality are becoming well established. Integration of waveguide laser sources, single photon emitters, photodetectors and non-linear optical elements can be realized in waveguide-coupled geometries with placement accuracies well into the sub-micron regime. A range of interlayer coupling mechanisms are available, including vertical grating couplers, direct facet coupling and waveguide directional couplers, allowing use of rapid low accuracy alignment processes, or high precision placement. The availability of PIC foundry technologies in silicon, silicon nitride, glass, and III-V materials, along with emerging capabilities in lithium-niobate-on-insulator, will underpin scaling to large, complex PICs with local device functions accessible through transfer printing of micrometer scale components that can be fabricated in more focused facilities. Outstanding challenges in automation, selective device printing, and *in situ* process monitoring need to be addressed to scale this technology to manufacturing throughput and yield levels.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Jack Andrew Smith: Data curation (equal); Investigation (equal); Writing – original draft (equal); Writing – review & editing (equal). **Dimitars Jevtics:** Investigation (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **Benoit Guilhabert:** Investigation (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **Martin D. Dawson:** Conceptualization (supporting); Funding acquisition (equal); Investigation (equal); Project administration (supporting); Supervision (equal); Writing – review & editing (equal). **Michael J. Strain:** Conceptualization (lead); Funding acquisition (equal); Investigation (equal); Project administration (equal); Supervision (lead); Writing – original draft (lead); Writing – review & editing (lead).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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