Adaptive Smith Predictor for Enhanced Stability of Power Hardware-in-the-Loop Setups

Zhiwang Feng, Rafael Peña-Alzola, Senior Member, IEEE, Mazheruddin H. Syed, Member, IEEE, Patrick J. Norman, Member, IEEE, and Graeme M. Burt, Member, IEEE

Abstract—The stability and accuracy of power hardware-in-the-loop (PHIL) setups are sensitive to and deteriorated by the dynamics and non-ideal characteristics of their power interfaces, such as time delay, noise perturbation, and signal distortion. In this paper, a compensation scheme comprising a Smith predictor compensator is proposed to mitigate the impact of time delay on PHIL stability. Furthermore, an online system impedance identification technique is leveraged to enhance the robustness of the compensator and facilitate the compensation scheme with adaptivity to system impedance variation. Analytical assessment, simulation results, and PHIL experimental results are presented to verify the proposed compensation scheme. This scheme enables robust and stable testing of novel power technologies under varying impedance ratios representative of the complex scenarios emerging within the power sector.

Index Terms—Power hardware-in-the-loop (PHIL), Smith predictor, time delay, compensation, robustness and stability.

NOMENCLATURE

Abbreviations
ADC  Analog-to-Digital Converter
DAC  Digital-to-Analog Converter
DFT  Discrete Fourier Transformer
DRTS Digital Real-Time Simulation
GM  Gain Margin
GTAI Giga-Transceiver Analog Input
GTAO Giga-Transceiver Analog Output
HuT Hardware under Test
IR  Impedance Ratio
ITM  Ideal Transformer Model
LPF  Low-Pass Filter
PHIL  Power Hardware-in-the-Loop
PI  Power Interface
PM  Phase Margin
SDFT Sliding Discrete Fourier Transformer
SOI System of Interest
SP  Smith Predictor

Functions
\( C_{eq}(s) \) Smith predictor compensator transfer function
\( G_1(s) \) DAC card transfer function
\( G_2(s) \) Power amplifier transfer function
\( G_3(s) \) Current sensor transfer function
\( G_4(s) \) ADC card and low-pass filter transfer function
\( G_{PI}(s) \) Power interface transfer function
\( G_{PI}^*(s) \) Delay-free power interface transfer function

This work was supported by the European Union’s Horizon 2020 research and innovation program under grant agreement No 870620 in the ERIGrid 2.0 project. The authors are with the Institute for Energy and Environment, University of Strathclyde, Glasgow, G1 1RD, UK.

\( T_C(s) \) PHIL system closed-loop transfer function
\( T_{CI}(s) \) Ideal system of interest closed-loop transfer function
\( T_O(s) \) PHIL system open-loop transfer function
\( T_{OI}(s) \) Delay-free open-loop transfer function
\( \delta T_O(s) \) Estimation of the nominal delay-free model \( T^*_{O}(s) \)

I. INTRODUCTION

POWER hardware-in-the-loop (PHIL) plays a significant role in accelerating the research and development of power technologies by enabling repeated and non-destructive real-time testing under a broad range of scenarios [1]–[10]. This advanced real-time testing methodology has been extensively leveraged for the in-depth modelling and assessment of renewable energy technologies including photovoltaic system [3], [4], energy storage system [5], variable-speed wind turbines [6], etc., prototyping of power apparatus [2], [7], verification of control strategies [8], black start testing of grid-forming converter [9], and power system education [10].

An interface algorithm defines the manner of power transfer and the configuration of a PHIL setup, examples of which include the ideal transformer model (ITM), damping impedance method (DIM), and partial circuit duplication (PCD), etc. [1], [11]. The ITM interface is widely-utilized owing to its ease of implementation. However, as demonstrated in [11], [12], its stability is strictly constrained by the impedance ratio between the simulation side and hardware side and the time delay as characterized in [13]. Such a stringent impedance ratio constraint is not always ensured in practice due to the impedance variations of the emulated power network and hardware components during an experimental scenario run.

Many research efforts have been devoted to improving the stability of a PHIL system either by decreasing the impedance ratio between the software and hardware side or by improving the system stability margin through the implementation of compensation schemes. The former includes the impedance shifting method [14], the hardware inductance addition method [15], while the latter involves the feedback current filtering [15], [16], multi-rate partitioning interface [15], [17], Bergeron transmission line model based multi-time-step interface [18], \( H_\infty \) optimal control based interface [19], and open-loop inverter based interface [20], [21] and its optimal compensation [20]. The impedance shifting approaches are limited by the availability of appropriate physical impedance and suffer from deteriorated simulation accuracy [14], [15], while the performance of the compensation methods is limited by the...
bandwidth of the power interface [15], [16], or is dependent on the dynamic coupling and clock synchronisation between subsystems with different time-steps [15], [17], [18]. Although the proposed methods realise stable PHIL setups by redefining the impedance ratio at the point of common coupling or by manipulation of interface signals, the methods are passive, i.e., only applicable to the setup for which they are designed and any changes in the hardware or software networks may lead the system to instability.

Considering the aforementioned limitations, inspired by the Smith predictor applied in [19], [22], this paper presents an adaptive Smith predictor based PHIL stabilization scheme that presents high robustness to variations of impedance. The main contributions of this paper are summarized as follows:

1) A Smith predictor (SP) criterion inspired compensator is designed to mitigate the negative impact of the time delay on the PHIL closed-loop stability. Although a passive approach, this passive compensator introduces a buffer in variability of the impedances and enables a stable PHIL experiment over a wider range of scenarios.

2) Robustness analysis of the passive compensator against the modelling error stemming from system impedance variation is presented and the stability constraint of the passive compensator-based PHIL system is defined.

3) To enhance the robustness of the compensator and overcome the limitation of passive approaches, an adaptive Smith predictor based on a computationally efficient online impedance parameter identification technique is proposed. The accurate impedance identification allows for the parameters of the Smith predictor being adapted in real-time to ensure seamless operation catering to any variations in impedance during the experimental run.

The remainder of this paper is organized as follows: Section II presents detailed modelling of the PHIL system along with its stability analysis. In section III, the in-depth design criteria of the Smith predictor compensator along with its robustness and stability constraints are elaborated. Section IV presents the online sliding discrete Fourier transformer (DFT) and vector-fitting based impedance identification method. Analytical assessments of the proposed compensation scheme are presented in section IV, followed by its experimental validation in Section VI. In-depth discussions are presented in Section VII. Section VIII concludes the paper.

II. PHIL SYSTEM MODELLING AND ANALYSIS

A. PHIL Architecture and System Modelling

A PHIL setup of a lumped voltage divider circuit incorporating ideal transformer model (ITM) interface algorithm is illustrated in Fig. 1. The setup comprises a Thévenin equivalent circuit of the emulated power network in digital real-time simulator (DRTS) and a power interface (PI) that couples the hardware under test (HuT) with the DRTS. The power interface comprises a power amplifier, signal conversion cards and current sensors. Two signal conversion cards are typically employed - a digital-to-analog converter (DAC) card and an analog-to-digital converter (ADC) card. The ADC card incorporates a low-pass filter in series to eliminate high frequency noise components within the analog signal. Fig. 1(c) presents the equivalent block diagram of the PHIL system, the open-loop transfer function of which can be represented as:

$$T_O(s) = \frac{G_1(s)G_2(s)G_3(s)G_4(s)\ Z_S(s)\ Z_H(s)}{G_{PI}(s)}$$

where $Z_S$ and $Z_H$ is the equivalent impedance of the power network within the DRTS platform and the HuT, respectively. $G_{PI}(s)$ is the transfer function of the power interface comprising the transfer functions of DAC card $G_1(s)$, power amplifier $G_2(s)$, current sensor $G_3(s)$, and ADC card in series with low-pass filter (LPF) $G_4(s)$. These components are modelled as:

$$\begin{cases}
G_1(s) = k_1 e^{-sT_{d1}} \\
G_2(s) = k_2 \frac{1}{\pi f_{cs}^2} e^{-sT_{d2}} \\
G_3(s) = e^{-sT_{d3}} \\
G_4(s) = \frac{1}{\pi f_{cs}^2} + e^{-sT_{d4}}
\end{cases}$$

where $k_1$ and $k_2$ are the scaling factor of DAC card and power amplifier, respectively. $T_{d1}$ and $T_{d4}$ represent the one time-step delay of the DRTS, $T_{d2}$ and $T_{d3}$ are the time delay of the power amplifier and sensor, respectively. $f_{cs}$ is the cut-off frequency of the power amplifier and $f_{d4}$ is the equivalent cut-off-frequency of the ADC anti-aliasing filter and low-pass filter. Representing the total time delay in the feed-forward path as $T_{d_{ff}}$ and in the feedback path as $T_{d_{fb}}$, the total time delay in the open-loop is given by:

$$T_d = \frac{T_{d_{d1}} + T_{d_{d2}} + T_{d_{d3}} + T_{d_{d4}}}{T_{d_{ff}} - T_{d_{fb}}}$$

The open-loop transfer function (1) is further expressed as:

$$T_O(s) = \frac{G_{PI}(s)e^{-sT_d}Z_S(s)}{G_{PI}(s)Z_H(s)} = \frac{G_{PI}(s)Z_S(s) e^{-sT_d}}{T_O(s)}$$

where $G_{PI}^*(s)$ and $T_O^*$ represent the delay-free part of interface $G_{PI}(s)$ and open loop system $T_O(s)$, respectively.
B. Stability and Accuracy Analysis of the PHIL Setups

An ideal ITM interface is delay-free and has transparent power amplification with unity-gain and infinite bandwidth. Under such conditions, the PHIL system is equivalent to the system of interest (SOI) duplicated in Fig. 1(a) and the closed-loop transfer function of such an ideal PHIL setup is given by:

\[ T_{cl}^{id}(s) = \frac{V_H}{V_S} = \frac{Z_H(s)}{Z_S(s) + Z_H(s)} \]  \hspace{1cm} (5)

However, the closed-loop transfer function of the actual PHIL setup with non-ideal interface is given by:

\[ T_C(s) = \frac{V_H}{V_S} = \frac{G_1(s)G_2(s)}{1 + T_O(s)} \]  \hspace{1cm} (6)

The accuracy can be assessed either by comparing the power signals of the actual PHIL against that of the ideal PHIL through the accuracy metrics as presented in [20] or by analysing the deviation between the closed-loop transfer functions of the ideal PHIL and the actual PHIL through the relative error \( \epsilon(s) \) defined as:

\[ \epsilon(s) = \left| \frac{T_C(s) - T_{cl}^{id}(s)}{T_{cl}^{id}(s)} \right| \]  \hspace{1cm} (7)

As shown in (4) and (6), the closed-loop characteristic polynomial \( (1 + T_O(s)) \) consists of the impedance, time delay and the non-unity power interface \( G_p^s(s) \). PHIL system stability can only be guaranteed provided that the gain margin (GM) and phase margin (PM) are both positive [23].

As shown in Fig. 2(a), the time delay presents unity magnitude but introduces additional phase lag, which degrades the PHIL system phase margin. Accordingly, the time delay destabilizes the PHIL system once it exceeds a critical limit \( T_{dc} \), which is defined as:

\[ \text{PM} = \angle \left[ G_p^s(j\omega_{cg}) \frac{Z_H(j\omega_{cg})}{Z_H(s) + Z_H(s)} e^{-j\omega_{cg}T_{dc}} \right] + 180^\circ = 0 \]  \hspace{1cm} (8)

where \( \omega_{cg} \) is the gain crossover frequency at which the magnitude of \( T_O(s) \) is equal to 0 dB.

Due to the phase lag introduced by the time delay, the PHIL system stability is more susceptible to the system impedance variance than that of a delay-free PHIL system. Even when the time delay is within the critical limit, as shown in Fig. 2(b), the closed-loop stability can only be maintained for certain impedance ratio (IR), where IR = \( Z_S/Z_H \). This presents a significant limitation in the realization of PHIL setups as in real-world applications the impedances in the simulation and hardware sides witness significant variations.

III. SMITH PREDICTOR COMPENSATOR

This section describes the design criterion and the functionality of Smith predictor compensator, and analyses the impact of modelling errors on its robustness and PHIL stability.

A. Smith Predictor-Based Compensator \( C_{eq}(s) \)

Smith predictor based predictive control, an effective time delay compensation scheme, has been extensively employed for power converter control [24], and microgrid hierarchical control [25]. According to the Smith predictor design criterion, a compensator \( C_{eq}(s) \) is designed to virtually mitigate the time delay impact on the PHIL closed-loop dynamics and the design principles are elaborated in [22]. An illustration of the compensator is enclosed in the dashed block (purple) in Fig. 3, the Smith predictor compensator is implemented at the point of common coupling in the feed-forward path to process the output signal from DRTS before it is amplified by the power amplifier. The Smith predictor is expressed as:

\[ C_{eq}(s) = \frac{1}{1 + T_O(s)(1 - e^{-sT_a})} \]  \hspace{1cm} (9)

where \( T_O^*(s) \) and \( T_a \) are the estimation of the nominal delay-free model \( T_O(s) \) and the aggregated delay \( T_a \), respectively.

By implementing this compensator, the closed-loop transfer function between \( V_C \) and \( V_H \) is given by:

\[ T_C(s) = \frac{G_1(s)G_2(s)}{1 + T_O^*(s)e^{-sT_a} + T_O^*(s)(1 - e^{-sT_a})} \]  \hspace{1cm} (10)

Assuming the time delay and the system model are estimated precisely, namely \( T_a = T_a \) and \( T_O^*(s) = T_O^*(s) \), the closed-loop transfer function can be further simplified as:

\[ T_C(s) = \frac{V_H}{V_S} = \frac{G_1(s)G_2(s)}{1 + T_O^*(s)} \]  \hspace{1cm} (11)

It is clear from (11) that the characteristic equation of the compensator-based PHIL setup excludes the time delay, thereby enhancing the system stability. Note that with accurate...
estimations of $\hat{T}_O(s)$ and $\hat{T}_d$, as shown in Fig. 3, the estimated output $\hat{V}_{Z_b}$ of the Smith predictor is equal to the actual feedback signal $V_f$ (i.e., the actual voltage drop $V_{Z_b}$ of the impedance $Z_b$). The voltage signal $\hat{V}_S$ applied to the inner loop of the Smith-predictor and the actual voltage $V_{S'}$ applied to the power interface are:

$$
\begin{align*}
\hat{V}_S &= V_S + \hat{V}_{Z_b} - V_f = V_S \\
\hat{V}_{S'} &= \frac{\hat{V}_S}{1 + T_O(s)} = \frac{V_S}{1 + T_O(s)}
\end{align*}
$$

Accordingly, the compensator outputs a delay-free signal $\hat{V}_{S'}$ to the power interface. Fig. 4 presents the equivalent diagram of Fig. 3, from the control point of view, the estimated output $\hat{V}_{Z_b}$ of the compensator counteracts the actual voltage drop $V_{Z_b}$ of the impedance $Z_b$ and results in a virtual zero feedback signal $V_f'$, which enables a virtually equivalent open-loop system operation, thus mitigating the destabilization impact stemming from the time delay.

**B. Robustness Analysis of Smith Predictor**

Assuming $\delta T_O(s)$ as the error between the estimation $\hat{T}_O(s)$ and the actual $T_O(s)$, the estimation model is represented as:

$$
\hat{T}_O(s) = T_O(s) + \delta T_O(s)
$$

The error in estimation is attributed to the imprecise modeling of the power interface and the variations in the HuT and DRTS impedances. Substituting (13) into (11), the closed-loop transfer function of the PHIL setup can be written as:

$$
T_C(s) = \frac{V_f(s)}{V_S(s)} = \frac{G_1(s)G_2(s)}{1 + T_O(s) + \delta T_O(s)(1 - e^{-sT_d})}
$$

The system characteristic equation is given by:

$$
1 + T_O(s) + \delta T_O(s)(1 - e^{-sT_d}) = 0
$$

As the modeling error is part of the system characteristic equation, the system stability is susceptible to this modeling error. As illustrated in the Nyquist diagram in Fig. 5, the minimum system stability margin is the shortest distance between $T_O(j\omega)$ and the critical point (-1,0) in the polar diagram. The condition for the PHIL closed-loop to maintain stability is that this minimum stability margin is always greater than the magnitude of $|\delta T_O(j\omega)(1 - e^{-j\omega T_d})|$ for all the frequencies, which yields:

$$
|\delta T_O(j\omega)(1 - e^{-j\omega T_d})| < |1 - T_O(j\omega)|, \forall \omega > 0
$$

The limit of the modelling error at which the overall PHIL closed-loop can maintain stability is given by:

$$
|\delta T_O(j\omega)| < \frac{|1 + T_O(j\omega)|}{|1 - e^{-j\omega T_d}|}, \forall \omega > 0
$$

The robustness of the Smith predictor compensator is quantitatively defined by the criteria derived in (16) and (17). With more advanced power amplifiers being made available in the market, the precise modeling of the power amplifier comprising subsystems (as in (2)) is feasible in a laboratory environment. Therefore, the error in model estimation stems from the impedance variations during the real-time testing. For a Smith predictor compensator designed for a system with impedance ratio IR, variations in impedance ratio can be accommodated to ensure a stable system until the inequality relationship in (16) fails. The value of impedance ratio at which the inequality no longer valid is defined as the critical impedance ratio $IR_c$, which serves as the buffer for variability in the impedance ratio guaranteeing the PHIL system stability.

**IV. ADAPTIVE SMITH PREDICTOR**

If the impedance of the system can be estimated in real-time, the model of Smith predictor based compensator adopted for a PHIL setup can be updated to ensure stability with varying impedance. This is the principle adopted for the development of adaptive Smith predictor in this paper. As shown in Fig. 6, the impedance model identification involves applying the Goertzel algorithm-based Sliding DFT (GSDFT) to process the external injected excitation voltage signals and the corresponding current signals for frequency-domain impedance responses calculation. The responses are successively processed by the least-square vector fitting algorithm to get the rational impedance model that is employed to update the adaptive Smith predictor. The following two subsections elaborate on these steps in more detail.
A. Impedance Frequency Response Calculation by GSDFT

In real-time application, the frequency-domain data must be processed frequently and promptly. Sliding DFT (SDF) is deduced from the DFT circular shift property [26] with the time-domain sequence circularly shifted by one sample through multiplying $e^{j2\pi k/N}$ and the signal spectral being updated on a sample-by-sample basis [26], [27]. This attribute enables the SDFT to present higher computation efficiency and low computation cost than Fast Fourier Transform (FFT) in processing signals with selective frequencies [26]. The transfer function of SDFT is:

$$H_{\text{SDFT}}(z) = \frac{S_k(n)}{X(n)} = \frac{(1 - z^{-N}) e^{j2\pi k/N}}{1 - e^{j2\pi k/N} z^{-1}} \quad (18)$$

where $N (N = \frac{L}{f_s})$ is the window size, $f_s$ is the sampling frequency, $f_0$ is the fundamental frequency, and $k (k = 1, 2, 3, \ldots N)$ represents the order of the recursive filter.

To further reduce the computation complexities of the SDFT for its real-time application, Goertzel algorithm [26]–[28] is applied to SDFT by multiplying the numerator and denominator of (18) with $(1 - e^{-j2\pi k/N} z^{-1})$. Accordingly, the transfer function of GSDFT consists of real-only coefficients in its denominator and is given by:

$$H_{\text{GSDFT}}(z) = \frac{(1 - e^{-j2\pi k/N} z^{-1})}{1 - 2 \cos(2\pi k/N) z^{-1} + z^{-2}} e^{j2\pi k/N} \quad (19)$$

As shown in Fig. 7, the structure of a GSDFT corresponds to the cascading of a comb filter, a Goertzel filter in second-order infinite impulse response (IIR) form, and a phase shift factor $e^{j2\pi k/N}$. This structure enhances its ease of implementation for frequency-domain response calculation in real-time application. The comb filter is equivalent to a notch filter with notches periodically spaced at the fundamental and harmonic frequencies. This enables the attenuation of the input signal with notch frequencies to an extremely low level. The $k$-th order IIR Goertzel filter is equivalent to a band-pass filter centred at the frequency $k f_0$ and amplifies the corresponding signal component. As presented in [22], [26], the GSDFT with $k$-th order Goertzel filter presents unity gain and zero phase shift characteristics at the frequency of concern. Thus the implementation of GSDFT with $k$-th order Goertzel filter enables the selective signal extraction at a certain frequency of interest without magnitude distortion and phase shift.

Based on the selective signal processing attribute of the GSDFT, the frequency-domain HuT impedance response with respect to an externally injected signal with frequency $\omega_k$ is:

$$Z_H(e^{j\omega_k T_s}) = \frac{S_{vk}(n)}{S_{ik}(n)} = R_{vk} + j I_{mk} \quad (20)$$

B. Impedance Parameters Calculation

As shown in Fig. 6, the multi-sine voltage excitation signal with predefined frequencies $(\omega_k, (k = 1, \ldots, K))$ is injected via the power amplifier and the corresponding frequency-domain system response data is calculated by GSDFT. The response data is further processed by exploiting the vector fitting algorithm in a least-square sense.

The rational transfer function of the impedance, a continuous-time linear time-invariant (LTI) system, is:

$$\tilde{Z}_H(s) = \frac{A(s)}{B(s)} = \frac{\sum_{i=0}^{n} a_i s^i}{1 + \sum_{i=1}^{m} b_i s^i} \quad (21)$$

where $n$ and $m$ are the order of the numerator and denominator respectively, $a_i$ and $b_i$ represent the coefficients of the transfer function to be estimated.

The frequency response data calculated by GSDFT over the predefined frequency, namely $[\omega_0, K \omega_0]$, are expressed as:

$$Z_H(j\omega_k) = R_{vk} + j I_{mk}, k = 1, \ldots, K \quad (22)$$

The residual $\epsilon_k$, representing the numerical difference between the measured $Z_H(j\omega_k)$ and the frequency response of the estimated $\tilde{Z}_H(j\omega_k)$ at frequency $\omega_k$ is given by:

$$\epsilon_k = (R_{vk} + j I_{mk}) - \frac{A(j\omega_k)}{B(j\omega_k)} \quad (23)$$

$$A(j\omega_k) = \sum_{i=0}^{n} a_i (j\omega_k)^i, B(j\omega_k) = 1 + \sum_{i=1}^{m} b_i (j\omega_k)^i \quad (24)$$

Exploiting the residual $\epsilon_k$ as a scalar to assess the estimation error, the weighted error $\tau_k$ is calculated by multiplying the residual $\epsilon_k$ with weighting function $B(j\omega_k)$, which yields:

$$\tau_k = \epsilon_k B(j\omega_k) = (R_{vk} + j I_{mk}) B(j\omega_k) - A(j\omega_k) \quad (25)$$

Quadratic cost function is further defined as the summed square of the weighted error $\tau_k$ over the experimentally-observed frequency-domain data, namely,

$$J(A, B) = \arg \min_{A, B} \sum_{k=1}^{K} |\tau_k|^2 \quad (26)$$

Coefficient matrices $A$ and $B$ are calculated by minimizing the quadratic cost function through differentiating it with respect to unknown coefficients (i.e., $a_i$ and $b_i$), that is

$$\frac{\partial J(A, B)}{\partial a_i} = 0, A = [a_0, a_1, a_2, \ldots a_n]^T \quad (27)$$

$$\frac{\partial J(A, B)}{\partial b_i} = 0, B = [1, b_1, b_2, \ldots b_m]^T \quad (28)$$

The linearization method as elaborated in [29] is applied to the non-linear matrices in (27) and the numerical values of the coefficient matrices $A$ and $B$ are further calculated by solving the corresponding linear algebraic equations.

The main advantage of this method is that the impedance measurement is based on GSDFT calculations over a selected set of frequencies with high-speed and low computation complexity. The compensator is updated based on the online impedance measurement without a requirement of prior knowledge of the parameters of the system to be tested, which is well-suited for the real-time PHIL simulation.
Adaptive Smith predictor for enhanced stability of power hardware-in-the-loop setups

Fig. 8: Current behaviour of the PHIL systems with (a) $Z_H = (1e^{-3}s + 1)\Omega$ and (b) $Z_H = (7.692e^{-4}s + 0.769)\Omega$.

TABLE I: Parameters for the analytical assessment and simulation.

<table>
<thead>
<tr>
<th>Setup</th>
<th>$k_1$</th>
<th>$k_2$</th>
<th>$f_{sc}$</th>
<th>$f_{sp}$</th>
<th>$T_{sp}$</th>
<th>$f_{tr}$</th>
<th>$T_{tr}$</th>
<th>$f_{sp}$</th>
<th>$T_{sp}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>–</td>
<td>–</td>
<td>kHz</td>
<td>kHz</td>
<td>µs</td>
<td>µs</td>
<td>µs</td>
<td>µs</td>
<td>µs</td>
</tr>
<tr>
<td>Value</td>
<td>0.2</td>
<td>5</td>
<td>8</td>
<td>10000</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>600</td>
<td></td>
</tr>
</tbody>
</table>

V. ANALYTICAL ASSESSMENT AND EVALUATION

This section presents the analytical assessment and evaluation of Smith predictor in improving the PHIL stability through simulation undertaken in Matlab/Simulink. The PHIL interface parameters (as in (2)) are given in Table I. The software side impedance is chosen as $Z_S = 3 \Omega$ (Note that, as the Smith predictor is designed according to the system impedance, the effectiveness validation of proposed approach is not limited by the choice of the impedance of the system under consideration) and the simulation side voltage is emulated as a 10 V step voltage signal in the cases presented in subsections A and B.

A. Stability Enhancement by Smith Predictor

The first case involves a PHIL system with hardware impedance $Z_H = (1e^{-3}s + 1)\Omega$ and the impedance ratio IR is the same as IR₀, for which the analytical stability assessment is presented in Fig. 2. The hardware side current is presented in Fig. 8(a). For the PHIL system without a compensator, the current reaches a stable state after some oscillations and is consistent with that of the SOI at the steady state. As for the PHIL with Smith predictor compensator, the current oscillations stemming from the time delay are mitigated as the time delay has been equivalently shifted out of the PHIL closed-loop by the compensator.

Fig. 8(b) presents the current behaviour of a PHIL system with hardware impedance $Z_H = (7.692e^{-4}s + 0.769)\Omega$ and an impedance ratio as $1.31 IR₀$. As analysed in Fig. 2, this impedance ratio exceeds the critical ratio limit and the closed-loop system is unstable. Correspondingly, the current of such a PHIL system without a compensator is not convergent in nature. While the current of the PHIL system with a compensator converges and is aligned with that of the SOI.

Comparing these two cases, the variation in system impedance can lead to instability if the variation breaches the critical IR boundary as shown in Fig. 2. The incorporation of Smith predictor compensator stabilizes the closed-loop system and also extends the range of impedance ratios over which the PHIL simulation can remain stable.

B. Robustness Assessment of Smith Predictor

Although the passive Smith predictor can ensure the stability of PHIL setups over an extended impedance range, the system can tend towards instability if modelling error between the estimated model and the actual model breaches the stability criterion defined by (16) and (17). Consider a PHIL system with impedance $Z_S = 3 \Omega$, $Z_H = (1e^{-3}s + 1)\Omega$. A Smith predictor compensator designed for the example PHIL system. Fig. 9 presents the inequalities in (16) against the variable impedance ratio as a result of hardware side impedance variations. Critical impedance ratio $IR_c$ is obtained as $IR_c = 2.88IR₀$ from the boundary of the two terms in (16). Provided the compensator is not updated according to the impedance variation, the PHIL system is unstable once the impedance ratio exceeds $IR_c$, otherwise, the system is stable but inaccurate due to the modelling error between the estimated model and the actual model.

This is further demonstrated in simulation where a passive Smith predictor is designed according to the impedance $Z_S = 3 \Omega$, $Z_H = (1e^{-3}s + 1)\Omega$ and hardware side impedance variation is emulated at $t = 0.15s$ for the two cases listed in Table II. For case a, as shown in Fig. 10 (a), the PHIL system with impedance ratio as $IR₀$ is stable before impedance change and becomes unstable after impedance change. Before the impedance change, as shown in Fig. 10 (b), the PHIL with compensator is stable and its current is consistent with that of the SOI. After impedance change, the compensator stabilizes the PHIL system as the impedance ratio is within the critical impedance ratio in Fig. 9, but the current deviates from that of the SOI. In terms of case b, as shown in Fig. 10 (c), the PHIL system without a compensator is stable before impedance change but becomes unstable after impedance change. For the PHIL system with a compensator, since the impedance ratio exceeds $IR_c$ after the impedance change, the compensator is not able to maintain the stability criterion defined in (16). At this point, as shown in Fig. 10(d), the current is divergent and tends to instability.
Adaptive Smith predictor for enhanced stability of power hardware-in-the-loop setups

C. Assessment of Real-Time Adaptive Smith Predictor

For the evaluation of adaptive Smith predictor, a single-phase ac voltage source $V_5$ rated at 230 V and 50 Hz and three hardware impedances (combination of resistive-inductive and resistive-inductive-capacitive) are chosen as presented Table III. The simulation begins with hardware side impedance as $Z_{H1}$, for which the Smith predictor is accordingly designed. Two cases are presented where impedance is varied at $t = 1.5s$, first from $Z_{H1}$ to $Z_{H2}$, and second from $Z_{H1}$ to $Z_{H3}$.

As presented in Section IV, the adaptive Smith predictor is dependent upon accurate estimation of the impedance change. Fig. 11 presents the GSDFT experimental measurement over the selected set of frequencies ranging from 10 Hz to 5 kHz and the frequency response of the reference model and estimated model identified by the impedance identification units as presented in Fig. 6. Although there are some slight deviations between the experimental measurement data and reference model, most frequency-domain measurement data are well-fitted to the reference model. Good agreement between the estimated impedance transfer function and the reference impedance transfer function has been achieved.

Fig. 12 shows the hardware side currents of the original SOI PHIL system with passive compensator and with adaptive compensator. Before the impedance change, the PHIL systems implemented with these compensators are stable and their currents lag the SOI current by $T_d$. However, after the impedance change, the PHIL system with a passive compensator is unstable. On the contrary, the PHIL system with real-time adaptive compensator is stable and the short-period oscillations after the impedance change are suppressed.

TABLE III: Hardware-side impedance variation.

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Element</th>
<th>Reference</th>
<th>Estimation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_{H1}$</td>
<td>$R_1 + L_1$</td>
<td>$R_1 + sL_1$</td>
<td>$1.005e^{-3}s + 1$</td>
</tr>
<tr>
<td>$Z_{H2}$</td>
<td>$R_2 + L_2$</td>
<td>$R_2 + sL_2$</td>
<td>$3.33e^{-4}s + 0.5$</td>
</tr>
<tr>
<td>$Z_{H3}$</td>
<td>$(R_3 + C)/L_3$</td>
<td>$R_3 + L_3s^2 + L_3s + 1$</td>
<td>$2.509e^{-7}s^2 + 9.964e^{-4}s + 1$</td>
</tr>
</tbody>
</table>

Fig. 11: Frequency response of the impedance model.

Fig. 12: Current behaviour of the PHIL systems with impedance variations: (a) $Z_{H1}$ to $Z_{H2}$ (b) $Z_{H1}$ to $Z_{H3}$.

VI. EXPERIMENT VALIDATION

This section is dedicated to the experimental validation of the proposed PHIL stability enhancement scheme. The experiment was undertaken in the Dynamic Power System Laboratory (DPSL) at the University of Strathclyde. Fig. 13 shows the experimental setup. An equivalent voltage source and a low $X/R$ ratio grid impedance, as listed in Table IV, are employed to emulate a low-voltage grid within the DRTS. A 256-step passive load bank is incorporated within the PHIL simulation by a Triphase 90 kVA voltage source back-to-back converter (TP90 kVA) acting as the power amplifier. The signal conversion between DRTS and TP90 kVA are achieved by employing two signal conversion cards (i.e., Giga-transceiver analog output (GTAO) card and Giga-transceiver analog input (GTAI) card). The remainder of the parameters for this PHIL setup are presented in Table IV.

The digital voltage signal $V_s'$ measured from the point of common coupling of the equivalent network is transmitted to
Adaptive Smith predictor for enhanced stability of power hardware-in-the-loop setups

Table IV: Parameters of the PHIL experimental setup.

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software side voltage source</td>
<td>( V_{\text{in}} )</td>
<td>V</td>
<td>400</td>
</tr>
<tr>
<td>System fundamental frequency</td>
<td>( f_0 )</td>
<td>Hz</td>
<td>50</td>
</tr>
<tr>
<td>Total time delay</td>
<td>( T_d )</td>
<td>( \mu ) s</td>
<td>250</td>
</tr>
<tr>
<td>Software impedance</td>
<td>( Z_G )</td>
<td>( \Omega )</td>
<td>12</td>
</tr>
<tr>
<td>Hardware system impedance</td>
<td>( Z_{\text{He1}} )</td>
<td>( \Omega )</td>
<td>( 5 \times 10^{-4} s + 12 )</td>
</tr>
<tr>
<td></td>
<td>( Z_{\text{He2}} )</td>
<td>( \Omega )</td>
<td>( 1 \times 10^{-5} s + 10 )</td>
</tr>
<tr>
<td>Power amplifier (TP90kVA)</td>
<td>( G_2(s) )</td>
<td>-</td>
<td>( \frac{1}{350s^2 + 9s^2 + 23} )</td>
</tr>
</tbody>
</table>

Fig. 14: Hardware current of the PHIL system with impedance \( Z_{\text{He1}} \): (a) without and (b) with Smith predictor compensator.

The TP90kVA as its command signal, which is processed by the proposed compensator. The passive load bank is coupled with the output terminal of the TP90kVA. The current response of the passive load bank \( I_H \) is measured and transmitted to the DRTS as the command signal for the controllable current source. The analogue signals \( U_H \) and \( I_H \) and the impedance measurement are recorded by the Triphase datalogger with a sampling rate of 16 kHz and are replotted by Matlab.

Fig. 14 presents the hardware current signal of the PHIL setup with hardware impedance \( Z_{\text{He1}} \). For the PHIL system without a compensator, as shown in Fig. 14 (a), the hardware current diverges once the compensator is disabled and the closed-loop system tends to instability. This is aligned with the stability assessment as presented in Fig. 15 (a). Once the compensator is enabled, the hardware current converges and reaches a stable state as in Fig. 14 (b). This is in agreement with the stability assessment of the open-loop transfer function of the Smith predictor based PHIL system in Fig. 15 (b).

Fig. 15: Nyquist diagram of the open-loop transfer function of a PHIL system with (a) \( Z_{\text{He1}} \) and \( Z_{\text{He2}} \), (b) SP (based on \( Z_{\text{He1}} \)) and \( Z_{\text{He1}} \), (c) SP (based on \( Z_{\text{He1}} \)) and \( Z_{\text{He2}} \), (d) SP (based on \( Z_{\text{He2}} \)) and \( Z_{\text{He2}} \).

Fig. 16: Hardware current of the PHIL system with passive Smith predictor (based on \( Z_{\text{He1}} \)) and impedance vary from \( Z_{\text{He1}} \) to \( Z_{\text{He2}} \). The robustness of the Smith predictor compensator is assessed by implementing an impedance variation in the passive
Adaptive compensator enabled

Fig. 17: Hardware current of the PHIL system with impedance $Z_{He2}$ and adaptive Smith predictor that is initially based on $Z_{He1}$ and is updated according to the online impedance measurement.

load bank. Fig. 16 (b) and (c) show the impedance measured by the GSDFT-based impedance identification unit. As shown in Fig. 16 (a), the hardware side current presents significant oscillations and reaches an unstable state after the impedance varies from $Z_{He1}$ to $Z_{He2}$. Corresponding to the stability assessment as presented in Fig. 15 (c), the compensator that is designed for the hardware impedance $Z_{He1}$ is no longer capable to stabilize the PHIL closed system as the stability criterion defined in (16) is not maintained. Upon activation of the adaptive compensator, the current converges to a stable state and the GSDFT-based impedance measurement presents more accurate results due to the stabilization of the online updated adaptive compensator as shown in Fig. 17. This is consistent with the stability assessment in Fig. 15 (d).

VII. DISCUSSIONS

The performance of the passive Smith predictor and the distinct advantage offered by the adaptive Smith predictor have been demonstrated by analytical assessment, simulation and experimental results. This section presents a brief discussion on the applicability and limitation of the proposed approach.

As demonstrated in the above sections, the proposed adaptive Smith predictor scheme stabilizes the PHIL system with inherent impedance variation. Although the applicability of the approach in this paper has been limited to passive loads for the purpose of proof of concept demonstration, the approach is extensible and applicable in theory for a stable PHIL system incorporating parallel connected power converters, active or passive loads, of which the equivalent impedance may witness variation when single or multiple power apparatus plugged in or out. This can be explored in frame of future research.

The Smith predictor based PHIL system presents accurate simulation results as that of the original system of interest when it reaches steady state. In terms of the transient state performance, as demonstrated in Fig. 8, the Smith predictor based PHIL system presents less oscillations than that of the PHIL system without Smith predictor when the system is subject to a step change in voltage. The improved transient performance of the Smith predictor based PHIL system is achieved by the mitigation of the time delay that degrades the system convergence speed as a result of deteriorated system stability margin.

Even though the Smith predictor contributes to improved transient and steady state performance, its online impedance identification approach presents a limitation for its applicability to fast changes in impedances. As shown in Fig. 12 (b), the adaptive Smith predictor stabilizes the PHIL system 0.02 s after a step change in impedance is applied. This arises from the natural circular signal processing attribute of the sliding DFT based on-line impedance identification scheme that requires one-cycle processing time (i.e., 0.02 s) for calculating the impedance parameters and updating the Smith predictor. This limitation does not deteriorate the performance of the proposed Smith predictor in stabilizing the PHIL system with inherent impedance variation that could challenge the closed-loop stability as demonstrated by the simulation results and the experimental results. Development of faster online impedance parameters identification schemes can enhance the applicability of the proposed methodology for the faster impedance change scenario and associated transient studies. This forms an interesting direction for future research.

VIII. CONCLUSIONS

In this paper, the impact of the time delay and impedance ratio on the PHIL closed-loop stability has been analysed. To mitigate the stability deteriorating impact stemming from the time delay and impedance variation, this paper proposed a PHIL closed-loop stability enhancement scheme involving the Smith predictor compensator and GSDFT-based impedance identification techniques. The effectiveness and robustness of the proposed adaptive Smith predictor compensator based stabilization scheme have been analysed and assessed by simulation and experiment. Moreover, the simulation and experimental results reveal that the proposed adaptive Smith predictor enables a stable PHIL system over a wider range of impedance ratios, allowing for a broader range of scenarios being investigated at one experimental run than that of the PHIL system without the proposed compensator. This is critical for a stable and robust PHIL experimental assessment of the candidate hardware systems with inherently variable impedance.

REFERENCES


