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ORIGINAL RESEARCH

An improved nine-level switched capacitor-based inverter with voltage boosting capability and limitation of capacitor current spikes for PV applications

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Abstract

To proceed to a net zero carbon world and to mitigate the environmental challenges associated with it, integration speed of renewable energy sources such as photovoltaic (PV) systems has been increased around the world. Here, an improved switched-capacitor based nine-level inverter is introduced for PV applications. This topology has several benefits such as, voltage boosting feature, using a single DC source, reduction of capacitor charging current spike and extendable input voltage. This inverter produces nine-level output voltage waveform using single power supply. This topology, using identical two capacitors in parallel with a single DC source, can boost the input voltage. In this inverter to limit spike current of capacitor charging mode, an inductor is placed in the charging path of capacitors with a parallel diode. The power losses and overall efficiency analysis of the improved inverter are considered. To verify the accurate performance of inverter under a step change on power flows, simulation results are obtained by MATLAB/Simulink software and presented. To highlight the benefits of the inverter, a comparison of improved topology with most recent topologies is performed. Finally, to verify the feasibility and performance of the improved inverter, experimental results of a 770 W grid-tied prototype are presented.

1 | INTRODUCTION

Nowadays, global warming, increasing energy demand, concerns about carbon emissions, and fossil fuels limitations are definitely considered as the most important energy challenges around world [1–3]. To solve and/or mitigate these concerns, different solutions and technologies have been introduced. Among these solutions, integration of renewable energy sources (RESs) into power systems is one of the most popular and widely accepted solutions. At the large family of RESs, photovoltaic (PV) systems are of the widely used members [4–6]. However, to employ and integrate these sources into the power systems, power electronic based interfaces, that is, power converters, are inevitable [7–10]. It is worth noting that besides RES applications, power converters are widely used in numerous modern applications [11–13]. Among these converters, multi-level inverters (MLI) are one of the most popular solutions to improve the performance of electric vehicles, renewable energy systems (RES) such as photovoltaic (PV) systems, and other power electronic devices in medium- and high-power applications [14–18]. Multilevel inverters (MLIs) are favourite structures due to their low total harmonic distortion (THD), small filter size, high efficiency, reduced voltage rating of power semiconductors and many other features [15, 19–21]. Neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) MLIs are three main topologies which have been studied comprehensively [22]. However, mentioned topologies suffer from high number of components and requiring complex

control methods especially for higher number of levels [23]. Moreover, the NPC and FC inverters are incompetent in boosting the input voltage [24]. The CHB converter is dominant over NPC and FC due to its modularity, which makes it a more feasible choice to be applied in high voltage applications. Thus, it requires several input DC sources and more switches leading to augmentation of the overall size, volume and weight. Hybrid MLIs combine different topologies to achieve multiple voltage levels [25]. In recent years, SC based circuits in which the input voltage sources are replaced by capacitors have been emerged [26]. In these converters, the combination of charging and discharging of the capacitors forms the multiple output levels.

In [27], the virtual DC bus is introduced in which the capacitor contributes to the polarity reversion in the output side. This concept is the principle of SC- based inverters. In [28], three different topologies are presented in which single capacitor helps producing three-level output voltage. However, the inverter is incapable of boosting the voltage magnitude in the ac side. In [29], two capacitors have been applied for the same voltage levels. But in this case, the output voltage magnitude is boosted twice the input DC link. In [30], the same number of capacitors as in previous structures is aimed to produce more output levels with boosting capability. The five-level inverters in [31] is designed exclusively for being supplied by photovoltaic panels to integrate with the grid using two capacitors. In [23], the two floating capacitors generate seven-level output voltage. Although it has the features of inherent polarity reversion and boosting gain of three, still the component count is a matter of case. In [32], the same voltage levels are produced with a smaller number of switches. In [33–43], nine-level SC-based inverters have been introduced. In some SC-based topologies, the capacitors do not play a role to produce a reversed output voltage, and they are charged and discharged only for boosting purposes. In such structures, an H-bridge or a half bridge inverter is added to produce negative voltage in the negative half cycles which helps extend the output levels, even more. Topology presented in [44] obtains its boosted output voltage by multi-dc link formed by single voltage source and several SC sub-modules connected to an H-bridge inverter. The high number of switch count in this structure is a matter of concern which has been solved in [45]. However, [45] uses separated DC sources for each sub-module, which Consequently, increases the size and the volume. Additionally, it has applied two half-bridges to diminish the conducting components in the current path for its extensible MLI.

The major disadvantage of the SC-based topologies is that spike currents pass through the capacitors while they are being charged which can cause harmful current stress on the components [46]. In [47], the capacitors stay in charged state in every switching cycles and they are not discharged completely that leads to less severe inrush currents without adding an inductor. However, these unwanted currents are not mitigated completely and the modified topology can solve this vital challenge. In [48], the quasi-resonant inductor overcomes the instant inrush currents in the series-connected capacitors. Depending on the desired number of output voltage levels, different number of capacitors are utilized to generate multiple output by only one DC source.

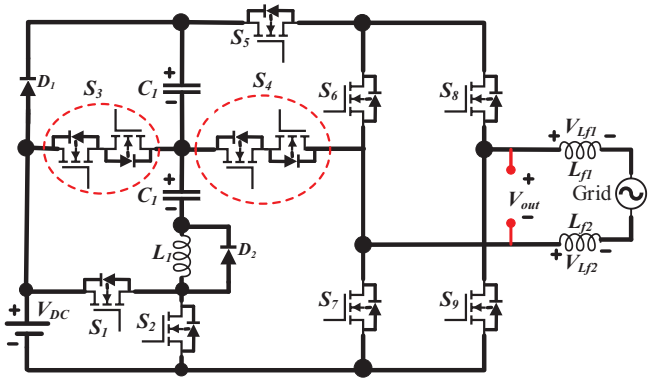


FIGURE 1 Improved nine-level SC-based inverter

Considering the above-mentioned issues, nine-level switched capacitor-based single DC source inverter is introduced in this paper. The improved topology is a combination of the SC unit and a full bridge inverter. In the improved switched capacitor inverters, by utilizing SC unit, two-times boost factor can be achieved without using any additional boosting stages. As mentioned, the major disadvantage in the SC-based multilevel inverters is the current spikes while charging the capacitors. The improved nine-level inverter can limit this spike current. In the improved structure, both of the utilized capacitors (C_1 and C_2) will be charged to desired values and will be discharged periodically. It is worth mentioning that these charge and discharge operations will be done needless of complex control systems. The rest of paper is organized as follows:

In the next section, the improved nine-level SC-based inverter is described in detail. In Section 3 the operation principle for the improved structure will be explained comprehensively. The sizing of utilized capacitors and output filter is calculated in Section 4. The power loss and overall efficiency analysis of improved inverter is provided in Section 5. In Section 6, to show the accurate performance of improved inverter and its control system under a step change on output power, some simulation results are obtained by using MATLAB/Simulink and provided. In Section 7, the comparison of the improved inverters with some other conventional switched capacitors is done. In order to confirm accurate performance of the first improved switched capacitor inverter, the grid-connected experimental results are provided in Section 8. Finally, conclusions are summarized in Section 9.

2 | IMPROVED NINE-LEVEL SC-BASED INVERTER

The power circuit of the improved SC-based inverter is shown in Figure 1. The improved topology can generate nine-level out-

put voltage waveforms. This aim can be obtained by combining a new SC unit and a full bridge inverter. Based on Figure 1, the first improved topology consists of seven unidirectional power electronic switches, two bidirectional power switches (S_3 and S_4), and two power diodes. With respect to Figure 1, it can be seen that the first improved inverter consists of two capacitors (C_1 and C_2) which have been paralleled to a single input voltage. Considering Figure 1, the used capacitors (C_1 and C_2) are applied to increase the number of dc-link and present voltage boosting features of the topology. Capacitor current spike is a major defect in SC-based inverter and can cause extensive damages to the components, and can reduce the lifetime of the components. Hence an inductor (L_1) has been applied to smoothly charge the capacitors. Also, a power diode has been connected in parallel with the inductor to assure that there is a freewheeling path for the currents in the opposite direction. On this account, the improved topologies can limit the spike current of the capacitors during charging modes. Utilizing bidirectional switches is essential since the switches should with stand a voltage stress in both positive and negative half cycles under different circuit conditions.

3 | OPERATION MODES OF THE IMPROVED NINE-LEVEL INVERTER

The operation modes of the improved SC-based nine-level inverter are presented in this section. Different operation modes with current flowing paths of the nine-level improved inverter are depicted in Figure 2a–i. In Figure 2, the red, blue and green dashed lines indicate the active power flow, (injected grid current), reactive power flow and charging loop of the utilized capacitors (C_1 and C_2), respectively. Each of these operation modes of the first improved topology will be described in detail as follows.

3.1 | Positive half-cycle

3.1.1 | First operation mode

The first operation mode is shown in Figure 2a regarding which, in order to produce the zero-voltage level, two different current paths can be used. During this operation mode, the power switches S_1, S_2, S_3, S_4 S_7 and S_9 are in OFF-state. Also, the power diodes D_1 and D_2 are in connected and disconnected modes, respectively. During this mode the switches S_2, S_6 and S_8 are in the ON-state. Also, during this mode both utilized capacitors are in charging mode by the aim of turning on switch S_2. Therefore, the voltage of each utilized capacitor is equal to $0.5V_{DC}$ ($V_{C1} = V_{C2} = 0.5V_{DC}$). In this mode, the standing voltage on the OFF-power switches during this mode can be obtained as:

$$\begin{cases} V_{S1} = V_{S2} = 0.5V_{dc} \\ V_{S3} = V_{S4} = V_{S5} = V_{C1} = 0.5V_{DC} \\ V_{S7} = V_{S9} = V_{SC} \end{cases} \quad (1)$$

Also, the current stress of the ON-switches during this mode can be formulated as follows:

$$i_{S6} = i_{S8} = i_g(t) = \mathrm{I}_{mg} \cdot \sin(\omega t) \quad (2)$$

where i_g(t) and I_{mg} are the injected grid current and maximum value of the injected grid current, respectively.

3.1.2 | Second operation mode

This operation mode is indicated in Figure 2b. During this operation mode, first level of the output voltage waveform in positive half cycle will be generated. In order to obtain this aim, the switches S_2, S_4, S_5, S_6 and S_8 will be in the ON-state. Also, the switches S_1, S_3, S_7, S_9 and diode D_2 are in OFF-state. During this mode the capacitors C_1 and C_2 are in charging mode as the switch S_2 is turned on. Therefore, the capacitors C_1 and C_2 are connected to input voltage source in series and both of capacitors are charged to $0.5V_{DC}$. Also, the stored energy of capacitor C_1 is pumped to the output. The equations of capacitor's voltages and output voltage can be written as:

$$V_{C1} = V_{C2} = 0.5V_{DC} \quad (3)$$

$$V_{out} = V_{C2} = 0.5V_{DC} \quad (4)$$

The standing voltage of OFF switches can be written as:

$$\begin{cases} V_{S1} = V_{DC} \\ V_{S3} = V_{C1} = 0.5V_{DC} \\ V_{S6} = V_{S7} = V_{S9} = V_{DC} \end{cases} \quad (5)$$

The current stress of the ON switches can be obtained as:

$$i_{S4} = i_{S5} = i_{S8} = i_g(t) = \mathrm{I}_{\mathrm{mg}} \sin(\omega t) \quad (6)$$

3.1.3 | Third operation mode

Figure 2c indicates the equivalent electrical circuit of the third operation mode. During this mode, to generate the second level of the output voltage waveform in the positive half cycle, the DC source (V_{DC}) connects to the output directly through the power switch S_5 and power diode D_1. Figure 2c depicts that during this operation mode, none of the capacitors are in the load current path (red dashed line). With respect to Figure 2c, it can be seen that, both of the utilized capacitors will be charged to $0.5V_{DC}$ ($V_{C1} = V_{C2} = 0.5V_{DC}$) again as switch S_2 and diode D_1 are switched ON. Based on Figure 2c, the switches S_2, S_5, S_7, S_8 and diode D_1 are in ON-state. Also, the switches S_1, S_3, S_4, S_6, S_9 and diode D_2 are in OFF-state. The amplitude of output voltage can be written

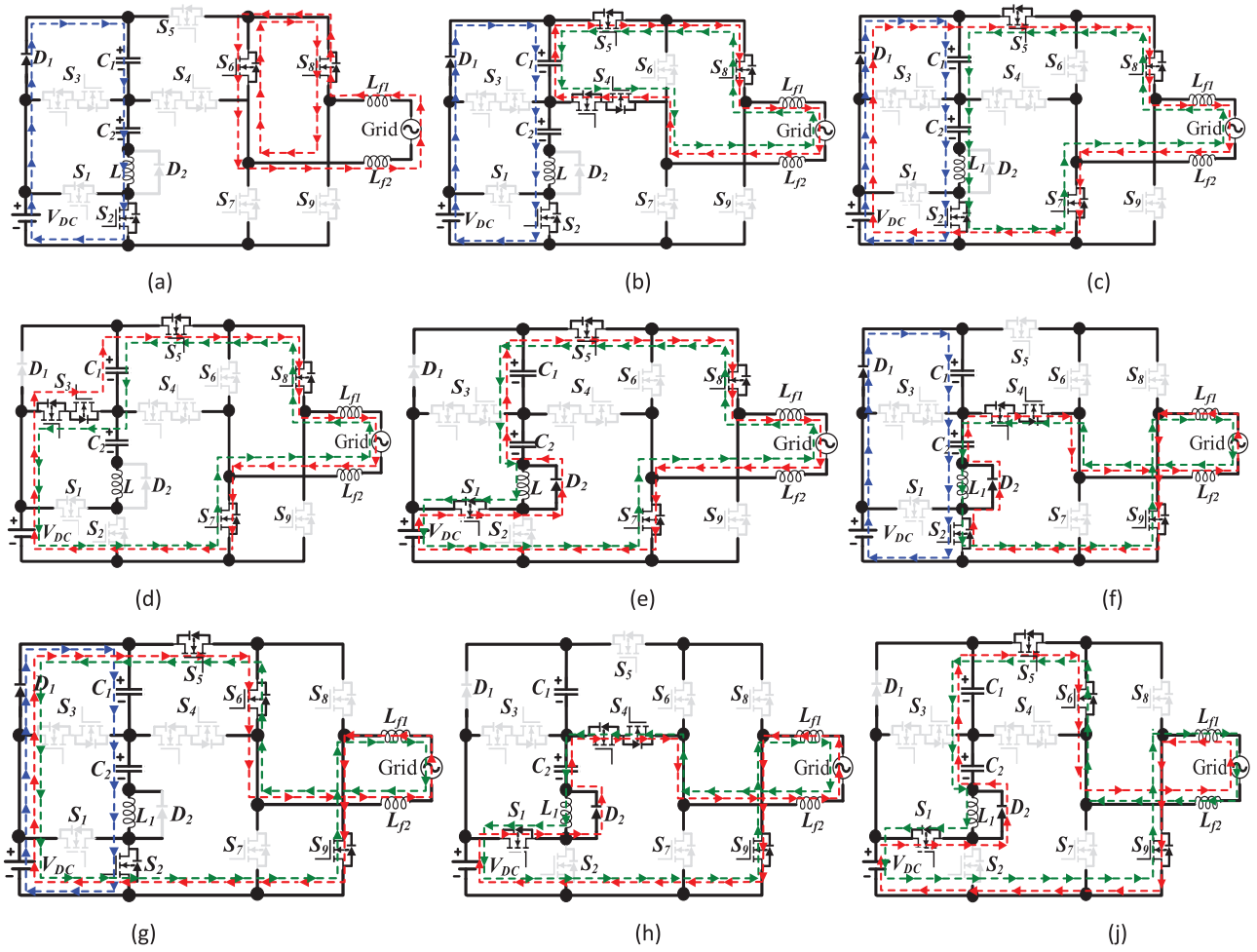


FIGURE 2 Operation modes of the improved 9-level inverter: (a) 1st operation mode, (b) 2nd operation mode, (c) 3rd operation mode, (d) 4th operation mode, (e) 5th operation mode, (f) 6th operation mode, (g) 7th operation mode, (h) 8th operation mode, (i) 9th operation mode

as:

$$V_{out} = V_{DC} \tag{7}$$

The standing voltage of OFF switches can be formulated as follows:

$$\begin{cases} V_{S1} = V_{DC} \\ V_{S3} = V_{C1} = 0.5V_{DC} \\ V_{S4} = V_{S6} = V_{C1} = 0.5V_{DC} \\ V_{S6} = V_{S9} = V_{C1} + V_{C2} = V_{DC} \end{cases} \tag{8}$$

Also, the current stress of power switches which are in ON-state can be written as:

$$\begin{cases} i_{S5} = i_{S7} = i_{S8} = i_g(t) = I_{mg}\sin(\omega t) \\ i_{S2} = i_{C1} = i_{C2} \end{cases} \tag{9}$$

3.1.4 | Fourth operation mode

Respecting Figure 2d, to generate the fourth level of output voltage waveform in the positive half cycle, switches S_3, S_5, S_7 and S_8 are in ON-state, so that, the stored energy of capacitor C_1 along with power supply are pumped to the output. Therefore, the output voltage of improved inverter will be $1.5V_{DC}$. Considering Figure 2d, the switches S_1, S_2, S_4, S_6, S_9 and diodes D_1 and D_2 are in OFF-state. To avoid any malfunction during the capacitor charging mode for each of the utilized capacitors, the switch S_2 should be turned OFF to disconnect the capacitor C_2. The amplitude of output voltage can be formulated as:

$$V_{out} = V_{DC} + V_{C1} = 1.5V_{DC} \tag{10}$$

The standing voltage of the switches during this mode can be calculated as:

$$\begin{cases} V_{S1} = V_{S2} = V_{DC} \\ V_{S4} = V_{S6} = V_{C1} = 0.5V_{DC} \\ V_{S9} = V_{DC} \end{cases} \tag{11}$$

The current stress of on switches can be calculated as:

$$i_{S3} = i_{S5} = i_{S8} = i_{S7} = i_g(t) = \mathrm{I}_{mg}\sin(\omega t) \tag{12}$$

3.1.5 | Fifth operation mode

This operation mode is indicated in Figure 2e based on which, switches S_1, S_5, S_7, S_8 and diode D_2 are turned ON. During this operation mode, by the series connection the input dc source and both capacitors the fourth level in the positive half cycle of the output voltage is produced. So that, both of the capacitors will theoretically be discharged and the output voltage will be $2V_{DC}$. In addition, during this mode switches S_2, S_3, S_4, S_6, S_9 and diode D_1 are in OFF-state. The standing voltage of these switches can be calculated as:

$$\begin{cases} V_{S2} = V_{DC} \\ V_{S3} = V_{C2} = 0.5V_{DC} \\ V_{S4} = V_{C2} + V_{dc} = 1.5V_{DC} \\ V_{S6} = V_{S9} = V_{dc} + V_{C1} + V_{C2} = 2V_{DC} \end{cases} \tag{13}$$

The current stress of ON switches can be obtained as:

$$i_{S1} = i_{S5} = i_{S7} = i_{S8} = i_g(t) = \mathrm{I}_{mg}\sin(\omega t) \tag{14}$$

3.2 | Negative half-cycle

3.2.1 | Sixth operation mode

The sixth operation mode is shown in Figure 2f. The aim of this mode is to generate the first negative output voltage level ($-0.5V_{DC}$). Considering Figure 2f, it can be seen that capacitor C_2 is discharged to the output of the inverter. Also, during this operation mode the power switch S_2 and D_1 are in ON-state. Therefore, the capacitor C_1 is being charged using input DC source of the inverter. The switches S_2, S_5, S_6, and S_9 are in ON-state, therefor the output voltage of the inverter is equal to $-0.5V_{DC}$. During this mode, the switches S_1, S_3, S_4, S_7 and S_8 are in OFF-state.

3.2.2 | Seventh operation mode

This mode is illustrated in Figure 2g shows the generation of the second level of output voltage waveform during the negative half cycle ($-V_{DC}$), the switches S_2, S_5, S_6 and S_9 should be turned ON. Also, in this mode the switches S_1, S_3, S_4, S_7 and S_8 are in OFF-state. Both capacitors (C_1 and C_2) are in charging mode through switch S_2 and voltage of each capacitor is $0.5V_{DC}$.

3.2.3 | Eight operation mode

Considering Figure 2, the aim of the eights mode of operation which is shown in Figure 2h is to generate the third negative level of output voltage waveform ($-1.5V_{DC}$) through the series connection of input dc power supply (V_{DC}) and the capacitor C_2 ($V_{C2} = 0.5V_{DC}$). This aim is obtained by turning ON the switches S_1, S_4 and S_9. Also, during this mode the switches S_2, S_3, S_5, S_6, S_7 and S_8 are in OFF-state.

3.2.4 | Ninth operation mode

Considering Figure 2i, in this mode, the switches S_1, S_5, S_6 and S_9 are turned ON. Also, switches S_2, S_3, S_4, S_7 and S_8 are in OFF-state. Since the duration of charging, discharging and unconnecting modes for both capacitors (C_1 and C_2) are equal, the voltage of these capacitors will be fixed to half value of the DC power supply ($V_{C1} = V_{C2} = 0.5V_{DC}$). Therefore, the peak value of output voltage will be two times of the peak value of the DC power supply. Therefore, the voltage boosting feature of the improved inverter is validated.

One of the advantages of the improved structure is that it can inject power to the grid properly in an extended range of input voltages.

The Maximum Blocked Voltage of switches of the improved inverter can be obtained as follows:

$$\begin{cases} V_{S1} = V_{S2} = V_{DC} \\ V_{S3} = V_{C1} = 0.5V_{DC} \\ V_{S4} = V_{DC} + V_{C2} = 1.5V_{DC} \\ V_{S5} = V_{C1} + V_{C2} + V_{DC} = 2V_{DC} \\ V_{S6} = V_{S7} = V_{S8} = V_{S9} = 2V_{DC} \end{cases} \tag{15}$$

Therefore, the Total Standing Voltage (TSV) of the modified inverter can be calculated as follows:

$$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{S5} + V_{S6} + V_{S7} + V_{S8} + V_{S9} = 14V_{DC} \tag{16}$$

In this case, duty cycle of the different operation modes of proposed inverter are calculated as follows. The positive half cycle of output voltage waveform of the inverter and grid voltage with four operation zones (zone1–zone4) of the both improved inverters are presented in Figure 3, with respect to which, the control technique of the improved inverters can be designed. Maximum switching frequency of the inverter is f_S, also, the sampling frequency is f_{SA}. It should be noted that, the maximum switching frequency is half of the sampling frequency. Applying the inductor volt-second balanced (IVSB) technique to the voltage across of the inductor in a full operation period (T_S), the switching duty cycle of the inverter during each mentioned zone is calculated in (19)–(33) using which, the control

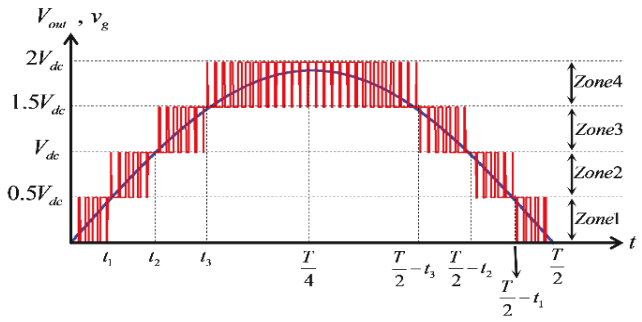


FIGURE 3 Output voltage waveform of inverter, grid voltage, and four operation zone of improved inverter

technique of the proposed inverter can be designed. Maximum switching frequency of the inverter is f_S, also, the sampling frequency is f_{SA}. It should be noted that, the maximum switching frequency is half of the sampling frequency.

Here, V_{out} and V_g are the output voltages of inverter and grid, respectively. The equations for voltage and current of the grid can be written as follows:

$$v_g = V_{mg}\sin(\omega t) \tag{17}$$

$$i_g = I_{mg}\sin(\omega t - \varphi) \tag{18}$$

Zone 1

Regarding Figure 3, in zone 1, the inverter's output voltage is between 0 and $0.5V_{dc}$ during. Therefore, by applying the IVSB rule for the voltage across the filter inductor in this zone for the switching period, the switching duty cycle of the inverter (d_1) can be obtained as (19)–(21).

$$\int_0^{d_1.T_s}(V_{out}-v_g)\,dt + \int_{d_1.Ts}^{T_s}(-v_g)\,dt = 0 \tag{19}$$

$$d_1(t) = \frac{v_g}{V_{out}} \tag{20}$$

By substituting (17) in (20), the duty cycle of zone 1 can be written as:

$$d_1(t) = \frac{2V_{mg}}{V_{DC}}\cdot\sin(\omega t);\quad 0 \le t < t_1 \tag{21}$$

Zone 2

With respect to Figure 3, in zone 2, the output voltage of the inverter is between $0.5V_{dc}$ and V_{dc}. By applying the IVSB strategy for the voltage across the output filter in this zone for the switching period, the switching duty cycle of the inverter (d_2) can be calculated as (22)–(24).

$$\int_0^{d_2T_S}\left(V_{DC}-v_g\right)dt + \int_{d_2T_S}^{T_S}\left(0.5V_{DC}-v_g\right)dt = 0;$$

$$t_1 \le t < t_2 \tag{22}$$

$$d_2(t) = \frac{2V_g}{V_{DC}} - 1 = \frac{2V_{mg}}{V_{DC}}\sin(\omega t) - 1;\quad t_1 \le t < t_2 \tag{23}$$

Considering (21), the Equation (23) can be rewritten as:

$$d_2(t) = d_1(t) - 1;\quad t_1 \le t < t_2 \tag{24}$$

Zone 3

As seen in Figure 3, in zone 3, the inverter's output voltage is between V_{dc} and $1.5V_{dc}$. So, by using the IVSB rule for the voltage across the inductor filter during zone 3 for the switching period, the switching duty cycle of the inverter (d_3) can be written as (25)–(27).

$$\int_0^{d_3.T_S}\left(1.5V_{DC}-v_g\right)dt + \int_{d_3.T_S}^{T_S}\left(V_{DC}-v_g\right)dt = 0\ ;$$

$$t_2 \le t < t_3 \tag{25}$$

$$d_3(t) = \frac{2v_g}{V_{DC}} - 2 = \frac{2V_{mg}}{V_{DC}}\cdot\sin(\omega t) - 2;\quad t_2 \le t < t_3 \tag{26}$$

Considering (24), the Equation (26) could be written as:

$$d_3(t) = d_2(t) - 1\ ;\quad t_2 \le t < t_3 \tag{27}$$

Zone 4

Considering Figure 3, in zone 2, the output voltage of the inverter is between $1.5V_{dc}$ and $2V_{dc}$. By applying the IVSB rule for the voltage across the inductor filter during zone 2 for the switching period, the switching duty cycle of the inverter (d_4) can be calculated as (28)–(30).

$$\int_0^{d_4.T_S}\left(2V_{DC}-v_g\right)dt + \int_{d_4.T_S}^{T_S}\left(1.5V_{DC}-v_g\right)dt = 0;$$

$$t_3 \le t < \frac{T}{2} - t_3 \tag{28}$$

$$d_4(t) = \frac{2v_g}{V_{DC}} - 3 = \frac{2V_{mg}}{V_{DC}}\cdot\sin(\omega t) - 3;\quad t_3 \le t < \frac{T}{2} - t_3 \tag{29}$$

With regard to (27), the Equation (29) can be obtained as follows:

$$d_4(t) = d_3(t) - 1;\quad t_3 \le t < \frac{T}{2} - t_3 \tag{30}$$

where from Figure 3, the equations of t_1, t_2 and t_3 can be obtained as:

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{0.5V_{DC}}{V_{mg}}\right) \tag{31}$$

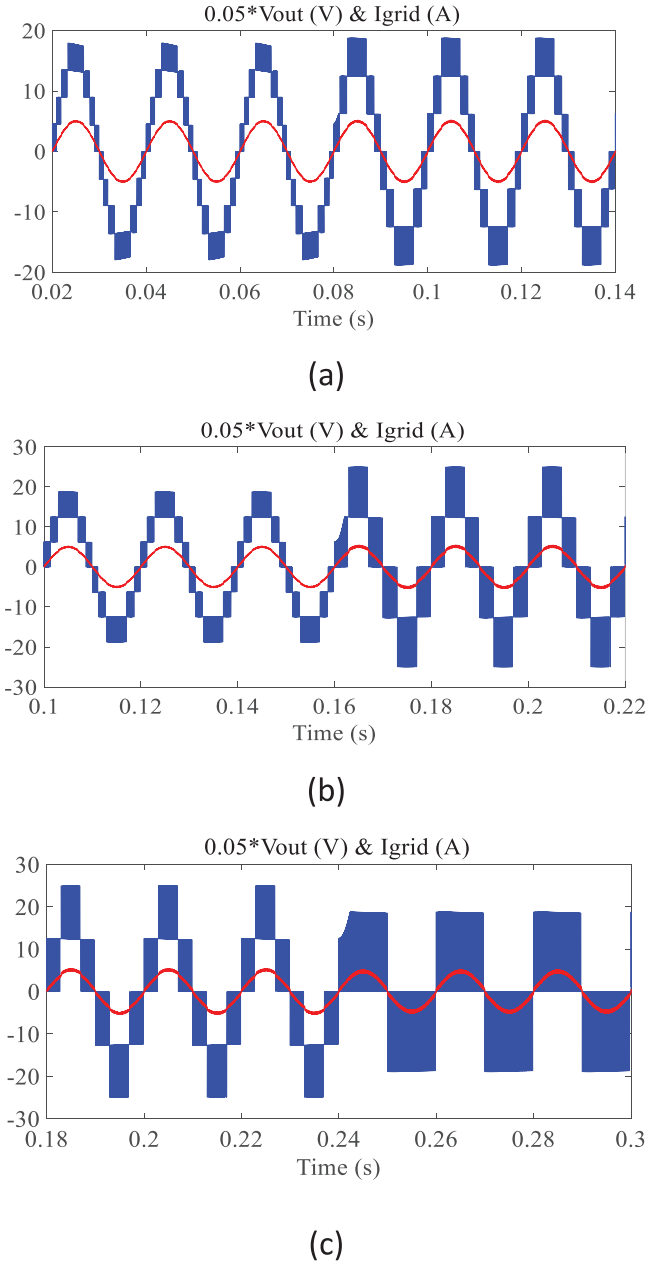


FIGURE 4 Simulation results for verification input voltage extendibility: (a) 180–250 V, (b) 250–500 V (c) 500–750 V

$$t_2 = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{DC}}{V_{mg}}\right) \tag{32}$$

$$t_3 = \frac{1}{\omega}\sin^{-1}\left(\frac{1.5V_{DC}}{V_{mg}}\right) \tag{33}$$

In order to verify these advantages of the first improved topology, simulation results are Provided by SIMULINK/MATLAB software and presented in Figure 4. Based on this figure, the input voltage varies between 180 and 750 V. In proportion to this change, the output voltage changes from 9 levels to 3 levels and the improved topology can inject power to the grid under this condition properly. Considering Figure 4a, when the input voltage changes from 180 to 250 V the output voltage waveform changes from 9-level to 7-level. Figure 4b indicates that the input voltage changes from 250 to 500 V. Under this condition, the output voltage waveform changes from 7-level to 5-level.

Based on Figure 4c, when the input voltage changes from 500 to 750 V the output voltage waveform changes from 5-level to 3-level.

4 | SIZING OF CAPACITORS AND OUTPUT FILTER OF THE IMPROVED INVERTER

The capacitance values of used capacitors (C_1 and C_2) in the introduced topology, are calculated based on the longest discharging cycle (LDC) of each capacitor. A 9-level output voltage waveform of the improved topology is indicated in Figure 5, which is considered in the fundamental frequency. Longest discharging cycle happens during the positive and negative half cycles for utilized capacitors C_1 and C_2 respectively.

The peak discharging value of each capacitor during the mentioned LDC can be obtained as:

$$I_{Cap} = \frac{dQ_{Cap}}{dt} = \frac{d}{dt}\left(\int I_{Cap}dt\right) \tag{34}$$

Since the inverter output voltage waveform is a symmetric waveform relative to the origin of coordinates, it has only odd order of harmonics. Therefore, the LDC for capacitors (C_1 and C_2) will be equal. During the fifth operation mode of the improved inverters the current passing through the capacitors C_1 and C_2 will be equal to output current of inverter or injected grid current ($i_g(t)$). Therefore, Equation (33) can be written as:

$$\begin{aligned} Q_{C1} = Q_{C2} &= 2\times\int i_g(t).dt = 2\times\int I_{mg}\sin(\omega t).d(\omega t) \\ &= 2I_{mg}\cos(\omega t) \end{aligned} \tag{35}$$

The value for utilized capacitors can be obtained as follows:

$$\Delta Q_{Cj} = Q_{Cj}\times\Delta V \quad j = 1,2 \tag{36}$$

$$C_j = \frac{\Delta Q_{Cj}}{\Delta V} = \frac{Q_{Cj}}{\Delta V} \tag{37}$$

where ΔV is the maximum admissible value for capacitors voltage ripple and it can be written as:

$$\Delta V = N\times V_{DC} \tag{38}$$

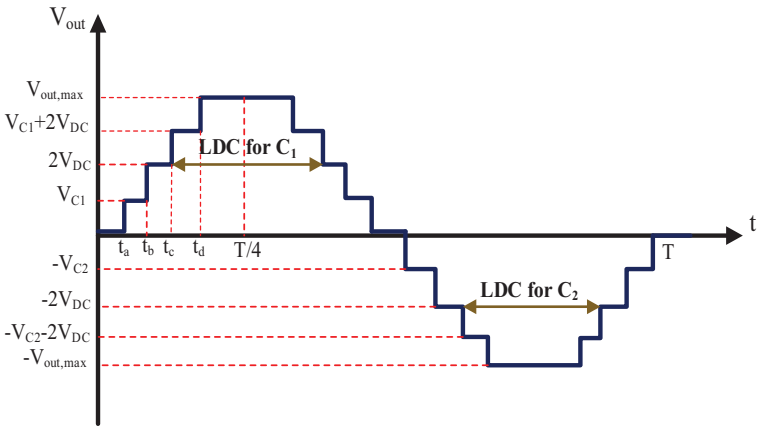


FIGURE 5 A nine-level output voltage waveform

With respect to Equations (35) and (36), the capacitance of capacitors can be calculated as:

$$C_j = \frac{Q_{Cj}}{N \times V_{DC}}; \quad j = 1, 2 \tag{39}$$

Based on Figure 1, the inductance of output filter can be written as:

$$L_f = L_{f1} + L_{f2} \tag{40}$$

The maximum value of the current ripple of the output filter inductor occurs in the unity power factor and peak value of the injected current to grid ($t = T/4$). At this time ($t = T/4$), the improved topology works in fifth operation mode and output voltage is equal to $2V_{DC}$ ($V_{out} = 2V_{DC}$). The current equation of the inductor $i_{Lf}(t)$ in a full period of switching can be obtained as:

$$i_{Lf}(t) = \frac{1}{L_f}\int_0^t V_{Lf}dt + i_{Lf}(0) \tag{41}$$

where V_{Lf} is the voltage across of the output filter. The current ripple of the output filter can be calculated as:

$$\Delta I_{Lf} = i_{Lf}(t = d \cdot T_S) - i_{Lf}(0) = \left(\frac{2V_{DC} - v_g}{L_f \cdot f_S}\right) \tag{42}$$

Therefore, using (27), the final value of L_f can be obtained as follows:

$$L_f = \frac{1}{\Delta I_{Lf} \cdot f_S}\left[7V_{mg}.\sin(\omega t) - \frac{2V_{mg}^{\ 2}}{V_{DC}}.\sin^2(\omega t) - 6V_{DC}\right] \tag{43}$$

For the maximum value of the inductor current ripple, L_f can be calculated as:

$$L_f = \frac{1}{\Delta I_{Lf,max} \cdot f_S}\left[7V_{mg} - \frac{2V^2_{mg}}{V_{DC}} - 6V_{DC}\right] \tag{44}$$

The values of L_{f1} and L_{f2} are the same and equal to half of L_f.

5 | POWER LOSS AND EFFICIENCY ANALYSIS

In this section, the switching and conduction loss of each switch is calculated. Also, the total power loss and overall efficiency of the improved inverter are provided. Figure 6 shows the a typical nine-level output current waveform. Note that, in order to calculate the power losses, the Power Factor (PF) is considered 1 ($PF = 1$). So, the value of the angle φ is equal to zero. Based on Figure 7, the average value of duty cycles of inverter ($d_1(t)$–$d_2(t)$) can be calculated as follows:

$$D_{1,ave} = \frac{1}{\omega t_1}\int_0^{\omega t_1}\left(\frac{2V_{mg}}{V_{DC}} \cdot \sin(\omega t)\right)$$

$$d\omega t = \frac{V_{mg}}{V_{DC} \cdot \omega t_1}\left(1 - \cos(\omega t_1)\right) \tag{45}$$

$$D_{2,ave} = \frac{1}{\omega t_2 - \omega t_1}\int_{\omega t_1}^{\omega t_2}\left(\frac{2V_{mg}}{V_{DC}} \cdot \sin(\omega t) - 1\right)$$

$$d\omega t = \frac{1}{\omega t_2 - \omega t_1}\left[\frac{2V_{mg}}{V_{DC}}\left(\cos(\omega t_1) - \cos(\omega t_1)\right) + \omega t_1 - \omega t_2\right] \tag{46}$$

$$D_{3,ave} = \frac{1}{\omega t_3 - \omega t_2}\int_{\omega t_2}^{\omega t_3}\left(\frac{2V_{mg}}{V_{DC}} \cdot \sin(\omega t) - 2\right)$$

$$d\omega t = \frac{1}{\omega t_3 - \omega t_2}\left[\frac{2V_{mg}}{V_{DC}}\left(\cos(\omega t_2) - \cos(\omega t_3)\right) + 2(\omega t_2 - \omega t_3)\right] \tag{47}$$

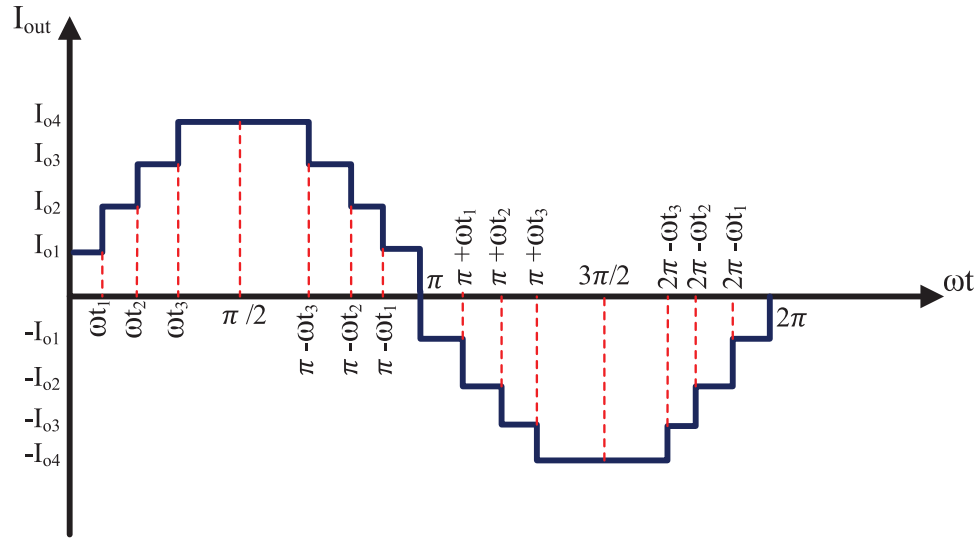


FIGURE 6 A typical nine-level output current waveform

$$D_{4,ave} = \frac{1}{\pi/2 - \omega t_3}\int_{\omega t_3}^{\pi/2}\left(\frac{2V_{mg}}{V_{DC}}\cdot\sin(\omega t) - 3\right)$$

$$d\omega t = \frac{1}{\pi/2 - \omega t_3}\left[\frac{2V_{mg}}{V_{DC}}(\cos(\omega t_3)) + 3(\omega t_3 - \pi/2)\right] \quad (48)$$

The number of times that switches are turned on and off from zero moment to $\pi/2$ are calculated as follows:

$$N_{SW1} = \frac{t_1}{T_S}; \quad 0 \le \omega t < \omega t_1 \quad (49)$$

$$N_{SW2} = \frac{t_2 - t_1}{T_S}; \quad \omega t_1 \le \omega t < \omega t_2 \quad (50)$$

$$N_{SW3} = \frac{t_3 - t_2}{T_S}; \quad \omega t_2 \le \omega t < \omega t_3 \quad (51)$$

$$N_{SW4} = \frac{5000 - t_3}{T_S}; \quad \omega t_3 \le \omega t < \pi/2 \quad (52)$$

where T_S is the switching period time. Based on Figure 7, the current values of I_{o1}, I_{o2}, I_{o3}, and I_{o4} can be calculated as follows:

$$I_{o1} = \left[\frac{1}{\omega t_1}\int_0^{\omega t_1} \mathrm{I}^2{}_{mg}\cdot\sin(\omega t)d\omega t\right]^{1/2}$$

$$= \mathrm{I}_{mg}\cdot\left[\frac{1}{\omega t_1}\left(\frac{1}{2}\omega t_1 - \frac{1}{4}\sin(2\omega t_1)\right)\right]^{1/2} \quad (53)$$

$$I_{o2} = \left[\frac{1}{\omega t_2 - \omega t_1}\int_{\omega t_1}^{\omega t_2} \mathrm{I}^2{}_{mg}\cdot\sin^2(\omega t)d\omega t\right]^{1/2}$$

$$= \mathrm{I}_{mg}\cdot\left[\frac{1}{\omega t_2 - \omega t_1}\left(\frac{1}{2}(\omega t_2 - \omega t_1) + \frac{1}{4}(\sin(2\omega t_1) - \sin(2\omega t_2))\right)\right]^{1/2} \quad (54)$$

$$I_{o3} = \left[\frac{1}{\omega t_3 - \omega t_2}\int_{\omega t_2}^{\omega t_3} \mathrm{I}^2{}_{mg}\cdot\sin^2(\omega t)d\omega t\right]^{1/2}$$

$$= \mathrm{I}_{mg}\cdot\left[\frac{1}{\omega t_3 - \omega t_2}\left(\frac{1}{2}(\omega t_3 - \omega t_2) + \frac{1}{4}(\sin(2\omega t_2) - \sin(2\omega t_3))\right)\right]^{1/2} \quad (55)$$

$$I_{o4} = \left[\frac{1}{\pi - \omega t_3}\int_{\omega t_3}^{\pi} \mathrm{I}^2{}_{mg}\cdot\sin^2(\omega t)d\omega t\right]^{1/2}$$

$$= \mathrm{I}_{mg}\cdot\left[\frac{1}{\pi - \omega t_3}\left(\frac{1}{2}(\pi - \omega t_3) + \frac{1}{4}\sin(2\omega t_3)\right)\right]^{1/2} \quad (56)$$

Considering the operation modes in Figure 2, the switch S_1 in the voltage levels $+L_4$, $-L_3$, and $-L_4$ is in ON-state or conduction mode. So, it should be calculated the switching and conduction losses of this switch during the mentioned intervals as follows:

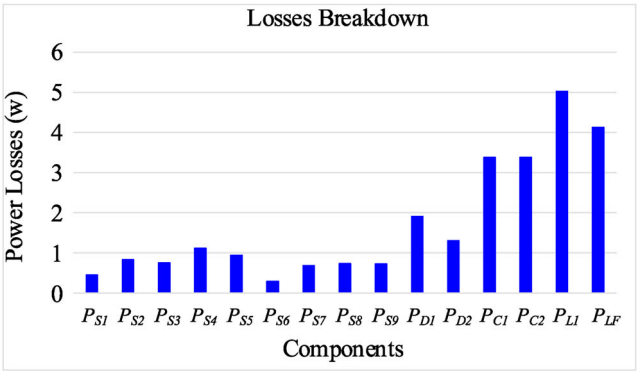
Time interval ($\omega t_3 \sim \pi - \omega t_3$):

The equation of passing current through the switch S_1 during time interval ($\omega t_3 \sim \pi - \omega t_3$) can be expressed as follows:

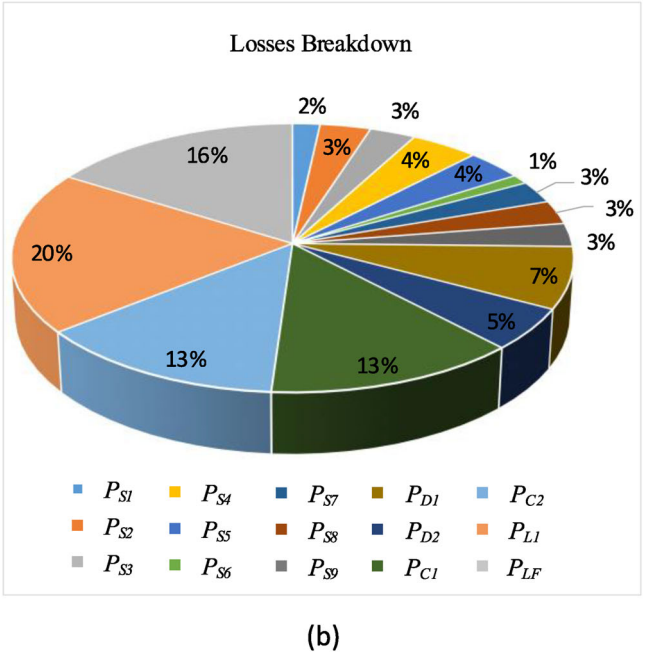
$$i_{S1} = \begin{cases} I_{o4}; & 0 \le t < D_{4,ave}T_s \\ 0 \ ; & d_{4,ave}T_S \le t < T_S \end{cases} \quad (57)$$

$$I_{S1,rms,(\omega t_3 \sim \pi - \omega t_3)} = \left[\frac{\pi - 2\omega t_3}{2\pi}\cdot\frac{1}{T_S}\int_0^{d_4 T_S} I^2{}_{o4}dt\right]^{1/2}$$

$$= I_{o4}\sqrt{\frac{(\pi - 2\omega t_3)D_{4,ave}}{2\pi}} \quad (58)$$



(a)



(b)

FIGURE 7 losses breakdown analysis of improved inverter: (a) Bar chart, (b) pie chart

In this time interval, the switching and conduction losses of the switch S_1 can be obtained as follows:

$$P_{SW,S1,(\omega t_3 \sim \pi - \omega t_3)} = \frac{1}{6} \times V_{S1} \times I_{S1} \times \left(t_{on} + t_{off}\right) \times (2 \times N_{SW4}) \times f_g = \frac{1}{6} \times (0.5 V_{DC}) \times I_{o4} \times \left(t_{on} + t_{off}\right) \times (2 \times N_{SW4}) \times f_g \quad (59)$$

$$P_{con,S1,(\omega t_3 \sim \pi - \omega t_3)} = \frac{r_D \times I^2{}_{o4} \times (\pi - 2\omega t_3)\, D_{4,ave}}{2\pi} \quad (60)$$

$$\text{Time interval}(\pi + \omega t_2 \sim \pi + \omega t_3) \quad (61)$$

$$i_{S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} = \begin{cases} I_{o3}; & 0 \le t < D_{3,ave} T_S \\ 0; & D_{3,ave} T_S \le t < T_S \end{cases} \quad (62)$$

$$I_{S1,rms,S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} = \left[\frac{2(\omega t_3 - \omega t_2)}{2\pi} \cdot \frac{1}{T_S} \int_0^{D_{3,ave} T_S} I^2{}_{o3}\, dt\right]^{1/2} = I_{o3} \sqrt{\frac{(\omega t_3 - \omega t_2)\, D_{3,ave}}{\pi}} \quad (63)$$

In this time interval, the switching and conduction losses of the switch S_1 can be obtained as follows:

$$P_{SW,S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} = \frac{1}{6} \times V_{DC} \times I_{o,3} \times \left(t_{on} + t_{off}\right) \times (2 N_{SW3}) \times f_g \quad (64)$$

$$P_{con,S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} = \frac{r_{DS} \times I^2{}_{o3} \times (\omega t_3 - \omega t_2) \times D_{3,ave}}{\pi} \quad (65)$$

Time interval $(\pi + \omega t_3 \sim 2\pi - \omega t_3)$

In this time interval, the switch S_1 is always in on-state. So, the switch S_1 has only conduction losses and switching losses of this switch is equal to zero. In this time interval, the passing current equation of switch S_1 can be expressed as follows:

$$i_{S1,(\pi+\omega t_3 \sim 2\pi-\omega t_3)} = \begin{cases} I_{o4}; & 0 \le t < D_{4,ave} T_S \\ I_{o4}; & D_{4,ave} T_S \le t < T_S \end{cases} \quad (66)$$

$$I_{S1,(\pi+\omega t_3 \sim 2\pi-\omega t_3)} = \left[\frac{\pi - 2\omega t_3}{2\pi} \cdot \frac{1}{T_S} \int_0^{T_S} I^2{}_{o4}\, dt\right]^{1/2} = I_{o4} \sqrt{\frac{\pi - 2\omega t_3}{2\pi}} \quad (67)$$

$$P_{con,S1,(\pi+\omega t_3 \sim 2\pi-\omega t_3)} = \frac{r_{DS} \cdot I^2{}_{o4} \times (\pi - 2\omega t_3)}{2\pi} \quad (68)$$

So, the total power losses of switch S_1 can be obtained as follows:

$$P_{S1} = P_{SW,S1,(\omega t_3 \sim \pi - \omega t_3)} + P_{SW,S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} + P_{con,S1,(\omega t_3 \sim \pi - \omega t_3)} + P_{con,S1,(\pi+\omega t_2 \sim \pi+\omega t_3)} + P_{con,S1,(\pi+\omega t_3 \sim 2\pi-\omega t_3)} \quad (69)$$

The Passing current and RMS value of passing current of other used semiconductors such switches (S_2–S_9) and diodes (D_1–D_2) are summarized in Tables 1–4. The power losses of other switches (S_2–S_9) can be obtained as the similar method of switch S_1 and summarized in Tables 5 and 6. Also, the conduction losses and power losses of diodes D_1 and D_2 are summarized in Table 6.

TABLE 1 Passing current and RMS value of passing current of switches S_1, S_2, S_3 and S_4

Switch	Passing current during given time interval	RMS value of passing current during given time interval
S_2	$i_{S2(\omega t_2\sim\omega t_3)} = \begin{cases} 0 & ; \quad 0 \le t < D_{3,ave}T_S \\ \dfrac{D_{3,ave}\cdot I_{o3}}{1-D_{3,ave}} & ; \quad D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{S2,rms,(\omega t_2\sim\omega t_3)} = \left[\dfrac{4\,(\omega t_3-\omega t_2)}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_{D_{3,ave}T_S}^{T_S}\left(\dfrac{D_{3,ave}\cdot I_{o3}}{1-D_{3,ave}}\right)dt\right] = D_{3,ave}I_{o3}\times\sqrt{\dfrac{2\,(\omega t_3-\omega t_2)}{\pi\,(1-D_{3,ave})}}$
	$i_{S2,(\pi\sim\pi+\omega t_1)} = \begin{cases} I_{o1}\ ; & 0 \le t < D_{1,ave}T_S \\ 0 \ ; & D_{1,ave}T_S \le t < T_S \end{cases}$	$I_{S2,rms,(\pi\sim\pi+\omega t_1)} = \left[\dfrac{2\omega t_1}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_0^{D_{1,ave}T_S} I^2{}_{o1}\,dt\right]^{1/2} = I_{o1}\times\sqrt{\dfrac{\omega t_1\times D_{1,ave}}{\pi}}$
	$i_{S2,(\pi+\omega t_1\sim\pi+\omega t_2)} = \begin{cases} 0\ ; & 0 \le t < D_{2,ave}T_S \\ I_{o2} \ ; & D_{2,ave}T_S \le t < T_S \end{cases}$	$I_{S2,rms,(\pi+\omega t_1\sim\pi+\omega t_2)} = \left[\dfrac{2(\omega t_2-\omega t_1)}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_{D_{2,ave}T_S}^{T_S} I^2{}_{o2}\,dt\right]^{1/2} = I_{o2}\times\sqrt{\dfrac{(\omega t_2-\omega t_1)(1-D_{2,ave})}{\pi}}$
S_3	$i_{S3,(\omega t_2\sim\omega t_3)} = \begin{cases} I_{o3}\,; & 0 \le t < D_{3,ave}T_S \\ 0 \ ; & D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{S,rms,(\omega t_2\sim\omega t_3)} = \left[\dfrac{2(\omega t_3-\omega t_2)}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_0^{D_{3,ave}T_S} I^2{}_{o3}\,dt\right]^{1/2} = I_{o3}\cdot\sqrt{\dfrac{(\omega t_3-\omega t_2)D_{3,ave}}{\pi}}$
	$i_{S3,(\omega t_3\sim\pi-\omega t_3)} = \begin{cases} 0\,; & 0 \le t < D_{4,ave}T_S \\ I_{o4} \ ; & D_{4,ave}T_S \le t < T_S \end{cases}$	$I_{S3,rms,(\omega t_3\sim\pi-\omega t_3)} = \left[\dfrac{\pi-2\omega t_3}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_{D_{4,ave}T_S}^{T_S} I^2{}_{o4}\,dt\right]^{1/2} = I_{o4}\sqrt{\dfrac{(\pi-2\omega t_3)(1-D_{4,ave})}{2\pi}}$
S_4	$i_{S4,(0\sim\omega t_1)} = \begin{cases} I_{o1}\ ; & 0 \le t < D_{1,ave}T_S \\ 0 \ ; & D_{1,ave}T_S \le t < T_S \end{cases}$	$I_{S4,rms,(0\sim\omega t_1)} = \sqrt{\dfrac{4\omega t_1}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_0^{D_{1,ave}T_S} I^2{}_{o1}\,dt} = I_{o1}\sqrt{\dfrac{2\omega t_1\times D_{1,ave}}{\pi}}$
	$i_{S4,(\omega t_1\sim\omega t_2)} = \begin{cases} I_{o2}\ ; & 0 \le t < D_{2,ave}T_S \\ 0 \ ; & D_{2,ave}T_S \le t < T_S \end{cases}$	$I_{S4,rms,(\omega t_1\sim\omega t_2)} = \left[\dfrac{4(\omega t_2-\omega t_1)}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_0^{D_{2,ave}T_S} I^2{}_{o2}\,dt\right]^{1/2} = I_{o2}\sqrt{\dfrac{2(\omega t_2-\omega t_1)D_{2,ave}}{\pi}}$
	$i_{S4,(\pi+\omega t_2\sim\pi+\omega t_3)} = \begin{cases} I_{o3}\ ; & 0 \le t < D_{3,ave}T_S \\ 0 \ ; & D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{S4,rms,(\pi+\omega t_2\sim\pi+\omega t_3)} = \left[\dfrac{2(\omega t_3-\omega t_2)}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_0^{D_{3,ave}T_S} I^2{}_{o3}\,dt\right]^{1/2} = I_{o3}\sqrt{\dfrac{(\omega t_3-\omega t_2)D_{3,ave}}{\pi}}$
	$i_{S4,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \begin{cases} 0\ ; & 0 \le t < D_{4,ave}T_S \\ I_{o4}\,; & D_{4,ave}T \le t < T_S \end{cases}$	$I_{S4,rms,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \left[\dfrac{\pi-2\omega t_3}{2\pi}\cdot\dfrac{1}{T_S}\displaystyle\int_{D_{4,ave}T_S}^{T_S} I^2{}_{o4}\right]^{1/2} = I_{o4}\sqrt{\dfrac{(\pi-2\omega t_3)(1-D_{4,ave})}{2\pi}}$

In addition, the power losses of output filter inductors L_{f1} and L_{f2} can be calculated as follows:

$$r_{Lf} = r_{Lf1} + r_{Lf2} \tag{70}$$

$$I_{Lf,rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} \mathrm{I}^2{}_{mg}\sin^2(\omega t)\cdot d\omega t\right]^{1/2} = \frac{\mathrm{I}_{mg}}{\sqrt{2}} \tag{71}$$

$$P_{Lf} = r_{Lf}\times\left(\frac{\mathrm{I}_{mg}}{\sqrt{2}}\right)^2 \tag{72}$$

So, the power losses of inductors L_{f1} and L_{f2} can be obtained as follows:

$$P_{Lf1} = P_{Lf2} = \frac{1}{2}r_{Lf}\times\left(\frac{\mathrm{I}_{mg}}{\sqrt{2}}\right)^2 \tag{73}$$

In order to calculate the power losses of capacitors C_1 and C_2, the RMS values of passing currents of these capacitors are calculated based on simulation (at 1 kW output power) and used in the following equations:

$$P_{C1} = r_{C1}\times I^2{}_{C1,rms} \tag{74}$$

TABLE 2 Passing current and RMS value of passing current of switches S_5 and S_6

Switch	Passing current during given time interval	RMS value of passing current during given time interval
S_5	$i_{S5,(0\sim\omega t_1)} = \begin{cases} I_{o1} & ; \quad 0 \le t < D_{1,ave}T_S \\ 0 & ; \quad D_{1,ave}T_S \le t < T_S \end{cases}$	$I_{S5,rms,(0\sim\omega t_1)} = \left[\frac{2\omega t_1}{2\pi}\cdot\frac{1}{T_S}\int_0^{D_{1,ave}T_S} I^2_{o1}\,dt\right]^{1/2} = I_{o1}\sqrt{\frac{\omega t_1 \cdot D_{1,ave}}{\pi}}$
	–	$I_{S5,rms,(\omega t_1\sim\pi-\omega t_1)} = \left[\frac{1}{2\pi}\int_{\omega t_1}^{\pi-\omega t_1} \mathrm{I}^2_{mg}\sin^2(\omega t)\cdot d\omega t\right] =$
		$= \mathrm{I}_{mg}\sqrt{\frac{1}{2\pi}\left(\frac{\pi-2\omega t_1}{2}+\frac{1}{2}(\sin(2\omega t_1))\right)}$
		$= \frac{\mathrm{I}_{mg}}{2}\sqrt{\frac{1}{\pi}(\pi-2\omega t_1+\sin(2\omega t_1))}$
	$i_{S5,(\pi+\omega t_1\sim\pi+\omega t_2)} = \begin{cases} I_{o2} & ; \quad 0 \le t < D_{2,ave}T_S \\ 0 & ; \quad D_{2,ave}T \le t < T_S \end{cases}$	$I_{S5,rms,(\pi+\omega t_1\sim\pi+\omega t_2)} = \left[\frac{2(\omega t_2-\omega t_1)}{2\pi}\cdot\frac{1}{T_S}\int_0^{D_{2,ave}T_S} I^2_{o2}dt\right]^{1/2}$
		$= I_{o2}\sqrt{\frac{(\omega t_2-\omega t_1)D_{2,ave}}{\pi}}$
	$i_{S5,(\pi+\omega t_2\sim\pi+\omega t_3)} = \begin{cases} 0 & ; \quad 0 \le t < D_{3,ave}T_S \\ I_{o3} & ; \quad D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{S5,rms,(\pi+\omega t_2\sim\pi+\omega t_3)} = \left[\frac{2(\omega t_3-\omega t_2)}{2\pi}\cdot\frac{1}{T_S}\int_{D_{3,ave}T_S}^{T_S} I^2_{o3}dt\right]^{1/2}$
		$= I_{o3}\times\sqrt{\frac{(\omega t_3-\omega t_2)(1-D_{3,ave})}{\pi}}$
	$i_{S5,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \begin{cases} I_{o4} & ; \quad 0 \le t < D_{4,ave}T_S \\ 0 & ; \quad D_{4,ave}T_S \le t < T_S \end{cases}$	$I_{S5,rms,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \left[\frac{\pi-2\omega t_3}{2\pi}\cdot\frac{1}{T_S}\int_0^{D_{4,ave}T_S} I^2_{o4}dt\right]^{1/2}$
		$= I_{o4}\sqrt{\frac{(\pi-2\omega t_3)D_{4,ave}}{2\pi}}$
S_6	$i_{S6,(0\sim\omega t_1)} = \begin{cases} 0 & ; \quad 0 \le t < D_{1,ave}T_S \\ I_{o1} & ; \quad D_{1,ave}T_S \le t < DT_S \end{cases}$	$I_{S6,rms,(0\sim\omega t_1)} = \left[\frac{4\omega t_1}{2\pi}\cdot\frac{1}{T_S}\int_{D_{1,ave}T_S}^{T_S} I^2_{o1}dt\right]^{1/2} = I_{o1}\sqrt{\frac{2\omega t_1\cdot(1-D_{1,ave})}{\pi}}$
	$i_{S6,(\pi+\omega t_1\sim\pi+\omega t_2)} = \begin{cases} I_{o2} & ; \quad 0 \le t < D_{2,ave}T_S \\ 0 & ; \quad D_{2,ave}T \le t < T_S \end{cases}$	$I_{S6,rms,(\pi+\omega t_1\sim\pi+\omega t_2)} = \left[\frac{2(\omega t_2-\omega t_1)}{2\pi}\cdot\frac{1}{T_S}\int_0^{D_{2,ave}T_S} I^2_{o2}\right]^{1/2} = I_{o2}\sqrt{\frac{(\omega t_2-\omega t_1)D_{2,ave}}{\pi}}$
	$i_{S6,(\pi+\omega t_2\sim\pi+\omega t_3)} = \begin{cases} 0 & ; \quad 0 \le t < D_{3,ave}T_S \\ I_{o3}; & \quad D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{S6,rms,(\pi+\omega t_2\sim\pi+\omega t_3)} = \left[\frac{2(\omega t_3-\omega t_2)}{2\pi}\cdot\frac{1}{T_S}\int_{D_{3,ave}T_S}^{T_S} I^2_{o3}dt\right]^{1/2}$
		$= I_{o3}\sqrt{\frac{(\omega t_3-\omega t_2)(1-D_{3,ave})}{\pi}}$
	$i_{S6,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \begin{cases} I_{o4} & ; \quad 0 \le t < D_{4,ave}T_S \\ 0 & ; \quad D_{4,ave}T_S \le t < T_S \end{cases}$	$I_{S6,rms,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \left[\frac{\pi-2\omega t_3}{2\pi}\cdot\frac{1}{T_S}\int_0^{D_{4,ave}T_S} I^2_{o4}dt\right]^{1/2} = I_{o4}\sqrt{\frac{(\pi-2\omega t_3)D_{4,ave}}{2\pi}}$

$$P_{C2} = r_{C2}\times I^2{}_{C2,rms} \tag{75}$$

Also, to calculate the power losses of inductor L_1, the average value of passing current of this inductor is calculated based on simulation (at 1 kW output power) and used in the following equation:

$$P_{L1} = r_{L1}\times I^2{}_{L1,rms} \tag{76}$$

Therefore, the total power losses of improved nine-level inverter can be calculated as follows:

$$P_{Loss} = P_{S1}+P_{S2}+P_{S3}+P_{S4}+P_{S5}+P_{S6}+P_{S7}+P_{S8}+P_{S9} + P_{D1}+P_{D2}+P_{C1}+P_{C2}+P_{L1}+P_{Lf} \tag{77}$$

So, the overall efficiency of the improved inverter can be obtained as follows:

$$Efficiancy(\%) = \frac{P_{out}}{P_{in}}\times 100 = \frac{P_{out}}{P_{out}+P_{Loss}}\times 100 \tag{78}$$

TABLE 3 Passing current and RMS value of passing current of switches S_7, S_8, and S_9

S_7	$I_{S7,(\omega t_1 \sim \omega t_2)} = \begin{cases} I_{o2} & ; \quad 0 \le t < D_{2,ave} T_S \\ 0 & ; \quad D_{2,ave} T_S \le t < T_S \end{cases}$	$I_{S7,rms,(\omega t_1 \sim \omega t_2)} = \left[\frac{2(\omega t_2 - \omega t_1)}{2\pi} \cdot \frac{1}{T_S} \int_0^{D_{2,ave} T_S} I^2{}_{o2} dt \right]^{1/2} = I_{o2} \sqrt{\frac{(\omega t_2 - \omega t_1) D_{2,ave}}{\pi}}$
	–	$I_{S7,rms,(\omega t_2 \sim \pi - \omega t_2)} = \left[\frac{1}{2\pi} \int_{\omega t_2}^{\pi - \omega t_2} \mathrm{I}^2{}_{mg} \sin^2(\omega t) d\omega t \right]^{1/2}$ $= \frac{\mathrm{I}_{mg}}{2} \sqrt{\frac{1}{\pi} \times (\pi - 2\omega t_2 + \sin(2\omega t_2))}$
S_8	–	$I_{S8,rms,(0 \sim \pi)} = \left[\frac{1}{2\pi} \int_0^{\pi} \mathrm{I}^2{}_{mg} \cdot \sin^2(\omega t) d\omega t \right]^{1/2} = \frac{\mathrm{I}_{mg}}{2}$
	$i_{S8,(\pi \sim \pi + \omega t_1)} = \begin{cases} 0 & ; \quad 0 \le t < D_{1,ave} T_S \\ I_{o1} & ; \quad D_{1,ave} T_S \le t < T_S \end{cases}$	$I_{S8,rms,(\pi \sim \pi + \omega t_1)} = \left[\frac{2\omega t_1}{2\pi} \cdot \frac{1}{T_S} \int_{D_{1,ave} T_S}^{T_S} I^2{}_{o1} dt \right]^{1/2} = I_{o1} \sqrt{\frac{\omega t_1 (1 - D_{1,ave})}{\pi}}$
S_9	$i_{S9,(\pi \sim \pi + \omega t_1)} = \begin{cases} I_{o1} & ; \quad 0 \le t < D_{1,ave} T_S \\ 0 & ; \quad D_{1,ave} T_S \le t < T_S \end{cases}$	$I_{S9,rms,(\pi \sim \pi + \omega t_1)} = \left[\frac{2\omega t_1}{2\pi} \cdot \frac{1}{T_S} \int_0^{D_{1,ave} T_S} I^2{}_{o1} dt \right]^{1/2} = I_{o1} \sqrt{\frac{\omega t_1 \cdot D_{1,ave}}{\pi}}$
	–	$I_{S9,rms,(\pi + \omega t_1 \sim 2\pi - \omega t_1)} = \left[\frac{1}{2\pi} \int_{\pi + \omega t_1}^{2\pi - \omega t_1} \mathrm{I}^2{}_{mg} \cdot \sin(\omega t) d\omega t \right]^{1/2}$ $= \frac{\mathrm{I}_{mg}}{2} \sqrt{\frac{1}{\pi} (\pi - 2\omega t_1 + \sin(2\omega t_1))}$

TABLE 4 Passing current, RMS and average values of passing current of diodes D_1 and D_2

Diode	Passing current during given time interval	RMS and average values of passing current during given time interval
D_1	$i_{D1,(\omega t_1 \sim \omega t_2)} = \begin{cases} I_{o2} & ; \quad 0 \le t < D_{2,ave}T_S \\ 0 & ; \quad D_{2,ave}T_S \le t < T_S \end{cases}$	$I_{D1,rms,(\omega t_1 \sim \omega t_2)} = \left[\frac{4(\omega t_2 - \omega t_1)}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{2,ave}T_S} I^2{}_{o2}\,dt\right]^{1/2} = I_{o2}\sqrt{\frac{2(\omega t_2 - \omega t_1)\cdot D_{2,ave}}{\pi}}$ $I_{D1,ave,(\omega t_1 \sim \omega t_2)} = \frac{4(\omega t_2 - \omega t_1)}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{2,ave}T_S} I_{o2}\,dt = I_{o2} \times \frac{2(\omega t_2 - \omega t_1)D_{2,ave}}{\pi}$
	$i_{D1,(\omega t_2 \sim \omega t_3)} \begin{cases} 0 & ; \quad 0 \le t < D_{3,ave}T_S \\ \frac{D_{3,ave}}{1 - D_{3,ave}} & ; \quad D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{D1,rms,(\omega t_2 \sim \omega t_3)} = \left[\frac{4(\omega t_3 - \omega t_2)}{2\pi} \cdot \frac{1}{T_S}\int_{D_{3,ave}T_S}^{T_S} \left(\frac{D_{3,ave}}{1 - D_{3,ave}} I_{o3}\right)^2\right]^{1/2} = D_{3,ave} \cdot I_{o3} \times \sqrt{\frac{2(\omega t_3 - \omega t_2)}{\pi(1 - D_{3,ave})}}$ $I_{D1,ave,(\omega t_2 \sim \omega t_3)} = \frac{4(\omega t_3 - \omega t_2)}{2\pi} \cdot \frac{1}{T_S}\int_{D_{3,ave}T_S}^{T_S} \frac{D_{3,ave}}{1 - D_{3,ave}} I_{o3}\,dt = D_{3,ave} \times I_{o3} \times \frac{2(\omega t_3 - \omega t_2)}{\pi}$
D_2	$i_{D2,rms,(\omega t_3 \sim \pi - \omega t_3)} = \begin{cases} I_{o4} & ; \quad 0 \le t < D_{4,ave}T_S \\ 0 & ; \quad D_{4,ave}T_S \le t < T_S \end{cases}$	$I_{D2,rms,(\omega t_3 \sim \pi - \omega t_3)} = \left[\frac{\pi - 2\omega t_3}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{4,ave}T_S} I^2{}_{o4}\,dt\right]^{1/2} = I_{o4}\sqrt{\frac{(\pi - 2\omega t_3)D_{4,ave}}{2\pi}}$ $I_{D2,ave,(\omega t_3 \sim \pi - \omega t_3)} = \frac{\pi - 2\omega t_3}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{4,ave}T_S} I_{o4}\,dt = \frac{(\pi - 2\omega t_3)D_{4,ave}}{2\pi}$
	$i_{D2,(\pi \sim \pi + \omega t_1)} \begin{cases} I_{o1} & ; \quad 0 \le t < D_{1,ave}T_S \\ 0 & ; \quad D_{1,ave}T_S \le t < T_S \end{cases}$	$I_{D2,rms,(\pi \sim \pi + \omega t_1)} = \left[\frac{2\omega t_1}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{1,ave}T_S} I^2{}_{o1}\,dt\right]^{1/2} = I_{o1} \times \sqrt{\frac{\omega t_1}{\pi} \cdot D_{1,ave}}$ $I_{D2,ave,(\pi \sim \pi + \omega t_1)} = \frac{2\omega t_1}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{1,ave}T_S} I_{o1}\,dt = \frac{\omega t_1 \cdot I_{o1} \cdot D_{1,ave}}{\pi}$
	$i_{D2,(\pi + \omega t_1 \sim \pi + \omega t_2)} = \begin{cases} 0 & ; \quad 0 \le t < D_{2,ave}T_S \\ I_{o2} & ; \quad D_{2,ave}T_S \le t < T_S \end{cases}$	$I_{D2,rms,(\pi + \omega t_1 \sim \pi + \omega t_2)} = \left[\frac{2(\omega t_2 - \omega t_1)}{2\pi} \cdot \frac{1}{T_S}\int_{D_{2,ave}T_S}^{T_S} I^2{}_{o2}\,dt\right]^{1/2}$ $= I_{o2} \times \sqrt{\frac{(\omega t_2 - \omega t_1)(1 - D_{2,ave})}{\pi}}$ $I_{D2,ave,(\pi + \omega t_1 \sim \pi + \omega t_2)} = \frac{2(\omega t_2 - \omega t_1)}{2\pi} \cdot \frac{1}{T_S}\int_{D_{2,ave}\cdot T_S}^{T_S} I_{o2}\,dt = \frac{(\omega t_2 - \omega t_1)(1 - D_{2,ave})I_{o2}}{\pi}$
	$i_{D2,(\pi + \omega t_2 \sim \pi + \omega t_3)} = \begin{cases} I_{o3} & ; \quad 0 \le t < D_{3,ave}T_S \\ 0 & ; \quad D_{3,ave}T_S \le t < T_S \end{cases}$	$I_{D2,rms,(\pi + \omega t_2 \sim \pi + \omega t_3)} = \left[\frac{2(\omega t_3 - \omega t_2)}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{3,ave}T_S} I^2{}_{o3}\,dt\right]^{1/2} = I_{o3} \times \sqrt{\frac{(\omega t_3 - \omega t_2) \times D_{3,ave}}{\pi}}$ $I_{o2,ave,(\pi + \omega t_2 \sim \pi + \omega t_3)} = \frac{2(\omega t_3 - \omega t_2)}{2\pi} \cdot \frac{1}{T_S}\int_0^{D_{3,ave}T_S} I_{o3,ave}\,dt = \frac{(\omega t_3 - \omega t_2) \times I_{o3} \times D_{3,ave}}{\pi}$
	$i_{D2,(\pi + \omega t_3 \sim 2\pi - \omega t_3)} = \begin{cases} I_{o4} & ; \quad 0 \le t < D_{4,ave}T_S \\ I_{o4} & ; \quad D_{4,ave}T_S \le t < T_S \end{cases}$	$I_{D2,rms,(\pi + \omega t_3 \sim 2\pi - \omega t_3)} = \left[\frac{\pi - 2\omega t_3}{2\pi} \cdot \frac{1}{T_S}\int_0^{T_S} I^2{}_{o4}\,dt\right]^{1/2} = I_{o4} \times \sqrt{\frac{\pi - 2\omega t_3}{2\pi}}$ $I_{D2,ave,(\pi + \omega t_3 \sim 2\pi - \omega t_3)} = \frac{\pi - 2\omega t_3}{2\pi} \cdot \frac{1}{T_S}\int_0^{T_S} I_{o4}\,dt = I_{o4} \times \frac{\pi - 2\omega t_3}{2\pi}$

Required parameters for calculating the switching and conducting losses of the semiconductor devices of the mentioned inverter are given as follows:

$$\begin{cases} r_{DS} = 0.07\,\Omega, \quad r_d = 0.07\,\Omega \\ r_{C1} = r_{C2} = 0.15\ \Omega \\ r_{Lf} = 0.2\ \Omega, \quad r_{L1} = 0.1\,\Omega \\ V_{DC} = 200\,\text{V}, \quad V_{mg} = 311.12\,\text{V}, \quad V_\gamma = 0.7\,\text{V} \\ \textit{Switches}: \ t_{on} = 53\,\text{ns}, \quad t_{off} = 35\,\text{ns} \\ \textit{Diodes}: \ t_{on} = 30\,\text{ns}, \quad t_{off} = 20\,\text{ns} \\ t_1 = 1ms.\,\text{s}, \quad t_2 = 2.2mS\,\text{s}, \quad t_3 = 4.1ms\,\text{s}, \\ \omega = 2\pi f = 314.15Rad/s \\ T_S = 50\,\mu\text{s} \end{cases} \tag{79}$$

where r_{DS}, r_d, r_{C1}, r_{C2}, r_{Lf}, and r_{L1}, are the internal resistance of switches, diodes, capacitors C_1, capacitor C_2, and inductor L_{fs} and inductor L_1, respectively. Also, V_γ, t_{on} and t_{off} are voltage drop of diodes, turn-on delay time and turn-off delay time of switches and diodes, respectively.

The conduction losses, switching losses and total losses of each switch and diodes are calculated at 1000 W output power and presented in Table 7. Based on Table 7, it can be seen that the total losses (P_{Loss}) of inverter at 1000 W output power is equal to 25.64 W. So, by using (80), the overall efficiency of the improved inverter at 1000 W output power can be obtained as follows:

$$\begin{aligned} Efficiancy(\%) &= \frac{P_{out}}{P_{in}} \times 100 = \frac{P_{out}}{P_{out} + P_{Loss}} \times 100 \\ &= \frac{1000\,(W)}{1000\,(W) + 25.64\,(W)} = 97.50(\%) \end{aligned} \tag{80}$$

TABLE 5 Switching and conduction losses of switches S_2, S_3, S_4, S_5, and S_6

Switch	Switching losses	Conduction losses
S_2	$P_{SW,S2,(\omega t_2\sim\omega t_3)} = \frac{1}{6}\times V_{DC}\times\frac{D_{3,ave}\cdot I_{o3}}{1-D_{3,ave}}\times(t_{on}+t_{off})\times(4N_{SW3})\times f_g$	$P_{con,S2,(\omega t_2\sim\omega t_3)} = \frac{r_{DS}\times(D_{3,ave}\cdot I_{o3})^2\times 2(\omega t_3-\omega t_2)}{\pi(1-D_{3,ave})}$
	0	$P_{con,S2,(\pi\sim\pi+\omega t_1)} = \frac{r_{DS}\times I_{o1}\times\omega t_1\times D_{1,ave}}{\pi}$
	0	$P_{con,S2,(\pi+\omega t_1\sim\pi+\omega t_2)} = \frac{r_{DS}\times(I_{o2})^2\times(\omega t_2-\omega t_1)(1-D_{2,ave})}{\pi}$
S_3	$P_{SW,S3,(\omega t_2\sim\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o3}\times(t_{on}+t_{off})\times(2N_{SW3})\times f_g$	$P_{con,S3,(\omega t_2\sim\omega t_3)} = \frac{2r_{DS}\times I^2_{o3}\times(\omega t_3-\omega t_2)D_{3,ave}}{\pi}$
	$P_{SW,S3,(\omega t_3\sim\pi-\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o4}\times(t_{on}+t_{off})\times(2N_{SW4})\times f_g$	$P_{con,S3,(\omega t_3\sim\pi-\omega t_3)} = \frac{2r_{DS}\times I^2_{o4}\times(\pi-2\omega t_3)(1-D_{4,ave})}{2\pi}$
S_4	$P_{S4,SW,(0\sim\omega t_1)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o1}\times(t_{on}+t_{off})\times(4N_{SW1})\times f_g$	$P_{con,S4,(0\sim\omega t_1)} = \frac{(2r_{DS})\times(I_{o1})^2\times 2\omega t_1\times D_{1,ave}}{\pi}$
	$P_{SW,S4,(\omega t_1\sim\omega t_2)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o2}\times(t_{on}+t_{off})\times(4N_{SW2})\times f_g$	$P_{con,S4,(\omega t_1\sim\omega t_2)} = \frac{(2r_{DS})\times I^2_{o2}\times 2(\omega t_2-\omega t_1)D_{2,ave}}{\pi}$
	$P_{SW,S4,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o3}\times(t_{on}+t_{off})\times(2N_{SW3})\times f_g$	$P_{con,S4,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{(2r_{DS})\times I^2_{o3}\times(\omega t_3-\omega t_2)D_{3,ave}}{\pi}$
	$P_{SW,S4,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o4}\times(t_{on}+t_{off})\times(2N_{SW4})\times f_g$	$P_{con,S4,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{(2r_{DS})\times I^2_{o4}\times(\pi-2\omega t_3)(1-D_{4,ave})}{2\pi}$
S_5	$P_{SW,S5,(0\sim\omega t_1)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o1}\times(t_{on}+t_{off})\times(2N_{SW1})\times f_g$	$P_{con,S5,(0\sim\omega t_1)} = \frac{r_{DS}\times I^2_{o1}\times\omega t_1\times D_{1,ave}}{\pi}$
	0	$P_{con,S5,(\omega t_1\sim\pi-\omega t_1)} = \frac{r_{DS}\times I^2_{mg}\times(\pi-2\omega t_1+\sin(2\omega t_1))}{4\pi}$
	$P_{SW,S5,(\pi+\omega t_1\sim\pi+\omega t_2)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o2}\times(t_{on}+t_{off})\times(2N_{SW2})\times f_g$	$P_{con,S5,(\pi+\omega t_1\sim\pi+\omega t_2)} = \frac{r_{DS}\cdot I^2_{o2}(\omega t_2-\omega t_1)D_{2,ave}}{\pi}$
	$P_{SW,S5,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o3}\times(t_{on}+t_{off})\times(2N_{SW3})\times f_g$	$P_{con,S5,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{r_{DS}\times I^2_{o3}\times(\omega t_3-\omega t_2)(1-D_{3,ave})}{\pi}$
	$P_{SW,S5,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o4}\times(t_{on}+t_{off})\times(2N_{SW4})\times f_g$	$P_{con,S5,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{r_{DS}\times I^2_{o4}\times(\pi-2\omega t_3)D_{4,ave}}{2\pi}$
S_6	$P_{SW,S6,(0\sim\omega t_1)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o1}\times(t_{on}+t_{off})\times(4N_{SW1})\times f_g$	$P_{con,S6,(0\sim\omega t_1)} = \frac{r_{DS}\times I^2_{o1}\times 2\omega t_1\times(1-D_{1,ave})}{\pi}$
	$P_{SW,S6,(\pi+\omega t_1\sim\pi+\omega t_2)} = \frac{1}{6}\times(0.5V_{DC})\times(I_{o2})\times(t_{on}+t_{off})\times(2N_{SW2})\times f_g$	$P_{con,S6,(\pi+\omega t_1\sim\pi+\omega t_2)} = \frac{r_{DS}\times I^2_{o2}\times(\omega t_2-\omega t_1)\times D_{2,ave}}{\pi}$
	$P_{SW,S6,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o3}\times(t_{on}+t_{off})\times(2N_{SW3})\times f_g$	$P_{con,S6,(\pi+\omega t_2\sim\pi+\omega t_3)} = \frac{r_{DS}\times I^2_{o3}\times(\omega t_3-\omega t_2)(1-D_{3,ave})}{\pi}$
	$P_{SW,S6,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{1}{6}\times(0.5V_{DC})\times I_{o4}\times(t_{on}+t_{off})\times(2N_{SW4})\times f_g$	$P_{con,S6,(\pi+\omega t_3\sim 2\pi-\omega t_3)} = \frac{r_{DS}\times I^2_{o4}\times(\pi-2\omega t_3)\times D_{4,ave}}{2\pi}$

Based on above power losses analysis of improved inverter and Table 7, the bar and pie chart of loss breakdown of improved inverter are shown in Figure 7a and 7b, respectively. In Figure 7a, the power losses of switches (S_1–S_9), diodes (D_1–D_2), capacitors (C_1 and C_2), and inductors (L_1 and L_f) are shown by P_{S1}–P_{S9}, P_{D1}–P_{D2}, P_{C1} and P_{C2}, and P_{L1} and P_{Lf}, respectively. Figure 7b also shows the percentage share of each component (switches, diodes and inductors) of the total power losses of the improved inverter. Figure 8 indicates the simulation efficiency curve of improved topology at different output powers.

Based on this figure, the maximum simulation efficiency is equal to 97.44 which is occurred at 430 W.

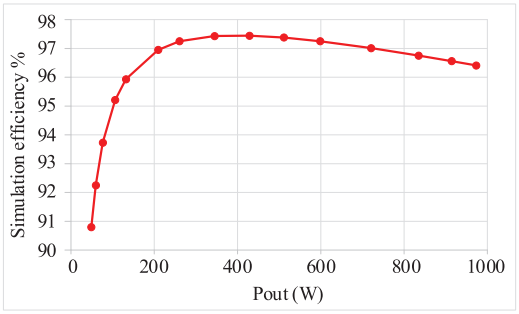


FIGURE 8 Simulation efficiency curve of the improved converter at different output powers

6 | SIMULATION RESULTS DURING THE STEP CHANGE ON THE OUTPUT ACTIVE AND REACTIVE POWERS

In this section, to show the accurate performance of improved inverter and its control system under a step change on output power, some simulation results are obtained by using MATLAB/Simulink and provided. Figure 9 shows the output voltage (V_{out}), grid voltage (V_G) and injected grid current (IG) at unity power factor and step change on output power. In Figure 9a, output power changes from 0.38 to 0.77 kW. Also, based on Figure 9b it can be seen that the output power decrease from 0.77 to 0.37 kW. Considering Figure 9, it can be understood

TABLE 6 Switching and conduction losses of switches S_7–S_9 and diodes D_1 and D_2

Switch	Switching losses	Conduction losses
S_7	$P_{S7,(\omega t_1 \sim \omega t_2)} = \frac{1}{6} \times (0.5V_{DC}) \times I_{o2} \times (t_{on} + t_{off}) \times (2N_{SW2}) \times f_g$	$P_{con,S7,(\omega t_1 \sim \omega t_2)} = \frac{r_{DS} \times (\omega t_2 - \omega t_1) D_{2,ave}}{\pi}$
	0	$P_{con,S_7,(\omega t_2 \sim \pi - \omega t_2)} = \frac{r_{DS} \times I^2{}_{mg} \times \left(\pi - 2\omega t_2 + \sin(2\omega t_2)\right)}{4\pi}$
S_8	0	$P_{con,S8,(0 \sim \pi)} = r_{DS} \times (\frac{\mathrm{I}_{mg}}{2})^2$
	$P_{SW,S8,(\pi \sim \pi + \omega t_1)} = \frac{1}{6} \times (0.5V_{DC}) \times I_{o1} \times (t_{on} + t_{off}) \times (2N_{SW1}) \times f_g$	$P_{con,S8,(\pi \sim \pi + \omega t_1)} = \frac{r_{DS} \times I^2{}_{o1} \times \omega t_1 (1 - D_{1,ave})}{\pi}$
S_9	$P_{SW,S9,(\pi \sim \pi + \omega t_1)} = \frac{1}{6} \times (0.5V_{DC}) \times I_{o1} \times (t_{on} + t_{off}) \times (2N_{SW1}) \times f_g$	$P_{con,S9,(\pi \sim \pi + \omega t_1)} = \frac{r_{DS} \times I^2_{o1} \times \omega t_1 \times D_{1,ave}}{\pi}$
	0	$P_{con,S9,(\pi + \omega t_1 \sim 2\pi - \omega t_1)} = \frac{r_{DS} \times \mathrm{I}^2{}_{mg} \times \left(\pi - 2\omega t_1 + \sin(2\omega t_1)\right)}{4\pi}$
D_1	0	$P_{con,D1,(\omega t_1 \sim \omega t_2)} = \frac{r_d \times I^2{}_{o2} \times 2(\omega t_2 - \omega t_1) \times D_{2,ave}}{\pi} + \frac{2I_{o2} \times (\omega t_2 - \omega t_1) \times D_{2,ave}}{\pi} \times V_\gamma$
	$P_{SW,D1,(\omega t_2 \sim \omega t_3)} = \frac{1}{6} \times V_{DC} \times \frac{D_{3,ave} \times I_{o3}}{1 - D_{3,ave}} \times (t_{on} + t_{off}) \times (4N_{SW3}) \times f_g$	$P_{con,D1,(\omega t_2 \sim \omega t_3)} = \frac{r_d \times (D_{3,ave} \times I_{o3})^2 \times 2(\omega t_3 - \omega t_2)}{\pi(1 - D_{3,ave})} + \frac{D_{3,ave} \cdot I_{o3} \times 2(\omega t_3 - \omega t_2) \times V_\gamma}{\pi}$
D_2	0	$P_{con,D2,(\omega t_3 \sim \pi - \omega t_3)} = \frac{r_d \times I^2{}_{o4} \times (\pi - 2\omega t_3) D_{4,ave}}{2\pi} + \frac{(\pi - 2\omega t_3) D_{4,ave}}{2\pi} \times V_\gamma$
	0	$P_{con,D2,(\pi \sim \pi + \omega t_1)} = \frac{r_d \times I^2{}_{o1} \times \omega t_1 \times D_{1,ave}}{\pi} + \frac{\omega t_1 \times I_{o1} \times D_{1,ave}}{\pi} \times V_\gamma$
	0	$P_{con,D2,(\pi + \omega t_1 \sim \pi + \omega t_2)} = \frac{r_d \times I^2{}_{o2} \times (\omega t_2 - \omega t_1) \times (1 - D_{2,ave})}{\pi} + \frac{(\omega t_2 - \omega t_1) \times I_{o2} \times (1 - D_{2,ave})}{\pi} \times V_\gamma$
	0	$P_{con,D2,(\pi + \omega t_2 \sim \pi + \omega t_3)} = \frac{r_d \cdot I^2{}_{o3} \times (\omega t_3 - \omega t_2) \times D_{3,ave}}{\pi} + \frac{(\omega t_3 - \omega t_2) \times I_{o3} \times D_{3,ave}}{\pi} \times V_\gamma$
	0	$P_{con,D2,(\pi + \omega t_3 \sim 2\pi - \omega t_3)} = \frac{r_D \times I^2{}_{o4} \times (\pi - 2\omega t_3)}{2\pi} + \frac{I_{o4} \times (\pi - 2\omega t_3)}{2\pi} \times V_\gamma$

TABLE 7 Detailed presentation of the switching and conducting losses of the semiconductor devises of the proposed inverter

P_{out} = 1000 W			
Switches & diodes	P_{con} (W)	P_{SW} (W)	P_S & P_D & P_C & P_L
S_1	0.3753	0.07270	0.4480
S_2	0.6626	0.1665	0.8291
S_3	0.7088	0.0425	0.7513
S_4	1.0425	0.0719	1.1144
S_5	0.8803	0.0573	0.9376
S_6	0.2274	0.0609	0.2883
S_7	0.6719	0.0111	0.6830
S_8	0.7283	0.0037	0.7320
S_9	0.7179	0.0037	0.7216
D_1	1.8131	0.0946	1.9077
D_2	1.3051	0	1.3052
C_1 & C_2	3.3844	–	6.7688
L_1	5.0268	–	5.0268
L_f	4.1322	–	4.1322

that the improved inverter operates at unity power factor (PF). Regarding Figure 9, it can be verified that the improved inverter along with its control strategy can support the step change on output power at unity PF.

Figure 10 illustrates the output voltage, grid voltage and injected current to the grid at lag power factor. Based on this figure, it can be seen that the improved inverter injects reactive power to the grid. With respect to Figure 10a, the value of apparent output power (KVA) changes from 0.38 to 0.77 kVA. Regarding this figure, despite of that the improved inverter along with its control system can support the reactive power, also it can handle the step change under the non-unity power factor. Figure 10b shows the output voltage, grid voltage and injected current to the grid at lead PF. In the other words, the inverter absorbs reactive power from the grid. According to this figure, it can be seen that the amount of apparent power injected into the grid has increased from 0.38 to 0.77 kVA.

Figure 11 indicates the output voltage (V_{out}), grid voltage (V_G) and injected current to the grid (I_G) under step change on phase angle of injected current to the grid. Considering this

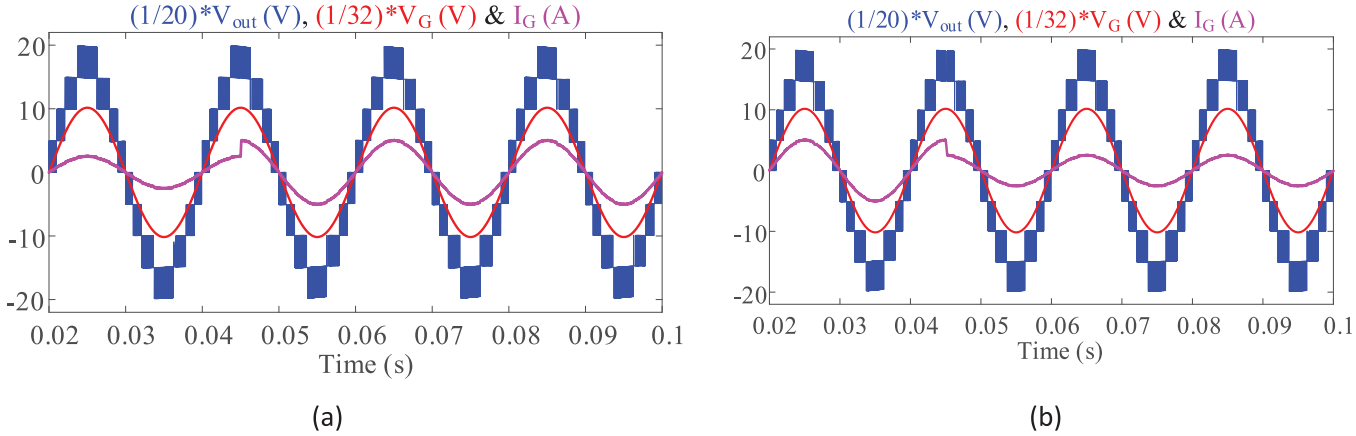


FIGURE 9 Simulation results of output voltage (V_{out}), grid voltage (V_G) and injected current to the grid (I_G) in unity PF under step change on output power: (a) From 0.38 to 0.77 kW, (b) from 0.77 to 0.38 kW

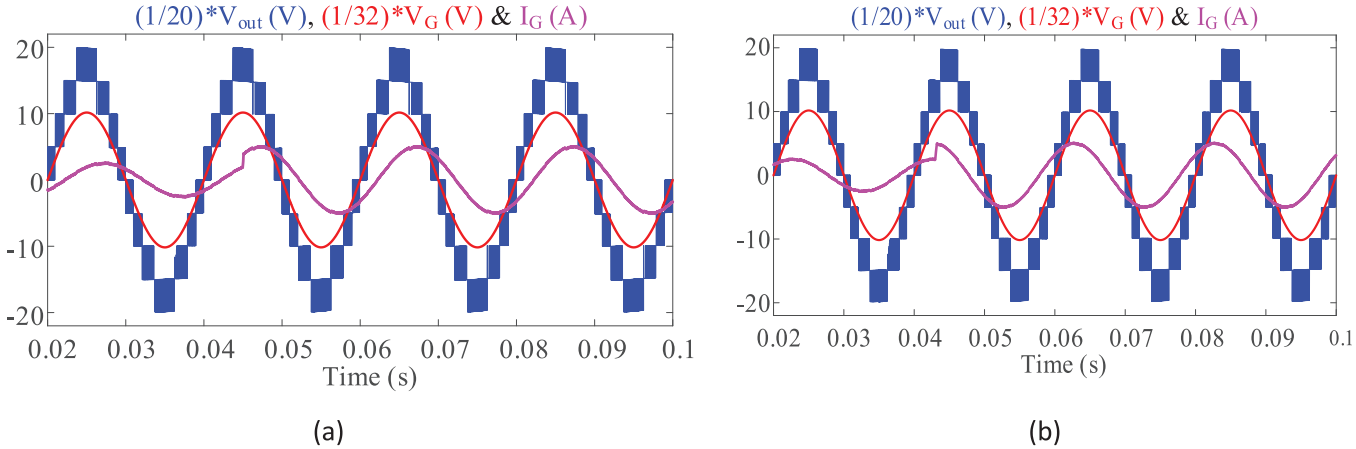


FIGURE 10 Simulation results of output voltage (V_{out}), grid voltage (V_G) and injected current to the grid (I_G): (a) At lag PF and under step change on output power from 0.38 to 0.77 kVA, (b) at lead PF from 0.77 to 0.38 kW and under step change on output power from 0.77 to 0.38 kVA

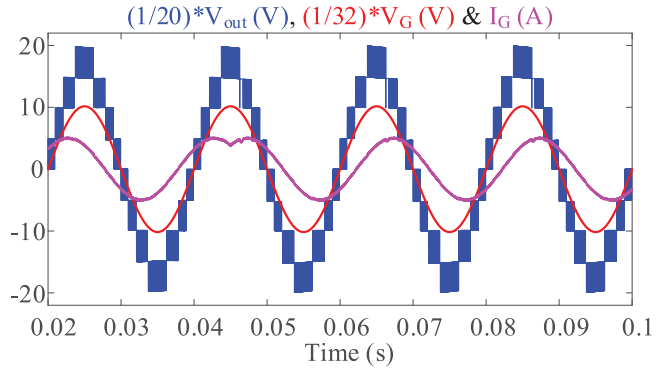


FIGURE 11 Simulation results: Output voltage (V_{out}), grid voltage (V_G) and injected current to the grid (I_G) under step change on phase angle of injected current to the grid

figure, the amplitude of the apparent power injected into the grid is constant and the step change has occurred in the phase angle of the injected grid current.

In the other words, the operation of the inverter has changed from lead PF condition to lag PF condition. Also, it can be verified that the improved inverter along with its control strategy can support the step change on phase angle of injected current to the grid.

Based on the presented simulation results, it can be seen that the use of inductor L_1 along with anti-parallel diode in the improved inverter does not create any restrictions for the system and the inverter can continue to operate correctly even in non-unity PF. In addition to correct performance in non-unity power factor and in steady state, the inverter can also handle step change in non-unity PF.

7 | COMPARISON OF IMPROVED TOPOLOGY WITH OTHER STRUCTURES

In order to highlight some attractive features of the improved structure, it is compared with several nine-level inverters as shown in Table 8. This comparison is performed in terms of number of switches (N_{Sw}), number of utilized diodes (N_D),

TABLE 8 Comparison of improved topology with some 9-level inverters

	Number of Components												
Ref	N_{Sw}	N_D	N_{Cap}	N_{DC}	**T.C.**	V_{in} **(V)**	**Voltage gain**	**Voltage boosting ability**	**Reduction of spike current**	P_{OUT} **(W)**	**Total volume (mm^3)**	**Power density (W/mm^3)**	**Total Cost ($)**	$Cost/P_{OUT}$ **(P.U.)**
[33]	11	0	2	1	13	320	2	Yes	No	100	120,824.9	0.82×10^{-3}	33.26	0.33
[35]	12	0	3	1	15	80	4	Yes	No	2000	151,433.6	13.2×10^{-3}	104.87	0.052
[36]	9	1	2	1	13	45	4	Yes	No	350	324,841.1	1.077×10^{-3}	162.62	0.14
[38]	9	3	2	1	14	25	4	Yes	No	240	93,555.92	2.56×10^{-3}	63.27	0.26
[39]	8	3	3	1	14	80	4	Yes	No	512	565,735.9	0.905×10^{-3}	81.40	0.15
[23]	10	0	2	1	12	100	2	Yes	No	200	123,311.1	1.62×10^{-3}	131.5	0.66
[37]	12	0	1	2	14	200	1	No	No	200	26,236.1	7.62×10^{-3}	71.9	0.36
[54]	17	0	4	1	21	100	1	No	No	500	240,080.8	2.08×10^{-3}	202.4	0.40
[55]	12	0	2	1	14	200	2	Yes	No	600	125,879.7	4.76×10^{-3}	164.08	0.30
[51]	10	0	2	1	12	100	2	Yes	No	200	113,663.3	1.75×10^{-3}	232.12	1.16
[49]	12	0	2	1	14	200	2	Yes	No	612	1,314,343	0.46×10^{-3}	118.35	0.20
[52]	10	0	2	1	12	50	2	Yes	No	200	23,561.23	8.48×10^{-3}	27.51	0.14
[53]	10	1	2	1	13	50	4	Yes	No	500	522,340.2	0.95×10^{-3}	228.02	0.45
[50]	9	3	3	1	15	100	4	Yes	No	1000	578,032.2	1.73×10^{-3}	143.78	0.14
Improved	9	2	2	1	13	200	2	Yes	Yes	770	76,767.56	10.03×10^{-3}	106.23	0.13

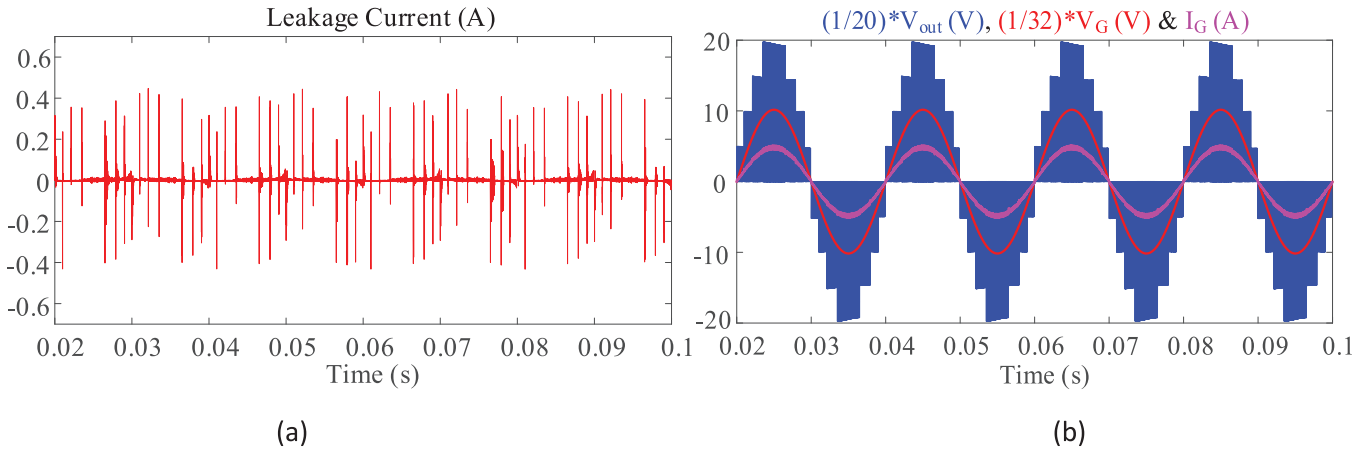


FIGURE 12 Simulation results of improved inverter: (a) Leakage current, (b) output voltage, grid voltage and injected current to the grid

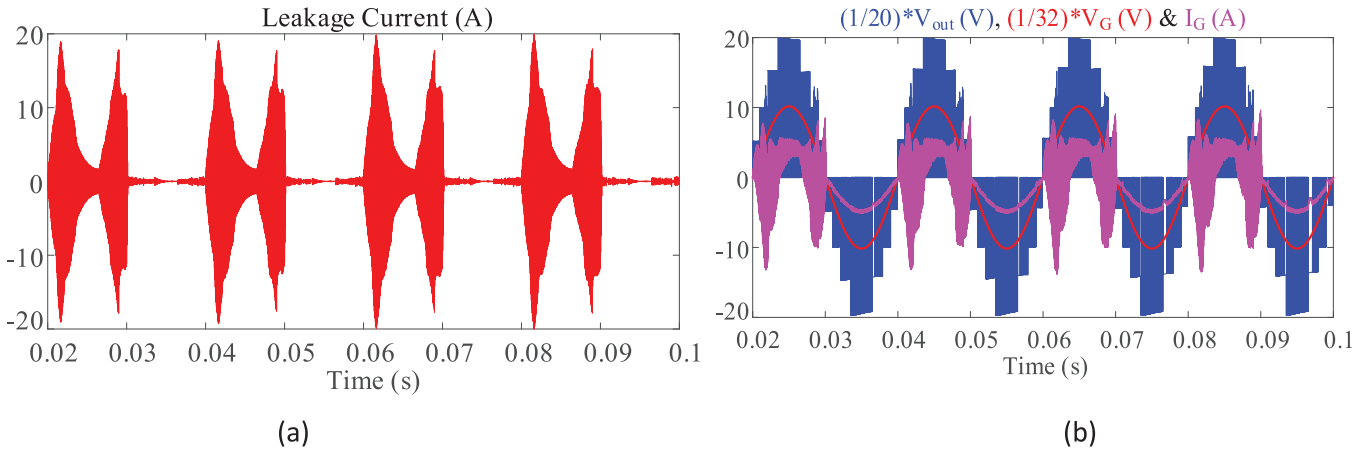


FIGURE 13 Simulation results of topology of [46]: (a) Leakage current, (b) output voltage, grid voltage and injected current to the grid

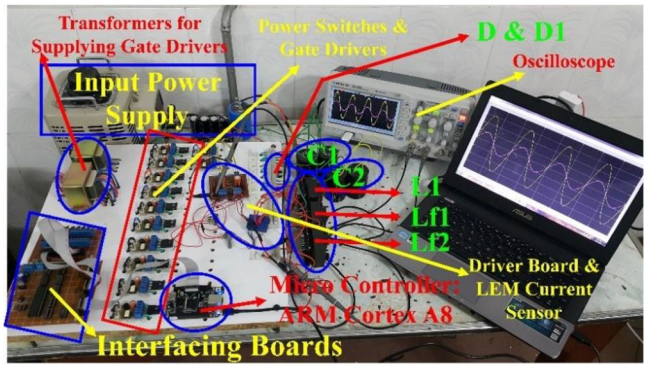


FIGURE 14 Photograph of the modified 9-level laboratory prototype

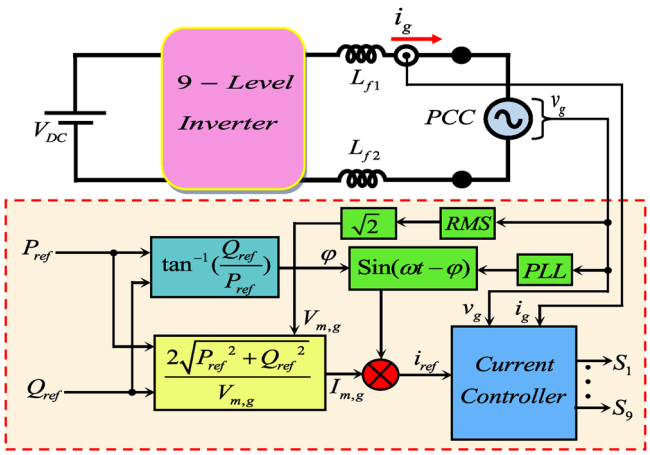


FIGURE 15 Applied control block diagram of the improved inverter

number of capacitors (N_{Cap}), number of input DC sources (N_{DC}), total components (T.C. = total) number of utilized switches, diodes, capacitors in each compared topologies), amplitude of input voltage (V_{in}), voltage gain, voltage boosting ability, reducing spike current of switched capacitors, output power (P_{OUT}), total cost ($), cost/$P_{OUT}$ (P.U.).

Based on Table 1, the total number of utilized components (T.C.) of the first improved inverter is less than all of the compared topologies except [36] and [23]. However, the values of

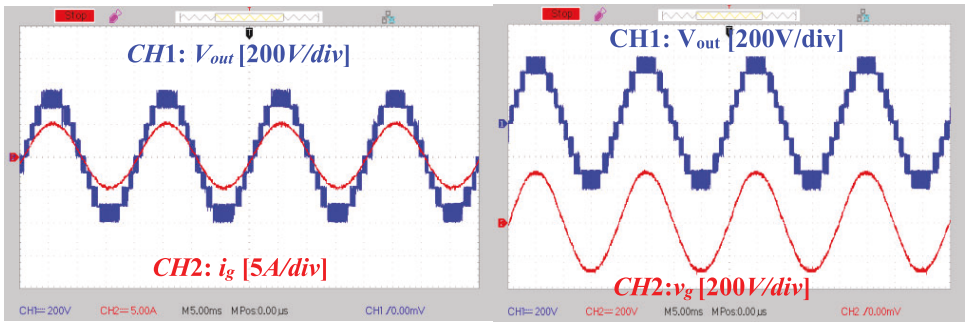


FIGURE 16 Excremental results: (a) Output voltage (200 V/div) and injected current to the grid (5 A/div), (b) output voltage (200 V/div) and grid voltage (200 V)

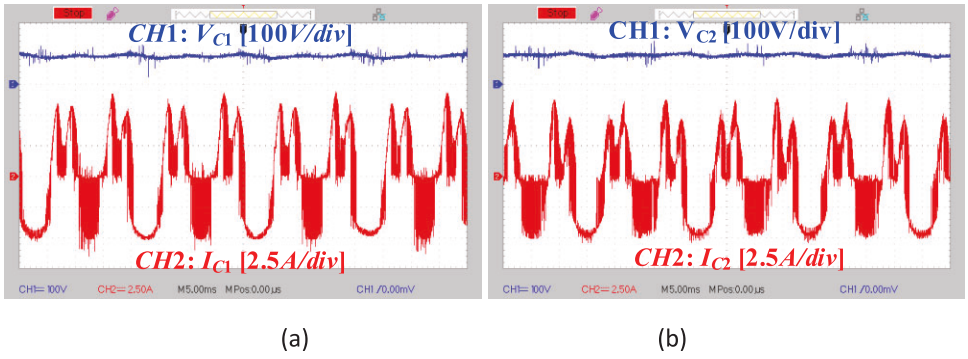


FIGURE 17 Across voltage (100 V/div) and passing current (2.5 A/div) of utilized capacitors: (a) Capacitor C_1 (b) capacitor C_2

TABLE 9 Circuit components and their descriptions

Element	Type	Description
Input DC source (V_{DC})	–	200 V
Power electronic switches	47N60C	650 V/47 A
Gate driver	TLP 250	IC
Power diodes	MUR1560	600 V/15 A
Current transducer	LA55P	Hall effect
Microcontroller	Beagle Bone Black	ARM
Local grid's frequency	50 Hz	–
Sampling frequency	40KHz	–
C_1, C_2	1000 μF	150 V
Inductor L_1	Ferrite core	1 mH
Inductor L_{f1} and L_{f2}	Ferrite core	1 mH

total cost (\$) and $cost/P_{OUT}$ (P.U.) of the topologies [36] and [23] are more than the improved topology. As mentioned before, one of the major disadvantages of the switched capacitor-based topologies is the spike current of capacitors. With respect to Table 1, only improved inverter can reduce the spike current of the capacitors during charging mode.

Considering Table 8, it can be understood that the value of $cost/P_{OUT}$ of the improved inverter is less than all of the compared topologies. Finally, from the above comparison, it can be concluded that the improved inverter has an acceptable rank when compared with the recently proposed topologies on total number of utilized components (T.C.), reduction of spike current of capacitors in charging mode, output power (W), Power density (W/mm^3), total cost (\$), and $cost/P_{OUT}$ (P.U). Based on Table 8, total used components in improved topology are less than topologies [49] and [50].

With respect to Table 8, it can be obvious that despite of topologies [49–53], the improved inverter can limit the capacitor charging spike by using inductor in the charging path of capacitors.

Note that, the power density of the modified topology and other compared topologies are calculated as follows:

$$Power\ density\ (\mathrm{W/mm^3}) = \frac{P_{out}\ (\mathrm{W})}{Total\ volume\ (\mathrm{mm^3})} \tag{81}$$

where P_{out} and total volume denote the output power and total volume of each topology. To calculate the total volume of each topology, the volume of each of the energy storage components, such as the capacitors and inductors (inductor core), the volume of the used power switches and power diodes, according to the information contained in the datasheet of the mentioned components, have been obtained and added together numerically.

Compared with multilevel inverters which are presented in [49–53], the improved nine-level switched-capacitor based

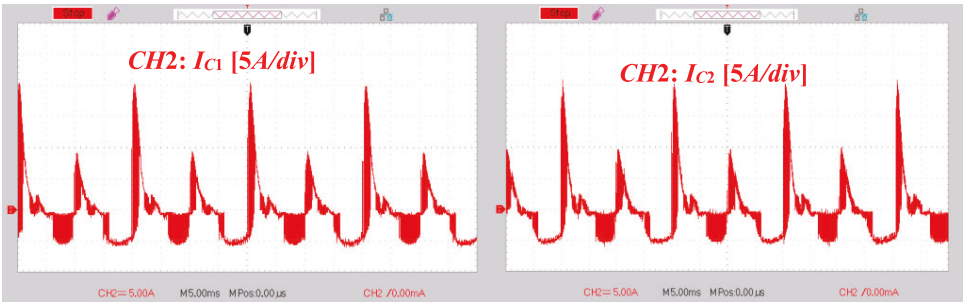


FIGURE 18 Current of Capacitors C_1 and C_2 in absence of peak current limiter inductance L_1. (a) Capacitor C_1 current, (b) capacitor C_2 current

inverter has the minimum values of total volume and $cost/P_{OUT}$ (P.U.). So, the improved topology has the maximum value of power density among the mentioned compared topologies. Also, the improved inverter is an economical and efficient structure among the mentioned topologies. Regarding Table 7, among topologies [49–53], the improved inverter has the minimum value of total cost ($). As a result, the modified inverter is an economical topology among the mentioned inverters.

In addition, in order to compare the improved inverter and proposed topology in [46] and show the difference between the improved inverter and the mentioned topology, the simulation results are obtained by MATLAB/Simulink and presented as follows:

Figures 12 and 13 present the simulation results of improved inverter and topology of [46], respectively. The leakage current waveform of improved inverter is illustrated in Figure 12a. Figure 10b indicates the output voltage (V_{out}), grid voltage (V_G), and injected current to the grid (I_G) waveforms of improved inverter at unity PF. Also, Figures 12a and 12b show the leakage current waveform and the output voltage (V_{out}), grid voltage (V_G), and injected current to the grid (I_G) waveforms of improved inverter at unity PF, respectively.

In order to measure the leakage current waveform in both improved and topology of [46], a capacitor with the capacitance value of 50 nF is located between negative terminal of input DC source and null of grid. Based on Figure 13a, the RMS value of leakage current of improved inverter is equal to 45 mA. Also, the RMS value of leakage current of proposed topology in [R1] is equal to 5 A. So, it can be concluded that the improved topology has the less value of leakage current and neat output voltage waveform compared with the proposed inverter in [46].

Note that, waveforms of output voltage, grid voltage and injected current to the grid of both topologies are obtained in the presence of a capacitor of 50 nF, which is located between null of grid and negative terminal input dc source. Based on Figure 12b, it can be seen that the waveforms of output voltage, grid voltage and injected grid current have a good quality during both positive and negative half cycles. But, in topology of [46], the output voltage and injected grid current waveforms have a bad quality during positive half cycle. By comparing Figures 12b and 13b, it can be seen that the power quality of improved inverter is better that the compared topology.

Finally, it can be concluded that compared with topology of [46] the improved inverter has less value of leakage current and provide a good quality of output voltage and grid voltage and injected current to the grid in the presence of a capacitor of 50 nF, which is located between null of grid and negative terminal input DC source.

8 | EXPERIMENTAL RESULTS

In this part in order to confirm the performance of the improved topology some experimental results based on a 770 W laboratory prototype have been provided. Also, as shown in Figure 14, a prototype of the second improved 9-level inverter has been built in order to obtain experimental results. It should be noted that the experimental results are for grid-connected mode of operation. In this case, the control block diagram of the improved inverter is shown in Figure 15, in which to generate the gate pulse of utilized power switches in the improved inverter a peak current control (PCC) strategy is applied [15]. By applying this strategy both active and reactive powers is controlled. With respect to Figure 15, in order to obtain the appropriate amplitude and phase of the grid, a phased locked loop (PLL) unit is considered. The amplitude and phase of the injected current to the grid (i_{ref}) could be generated based on the reference values of active and reactive powers (P_{ref} and Q_{ref}). Finally, in order to generate the switching pulses of the switches i_{ref} is sent to the current controller block.

The list of used circuit elements is presented in Table 9. Figure 16a illustrates the 9-level output voltage waveform of the improved topology. Based on this figure, the peak value of output voltage waveform is 400 V which verifies the voltage boosting capability of inverter. Also, Figure 16a shows the sinusoidal waveform of injected current to the grid. Figure 16b presents the output voltage waveform along with grid voltage waveform.

Considering this figure, it can be seen that the improved topology can operate in grid-connected condition with a high capability of tracking the reference current (i_{ref}). The peak value of injected current to the grid is approximately 5A.

The voltage of capacitors C_1 and C_2 and passing current of these capacitors are illustrated in Figures 17a and 17b respec-

tively. Regarding this figure, self- voltage balancing feature is validated. Considering Figure 17, it can be seen that, both capacitors C_1 and C_2 is charged to half value of input dc source or 100 V. Based on Figure 17, the peak value of passing current of the capacitors is approximately 6.5 A. In conventional SC-based inverters, the spike charging current of the capacitors could not be reduced and the conventional topologies need to use high current power switches. As mentioned before, in the improved topology the capacitors charging current spike is reduced.

The peak current of capacitors C_1 and C_2 in absence of Inductance L_1, is shown in Figure 18. In Figure 18a,b, charging currents of C_1 and C_2 in absence of inductance L_1 is shown, regarding this figure, the peak charging current of capacitors, reaches 20 A which is four times of the grid peak current ($20/5 = 4$). This big current spike will definitely decrease the life span of the capacitors and will increase the losses dramatically. So, the importance of peak current limiting inductance presence is clear, which decreases the peak current of capacitor charging more than three times.

Based on the grid-connected case study, the improved inverter can support both active and reactive power flow controls. Figures 19a–19c illustrates that the improved inverter can inject current to the grid under different conditions of power factors such as leading, lagging and unity power factors respectively.

The voltage stress and passing current of utilized power switches S_1, S_2, S_3, S_4, S_6, S_7, S_8 and S_9 are illustrated in Figures 20a–20h, respectively. Considering these figures, it could be validated that the voltage stress of power switches S_1, S_2, S_3, S_4, S_6, S_7, S_8 and S_9 are equal to V_{DC}, V_{DC}, V_{DC}, $1.5V_{DC}$, $2V_{DC}$, $2V_{DC}$, $2V_{DC}$, and $2V_{DC}$, respectively.

In order to further investigate the performance of the improved 9-level grid-tied inverter and its applied control system, the current injected into the grid and the grid voltage at different values of the injected power to the grid have been measured and the relevant results are shown in Figure 21. Regarding Figures 21a and 12b, the injected current to the grid by the improved inverter is 155 and 233 W, respectively.

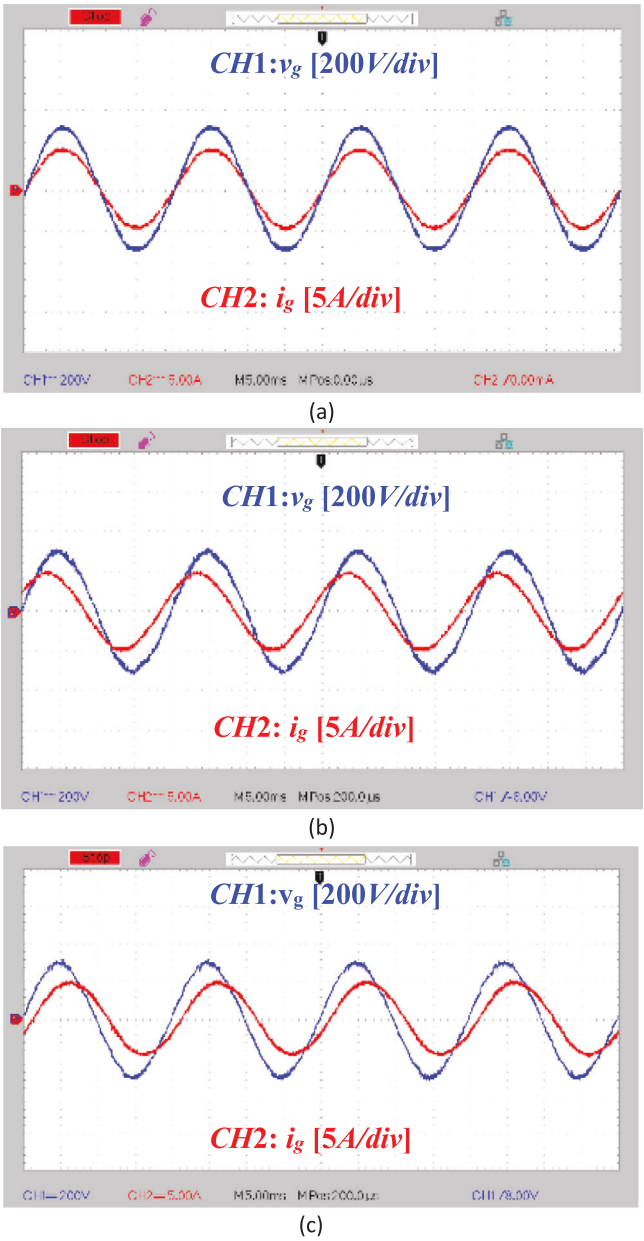


FIGURE 19 The grid voltage (200 V/div) and injected current to the grid (5 A/div) under different conditions of PF: (a) Leading PF (b) lagging PF and (c) unity PF

9 | CONCLUSION

In this study, an improved topology of switched capacitor multilevel inverter has been presented. This structure has some advantages compared with recently provided topologies such as; voltage boosting ability, extendable input voltage, reduction of capacitor charging spike current and reactive power supporting. The improved inverter uses only one dc source at the input.

In this topology, in order to produce a 9-level output voltage waveform with only nine power switches the series-parallel conversion of power switches and the redundant switching states has been applied. The modified inverter can provide voltage boosting feature with the gain factor of 2. Also, it can limit the capacitor charging current spike using a unit which consists of one diode and one inductor in parallel connection. So, the overall efficiency of the inverter and life span of the capacitors are increased. In addition, the power losses and overall efficiency of the improved inverter have been performed.

In order to highlight the advantages of the improved inverter, a comparison with several most recently proposed 9-level inverters has been performed and the comparison outcome verifies the advantages of the proposed topology over previously proposed topologies.

In order to further investigate the performance of the improved 9-level grid-tied inverter and its applied control system, the current injected into the grid and the grid voltage at different values of the injected power to the grid have been measured and the relevant results have been provided.

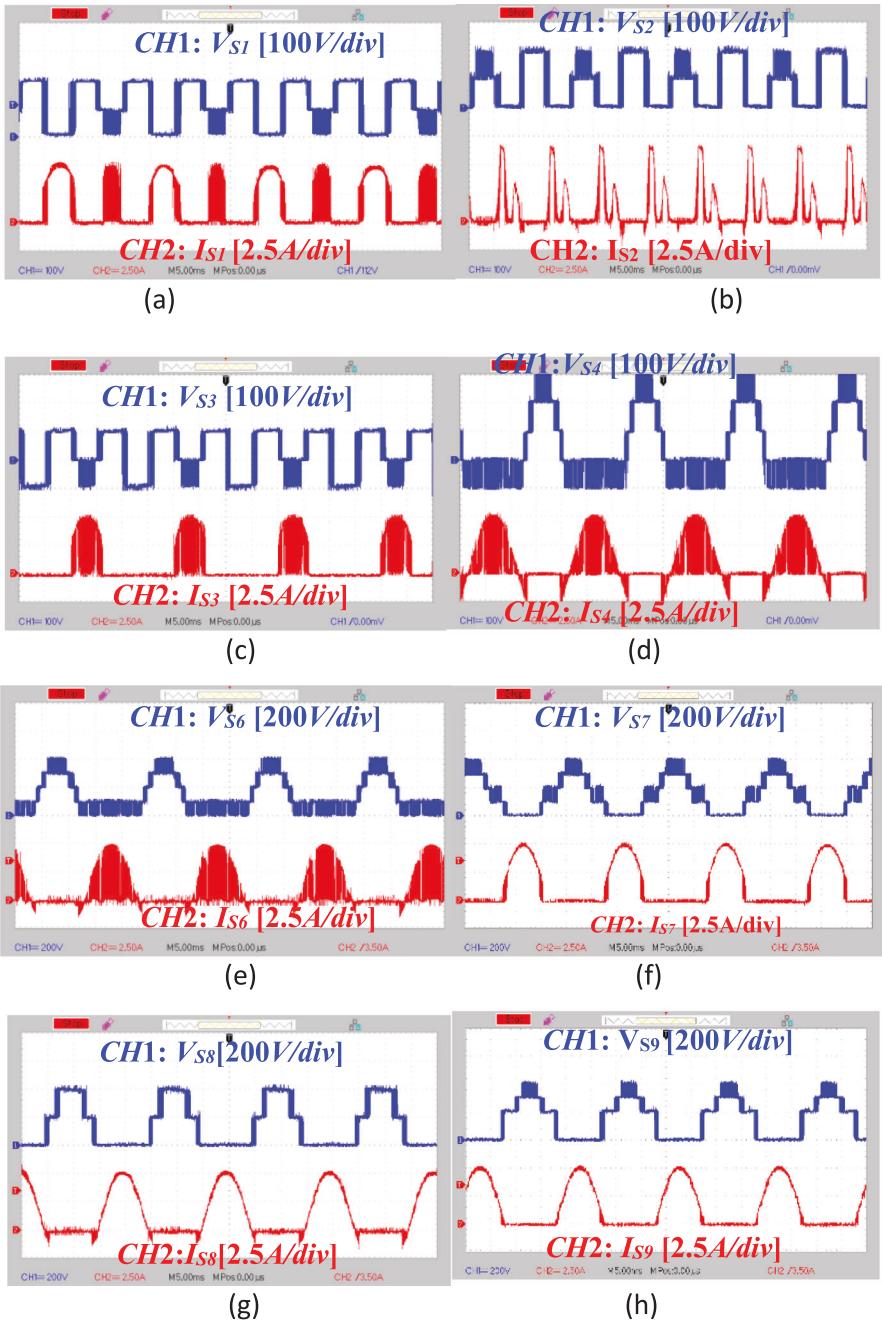
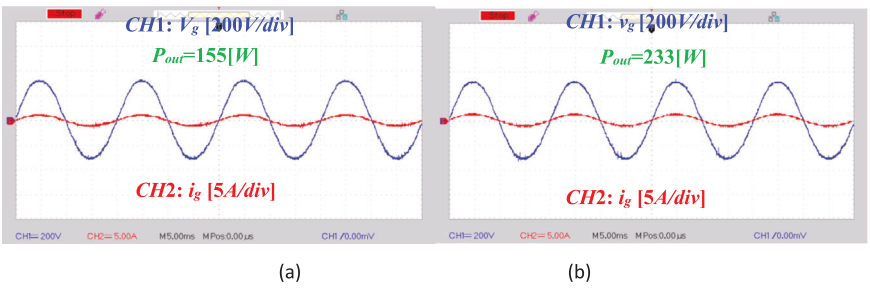


FIGURE 20 The voltage and current stress of power switches. (a) V_{S1} (100 V/div) and I_{S1} (2.5 A/div), (b) V_{S2} (100 V/div) and I_{S2} (2.5 A/div), (c) V_{S3} (100 V/div) and I_{S3} (2.5 A/div), (d) V_{S4} (100 V/div) and I_{S4} (2.5 A/div), (e) V_{S6} (200 V/div) and I_{S6} (2.5 A/div), (f) V_{S7} (200 V/div) and I_{S7} (2.5 A/div), (g) V_{S8} (200 V/div) and I_{S8} (2.5 A/div), (h) V_{S9} (200 V/div) and I_{S9} (2.5 A/div)

FIGURE 21 The experimental results of grid voltage (200 V/div) and injected grid current (5 A/div) at different values of the injected grid power: (a) At 155 W, (b) at 233 W



Finally, in order to verify the accurate performance of the improved switched capacitor inverter, and also to verify the simulation results, a prototype of the proposed inverter is built and a set of experimental results for grid-connected condition of the improved topology has been provided.

AUTHOR CONTRIBUTIONS

N.V.K.: Conceptualization; Project administration; Supervision; Validation; Writing – review and editing. M.G.M.: Conceptualization; Writing – original draft; Writing – review and editing. Y.N.: Writing – review and editing. O.H.: Supervision. S.H.H.: Supervision. A.M.-S.: Supervision

CONFLICT OF INTEREST

The authors do not have a conflict of interest.

DATA AVAILABILITY STATEMENT

Data available on request due to privacy/ethical restrictions.

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