REALISING SiC MOSFET SWITCHING SPEED CONTROL
BASED ON A NOVEL SERIES VARIABLE-RESISTANCE GATE DRIVER

Shuren Wang1, Richard Pollock2, Neville McNeil3, Derrick Holliday3, Khaled Ahmed1, Barry Williams1

1University of Strathclyde, Glasgow, Scotland, U.K.
2Technolec Ltd., Rutland, England, U.K.
3University of Newcastle, Newcastle, England, U.K.
*shuren.wang@strath.ac.uk

Keywords: EMI CONTROL, GATE DRIVER, SiC MOSFETS, SWITCHING SPEED

Abstract

Silicon carbide (SiC) MOSFETs feature salient characteristics such as higher breakdown voltage, lower losses and higher switching speed when compared to Silicon (Si) MOSFETs. However, due to the high switching speed and parasitic parameters, the SiC MOSFET turn-on and turn-off dynamics lead to overvoltage, overcurrent and electromagnetic interference (EMI) issues. This paper proposes a SiC MOSFET switching speed control concept based on a gate driver that features dynamically changeable gate resistance allowing microcontroller-based adjustment of the SiC MOSFET switching speed. This function therefore enables a closed-loop SiC MOSFET switching speed control, which is suited to device safety and EMI control. The configuration and operation of the proposed concept are presented. Both simulation and experimental results are provided to verify the proposed circuit.

1 Introduction

Silicon carbide (SiC) MOSFETs are attractive power semiconductor devices for improving the performance of power electronic converters. However, due to the high switching speed and parasitic parameters, SiC MOSFET turn-on and turn-off behaviours are generally more severe than those of Si-based devices [1]. A conventional gate driver achieves MOSFET gate voltage shifting by manipulating two high-speed switches to charge and discharge the gate terminal, while the switching speed can be determined by the gate resistors. Typical switching behaviour is illustrated in Fig. 1, where the gate-source voltage \( V_{GS} \) increases/decreases at a rate determined by the pre-set gate resistors. The drain current \( I_D \) and drain-source voltage \( V_{DS} \) vary depending on the switching process. Low gate resistances will lead to high switching speed and thereby high \( |dV_{DS}/dt| \) which deteriorate switching behaviour as a result of increased overshoots and oscillations. Also, electromagnetic interference (EMI) becomes more severe. Gate drivers play an important role for wider application of SiC MOSFETs, given their ability to manipulate the gate voltage characteristics and thereby the device switching speed [2]. In general, the reduced gate charging and discharging rates resulting from higher gate resistance can slow down the switching speed and achieve low \( |dV_{DS}/dt| \). However, this is at the expense of increased switching losses, and therefore a trade-off among high switching speed, high switching losses, and design complexity exists.

In addition to generating the gate voltage levels required to switch a device, they are also expected to mitigate overcurrent/overvoltage and reduce EMI. Varying the gate terminal resistance and gate terminal voltage are two mainstream ways of controlling switching speed [3]. Shaped gate voltage profiles are proven to be effective in reducing EMI [4]. The method of varying gate resistance can be implemented by a fine-resolution gate driver based on Field Programmable Gate Arrays (FPGAs) [5]. However, these complex circuits are not always suited to commercial applications. In an effort to combine gate drivers to directly control the switch gate, ABB proposed a novel gate driver [6], where variable driving voltage and variable gate resistance are used to suppress overcurrent and overvoltage of SiC

![Illustrative gate driver turn-on and turn-off behaviour.](Image)

Fig. 1 Illustrative gate driver turn-on and turn-off behaviour.
MOSFETs. Another hybrid gate driver is proposed based on parallel-connected gate driver switches, and the control is implemented using high-speed complex programmable logic devices (CPLDs) [7].

Although various gate driver circuits have been proposed, the variable resistance method is the simplest one, as no extra isolated voltage source is required and gate resistances can be changed in different ways [8], [9]. The circuit proposed in [8] uses a parallel switch to bypass/insert an extra resistor for the turn-on/off process, and the control logics are determined by the instantaneous \( V_{on} \) level. However, the high-speed feedback mechanism might be affected by electrical noise in certain operating scenarios. A variable resistance gate driver consisting of three parallel-connected high-speed switch pairs is proposed in [9], where an FPGA varies gate voltage and resistance during switching transitions. Nevertheless, the design complexity increases with the three stages, with associated higher cost and larger layout area.

This paper proposes a SiC MOSFET switching speed control concept based on a novel series-connected gate driver. The proposed concept has the following features:
- The SiC MOSFET switching behaviour can be actively controlled by this switching approach with varied gate resistance achieved by the series-connected stages.
- An auxiliary stage enables low resistance gate charging/discharging, thereby accelerating the SiC MOSFET charging/discharging process (high gate currents).
- The overcurrent and overvoltage (high \( di/dt \) and \( dv_{GS}/dt \)) issues during turn on and off respectively can be mitigated by the high resistance based driving operation process;
- The dual-stage gate driver structure avoids the need for a complex digital controller.
- The proposed concept allows the host microcontroller to adjust the SiC MOSFET switching behaviour based on various factors (such as closed-loop EMI measurement), and enables smooth variation at different switching speed levels.

The paper is organised as follows: Section 2 describes the architecture and operation of the proposed gate driver. SPICE-based simulation, based on the manufacturer’s SiC MOSFET model, is presented in Section 3. Section 4 presents experimental results to verify the proposed gate driver. Section 5 discusses potential applications of the configuration, and Section 6 concludes the paper.

2. Gate Driver Structure and Operation

2.1 Gate Driver Circuit

As shown in Fig. 2, the proposed gate driver main circuit consists of two main stages (I and II), based on high-speed low-voltage switches and gate resistors (\( R_{on}, R_{\text{on}}' \), \( R_{off} \), and \( R_{\text{off}}' \)). The upper and lower switches within each stage operate in a complementary mode. The negative voltage (assuming \( V_i < V_o \)) is desired for most current SiC devices to meet operational requirements and accelerate turn-off speed [6].

Stage-I (controlled by \( S_{on} \) and \( S_{off} \)) is responsible for maintaining on/off status while Stage-II (controlled by \( S_{on}’ \) and \( S_{off}’ \)) is used to boost the switching speed. Also, in order to realise the switching speed variation, the resistances are related so that: \( R_{on} > R_{on}' \), and \( R_{off} > R_{off}' \). Therefore, through the manipulation of Stage-II, device switching speed can be changed.

From the device ratings perspective, the switches in Stage-I can have lower current rating than those in Stage-II, as the relatively higher charging/discharging resistances (\( R_{on} + R_{\text{on}}' \) and \( R_{off} + R_{\text{off}}' \)) can limit the maximum current. Therefore, the overall device cost is not increased significantly. Importantly, Stage-I can be physically located relatively far away from its SiC MOSFET, which may be advantageous during hardware PCB layout design. Necessary

![Fig. 2 The proposed series gate driver main circuit.](image)

![Fig. 3 Illustrative gate driver turn-on and turn-off behaviour based on the proposed series gate driver.](image)
discharging resistance is $R_{\text{off}}' + R_{\text{off}}$ and the SiC MOSFET gate terminal is discharged to $V$ by Stage-I. The increased resistance reduces switching speed, and this gate driver state is maintained throughout the SiC MOSFET’s off-state. As with State $ii$, the timing of switching from State $iii$ to State $iv$ (i.e. the duration $T_{\text{III}}$ of State $iii$) can be set using the low-pass-filter time delay method [10].

3 Simulation Results

This section compares simulated 400 V, 10 A double-pulse tests of a Wolfspeed C3M0075120K SiC MOSFET using

![Diagrams showing gate driver configurations and their impacts on turn-on and turn-off behaviors.](image-url)

**Fig. 5** Simulated SiC MOSFET turn-on behaviour with different gate driver configurations.

![Diagrams showing simulated gate drivers and their impacts on turn-on and turn-off behaviors.](image-url)

**Fig. 6** Simulated SiC MOSFET turn-off behaviour with different gate driver configurations.

![Diagram illustrating the series variable-resistance gate driver circuit.](image-url)

**Fig. 4** Main circuit states. (a) State $i$, (b) State $ii$ (c) State $iii$, (d) State $iv$.

Isolation (not shown) can allow a negative turn-off voltage as required by the MOSFET. This dual-stage gate driver structure enables dynamic SiC MOSFET gate resistance variation during the switching process, as explained in Section 2.2.

2.2 Gate Driver Operation

The series variable-resistance gate driver can be controlled, as illustrated in Fig. 3, to vary the SiC MOSFET switching speed. Also, gate driver turn-on and turn-off behaviours regarding different states ($i$ – $iv$) are given. Besides, the corresponding main circuit states, shown in Fig. 4, are as follows:

- **State $i$**: The upper switches of Stages I and II are closed. Gate charging resistance is dominated by $R_{\text{on}}'$ and the SiC MOSFET gate terminal is charged quickly. Thus, unlike the conventional gate driver turn-on process, the proposed gate driver has a high-speed initial turn-on characteristic which is realised using the boost switch $S_{\text{on}}'$ of Stage-II.

- **State $ii$**: The upper switch of Stage-II is opened. Gate charging resistance is $R_{\text{on}}' + R_{\text{on}}$, and the SiC MOSFET gate terminal is charged (by Stage-I) to $V_c$. The increased gate resistance reduces switching speed and this gate driver state is maintained throughout the SiC MOSFET’s on-state. It should be noted that the timing of switching from State $i$ to State $ii$ (i.e. the duration $T_i$ of State $i$) can be set using the low-pass-filter based time delay signal generation method investigated in [10].

- **State $iii$**: The lower switches of both Stages I and II are turned on. Gate discharging resistance is $R_{\text{off}}' + R_{\text{off}}$ and the SiC MOSFET gate terminal is discharged quickly. Unlike the conventional gate driver turn-off process, the proposed gate driver enables high-speed initial turn-off, which is realised using the boost switch $S_{\text{off}}'$ of Stage-II.

- **State $iv$**: The lower switch of Stage-II is opened. Gate
three different gate driving methods: a conventional gate driver with low gate resistance, a conventional gate driver with high gate resistance, and the proposed series variable-resistance gate driver. The device model used in the LTspice® simulation was sourced officially from the manufacturer. The durations of States $i$ and $iii$, namely $T_i$ and $T_{iii}$, are set to be 20 ns.

The simulation results are shown in Fig. 5, where the turn-on pulse is applied at 30 μs. The conventional gate driver with a 20 Ω gate resistor enables fast gate-source terminal voltage $V_{GS}$ charging throughout the turn-on process. It can be observed that the drain current $I_D$ has the largest overshoot (approximately 16 A) due to the fast switching action, and $|dV_{DS}/dt|$ and $|dI_S/dt|$ are the highest of the three gate driver approaches. The conventional gate driver with high gate resistance shows the slowest $V_{GS}$ rise. Due to the slow switching process, $I_D$ shows less overshoot (approximately 12.5 A) but a delay of approximately 400 ns following application of the gate pulse. The fall in drain-source voltage $V_{DS}$ also exhibits this 400 ns delay. The proposed gate driver shows the fast initial gate terminal charging process (State $i$) followed by the high-resistance mode (State $ii$), where gate-source voltage rises slowly to ensure a smooth turn-on process. Drain current $I_D$ has a low overshoot as conventional gate driver (approximately 12.5 A) and $|dV_{DS}/dt|$ and $|dI_S/dt|$ are similar to those with a high resistance conventional gate driver. Importantly, turn-on delay is also less than that for the conventional high resistance gate driver, due to the fast initial charging process, and oscillations are also reduced.

Simulation results of the turn-off behaviour with different gate driver configurations are shown in Fig. 6, where the turn-off pulse is applied at 25 μs. The conventional gate driver with a 10 Ω gate resistance enables fast gate-source voltage $V_{GS}$ discharging throughout the turn-off process. The drain-source voltage $V_{DS}$ has the largest overshoot (approximately 550 V) due to the fast switching action, and the rates of change of $V_{DS}$ and $I_D$ are the highest of the three approaches compared. The conventional gate driver with high gate resistance shows a slow turn-off process with slow $V_{GS}$ fall. Due to the slow switching process, $V_{DS}$ shows reduced overshoot (approximately 490 V), but exhibits approximately a 600 ns delay after the pulse signal is applied. The drain current $I_D$ reduces, also with this 600 ns delay. The proposed series variable-resistance gate driver shows a fast initial gate terminal discharging process (State $iii$), followed by the high-resistance mode (State $iv$), where the gate-source voltage reduces slowly to ensure slowdown of the turn-off process. It can be observed that the drain-source voltage $V_{DS}$ has the lowest overshoot (approximately 450 V), and that $|dV_{DS}/dt|$ and $|dI_S/dt|$ are similar to those of the high resistance conventional gate driver approach. Importantly, the turn-off delay is much less than in the case of the conventional high resistance approach due to the fast initial discharge process, and oscillations are also reduced.

### 4 Experimental Results

The proposed series variable-resistance gate driver concept was implemented and integrated into a double-pulse test circuit and experimentally evaluated, as shown in Fig. 7. The device under test was a Wolfspeed C3M0075120K SiC MOSFET. Due to space constraints, only the results for device turn-on are presented.

Turn-on performance of the conventional and series variable-resistance gate drivers is shown in Fig. 8. For the conventional gate driver case, 10 Ω gate resistance leads to a high turn-on speed with $I_D$ having an overshoot of approximately 17 A, whilst the increased gate driver resistances reduce the switching speed and, correspondingly, overshoot (to approximately 13 A in the 30 Ω gate resistance case). To facilitate simple comparison, the resistance configuration of the proposed series gate driver is $R_{on} = R_{off} = 10$ Ω, and $R_{on}$ and $R_{off}$ range between 10 Ω and 30 Ω. Fig. 8 shows the case with $R_{on} = R_{off} = 30$ Ω, and the duration $T_i$ of State $i$ varied from 12 ns to 18 ns using a low pass filter based delay circuit. A long duration $T_i$ (18 ns) leads to fast turn-on with $I_D$ reaching
REALISING SiC MOSFET SWITCHING SPEED CONTROL BASED ON A NOVEL SERIES VARIABLE-RESISTANCE GATE DRIVER

7 Acknowledgements

This research was supported by the UK Engineering and Physical Sciences Research Council (EPSRC) under grant EP/R029504/1 (‘Quieting ultra-low-loss SiC & GaN waveforms”).

8 References


Fig. 9 Relationship between turn-on losses and $i_D$ peak value.

Fig. 10 Envisaged application of the proposed series gate driver.

a peak value of approximately 14.5 A, whereas a short $T_i$ duration (12 ns) slows down the turn-on process with $i_D$ reaching a peak value of 12.5 A.

The switching loss variation caused by the dynamic manipulation of gate resistance is considered. The relationships between turn-on losses and $i_D$ peak value of the conventional (gate resistance ranging between 10 $\Omega$ and 30 $\Omega$) and the series variable-resistance gate driver ($R_{inv} = 10$ $\Omega$ and $R_{inv}$ ranging from 10 to 30 $\Omega$ and $T_i$ ranging from 12 ns to 18 ns) cases are tested and shown in Fig. 9. It can be seen that the switching loss performance of the proposed series gate driver follows the same trend as that of the conventional gate driver, with the limited number of outlying data points indicating additional overshoots due to resonance effects.

In summary, the results show the effectiveness of the proposed gate driver on device oscillation suppression.

5 Suggested Application of the Gate Driver

The proposed series variable-resistance gate driver provides a straightforward way of implementing different gate resistances for SiC MOSFETs given the addition and subtraction of resistive values based on series connection. Also, it enables microcontroller-based switching speed control with low-speed feedback of EMI detection.

6 Conclusion

This paper has proposed a novel series variable-resistance gate driver concept to enable smooth switching speed control of SiC MOSFETs. Circuit configuration and operation were detailed and both simulation and experimentation were provided to verify the effectiveness of the proposed approach.