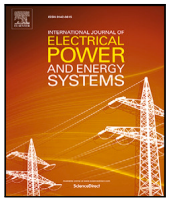
Electrical Power and Energy Systems 146 (2023) 108723

Contents lists available at ScienceDirect

International Journal of Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes



Three-phase inverter based on isolated SEPIC/CUK converters for large-scale PV applications

Saud Alotaibi [a,b,*], Ahmed Darwish [a], Barry W. Williams [c]

[a] School of Engineering, Lancaster University, Lancaster, United Kingdom
[b] Electrical Engineering Department, College of Engineering, Shaqra University, Riyadh, Saudi Arabia
[c] Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom

ARTICLE INFO

Keywords:
Modular multilevel inverter
Module integrated inverters
Large PV plant

ABSTRACT

Modular multilevel inverters (MMIs) for medium-voltage (MV) grid-connected systems are gaining attention in solar photovoltaic power (PV) applications. Existing MV power electronic converters require large passive components, huge line-frequency step-up transformers, and additional conversion power stages for maximum power extraction. This paper presents a new three-phase modular inverter (TPMI) based on a novel dual-isolated SEPIC/CUK (DISC) converter for large-scale PV (LSPV) plants. The proposed TPMI is synthesized from series DISC submodules (SMs) to reduce the size and improve the performance of the energy conversion system. Employing high-frequency transformers (HFTs) into the SMs can provide the required galvanic isolation and voltage boosting in addition to reducing the size compared with line-frequency step-up transformers. The chosen DISC converter reduces the required filtering capacitances thanks to its operation as a current-source converter, resulting in improved lifetime, scalability, and resilience of the inverter. The state-space model of the DISC is presented and its performance in PV grid-tied systems using simulations is evaluated. To validate the mathematical analyses and computer simulations, a small-scale experimental prototype is built and tested.

1. Introduction

Global warming is the primary driver of worldwide interest in renewable energy sources (RESs) for large-scale electricity generation. Solar photovoltaic (PV) has emerged as one of the most promising renewable forms of bulk power generation as a result of developments in solar cell fabrication and converter technology [1]. Therefore, new markets are emerging for PV energy and more gigawatts (GWs) power plants are being installed [2]. In this context, large-scale PV (LSPV) plants with a capacity of megawatts range can become key contributors for assuring high-energy conversion generated from RESs to loads and/or grids [3]. Globally, LSPV capacity is growing remarkably with plants over 80 GW are already in operation [4].

The ambitious plans to expand further LSPV power plants require more efficient power converters. However, the progress of LSPV power plants is hindered by the lack of suitable high-power converter topologies for the integration of LSPV systems to the medium/high voltage grids [5]. A conventional LSPV power plant is mainly composed of PV modules that are connected in series/parallel combinations to form PV arrays and strings. These arrays and strings are then connected to dc–dc converters that ensure maximum power point tracking (MPPT) operation and boost the dc voltage. The dc–dc converters' outputs are connected to a common DC bus operating at a voltage range of 415–690 V. The common dc bus is then connected to the utility grid via a step-up transformer by a central dc–ac inverter [6]. Fig. 1 shows the common configuration of present LSPV plants to harvest the energy from the PV modules.

Although this configuration is common for PV grid-connected systems, it does not yet meet all technical and cost-effective requirements for PV systems [7]. This configuration requires the use of bulky and heavy line frequency transformer(LFT), large line filters, and boost converters, which considerably increases the weight and volume of the energy conversion system, its operating costs, and losses [7]. Employing this single central inverter system to supply high power to the main grid is challenging due to the power rating restrictions of existing power inverters and the semiconductor [8]. In additional, the vast number of PV modules connected in series in a PV array is controlled by a common maximum power point tracking (MPPT) algorithm, which can limit the system's overall power output of the string [9].

The lack of these concerns in modular multilevel inverters (MMIs) has recently attracted the researchers' interest as a promising solution due to their competency in addressing the aforementioned issues and improving the performance of LSPV integration into the grid [10].

* Corresponding author at: School of Engineering, Lancaster University, Lancaster, United Kingdom.
E-mail address: s.alotaibi@lancaster.ac.uk (S. Alotaibi).

https://doi.org/10.1016/j.ijepes.2022.108723
Received 5 February 2022; Received in revised form 21 September 2022; Accepted 13 October 2022
Available online 5 November 2022

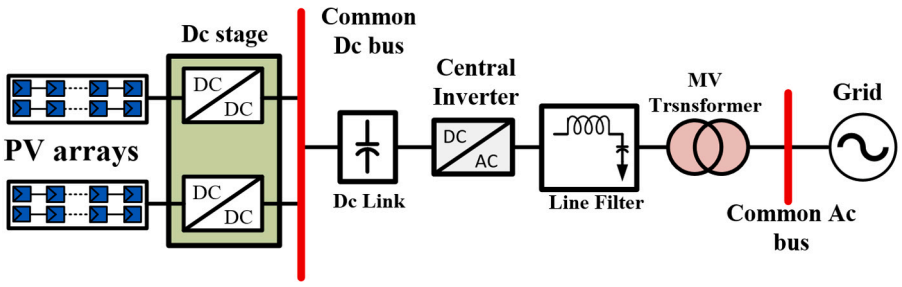


Fig. 1. Conventional large-scale PV plant conversion system.

Early multilevel converters relied on common dc sources with either a single dc-link capacitor or a series of capacitors connected on the dc side. In this group of converters, the most common topologies are neutral point clamped (NPC) and flying capacitor (FC) converters [11]. However, both topologies require a common dc bus, which decreases their modularity and efficiency of MPPT controller. Moreover, NPC uses a high number of clamping diodes to generate more voltage levels, whereas FC suffers from unbalanced capacitor difficulties, therefore they are unsuitable for the PV/MV applications. Thus, their primary application is limited to the low and medium voltage range [12].

In this aspect, several MMI topologies have been introduced in LSPV applications that shift towards a more distributed structure, such as cascaded H-bridge (CHB) converter and modular multilevel converter (MMC) [13]. These topologies use a submodule (SM) circuit in which the power is transferred from the PV side to the inverter ac terminals. They have the merits of modularity, independent MPPT operations, sustainability for managing high voltages ranging from several hundred kV to MV, high fault tolerance, and the absence of capacitor balancing issues [14]. Despite their widespread use in high-power applications, these topologies have several challenges in LSPV applications. The use of CHB inverters for PV integration has been presented in [15–17]. In [15], CHB star and delta configurations are evaluated from the perspective of PV integration where the focus is on the unbalanced power generation between the three phases due to partial shading conditions. The work in [16] examines the capabilities of the CHB and discusses various techniques of zero-sequence calculation. In [17], the authors study the shortcomings of current zero sequence methods for CHB under severe power unbalance and present a simpler optimal zero sequence approach. In these CHB-related configurations, the PV array is connected to the dc-links of individual SMs by using dc–dc converters known as two-stage inverters. On the other hand, the leakage current phenomenon is the key concern in CHB MMI structures in which their SMs are connected directly to PV modules [18]. In [19,20], the authors built and fitted passive filters at the output of each CHB SM to reduce the leakage current. However, these filters decrease the CHB's output voltage. Moreover, as the number of SMs increases, the cost, volume, and weight of the CHB grow considerably due to the extra of filter circuits. In addition, they need a complicated design procedure and cannot be applicable at high power levels [18].

A group of MMCs for PV systems connected to either one or several dc-links is described in [21,22]. However, these MMCs have some limitations when they are employed in PV systems. The direct connection of the PV array to the common dc link presents a challenge during partial shading because the MPPT distribution becomes difficult [23]. If the input side of the MMC is connected to several dc-links, the input dc voltage must be higher than the peak output ac voltage. As PV string voltages are frequently at or below 1.5 kV, an additional boost converter step is necessary to produce MVAC output, which increases the expense of the system and decreases its efficiency [24]. Motivated by the previous modular inverter structures, new MMIs have been developed in which dc/dc converters are used as SMs to increase their applicability for MV PV systems. These MMI structures are derived from a topological combination between the CHB and MMC topologies [25]. They are distinguished by their distributed MPPT control, galvanic isolation, low total harmonic distortion (THD), low voltage stress, and small overall system volume and weight [26]. These inverters are based on high-frequency transformers (HFTs), which have emerged as a viable alternative to LFTs due to their compact size and higher efficiency [27]. This contributes to SM structures meeting PV system safety requirements [28].

The fly-back converter lends itself well to the design of modular inverter SMs because of its simplicity, low cost, and ability to provide both isolation and unidirectional power flow when connected to a PV-tied grid [29]. In [30], a three-phase modular fly-back topology inverter is presented. The proposed inverter topology consists of parallel SMs based on isolated fly-back converters with an adequate level of power. These SMs are connected in parallel on the dc input side and differentially connected on the grid side. The performance of the fly-back converter is improved by the HFTs' voltage boosting and galvanic isolation capabilities. By connecting many fly-back SMs in parallel, the current can be distributed to increase the apparent switching frequency and decrease the size of HFTs. Despite the modular nature of the proposed structure, the power capability does not increase proportionally with the number of SMs. To increase the power output of this system, additional SMs and PV modules must be connected in parallel with the existing ones. According to its results, it is more suitable for low-power PV applications. Furthermore, the fly back converter has a large leakage inductance and discontinuous current behaviour at the input and output sides, limiting conversion efficiency. In [31] study, four different SM topologies of C5 (Cuk), F5, G5 (SEPIC), and P5 converters are investigated. These SM converters are used in an MMI structure that provides galvanic isolation via HFTs operating at a high switching frequency to allow for a significant reduction in the overall system footprint [32]. By inspecting the performance of these SMs topologies, both CUK and SEPIC converter topologies can provide higher efficiency and accomplish system-wide objectives [33].

In this paper, a three-phase modular inverter (TPMI) based on the novel dual-isolated SEPIC/CUK (DISC) converter is presented for the LSPV grid integration as shown in Fig. 2. The dual isolated SEPIC-Cuk (DISC) converter can generate two symmetrical dc voltages with a neural point to give balanced dual output voltages without further voltage balance control [34]. The total number of passive components is reduced because the input side inductor for both the Cuk and SEPIC converters can be shared. The employed DISC operates using identical gate signal for the output switches. Therefore, their output voltages are comparable in amplitude but different in polarity [35].

This emerging inverter offers several interesting features that promote it as a modern generation power inverter. These features can be summarized as follow:

i By adding more SMs, the output voltage and current can be scaled up and delivered into the grid.
ii An HFT can be embedded in the SM to achieve galvanic isolation, effectively addressing leakage current in PV inverters, adding more flexibility to step up or down the input voltage.

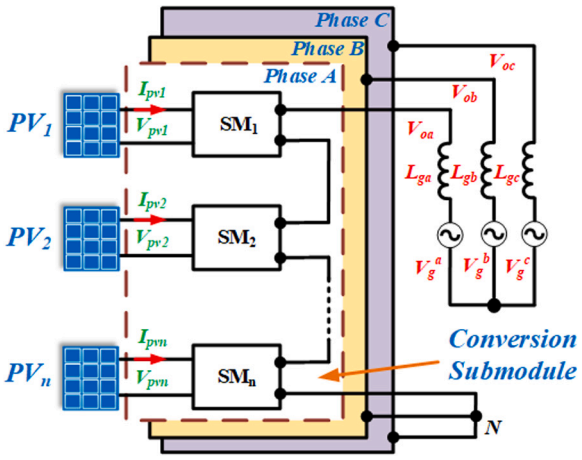


Fig. 2. Proposed new TPMI employing the DISC converter for SMs conversion.

iii Providing Continuous current flows through the input and output ports, which helps the MPPT controller harvest the maximum power from the PV arrays.

iv With its distributed MPPT operation, it is possible to yield the maximum possible energy under both uniform and non-uniform partial shading environments due to the independent connection of each PV module to its own SM.

v Due to the continuous current nature, it is possible to filter the PV system using a small film capacitor rather than a large electrolytic capacitor, which can result in a longer inverter life.

vi Possessing fault-blocking capability in the case of dc or ac power failure. SMs can be forwarded or replaced if they fail for any reason.

The rest of the paper is organized as follows: Section 2 describes the SM topology, the basic operation, and the modulation strategy. Section 3 discusses the details of steady-state analysis and the paper's average model contribution. Section 4 explains parameters design selection. Section 5 describes the developed control strategy for the inverter. Section 6 simulation results of the inverter system using MATLAB/Simulink. Section 7 illustrates system validations with the experimental prototype and TMS32028335 DSP controller.

2. SM unit description and operation

2.1. SM unit

The novel DISC converter will be used as the SM of the proposed TPMI where each SM will be connected to a PV module. As shown in Fig. 3, the DISC is formed as a combined SEPIC/Cuk converter with dual-winding isolation.

The combination SEPIC/Cuk converter structure is possible because both converters share one common front structure and two output structures for dual output voltages. This design can employ a compact HFT to obtain galvanic isolation, which is essential to handle effectively leakage current issues in PV inverters. In the steady state, the voltage gain ratio of the SM is the sum of the Cuk and SEPIC converters' output voltages. As both of these converters are buck-boost converters, the voltage gain ratio of the DISC SM is:

$$\frac{V_O}{V_{in}} = \frac{2ND}{1-D} \tag{1}$$

Where D is the steady state duty-cycle ratio and N is the HTF's turns ratio. The output voltage of the SM is doubled when compared with the conventional buck-boost converters. In addition, the HFT itself can contribute to increase the voltage gain by increasing N if necessary.

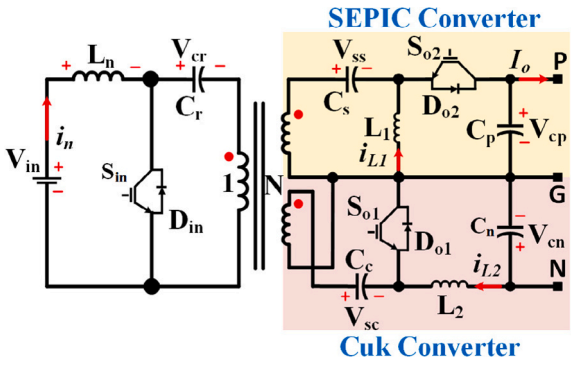


Fig. 3. SM unit of the TPMI inverter.

In this topology, the output switches S_{o1} and S_{o2} are operating in a complementary manner to the input side switch S_{in}. In addition, these switches should be equipped with antiparallel diodes to chop the current when the output current is negative. Consequently, their output voltages level have the same magnitude and opposite polarity. The upper structure (SEPIC) has a positive output voltage while the lower structure has a negative output voltage.

2.2. Basic of operation

The operation of the DISC SM in continuous conduction mode (CCM) will be discussed in this section. D is the ratio of the switch-on time t_{on} , where S_{in} is ON, to the complete switching period t_s. There are two operational states from the perspective of the SM. The two states of the SM are as follows.

- State 1 ($0 \le t < D\ t_s$)

By turning S_{in} ON and output switches OFF as shown in Fig. 4(a), the input current i_n begins to increase and the primary capacitors C_r starts to discharge. Meanwhile, C_S and C_C are discharged and their energy is released into output side inductors L_1 and L_2. Thus, the currents i_{L1} and i_{L2} will increase together while the output capacitors C_p and C_n are discharging in the output load.

- State 2 ($t_{\text{on}} < t < t_s$)

In contrast to previous state, the output switches S_{o1} and S_{o2} are turned ON together whereas S_{in} is turned OFF, see Fig. 4(b). i_n flows through the primary capacitor C_r, C_S and C_C capacitors. Thus, these capacitors are charging and their voltages increase together. As the output switches begin to conduct, the upper output inductor L_1 releases its energy to charge C_p and supply the load while the lower output inductor L_2 is discharged and its energy is transferred to C_n and the output load. Fig. 5 shows theoretical waveforms for the proposed DISC.

2.3. Modulation strategy

There are two possible connections of the SMs in phase j with the PV modules as shown in Fig. 6. In the first method, separate PV modules are connected with each SM to reduce the current of each PV module. In the second method, the same PV module is connected to the successive SMs to ease the dc connection but at expenses of increased current. The output ac voltage and current from the SMs will be the same in both connections. The output voltages of SM_{n-1} and SM_n in phase j can be expressed as:

$$\begin{aligned} \upsilon_{jn-1}(t) &= \frac{1}{2}V_{jn-1}\sin(\omega t) + V_{dcjn-1} \\ \upsilon_{jn}(t) &= \frac{1}{2}V_{jn}\sin(\omega t + \pi) + V_{dc\ jn} \end{aligned} \tag{2}$$

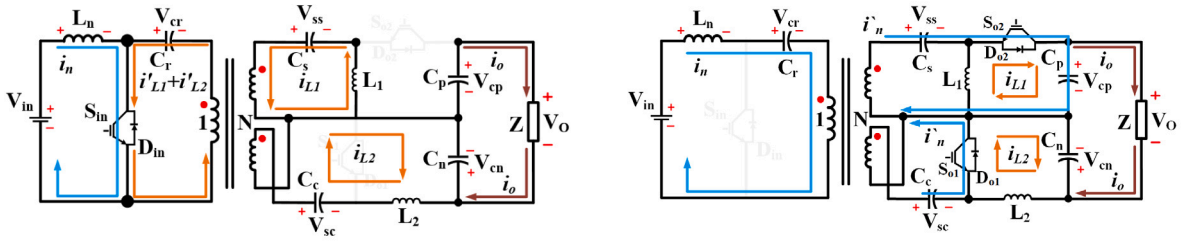


Fig. 4. DISC states.

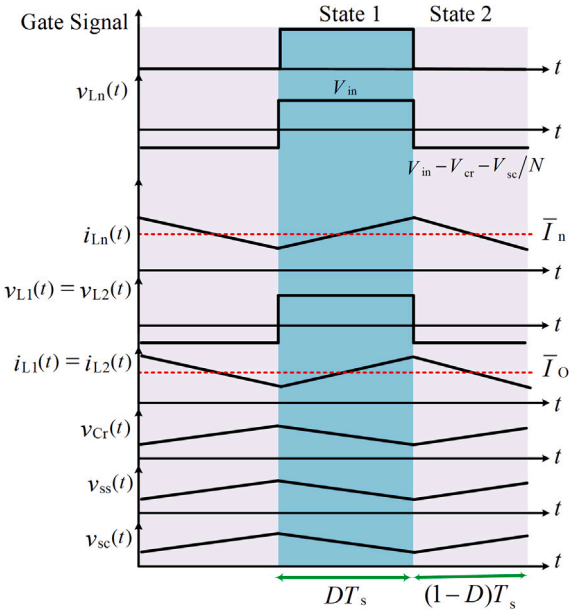


Fig. 5. Theoretical waveforms of proposed DISC.

The duty-cycle ratios to generate these voltages are calculated from:

$$D_{jn-1}(t)=\frac{v_{jn-1}}{v_{jn-1}+2NV_{innn-1}}$$
$$D_{jn}(t)=\frac{v_{jn}}{v_{jn}+2NV_{inn}} \tag{3}$$

If the magnitudes of the ac components and the dc offsets are equal in the two successive SMs, their total output voltage is

$$v_{ojn}(t)=v_{jn-1}(t)-v_{jn}(t)=V_{ojn}\sin(\omega t) \tag{4}$$

In both connections, the SM input currents can be expressed as:

$$i_{injn-1}(t)=2N\frac{D_{jn-1}}{1-D_{jn-1}}i_{gj}$$
$$i_{injn}(t)=-2N\frac{D_{jn}}{1-D_{jn}}i_{gj} \tag{5}$$

However, the total input current from the PV modules to supply the three phases will be doubled in the second method in Fig. 6(b) because every PV module will supply six SMs in this case.

3. State-space analysis of the DISC SM

3.1. Steady-state analysis

Because the DISC is an 8th order converter, the state-space average model is complicated and hence has not been presented in the literature yet. The state-space model is necessary to understand the behaviour of the SM, obtain the transfer function for control design, and use it in the parameters' selection. The state-space model can be represented by the following equations:

$$\dot{x}=Ax+Bu \tag{6}$$

$$y=Cx+Bu \tag{7}$$

Where x is a state variable vector, u is the input vector, while y is the output vector. The state vector is defined as

$$x(t)=\left[i_n(t)v_{cr}(t)v_{ss}(t)v_{sc}(t)i_{L1}(t)i_{L2}(t)v_{cs}(t)v_{cn}(t)\right]$$

Thus, the state-space model can be averaged during t_{on} and t_{off}, where S_{in} is OFF as follows:

1. State 1 ($0 \le t < D\,t_s$)
During *State*1, the differential equations of the states can be deduced from Fig. 4(a) as:

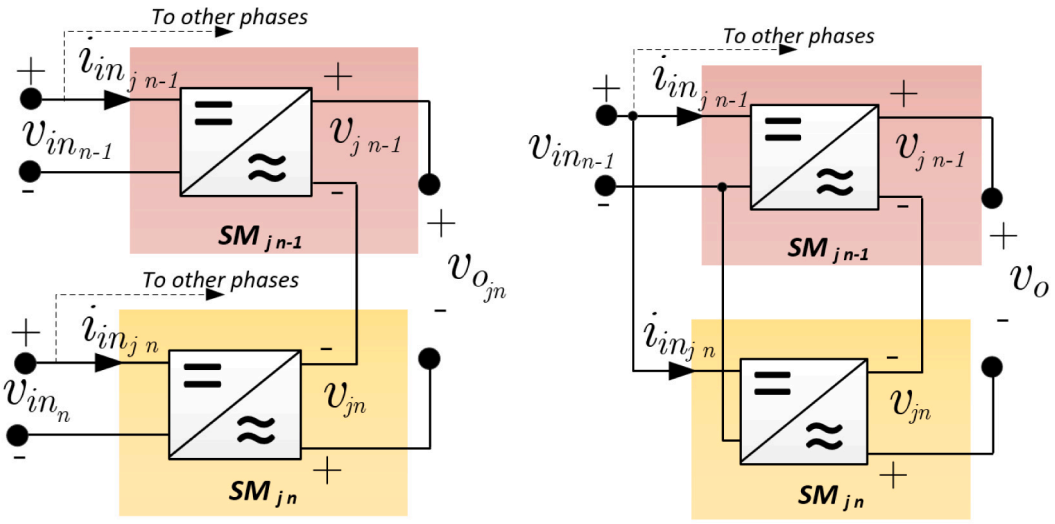
$$\frac{di_n}{dt}=\frac{1}{L_n}V_{in} \tag{8}$$
$$\frac{dv_{cr}}{dt}=-\frac{N}{C_r}\left(i_{L1}+i_{L2}\right) \tag{9}$$
$$\frac{dv_{SS}}{dt}=-\frac{1}{C_S}i_{L1} \tag{10}$$
$$\frac{dv_{SC}}{dt}=-\frac{1}{C_C}i_{L2} \tag{11}$$
$$\frac{di_{L1}}{dt}=\frac{N}{L_1}V_{cr}+\frac{1}{L_1}V_{SS} \tag{12}$$
$$\frac{di_{L2}}{dt}=\frac{N}{L_2}V_{cr}+\frac{1}{L_2}V_{SC}-\frac{1}{L_2}V_{Cn} \tag{13}$$
$$\frac{dv_{cp}}{dt}=-\frac{1}{C_pZ}V_{cp}-\frac{1}{C_pZ}V_{cn} \tag{14}$$
$$\frac{dv_{cn}}{dt}=\frac{1}{C_n}i_{L2}-\frac{1}{C_nZ}V_{cp}-\frac{1}{C_nZ}V_{cn} \tag{15}$$

2. State 2 ($t_{on} < t < t_s$)
The circuit combination of Cuk and SEPIC output sides becomes complicated and therefore the differential equations cannot be solved without some approximations. These approximations are made due to the following observations:

(A) The capacitors' average currents are zero along with the two states over one complete switching cycle (i.e., state 1 plus state 2), and hence the average currents of the inductors i_{L1} and i_{L2} are equal, as illustrated in the sub-circuit in Fig. 7(a).

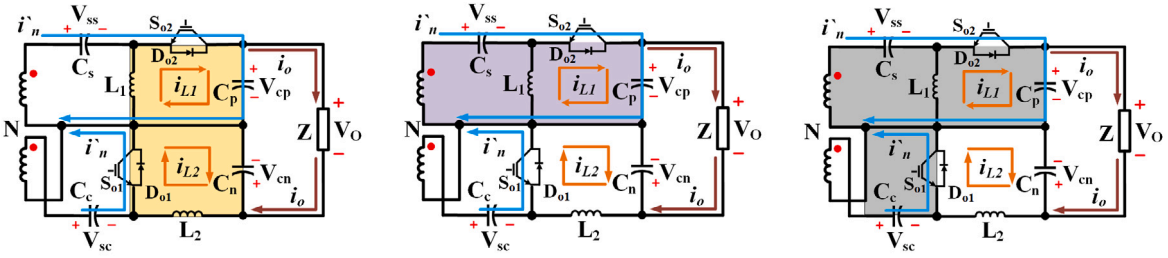
(B) The current flowing in the inductor L_1 which is i_{L1} is equal to the output current i_O. In addition, the current flowing into C_p is so close to and almost equals the current in C_S. Then, their equivalent series capacitance can be calculated from:

$$C_{eq}=\frac{C_s * C_p}{C_s+C_p} \tag{16}$$



(a) Different PV modules. (b) Same PV modules.

Fig. 6. Connecting the successive SMs in phase j with the PV modules.



(a) Sub-circuit current flow. (b) Series capacitors loop. (c) Current splitting.

Fig. 7. Observations made in state2.

(C) Accordingly, the input current i_n is divided according to the capacitors' impedances values in the converter's output sides according to the ratio ρ as seen in Fig. 7(c):

$$\rho = \frac{C_c}{C_{eq}} \tag{17}$$

Thus, the currents flowing through C_S and C_C can be expressed by:

$$i_{ss} = \frac{i_n}{N(1+\rho)} \tag{18}$$

$$i_{sc} = \frac{i_n \rho}{N(1+\rho)} \tag{19}$$

These observations and assumptions are necessary to reduce the complexity of the differential equations during *State*2. Then, the differential equations can be deduced as follows:

$$\frac{di_n}{dt} = \frac{1}{L_n}V_{in} - \frac{1}{L_n}V_{cr} - \frac{1}{NL_n}V_{sc} \tag{20}$$

$$\frac{dv_{cr}}{dt} = \frac{1}{C_r}i_n \tag{21}$$

$$\frac{dv_{ss}}{dt} = \frac{1}{C_s} * \frac{1}{N(1+\rho)}i_n \tag{22}$$

$$\frac{dv_{cc}}{dt} = \frac{1}{C_c} * \frac{\rho}{N(1+\rho)}i_n \tag{23}$$

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1}V_{cp} \tag{24}$$

$$\frac{di_{L2}}{dt} = -\frac{1}{L_2}V_{cn} \tag{25}$$

$$\frac{dv_{cp}}{dt} = \frac{1}{C_p} * \frac{1}{N(1+\rho)}i_n \tag{26}$$

$$\frac{dv_{cn}}{dt} = \frac{1}{C_n}i_{L2} - \frac{1}{C_nZ}V_{cp} - \frac{1}{C_nZ}V_{cn} \tag{27}$$

3.2. Modelling of DISC SM

The following matrices are associated with the state-space model of DISC topology: $A_{\text{on}} =$

$$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -N/C_r & -N/C_r & 0 & 0 \\ 0 & 0 & 0 & 0 & -1/C_S & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/C_C & 0 & 0 \\ 0 & N/L_1 & 1/L_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & N/L_2 & 0 & 1/L_2 & 0 & 0 & 0 & -1/L_2 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/C_pZ & -1/C_pZ \\ 0 & 0 & 0 & 0 & 0 & 1/C_n & -1/C_nZ & -1/C_nZ \end{pmatrix}$$

$B_{\text{on}} =$

$$\begin{pmatrix} 1/L_n & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}^T$$

$C_{\text{on}} =$

$$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{pmatrix}^T$$

$$\begin{pmatrix} 0 & D-1/L_n & 0 & D-1/L_nN & 0 & 0 & 0 & 0 \\ -(D-1)/C_r & 0 & 0 & 0 & -DN/C_r & -DN/C_r & 0 & 0 \\ -C_p(D-1)/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & -D/C_S & 0 & 0 & 0 \\ -(D-1)C_p+C_S/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & 0 & -D/C_C & 0 & 0 \\ 0 & DN/L_1 & D/L_1 & 0 & 0 & 0 & D-1/L_1 & 0 \\ 0 & DN/L_2 & 0 & D/L_2 & 0 & 0 & 0 & -1/L_2 \\ -C_S(D-1)/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & 0 & 0 & -D/C_pZ & -D/C_pZ \\ 0 & 0 & 0 & 0 & 0 & 1/C_n & -1/C_nZ & -1/C_nZ \end{pmatrix}$$

Box I.

$$A_{\text{off}} = \begin{pmatrix} 0 & -1/L_n & 0 & -1/L_nN & 0 & 0 & 0 & 0 \\ 1/C_r & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ C_p/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ C_p+C_S/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -1/L_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1/L_2 \\ C_S/(N*(C_CC_p+C_CC_S+C_pC_S)) & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1/C_n & -1/C_nZ & -1/C_nZ \end{pmatrix}$$

$$B_{\text{off}} = \begin{pmatrix} 1/L_n & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}^T$$

$$C_{\text{off}} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{pmatrix}^T$$

Thus, the two state-space representations are averaged over the two states during the switching period t_S, yielding the following averaged state-space matrices. See A_{avg} given in Box I.

$$B_{\text{avg}} = \begin{pmatrix} 1/L_n & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix}^T$$

$$C_{\text{avg}} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \end{pmatrix}^T$$

The s-domain transfer function of the SM is:

$$G(s) = C_{\text{avg}}(sI - A_{\text{avg}})^{-1}B_{\text{avg}} \tag{28}$$

$$G_{SM}(s) = \frac{a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0}{b_7s^7 + b_6s^6 + b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} \tag{29}$$

Where a_5,..a_0, and b_7,..b_0 are the numerator and denominator coefficients whose values are dependent on the DISC SM parameters. As expected, the steady-state voltage gain ratio of the SM is given from:

$$\lim_{s\to 0} G(s) = \frac{V_O}{V_{in}} = \frac{2ND}{1-D} \tag{30}$$

4. Parameters selection

Following the analysis of the proposed DISC SM during the two states, a set of design specifications can be obtained including the equations describing the size of the passive elements.

1. Input Inductor Design.
   As the SM's input side will be connected to a PV module, the input current ripples should be minimized to keep the operation at the maximum power point. Although an ideal inductor with zero Equivalent Series Resistance (ESR) is the best case for the total efficiency, it is the worst-case scenario for the current ripples through the inductor. Therefore, it will be considered in this analysis that the inductor is ideal to ensure that the current ripples will not exceed the maximum allowable limit. Eq. (8) described the voltage across L_n during $State1$ and can be re-written as:

$$L_n = \frac{Dt_s}{V_{in}di_n} \tag{31}$$

   The maximum ripple in inductor current $\Delta I\%$ can be expressed as a function of the average input current i_n as:

$$di_n = \Delta I\% * i_n \tag{32}$$

   Therefore, the duty cycle ratio D can be expressed as a function of the output voltage V_O and the output power Pout, Eq. (31) can be re-arranged as:

$$L_n = \frac{V_OV_{in}^2t_s}{2N\left(V_{in}+V_O\right)P_{out}\Delta \text{I}_{\text{in}}\%} \tag{33}$$

2. Output Inductor Design.
   The specifications of the output inductor can be simply derived by considering the switch entering $State1$. Thus, the values of L_1 and L_2 can be defined using Eqs. (12) and (13).

$$L_1 = \frac{\left(NV_{cr}+V_{SS}\right)Dt_s}{di_{L1}} \tag{34}$$

$$L_2 = \frac{\left(NV_{cr}+V_{SC}-V_{cn}\right)Dt_s}{di_{L2}} \tag{35}$$

   The voltage across the output inductors is expressed as a function of known parameters to determine the values of L_1 and L_2. Thus, it is possible to calculate the value of L_1 by assuming that the input voltage V_{in} is equal to the sum of the average voltage across the primary V_{cr} and SEPIC V_{SS} capacitors. Then, the following equation can be used to express the value of L_1:

$$L_1 = \frac{NV_{in}Dt_s}{di_{L1}} \tag{36}$$

   For the calculation L_2, the total average voltage of the primary V_{cr} and the CUK V_{SC} capacitor is twice the input voltage, while the negative output voltage V_{cn} is half the input voltage. Hence, the corresponding value of L_2 can be given by

$$L_2 = \frac{NV_{in}Dt_s}{di_{L2}} \tag{37}$$

   By substituting known parameters for D and $\Delta I\%$, the output inductors design can be derived as:

$$L_1 = L_2 = \frac{V_{\text{in}}\,V_o^2t_s}{2\left(V_{\text{in}}\,+V_O\right)P_{\text{out}}\,\Delta I_{L_{1,2}}\%} \tag{38}$$

3. Primary and Secondary Capacitors Design.
   During the circuit is in $State1$, the primary capacitor C_r design can be obtained from Eq. (9) and it is provided as

$$C_r = \frac{N\left(i_{L1}+i_{L2}\right)Dt_s}{dV_{cr}} \tag{39}$$

   By observing, $State1$ reveals the input current is equal to the sum of the maximum average currents flowing through the primary capacitor. Consequently, it is possible to re-write Eq. (39) as

$$C_r = \frac{Ni_nDt_s}{dV_{cr}} \tag{40}$$

   The following equation simplifies the previous one and calculates the primary capacitor as follows:

$$C_r = \frac{V_OP_{\text{out}}\,t_S}{2\left(V_{in}+V_O\right)V_{in}\Delta V_{cr}\%} \tag{41}$$

Where $\Delta V\%$ is an acceptable range of voltage ripples that is used to derive the individual capacitors' design formulas. Similarly, the currents flow through the secondary capacitors i_{L1} and i_{L2} each one with an average value equal to the output current i_o. Then, the values of C_S and C_C can then be computed using Eqs. (10) and (11).

$$C_s = C_c = \frac{i_o D t_s}{dV_{ss,cc}} \tag{42}$$

With D defined as a function of voltage V_O and power P_{out}, secondary capacitors can be selected using the following considerations.

$$C_S = C_C = \frac{P_{out} t_s}{2N\left(V_{in} + V_O\right)\Delta V_{SS,SC}\%} \tag{43}$$

4. Output Capacitors Design.
The following capacitor values are estimated for the proposed DISCs output:

$$C_p = \frac{i_{cp} D t_s}{dV_{cp}} \tag{44}$$

$$C_n = \frac{i_{cn} D t_s}{dV_{cn}} \tag{45}$$

The average current in C_p is equal to i_o, whereas the average current in C_n is zero, which allows for the use of a small capacitor. Output capacitors can be written as follows:

$$C_p = \frac{i_o D t_s}{dV_{cp}} \tag{46}$$

$$C_n = \frac{D t_s}{dV_{cn}} \tag{47}$$

This should be described in terms of output voltage and power, as these are the commonly regulated parameters. Thus, both C_p and C_n can be designed as follows:

$$C_p = \frac{P_{\text{out}}\ t_s}{2N\left(V_{\text{in}}\ + V_O\right)\Delta V_{Cp}\%} \tag{48}$$

$$C_n = \frac{V_o t_s}{2N\left(V_{in} + V_O\right)\Delta V_{CN}\%} \tag{49}$$

5. Control strategy

The control system for MMI configuration should accomplish three key objectives.

(i) To control the power flow from the PV modules to the grid. This is possible through the use of an overall controller.
(ii) To operate with a rapid dynamic response. This is accomplished through the overall controller and a second module-level controller at the SM level.
(iii) To harvest the maximum possible power from the PV modules in case of shading. This is achieved by the module-level controller.

5.1. Overall control

This system will consider that all the passive components are identical and have the same operational conditions. Therefore the full system can be viewed as one central inverter as shown in Fig. 8 and can be operated by a unified duty-cycle ratio D_{ov} and the same gate drive signals.

In this case, the equivalent circuit of the overall MMI can be obtained by the assumptions made in Table 1.

The overall transfer function can be obtained from Eq. (29) by replacing the equivalent parameters from Table 1 and represented as:

$$G_{ov}(s) = \frac{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_7 s^7 + b_6 s^6 + b_5 s^5 + b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{50}$$

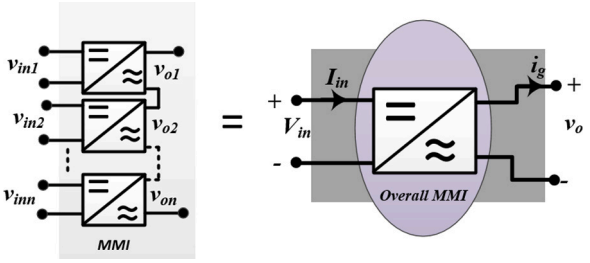


Fig. 8. Simplifying the modular series-connected inverter (1 phase).

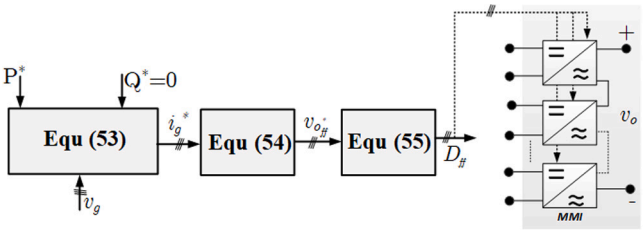


Fig. 9. Open-loop overall control system.

Table 1
Equivalent values for SM inductors and capacitors in the overall system.

SM Parameter	Equivalent	Value
Input inductor L_n	L_{nov}	$L_{nov} = L_n{}^*$ n
Sepic inductor L_1	L_{1ov}	$L_{1ov} = L_1{}^*$ n
Cuk Inductor L_2	L_{2ov}	$L_{2ov} = L_2{}^*$ n
Input capacitor C_r	C_{rov}	$C_{rov} = C_r$/n
Sepic capacitor C_S	C_{Sov}	$C_{Sov} = C_S$/n
Cuk capacitor C_C	C_{Cov}	$C_{Cov} = C_C$/n
Positive rail capacitor C_p	C_{pov}	$C_{pov} = C_p$/n
Negative rail capacitor C_n	C_{nov}	$C_{nov} = C_n$/n

5.1.1. Open-loop control

The open-loop value of the central duty-cycle ratio D_{ff} is calculated from the power equation and is fed-forward to all SMs as shown in Fig. 9

Assuming that MMI is connected to the MV grid through the grid inductor L_g with an internal resistance r_g, the total voltage delivered at the grid side equals the summation of the individual voltages of the series-connected SMs and can be expressed as:

$$v_o = \sum_{i=1}^{n} v_i = V\sin(\omega t + \theta) \tag{51}$$

Where V and θ are the magnitude of the output voltage of the SMs and the phase-shift with respect to the grid voltage, respectively. The grid voltage and current are expressed as:

$$\begin{aligned} v_g &= V_g \sin(\omega t) \\ i_g &= I_g \sin(\omega t - \varphi) \end{aligned} \tag{52}$$

The MMI delivers the active power P to the AC grid at a power factor $\cos\varphi$. Thus, the magnitude of the output voltage V, the phase-shift θ, and the magnitude of the grid current I_g is obtained from:

$$I_g = \frac{2P}{3V_g\cos(\varphi)} \tag{53}$$

The overall output voltage v_o of the MMI is calculated from:

$$\begin{aligned} \theta &= \tan^{-1}\left[\frac{r_g I_g \sin(\varphi) + \omega L_g I_g \cos(\varphi)}{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}\right] \\ V &= \left[\frac{V_g + r_g I_g \cos(\varphi) - \omega L_g I_g \sin(\varphi)}{\cos(\theta)}\right] \end{aligned} \tag{54}$$

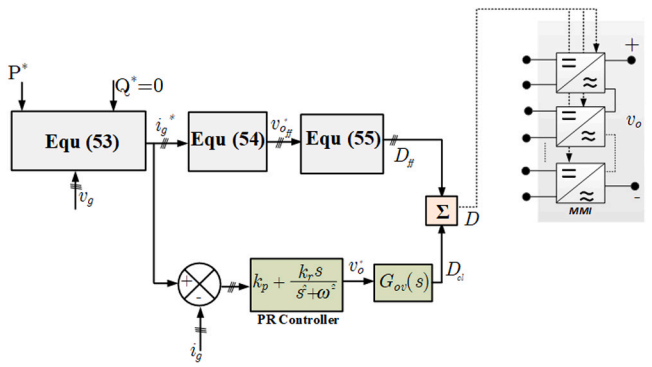


Fig. 10. Closed-loop overall control system.

The feed-forward duty-cycle ratio D_{ff} is calculated from:

$$D_{ff} = \frac{v_o(t) + V}{v_o + V + 2nNV_{in}} \tag{55}$$

Then, D_{ff} is fed to all SMs in phases a, b, and c respectively to generate the output voltage v_o. The peak value of the ac voltage V is added to generate the dc-bias voltage.

5.1.2. Closed-loop control

The open-loop control in the previous subsection will operate the MMI, generate the output voltages, and hence the output grid current. However, if there are mismatches in the passive elements values, parasitic resistances, or differences in the input voltage V_{in}, the calculated duty-cycle ratio D_{ff} will lead to an error in the output grid current. The closed-loop controller shown in Fig. 10 will fix the error by adding the closed-loop duty-cycle ratio D_{cl}. The proportional resonant (PR) controller is tuned at the grid frequency $\omega = 2\pi f$. To give an example for the selection process, the parameter values are selected and shown in Table 1. To ease the selection of the PR controller gains k_p and k_r, an average value of the duty-cycle ratio is selected at $D = 0.5$.

The root loci of the PR controller with the system are plotted in two different ways using the SISOTOOL interactive toolbox in MATLAB/SIMULINK®. Firstly, the proportional gain k_p is kept constant at 0.5 and the resonant gain k_r is increased in the range of [1:15]. Secondly, k_r is kept constant at 5 while k_p is changed from [0.1:2]. The resultant root loci are shown in Fig. 11. The values of the gains are selected in these ranges to keep the system stable, increase the bandwidth of the controller, and reduce the overshoot. A reasonable performance of the system is chosen when $k_p = 0.7$ and $k_r = 7$.

5.2. Module-level control

If the SMs are not identical, a module-level control will be required to compensate for the small mismatches in the passive elements values or the operational conditions. As this work is not considering the MPPT algorithms in particular, it will be assumed that the MPPT controller is already functioning to generate the reference point for each SM. Thus, the control scheme will start from the outputs of the MPPT controllers.

5.2.1. Open-loop control

Because all SMs in any phase share the same output current, the output voltages of module number k will depend on the ratio of the power generated by this module p_k with respect to the total generated by the full system P. As mentioned earlier, this power reference should come from the MPPT controller, which monitors the operational conditions and knows the power–voltage curves of the PV modules. Thus, if the desired output voltage of each SM is known, an open-loop duty-cycle ratio of module k can be obtained from the system in Fig. 12.

Table 2
Parameters of the TPMI.

Parameter	Value
Number of SMs (n)	80
Selected PV modules	AX500 W-96 M
PV module at maximum power	500 W, 48.63 V, 10.28 A
Transformer turns ratio	2
Rated power of the TPMI	1 MW
MVAC grid voltage	13.5 kV
SM Switching frequency	20 kHz
SM inductors	L_n = 1.5 mH and $L_1 = L_2$ = 1 mH
SM Capacitors	$C_r = C_S = C_C$ = 10 μF
Output capacitors	C_n = 10 μ F and C_p = 50 μF

The SM voltage output voltage v_{ok} is calculated from:

$$v_{ok} = \frac{p_k}{P} v_o \tag{56}$$

Then, the feed-forward duty-cycle ratio of SM number k is calculated from:

$$d_{ffk} = \frac{v_{ok}(t) + V_k}{v_{ok} + V_k + 2N v_{ink}} \tag{57}$$

Where V_k is the peak value of the SM output voltage.

5.2.2. Closed-loop control

The closed-loop controller shown in Fig. 13 will fix any errors in the open loop calculations by adding the closed-loop duty-cycle ratio d_{kcl}. The controller gains are chosen using the same methodology of the overall controller explained earlier using the SISOTOOL toolbox. In the computer simulation in the next subsection, it will be assumed that all SMs are identical with the same values for the passive components and therefore they all have the same controller gains. A reasonable performance of the system is obtained when $k_{pk} = 1.2$ and $k_{rk} = 10$.

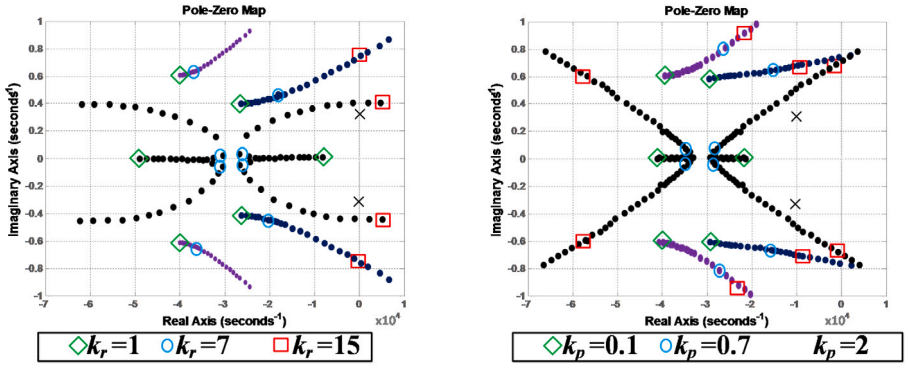
6. Simulation study

This section presents the MATLAB/Simulink simulation results for the proposed topology when used in a large-scale PV plant generating 1 MW and connected to the MVAC grid. Each SM is connected to a PV array formed of 5 series × 5 parallel PV modules. The control strategy has already been presented in Section 5 to effectively maintain inverter stability and ensure accurate tracking of the output voltages and currents. Two case studies are simulated to show the system's performance in the case of changing the irradiance level for all PV modules at the same time and partial shading of some PV modules. The simulation parameters used in these studies are listed in Table 2.

6.1. Equal irradiance

The case study shows the operation of the TPMI when the requested power is increased gradually from zero to the maximum at t=0.1 s. This can be seen from Fig. 14 when the operational point on the PV curves moves from point p_1 to point p_2. At t=0.3 s, the irradiance of the PV modules decreases suddenly to 50% leading the TPMI's power to decrease accordingly. This means that the operational point will move from p_2 to p_3.

Fig. 15 shows the output power of the TPMI where it reaches 1 MW harvested from the 80 PV arrays before dropping to 50% at t = 0.3 s and the solar irradiance of the PV modules. Fig. 16 shows the three-phase output voltage of the TPMI at the point of common coupling (PCC) with the MVAC grid and the output current of the TPMI injected into the grid when controlled at the unity power factor. At the module's level, the PV array's voltage and current of the first module are shown in Fig. 17. The output voltages of two successive SMs and their duty-cycle ratios in phase a are shown in Fig. 18.



(a) k_p= 0.5 and k_r = [1:15). (b) k_r= 5 and k_p =[0.1:2).

Fig. 11. Pole-Zero maps of the overall controller.

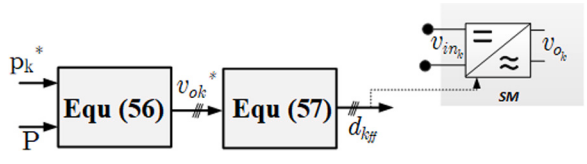


Fig. 12. Open-loop SM control system.

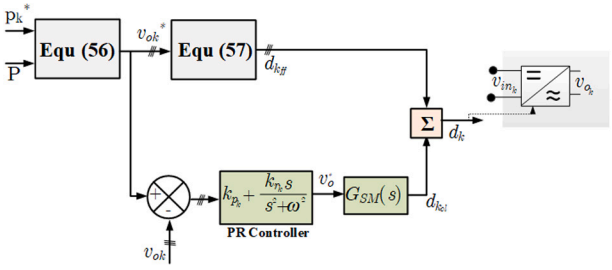


Fig. 13. Closed-loop SM control system.

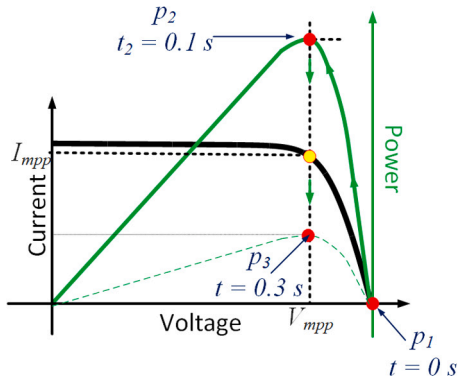


Fig. 14. Operational points on the PV curves for and equal shading.

6.2. Partial shading conditions

In this case study, half of the PV arrays will have their irradiances reduced by 50%, while the remaining PV arrays will continue to provide the maximum power. Based on the look-up table, the MPPT will make the new reference current shown in Fig. 19, and the TPMI controller will then start to track and control this calculated reference current following the MPPT.

At the time of shading, half of the PV modules lose 50% of their power, while the other half, which are not shaded, keep their full power. Fig. 20 shows the total power will be maintained at 0.75 MW during this time. The waveforms of voltages and currents for the proposed TPMI operates under shading conditions are seen in Fig. 21. Figs. 22 and 23 illustrate the voltages and currents of the PV modules for operating conditions with and without shade. The voltage output of the several shaded and unshaded SMs is shown in Fig. 24. It can be seen that unshaded SMs should increase their output voltages to compensate and match the grid voltage because shaded SMs were already affected by shading at time t = 0.3 and their voltages dropped .

7. Experimental validation

A scaled-down proof-of-concept prototype with four SMs has been developed to validate the performance of the TPMI system. Three experimental studies were conducted to determine the key operational principles and feasibility of the TPMI, which is connected to the local utility grid.

Initially, four SMs with PV at their inputs are shown to validate their fundamental functions under full-sun conditions. Next, an experiment with uniform irradiance on all PV modules was conducted, followed by an experiment with partial shade for some PV modules. The parameters for all setups are listed in Table 3 while Fig. 25 shows the system hardware and associated measurements.

7.1. Normal conditions

This experiment reveals that the TPMI is operating at full power and injecting 3 kW into the grid gradually, as shown in Fig. 26(a). This power is calculated based on the sensor boards that measure the voltage and current. Then, these values are sent to the DSP, which is connected to the code composer program on the PC, and the power is plotted using the appropriate software. Fig. 26(b) illustrates the voltage and current of grid. Fig. 26(c) depicts the first PV module's input current and voltage, whereas the output voltages of all four SMs are shown in Fig. 26(d).

7.2. Uniform shading conditions

An experiment was undertaken to demonstrate the TMPI system's capability to operate during a 50% reduction in solar irradiance across all PV modules connected to SMs. This corresponds to a 1.5 kW decrease in the power processed by SMs, as illustrated in Fig. 27(a).

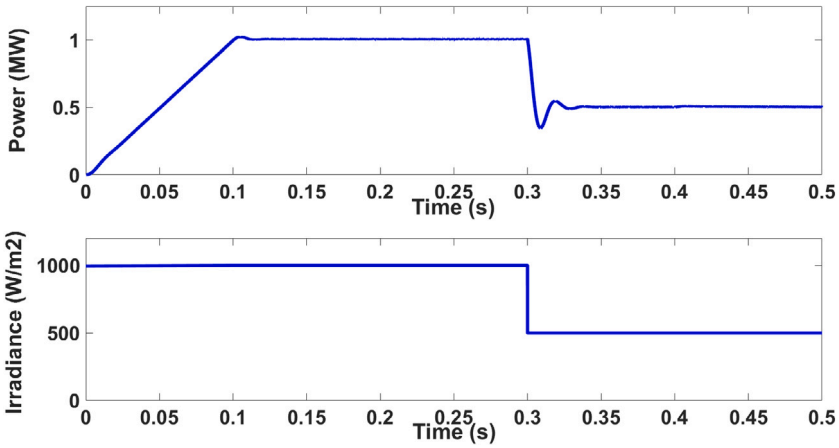


Fig. 15. Output power and irradiance.

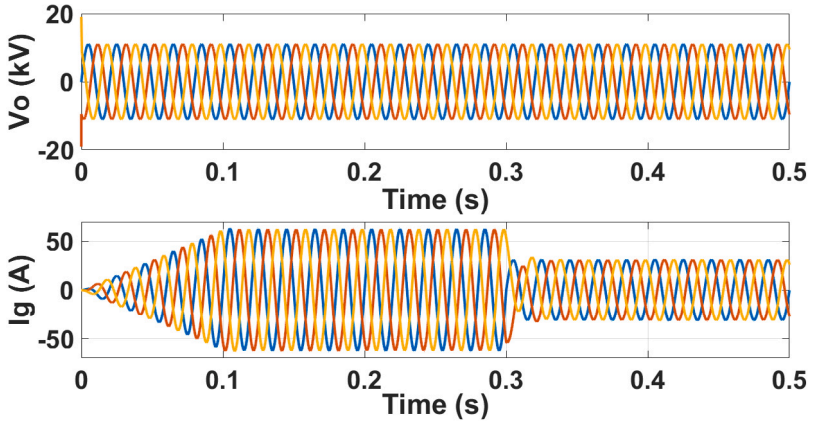


Fig. 16. Output voltages and grid currents.

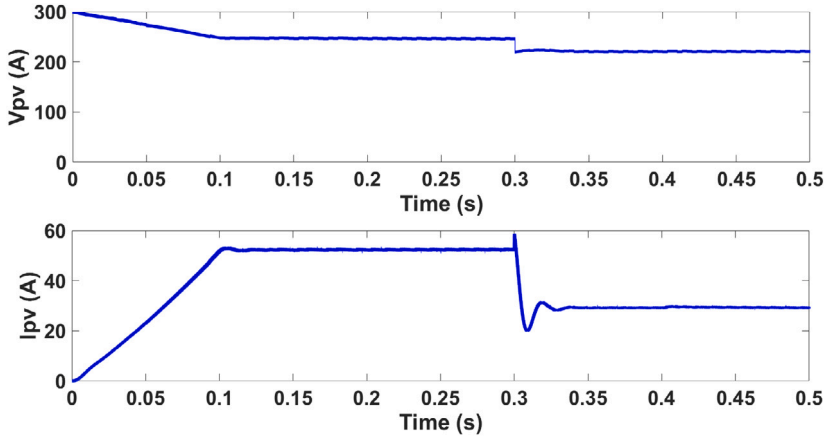


Fig. 17. PV array's voltage and current.

Fig. 27(b) shows that the grid-side voltage and current drop, while the input voltage and current of the PV module are reduced, as shown Fig. 27(c). The output voltages associated with the four SMs can be seen in Fig. 27(d).

7.3. Partial shading conditions

To further illustrate the system's performance under extreme shading conditions, an experiment was done in which 50% of the PV arrays' irradiances were reduced by 50% while the other half continued to generate maximum power. The overall system power is shown in Fig. 28(a) where there is a reduction of 25% compared to normal operating conditions. Fig. 28(b) shows grid voltage and current, whereas the input current and voltage for the 1st PV module (unshaded) and the 3rd (shaded) module are shown in Fig. 28(c). Fig. 28(d) shows SMs (1 and 2) connected to unshaded PV modules are increasing their voltage to adjust and match the grid voltage. While SMs (3 and 4) attached to shaded PV modules have already been affected by shading and have seen their voltages drop.

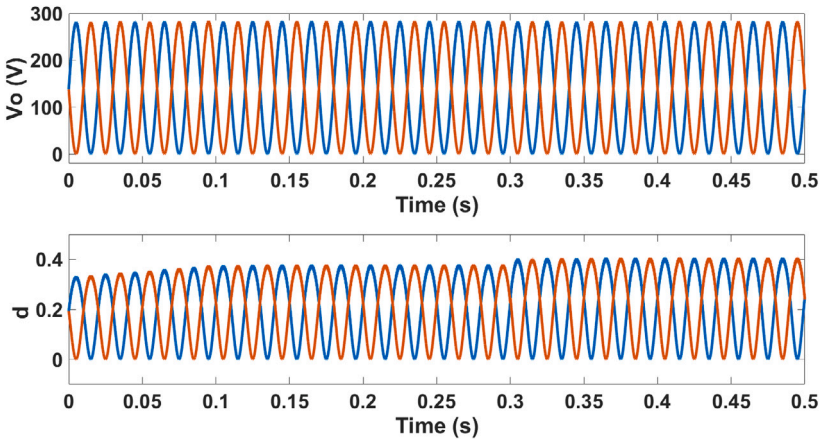


Fig. 18. Two SM voltages and their duty cycle.

Table 3
Parameters of experimental prototype.

Parameter	Value
Number of SMs (n)	4
Input Voltage and Grid voltage	50 V and 380 V R.M.S
Power generation	3 kW
Transformer turns ratio and Switching frequency	2 and 20 kHz
SM inductors	L_n = 1 mH and $L_1 = L_2$ = 1 mH
SM Capacitors	$C_r = C_S = C_C = 10\ \mu F$
Power supply devices	Keysight N8761A and Sorensen
Microcontroller	TMS320F28335
Semiconductor switch (IGBTS)	IRG4PC50FPbF (600 V–70 A)
Diodes	FFSH40120ADN

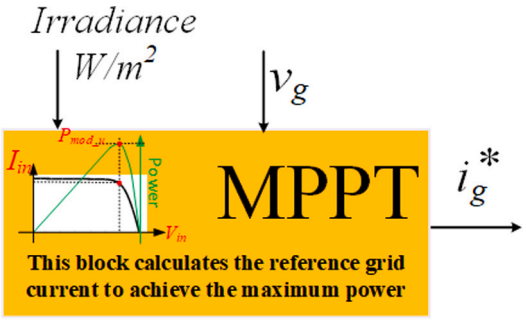


Fig. 19. MPPT look-up table in the simulations.

8. Conclusion

A new modular DC/AC inverter system suitable for LSPV systems has been introduced to improve the energy management of the PV modules. The proposed modular inverter has several advantages over the conventional centralized system, such as modularity, scalability, fault tolerance, and better performance during shading conditions because of the use of distributed MPPT controllers. A new SM has been employed using a combination of SEPIC and Cuk converters to add features to the system. The Dual-Isolated SEPIC/CUK (DISC) SM needs very small input capacitance in order to keep the input current constant, which will improve the reliability of the system. In addition, the DISC SM allowed for employing small-size high-frequency transformers to provide galvanic isolation between the PV arrays and the ac output side. Moreover, the DISC SM increases the output voltage of each module, which is favourable in this application. The mathematical analysis and state-space representation have been presented in this paper, and then the control schemes have been studied, designed, and presented. Two control systems have been used to control the proposed inverter at both general and SM levels. The operation of the inverter has been presented using MATLAB/Simulink simulations during normal, equal shading, and partial shading conditions to ensure that the controller is capable of extracting the maximum available power from the PV modules. Finally, the inverter's operation is tested and confirmed using a scaled-down experimental prototype with four SMs and a TMS320F28335 DSP. In future research, the proposed inverter can be improved by applying soft switching techniques to operate with lower switching losses and higher performance and efficiency. The HFT design has not been considered in detail in this paper. However, as it connects to two different converters on its secondary side, it needs more consideration in design when it is required to increase the switching frequency of the DISC converter.

CRediT authorship contribution statement

Saud Alotaibi: Conceptualization, Methodology, Software, Writing – original draft, Visualization. **Ahmed Darwish:** Conceptualization, Methodology, Writing – review & editing, Supervision. **Barry W. Williams:** Conceptualization, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgments

Saud Alotaibi would like to express his gratitude to Shaqra University for fully sponsoring his Ph.D. research at Lancaster University.

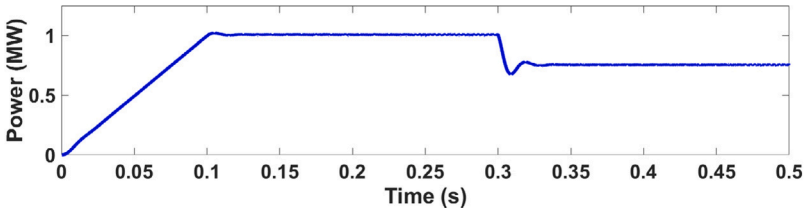


Fig. 20. Total power.

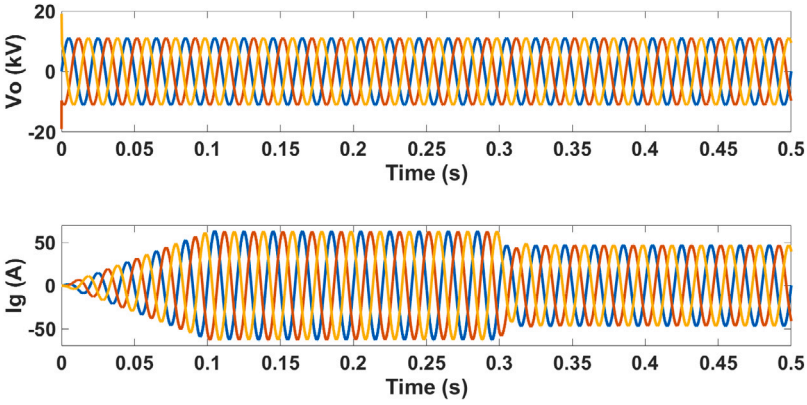


Fig. 21. Output voltages and currents.

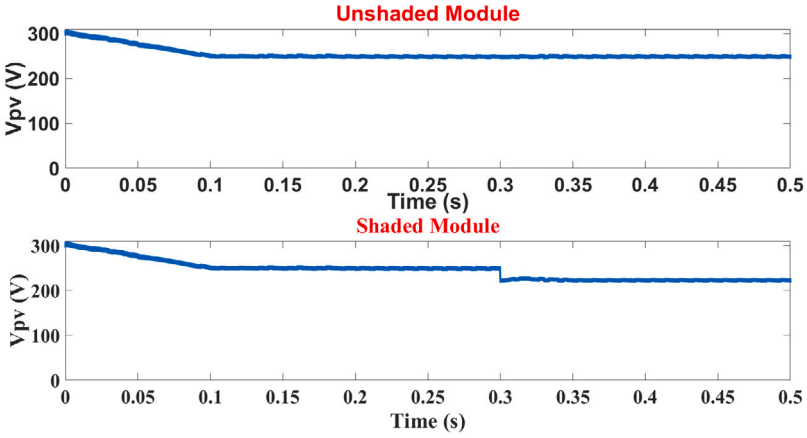


Fig. 22. PV voltage for modules without and with shading.

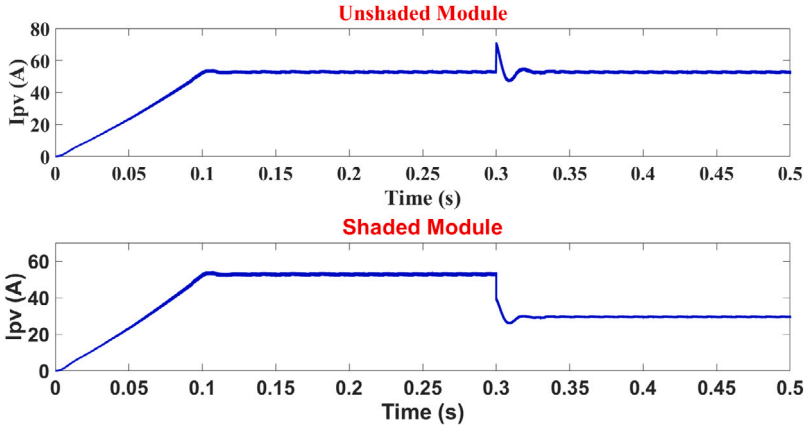


Fig. 23. PV current for modules without and with shading.

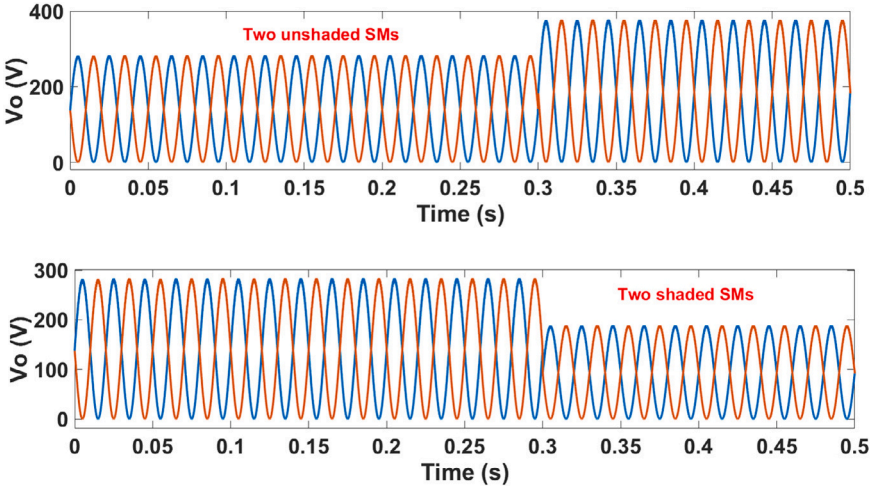


Fig. 24. Voltage of different shaded and unshaded SMs.

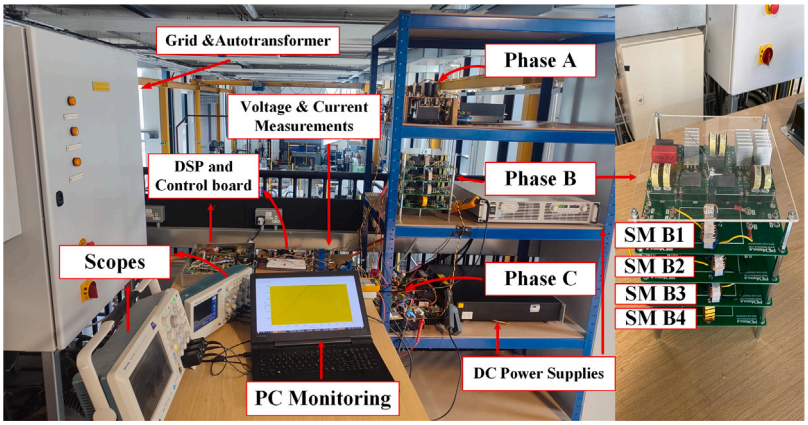
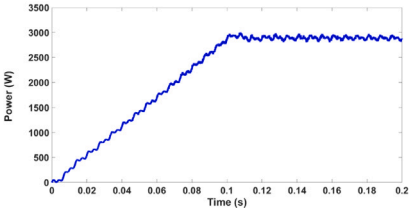
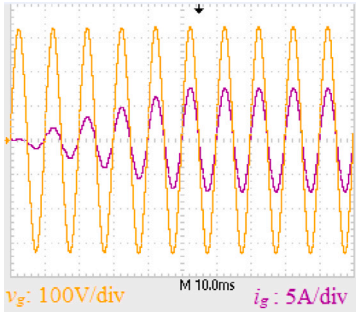


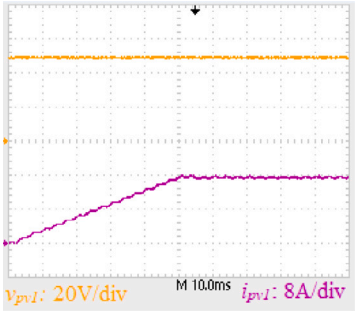
Fig. 25. Experimental setup of the TPMI.



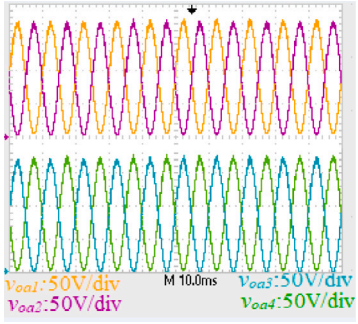
(a) Output power.



(b) Grid voltage and current.

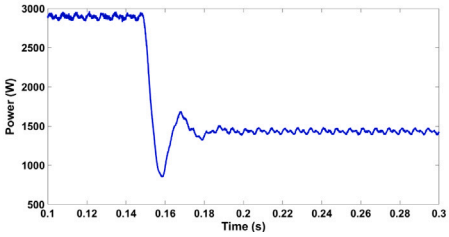


(c) Input PV voltage and current.

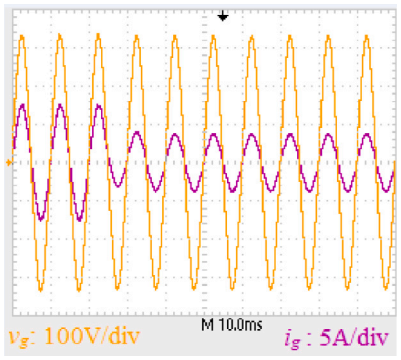


(d) SMs voltage.

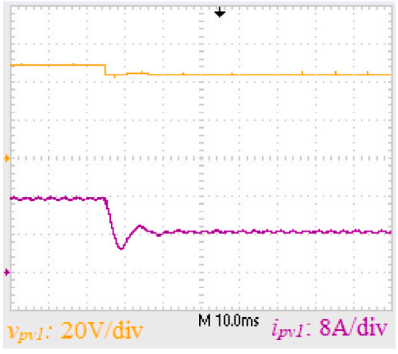
Fig. 26. Normal-condition results.



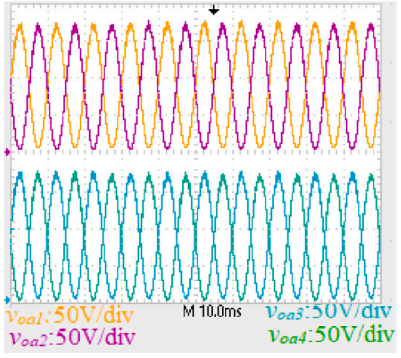
(a) Output power.



(b) Grid voltage and current.

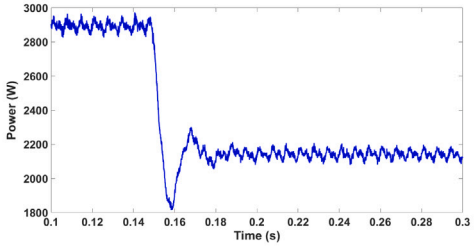


(c) Input PV voltage and current.

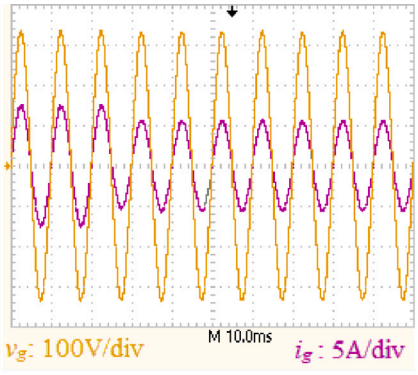


(d) SMs voltage.

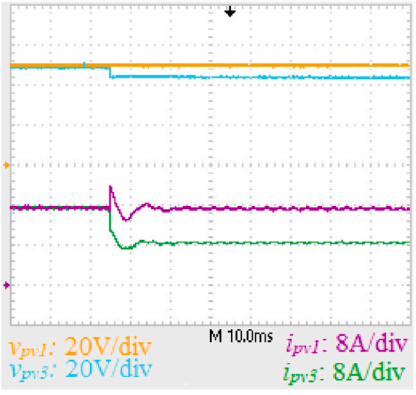
Fig. 27. Uniform shading conditions.



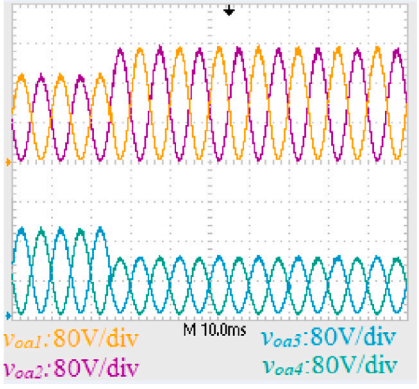
(a) Output power.



(b) Grid voltage and current.



(c) Input PV voltage and current.



(d) SMs voltage.

Fig. 28. Partial shading conditions.

References

[1] Karimi M, Mokhlis H, Naidu K, Uddin S, Bakar AA. Photovoltaic penetration issues and impacts in distribution network–A review. Renew Sustain Energy Rev 2016;53:594–605.

[2] Schmela M, Döring T. Global market outlook for solar power 2017–2021. SolarPower Europe 2017.

[3] IREN. Future of solar photovoltaic: Deployment, investment, technology, grid integration and socio-economic aspects. www.irena.org/publications/2019/Nov/Future-of-Solar-Photovoltaic.

[4] REN21. Renewables 2021 global status report. www.ren21.net/wp-content/uploads/2019/05/GSR2021_Full_Report.pdf.

[5] Blaabjerg F, Chen Z, Kjaer SB. Power electronics as efficient interface in dispersed power generation systems. IEEE Trans Power Electron 2004;19(5):1184–94.

[6] Choi H, Ciobotaru M, Jang M, Agelidis VG. Performance of medium-voltage DC-bus PV system architecture utilizing high-gain DC–DC converter. IEEE Trans Sustain Energy 2015;6(2):464–73.

[7] Islam MR, Mahfuz-Ur-Rahman A, Muttaqi KM, Sutanto D. State-of-the-art of the medium-voltage power converter technologies for grid integration of solar photovoltaic power plants. IEEE Trans Energy Convers 2018;34(1):372–84.

[8] Bella S, Houari A, Djerioui A, Chouder A, Machmoum M, Benkhoris M-F, et al. Robust model predictive control (MPC) for large-scale PV plant based on paralleled three-phase inverters. Sol Energy 2020;202:409–19.

[9] Xiao B, Hang L, Mei J, Riley C, Tolbert LM, Ozpineci B. Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid-connected applications. IEEE Trans Ind Appl 2014;51(2):1722–31.

[10] Basu TS, Maiti S, Chakraborty C. Performance improvement of PV-Fed hybrid modular multilevel converter under partial shading condition. IEEE Trans Ind Electron 2020.

[11] Zeb K, Uddin W, Khan MA, Ali Z, Ali MU, Christofides N, et al. A comprehensive review on inverter topologies and control strategies for grid connected photovoltaic system. Renew Sustain Energy Rev 2018;94:1120–41.

[12] Zhang X, Zhao T, Mao W, Tan D, Chang L. Multilevel inverters for grid-connected photovoltaic applications: Examining emerging trends. IEEE Power Electron Mag 2018;5(4):32–41.

[13] Elsanabary AI, Konstantinou G, Mekhilef S, Townsend CD, Seyedmahmoudian M, Stojcevski A. Medium voltage large-scale grid-connected photovoltaic systems using cascaded H-Bridge and modular multilevel converters: A review. IEEE Access 2020;8:223686–99.

[14] Lumbreras D, Barrios EL, Balda J, Navarrete M, González R, Sanchis P. Medium-voltage cascaded sequential topology for large-scale PV plants. IEEE Access 2021;9:130601–14.

[15] Sochor P, Akagi H. Theoretical comparison in energy-balancing capability between star-and delta-configured modular multilevel cascade inverters for utility-scale photovoltaic systems. IEEE Trans Power Electron 2015;31(3):1980–92.

[16] Yu Y, Konstantinou G, Townsend CD, Agelidis VG. Comparison of zero-sequence injection methods in cascaded H-bridge multilevel converters for large-scale photovoltaic integration. IET Renew Power Gener 2017;11(5):603–13.

[17] Yu Y, Konstantinou G, Hredzak B, Agelidis VG. Power balance optimization of cascaded H-bridge multilevel converters for large-scale photovoltaic integration. IEEE Trans Power Electron 2015;31(2):1108–20.

[18] Gunsal I, Stone DA, Foster MP. Suppressing leakage current for cascaded H-bridge inverters in renewable energy and storage systems. IEEE Trans Ind Electron 2020;68(11):11035–43.

[19] Zhou Y, Li H. Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems. IEEE Trans Power Electron 2013;29(10):5265–77.

[20] Kumar VP, Fernandes B. Minimization of inter-module leakage current in cascaded H-bridge multilevel inverters for grid connected solar PV applications. In: 2016 IEEE applied power electronics conference and exposition. IEEE; 2016, p. 2673–8.

[21] Nademi H, Das A, Burgos R, Norum LE. A new circuit performance of modular multilevel inverter suitable for photovoltaic conversion plants. IEEE J Emerg Sel Top Power Electron 2015;4(2):393–404.

[22] Rojas CA, Kouro S, Perez MA, Echeverria J. DC–DC MMC for HVdc grid interface of utility-scale photovoltaic conversion systems. IEEE Trans Ind Electron 2017;65(1):352–62.

[23] Acharya AB, Ricco M, Sera D, Teoderscu R, Norum LE. Performance analysis of medium-voltage grid integration of PV plant using modular multilevel converter. IEEE Trans Energy Convers 2019;34(4):1731–40.

[24] Achanta PK, Johnson BB, Seo G-S, Maksimovic D. A multilevel DC to three-phase AC architecture for photovoltaic power plants. IEEE Trans Energy Convers 2018;34(1):181–90.

[25] Alotaibi S, Darwish A. Modular multilevel converters for large-scale grid-connected photovoltaic systems: A review. Energies 2021;14(19):6213.

[26] Marei MI, Alajmi BN, Abdelsalam I, Ahmed NA. An integrated topology of three-port DC-DC converter for PV-battery power systems. IEEE Open J Ind Electron Soc 2022;3:409–19.

[27] Alajmi BN, Marei MI, Abdelsalam I. A multiport DC–DC converter based on two-quadrant inverter topology for PV systems. IEEE Trans Power Electron 2020;36(1):522–32.

[28] Nasr Esfahani F, Darwish A, Massoud A. PV/Battery grid integration using a modular multilevel isolated SEPIC-based converter. Energies 2022;15(15):5462.

[29] Edwin FF, Xiao W, Khadkikar V. Dynamic modeling and control of interleaved flyback module-integrated converter for PV power applications. IEEE Trans Ind Electron 2013;61(3):1377–88.

[30] Ali AIM, Tuan CA, Takeshita T, Sayed MA, Alaas ZM. Modular single-stage three-phase flyback differential inverter for medium/high-power grid integrated applications. Sensors 2022;22(5):2064.

[31] Badawy AD. Current source dc-dc and dc-ac converters with continuous energy flow. 2015.

[32] Darwish A, Elgenedy MA. Current-source modular medium-voltage grid-connected system with high-frequency isolation for photovoltaic applications. IEEE Trans Energy Convers 2018;34(1):255–66.

[33] Darwish A, Alotaibi S, Elgenedy MA. Current-source single-phase module integrated inverters for PV grid-connected applications. IEEE Access 2020;8:53082–96.

[34] Anand A, Singh B. Power factor correction in Cuk–SEPIC-based dual-output-converter-fed SRM drive. IEEE Trans Ind Electron 2017;65(2):1117–27.

[35] Alotaibi S, Darwish A, Ma X, Williams BW. A new modular three-phase inverter based on Sepic-Cuk combination converter for photovoltaic applications. In: The 9th renewable power generation conference (RPG Dublin Online 2021), Vol. 2021. IET; 2021, p. 259–64.