Gate driver power supply arrangement for cascode-connected super-junction MOSFETs in a bridge-leg

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This letter presents a circuit for powering cascode gate driver circuits with super-junction (SJ) MOSFETs in a bridge-leg. The cascode gate driver gives inherent MOSFET intrinsic diode deactivation, and the bridge-leg incorporates an inductive turn-on snubber which controls the charging currents into the MOSFETs' output capacitances. The cascode driver circuits and snubber inductor are configured such that the gate-drive energy is derived from the power stage.

Introduction: The super-junction (SJ) MOSFET [1] has a low on-state resistance and fast switching times. Other attributes include a robust gate drive requirement and good short-circuit withstand properties [2]. It operates with high efficiency in single-ended circuits such as boost converters used for power factor correction [3]. However, the intrinsic diode recovery behaviour and non-linear output capacitance of the SJ MOSFET are problematic in voltage source converter (VSC) bridge-legs. Diode recovery can be addressed by driving the MOSFET with the arrangement in [4], or by deploying it in a cascode-driven connection [5], both of which deactivate the intrinsic diode. A further advantage of the cascode switch is that the gate driver circuit normally only needs a single supply rail, and techniques such as those in [6–8] are not needed to produce a negative supply rail to protect against dv/dt-induced turn-on.

The *QV* characteristic for a SiHP080N60E SJ MOSFET in Figure 1 was obtained by entering the manufacturer's graphical data for the output capacitance C_{oss} against drain-source voltage V_{DS} into the *Engauge Digitizer* program. The device is rated at 650 V, and typically used in 400-V applications which provides a margin of approximately 50% between its operating and rated voltages. With V_{DS} at 400 V, the charge Q_{oss} stored on C_{oss} was estimated at 227 nC from Figure 1. It is seen that, when charged to 400 V, the *QV* curve is approximately rectangular, and most of the final $Q_{oss}V_{DS}$ product is composed of co-energy, rather than stored electric field ('self-discharge') energy. Even with intrinsic diode deactivation implemented with the techniques in [4] or [5], the SJ MOSFET cannot be used advantageously in a VSC bridge-leg [9] without also addressing C_{oss}. A technique for achieving this is to use a turn-on switching-aid ('snubber') circuit [10].

Gate driver power can be delivered via transformers, but these incur cost, bulk and footprint area. Furthermore, fast-switching devices such as the SJ MOSFET apply high dv/dts across the transformer's parasitic inter-winding capacitances. These dv/dts inject common-mode (CM) currents into the gate driver's low-side circuitry which can cause it, or the control circuitry connected to it, to malfunction. This can necessitate

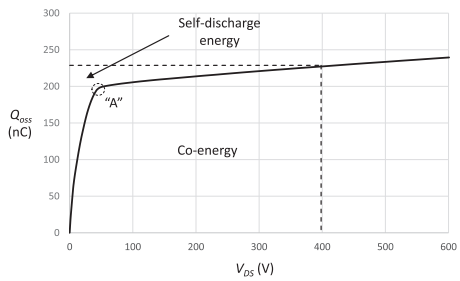

Fig. 1 *SiHP080N60E SJ MOSFET output capacitance* QV *characteristic. SJ, super-junction.*

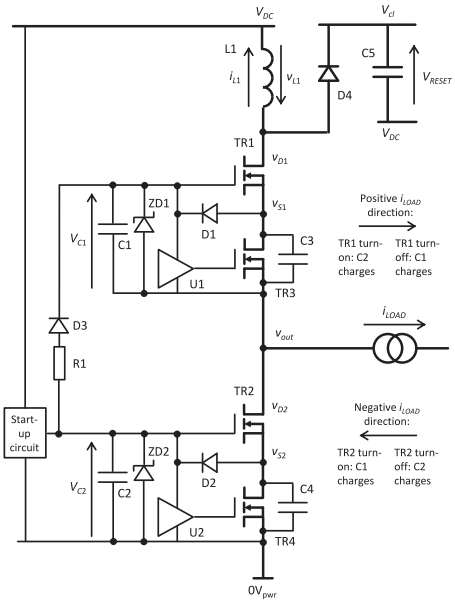

Fig. 2 *Proposed circuit*

the use of specialised transformer constructions [11, 12] or power supply architectures [13] to address dv/dt-induced CM currents. Supplying gate driver power by other means is therefore potentially desirable. This letter presents a bridge-leg with cascode-driven SJ MOSFETs and a snubber inductor, where the power for the gate driver circuits is derived from the charging currents into the SJ MOSFETs' output capacitances.

Proposed technique: Figure 2 shows the proposed circuit. TR1 and TR2 are the main SJ MOSFETs. TR3 and TR4 are the respective low-voltage MOSFETs connected in series with TR1 and TR2 to realise cascode switches. U1 and U2 are driver ICs. L1 is a turn-on snubber inductor which controls the charging currents into the output capacitances of TR1 and TR2. L1 is reset by means of clamping the voltage across it to V_{RESET}. The stored energy in L1 which is transferred into the local decoupling capacitor C5 can be dissipated, or recovered using a switched-mode circuit, as in [10]. Consider initially where the load current i_{LOAD} is positive, and TR1 turns on and turns off. When TR1 turns on, the drain current in TR2 reverses and v_{S2} rises to just below the voltage V_{C2} across C2, at which point the channel of TR2 cuts off. However, TR2's C_{oss} continues to source current into C2 via D2, with V_{C2} being clamped to the Zener voltage V_Z of ZD2. When the bulk of Q_{oss} has been supplied into C_{oss}, corresponding to Point A in Figure 1, the drain-source voltage of TR2 rises rapidly. The voltage v_{L1} reverses and stored energy in L1 is transferred into the clamp voltage V_{cl} via D4. The energy E_{ON} supplied into C2 and ZD2 due to TR1 turning on with a positive i_{LOAD} is given by

$$E_{ON} = V_{C2}Q_{oss}. \tag{1}$$

At TR1 turn-off, its source voltage rises and cuts off its channel. Its C_{oss} continues to conduct current into C1 via D1, with V_{C1} being clamped to the V_Z of ZD1. When the bulk of Q_{oss} has been supplied into C_{oss}, again corresponding to Point A in Figure 1, the drain-source voltage of TR1 rises. The energy E_{OFF} supplied into C1 and ZD1 due to TR1 turning off with a positive i_{LOAD} is given by

$$E_{OFF} = V_{C1}Q_{oss}. \tag{2}$$

With a negative i_{LOAD} the situation is essentially the same, except that V_{C1} is charged by the turn-on action of TR2, and V_{C2} is charged by the turn-off action of TR2.

C3 and C4 are included to mitigate divergent oscillations when TR1 or TR2 is being held off [14]. Small ferrite ring cores for damping are located around the conductors directly in series with L1 and D4 for the same reason. E_{ON} and E_{OFF} will normally be the same because V_{C1} and V_{C2} are both clamped to a voltage V_G by ZD1 and ZD2, respectively. The

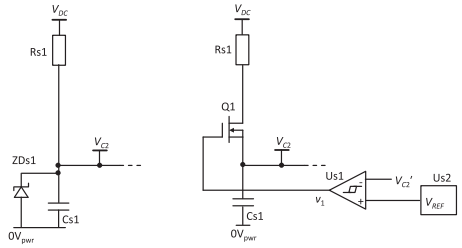

Fig. 3 *Start-up circuits: (a) passive shunt regulator, (b) main components of active series regulator for reduced power consumption*

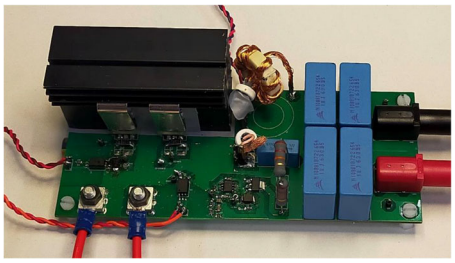

Fig. 4 *Experimental hardware*

energy E_{GATE} required to drive a cascode-connected MOSFET through a complete turn-on and turn-off switching cycle is given by

$$E_{GATE} = V_G \left(Q_g + Q_{g2}\right) \tag{3}$$

where Q_g and Q_{g2} are the charges drawn by the input capacitances of the SJ MOSFET and low-voltage series MOSFET, respectively. An important feature of the SJ MOSFET for the application in this letter is that Q_{oss} exceeds Q_g sufficiently so that the dynamic gate driver power requirements, and the quiescent and dynamic energy consumption of U1 and U2, can be met by deriving energy from the charging currents into the C_{oss} capacitances. The excess energy is dissipated in ZD1 and ZD2. Some recovery of the energy stored in the applicable SJ MOSFET's input capacitance is expected when its source voltage rises. Also, possible effects of the SJ MOSFETs' reverse transfer capacitances on the power flowing into V_{C1} and V_{C2} are neglected in the simplified analysis here.

The start-up circuit supplies initial power into V_{C2} to enable TR2 to start switching. The bootstrap diode D3 in turn transfers start-up energy from V_{C2} into V_{C1}, but is not needed to supply energy into V_{C1} during steady-state operation, as this is implemented by the methods that have been described in this section. R1 provides current limiting and damps capacitive currents through D3. Figure 3a shows a simple start-up circuit. However, the variant in Figure 3b was used to reduce the steady-state power dissipation in the series resistor Rs 1 to zero. Techniques for attaining this are described in [15], and the circuit in Figure 3b uses an N-channel depletion-mode MOSFET Q1 to disconnect Rs1 from V_{C2} when V_{C2} has risen sufficiently. A resistive potential divider produces a scaled-down voltage V_{C2}' from V_{C2}, and V_{C2}' is compared with a reference voltage V_{REF} by the comparator Us1. If V_{C2}' rises above V_{REF} then the output voltage v_1 of Us1 goes low, thereby turning off Q1. Hysteresis is included to prevent Us1 switching at an unnecessarily high frequency, and to provide noise immunity. V_{REF} is derived from Us2 which is a voltage reference IC. After TR1 and TR2 start switching, V_{C2} is supported via D2 by the current charging the C_{oss} capacitance of TR2. Q1 is then held permanently off and the power dissipated in Rs1 consequently drops to zero. It is noted that the power drawn from V_{C2} slightly exceeds that drawn from V_{C1} because of the start-up circuitry connected across V_{C2}.

The description of the proposed circuit has so far addressed its operation in the continuous conduction mode, but at low load currents it enters the triangular conduction mode (TCM). In the TCM, TR1 and TR2 always turn off with a positive drain current in them. Energy is not transferred into C1 or C2 when TR1 or TR2 turn on, but energy is transferred into C1 at TR1 turn-off, and into C2 at TR2 turn-off.

Experimental hardware: The construction of the circuit in Figure 2 is shown in Figure 4. L1 used a TX22/14/6.4 toroidal core in 3C90 material. Two air-gaps were cut into it, and it was wound with 10 turns of 42 twisted strands of 0.2-mm diameter copper wire. The inductance of L1 was measured at 2.41 μH. U1 and U2 were FOD8342 gate driver ICs, with optical isolation and a typical isolation capacitance specified at 1 pF. These ICs have an undervoltage lockout (UVLO) function. 10-**Ω** resistors were placed between the output of U1 and the gate of TR3, and between the output of U2 and the gate of TR4, but are not shown in Figure 2 for simplicity. ZD1 and ZD2 have a V_Z of 15 V. The SiHP080N60E and IPD031N03L MOSFETs used in experimentation have specified input capacitances of 2.6 and 4.0 nF, respectively, resulting in a total charge of 99 nC being drawn when charged to 15 V. This is less than the Q_{oss} which was estimated at 227 nC when charged to 400 V, as shown in Figure 1. Data for the experimental circuit are listed in Tables 1 and 2. Also, four 1 μF, 630 V, polypropylene capacitors were connected in parallel between V_{DC} and 0 V_{pwr} to provide DC rail local decoupling.

With respect to the supply of V_{C2}, the significant voltage levels are:

- Typical UVLO threshold levels of the gate driver ICs specified in the manufacturer's datasheet: 7.7 V (low) and 8.3 V (high)
- Nominal voltage limits between which the regulator circuit in Figure 3b controls V_{C2}: 11.5 V (low) and 12.8 V (high)
- Steady-state value of V_{C2} which is maintained once TR1 and TR2 start switching: approximately 15 V, as set by the clamping action of ZD2

Figure 5 shows the snubber reset circuit, which was designed to present a constant-voltage sink of 40 V across V_{RESET}. For simplicity, this was not a switched-mode circuit for recovering energy as in [10], but was dissipative. Details are: TR1d = STP310N10F7, R1d = 2.2 k**Ω**, ZD1d = BZX55C36-TAP. The reset circuit was located remotely from the PCB in Figure 4, with TR1d being mounted on a heatsink.

Start-up details: The drive signals to TR1 and TR2 are applied simultaneously when V_{DC} has been present for enough time to charge V_{C2} to

Table 1. Component data for the circuit in Figure 2

Component	Component details
R1	22 Ω
C1,2	Three 1 μF, ceramic, in parallel
C3,4	6.8 nF, polypropylene
C5	2.2 μF, 100 V, metallized polyester film
L1	2.41 μH, gapped ferrite toroidal core
D1,2	ES1A
D3	GB01SLT06-214
D4	IDD03SG60CXTMA2
ZD1,2	SMBZ5929B
TR1,2	SiHP080N60E
TR3,4	IPD031N03L
U1,2	FOD8342

Table 2. Key component data for the circuit in Figure 3b

Component	Component details
Rs 1	Two 22 kΩ, 3 W, carbon, plated through hole, in series
Cs1	220 μF, electrolytic and 1 μF, ceramic, in parallel
Q1	BSP135
Us1	TL071BCDR
Us2	TL431ACL3T

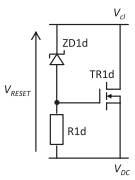

Fig. 5 *Dissipative snubber reset circuit used for experimentation*

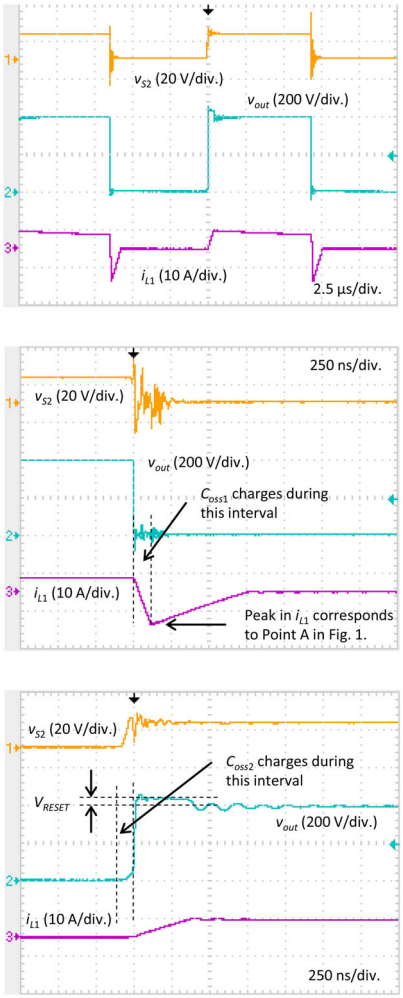

Fig. 6 *Experimental waveforms from circuit in Figure 2. Top: Switching-frequency waveforms; middle: TR2 turn-on; bottom: TR2 turn-off*

above 11.5 V. When TR2 starts switching, V_{C1} initially charges via D3. The sum of C2 and Cs1 is made sufficently greater than C1 such that V_{C1} rises above U1's high UVLO level, but without V_{C2} being pulled below U2's low UVLO level. The resistance of Rs1 is so that it can supply the circuitry across V_{C2} with sufficient current for V_{C2} to rise to where it is being regulated by Q1, when V_{DC} is at approximately 300 V. If V_{DC} is present, but without switching signals also being present, then V_{C2} is supplied solely via Rs1, and Rs1 is rated to manage the steady-state power consequently dissipated in it in this eventuality.

Experimental readings: V_{DC} was 400 V. A series RL load was connected between V_{DC} and v_{out}. i_{LOAD} was therefore negative. Its average value was 4.3 A. The circuit was switched at 75 kHz with a duty cycle of 50%, and the drive signals applied to U1 and U2 had dead-times of 400 ns. As expected, V_{C1} and V_{C2} were each measured at approximately 15 V during steady-state operation. Figure 6 shows key waveforms.

Conclusion: This letter has presented a circuit for powering cascode gate driver circuits for SJ MOSFETs in a bridge-leg. The cascode circuit inherently deactivates the MOSFETs' intrinsic diodes, and the bridge-leg incorporates an inductive snubber which controls the charging currents into the MOSFETs' output capacitances. These currents are used to supply the MOSFETs' gate driver power requirements. The technique has been demonstrated in a bridge-leg operating from 400 Vdc, and switching 4.3 A at 75 kHz. Further investigation will include assessing the circuit's applicability to three-phase power converters and SiC power devices, and a detailed evaluation of the circuit's power losses.

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Conflict of interest: The authors declare no conflict of interest.

Data availability statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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