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COMPARISON OF PHASE-LEG CIRCUITS FOR CRYOGENIC OPERATION IN THE ALL-ELECTRIC AIRCRAFT

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Abstract

Commercial all-electric aircraft are projected to be flying as early as 2035, where hydrogen is selected to supply fuel and coolant. The cryogenic aircraft's powertrain includes the turbines, generators, power electronics and fan motors. As most of the powertrain is located at cryogenic temperature, it is preferable to co-locate the power electronics in the same region to reduce the engineering system's complexity. Silicon super-junction MOSFETs are known for their high efficiency, thus lower cooling requirements at cryogenic temperature. However, in phase-leg circuits, the behaviour of the MOSFET's intrinsic diode, and its output capacitance are challenging. These issues can be addressed by using the MOSFET with ancillary power devices to realise diode deactivation. This paper compares different permutations of intrinsic diode deactivation devices at room temperature and cryogenic temperature. The paper presents a demonstrator phase-leg built with different ancillary power devices. It is operated from a DC voltage of 270 V, and supplies a phase current of up to 10 A.

1. Introduction

To reduce environmental emissions, research on the All-Electric Aircraft has been seeking to realise its practicality by increasing the power density of the system [1], [2]. Hydrogen is projected as a disruptor for the industry, and Rolls Royce and Airbus are currently in the race to transform their turbines and aircraft to be hydrogen-based [3], [4]. Previous literature has proposed architectures for the aircraft's power system [4], where everything including the converters and inverters is suggested to be operated at cryogenic temperature as it is better from an engineering point of view to have all the electrical components at the same temperature. Fig. 1 shows a proposed architecture based on the works of previous literature [1], [4], where superconducting cables, motors and power electronics are used at cryogenic temperature.

Without taking into account the cooling system's losses, research has indicated that the use of cryogenic power electronics can improve the systems' performance. This is mainly due to lower conduction losses and faster switching speeds [5]–[7].

Previous literature has reviewed the performance of different power semiconductor devices at cryogenic temperature [8]–[16]. Si and GaN devices have shown lower conduction losses at cryogenic temperatures. However, GaN has shown an increase of the kink effect at a cryogenic temperature which may result in them being unreliable. SiC devices show an increased conduction loss at cryogenic temperature and for that reason the use of SiC devices at cryogenic temperature can decrease efficiency. Thus, silicon-based devices are attractive at cryogenic temperatures. Table 1 summarises the approximate performance trends of some key power devices used for high-efficiency power conversion.

Table 1. Approximate MOSFET performance trends as the temperature is reduced from room temperature to 77 K.

Device type	Parameter	Trend as the temperature is reduced to 77 K
SiC MOSFET [6], [8], [10]-[14]	V_{DSS}	+60%
	$R_{DS(on)}$	+300%
	Intrinsic diode Q_{rr}	Improved
	$v_{GS(th)}$	Sparse data
GaN device [6], [9], [14], [15]	V_{DSS}	+6%
	$R_{DS(on)}$	-87.5%
	Intrinsic diode Q_{rr}	Very good
	$v_{GS(th)}$	Sparse data
Si SJ MOSFET [5]-[7], [16]	V_{DSS}	-25%
	$R_{DS(on)}$	-80%
	Intrinsic diode Q_{rr}	Very good
	$v_{GS(th)}$	+15%

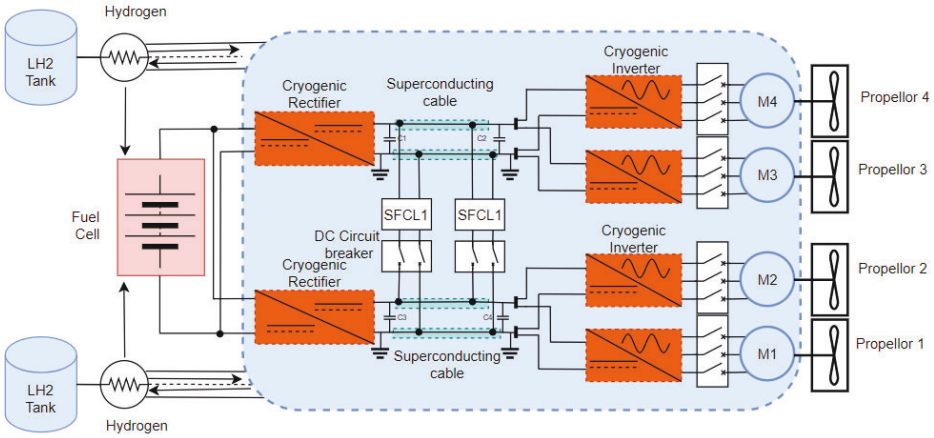


Fig. 1. Power distribution architecture for hydrogen electric aircraft.

Of the silicon devices, the super-junction (SJ) MOSFET has a high-voltage capability, low switching losses and low conduction losses [17], [18]. However, an important converter type used in aircraft applications is the voltage source converter (VSC) variant. In these converters, the SJ MOSFET's intrinsic diode incurs high losses due to its large reverse recovery charge Q_{rr}. To address this, [19] has patented a circuit to deactivate the intrinsic diode and avoid the passage of Q_{rr}. This technique has been implemented in a 40-kW cryogenic NPC inverter in [20]. However, there are different permutations of the circuit in [19], and a practical comparison of their performances is of interest. Apart from Q_{rr}, the non-linear output capacitance C_{oss} of the SJ MOSFET is problematic in VSC converters. This latter problem can be addressed with the dual-mode control technique in [21].

Based on this gap in the literature, the main goal of this paper is to compare four different diode deactivation circuits for the SJ MOSFET when operating in a two-level VSC phase-leg with dual-mode control. An initial comparison is carried out at room temperature (RT), and two of the circuits are then down-selected for evaluation at cryogenic temperature (CT) in liquid nitrogen. Section 2 gives background on the phase leg operation and methods of reducing the losses for the SJ MOSFET, in particular, discussing diode deactivation, the dual-mode control technique and dual-mode gate drivers. Section 3 tests four different diode deactivation permutations with the SJ MOSFET at RT. Based on the RT results, two permutations are chosen for further testing at CT and the results are given in Section 4 where simulations are also presented. Sections 5 and 6 are the discussions and the conclusion of the article.

2. Background

As mentioned in Section 1, the SJ MOSFET's intrinsic diode and output capacitance present challenges when used in VSCs. This section discusses how literature has addressed the issue of intrinsic diode deactivation, and how dual-mode control can improve the issue of non-linear capacitance.

2.1. Intrinsic diode deactivation circuitry

Fig. 2 shows a VSC phase-leg with SJ MOSFETs and intrinsic diode deactivation circuitry using ancillary power devices. The series diodes *Ds* prevent reverse current from flowing into the MOSFETs when they would otherwise be carrying a freewheeling current via their intrinsic diodes. The external diodes D_{ext} in anti-parallel, which replace the function of the intrinsic diodes, can be chosen to have a low reverse recovery charge characteristic [19]-[21]. This paper presents an experimental comparison between different diode deactivation circuits to assess the most efficient of them.

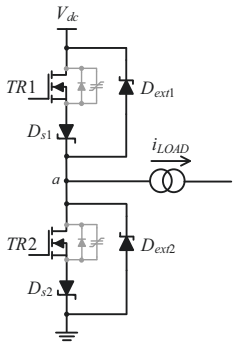
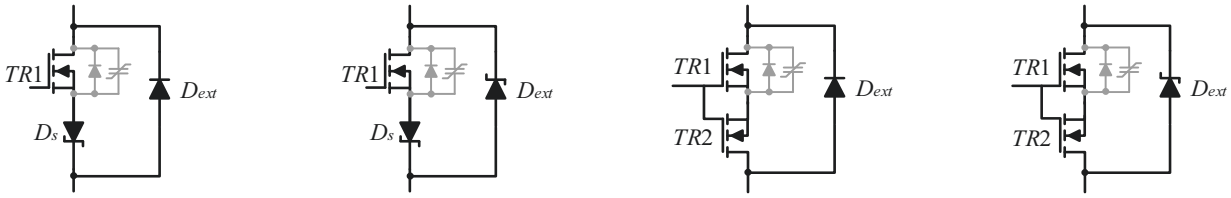


Fig. 2. SJ MOSFETs in bridge-leg with intrinsic diode deactivation circuitry.

2.2. Dual-mode gate-driver circuit

The gate driver circuit from [21] is implemented in this paper, where different gate resistances are used in the slow-switching and fast-switching paths to control the switching speed, thus reducing the losses incurred by the non-linear capacitance issue of C_{oss}. At low load currents, bipolar switching is implemented in the normal way, where TR1 and TR2 are switched complementarily, and the slow-switching mode is selected. At high load currents, unipolar switching is implemented, and the fast-switching mode is selected. This



(a) (b) (c) (d)

Fig. 3. Candidate component permutations for the switch module locations in Fig. 1.

latter mode avoids complete discharge of the C_{oss} of the freewheeling device, thus reducing switching losses in the incoming MOSFET

3. Experimental assessment of alternative phase-leg power device permutations at room temperature

For reducing the losses incurred by the SJ body diode, [19] offers a solution where low-voltage MOSFETs are used as anti-series devices. With a low-voltage MOSFET in the anti-series location, the C_{oss} of the SJ MOSFET is discharged down to the low-voltage MOSFET's breakdown voltage $V_{(BR)DSS}$. Si fast recovery PN diodes or SiC Schottky diodes can be used as anti-parallel devices. The candidate switch module permutations are shown in Fig. 3. In this paper, the study in [23] is extended to a phase-leg operating with an AC output current. Prior to the cryogenic tests, the modules were assessed at RT in the phase-leg in Fig. 1. The devices selected for experimentation and their key RT parameters are shown in Table 2.

Table 2. RT parameters of the selected devices in Fig. 3.

Device	Device specifications
Si SJ MOSFET (TR1 in all modules)	IPW60R041P6
	V_{DSS} = 650 V
	$R_{DS(on)}$ = 41 mΩ (maximum)
Si low-voltage Schottky diode (*Ds* in Modules (a) and (b))	MBR3060PT
	V_{RRM} = 60 V
Si fast recovery FRED diode (Dext in Modules (a) and (c))	DSEI30-06A
	V_{RRM} = 600 V
SiC Schottky diode (D_{ext} in Modules (b) and (d))	SCS220AE
	V_{RM} = 650 V
Si low-voltage MOSFET (TR2 in Modules (c) and (d))	IRFB7546PBF
	V_{DSS} = 60 V
	$R_{DS(on)}$ = 6.0 mΩ (typical)

The phase-leg was run in the inverter mode with V_{dc} = 420 V. Simple sinusoidal PWM was applied. Concerning *TR*1, the modulation depth was set such that it operated between a maximum and minimum duty cycle δ of 0.9 and 0.1. A series-connected *RL* load of 0.8 kVA was supplied. The load was at a power factor *PF* close to one. The controller implemented slow-switching mode for $0.4 < \delta < 0.6$. As the $PF \approx 1$, then i_{LOAD} is known to be in phase with the output voltage and, therefore, average duty cycle. Consequently, the fast-switching mode can be implemented for $\delta < 0.4$ and $\delta > 0.6$ with confidence that i_{LOAD} is not close to zero, and that it is negative or positive respectively. To assess the efficiency of the system, thermal superposition was implemented, and a thermal camera was used to measure the temperature rises of the modules' heatsinks.

Fig. 4 shows the results of the RT experimental comparison. Module (d) has the lowest losses over the frequency range of interest, and this can be attributed to the utilization of low resistance series MOSFET and the fast switching SiC Schottky diode. Module (a) has the worst performance.

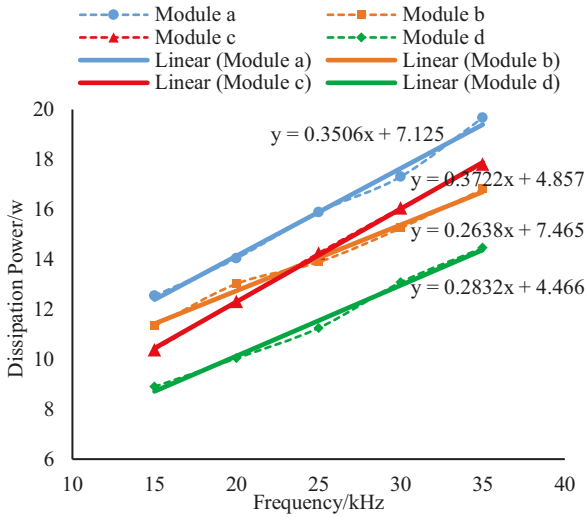


Fig. 4. Losses versus switching frequency for circuits in Fig. 3 are determined by thermal superposition.

Table 3 summarises the comparison results, where costs were based on a survey of available devices in May 2022. Module (c) is the least expensive, however, Module (b) is the most expensive. In terms of efficiency, Module (d) followed by Module (c) are the highest efficiency of all four circuits. From the comparison results aiming with the target of high efficiency in mind, Modules (c) and (d) were selected for further testing at cryogenic temperature.

Table 3. Comparison between four different modules in Fig. 3

Circuit	(a)	(b)	(c)	(d)
Cost	₤₤	₤₤₤₤	₤	₤₤₤
Complexity	>	>	>>	>>
Efficiency	*	**	**	***

4. Experimental assessment of phase-leg circuits at 77 K

In this section, a phase-leg is tested at cryogenic temperature. Even though in [20] a 40-kW NPC circuit utilising SJ MOSFET was tested at cryogenic temperature, the paper has not implemented dual-mode switching at that temperature. Also in the literature, there is little comparison between the performances of different diode deactivation circuits at that temperature. Thus, this section aims to address these issues.

This section starts with a simulation to compare the performance of Modules (c) and (d) in a phase-leg circuit at RT and CT. Afterwards, an experimental rig of these two phase-leg circuits is set up and the testing of devices is done at cryogenic and room temperature to compare the efficiencies

4.1. Simulation of the phase-leg circuit at room and cryogenic temperature

A simulation was built to forecast the performance of a phase-leg at RT and cryogenic temperature. To obtain the parameters to enter into the simulation, data from [23] was extracted for the CoolMOS MOSFET device. As for the SiC Schottky and Si diode, experiments were performed to obtain the forward conduction voltage. In terms of the reverse recovery charge Q_{rr}, both the SiC Schottky and Si fast recovery PN diode have shown no change in the literature, and thus they were assumed to be constant [6], [24], [25].

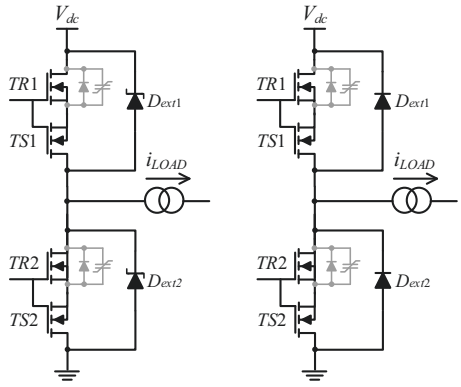


Fig. 5. Candidate cryogenic phase leg permutations. Left: using SiC Schottky diode as D_{ext}. Right: using Si diode as D_{ext}.

Modules (c) and (d) as shown in Fig. 5, were simulated. These modules were chosen as they showed the best performance at RT in Section 3. In Fig. 5, a series Si MOSFET is used with the SJ MOSFET, the only difference is in (a) and Schottky diode is used, whereas in (b) a Si fast recovery FRED is used as the anti-parallel device for both MOSFETs.

MATLAB/SIMULINK software was used for the simulations. For each of the circuits in Fig. 5, two simulations were run, one for RT and one for CT. In all of the simulations, the input and output voltages and currents were measured to calculate the efficiency of the phase-leg at room and cryogenic temperatures. The simulations were run at power levels of 250, 500, 750 and 1000 W, and frequencies of 15, 20, 25, 30 and 35 kHz. The results are presented in Figs. 6-9. From these figures, it can be deduced that the performance of both circuits improves with the decrease in temperature.

The improved efficiency of the circuitry in the simulation can be mainly attributed to the fact that the SJ MOSFET's on-state resistance has significantly decreased with the decrease in temperature. Even though both antiparallel diodes' forward voltages have increased at cryogenic temperature, the overall efficiency still increased. The difference in the efficiencies between the room and cryogenic temperature is more apparent at larger power levels. The SiC diode has shown better performance as both the aggregate of the switching and the conduction losses for the SiC diode are lower than that of the Si diode. In the next section, the phase leg is set up experimentally to validate the simulation results.

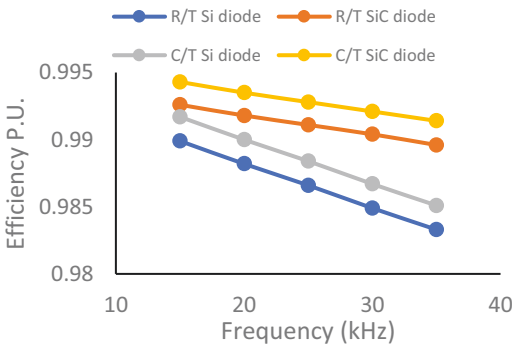


Fig. 6 Simulation results for the circuits in Fig. 5 at 1000 W output power at RT and CT.

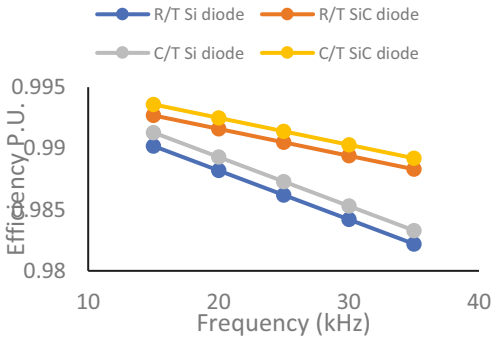


Fig. 7. Simulation results of the circuits in Fig. 5 at 750 W output power at RT and CT.

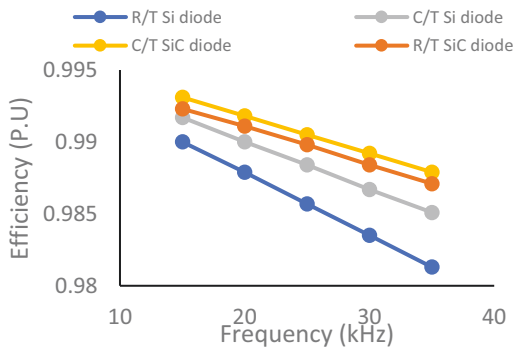


Fig. 8. Simulation results of the circuit in Fig. 5 at 500 W output power at RT and CT.

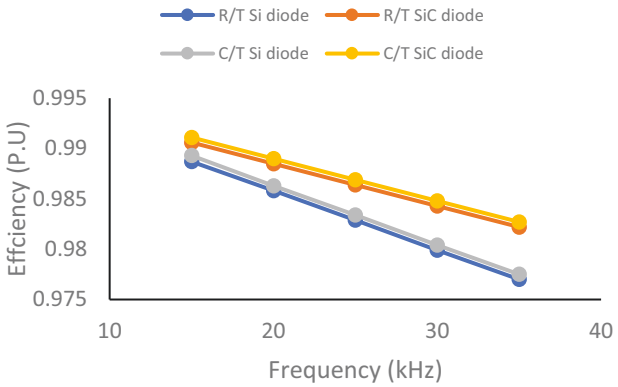


Fig. 9. Simulation results of the circuits in Fig. 5 at 250 W output power at RT and CT.

4.2. Cryogenic experimental rig and results

Following the simulations, an experimental rig for a phase-leg was built for testing at cryogenic temperature. As mentioned earlier, [20] was able to test an NPC that utilizes SJ MOSFET with an intrinsic diode deactivation circuit. However, this paper compares different diode deactivation circuits for the SJ MOSFET at CT, and also implements dual-mode control at that temperature. Using the previously built phase-leg [23] seen in Fig. 5, some adaptations were applied to obtain an AC output signal.

The experimental circuit, Fig. 10, was constructed and cryogenically tested by immersing it in liquid nitrogen (LN2). The drain-source breakdown voltage of SJ MOSFETs tends to drop by 20% at CT [6]. To operate the SJ MOSFET within a safe region Vdc was set at 270 V, lower than the 420 V used for the tests in Section 3. Two 50-µF 450-V polypropylene capacitors in parallel were used for local supply voltage decoupling. This capacitor type has shown reliable performance at 77 K, where its capacitance value does not change significantly [6]. The gate driver circuit was located remotely and was not submerged in the LN2, hence the lengthy gate driver connections. As mentioned in [23], applying a tightly-controlled gate-source voltage is challenging due to the stray inductances introduced with this arrangement. However, the gate-source junction of the Si MOSFET is tolerant of a wider voltage range than is the case with SiC or GaN devices. Furthermore, the gate-source threshold voltage $V_{GS(th)}$ of Si MOSFETs typically rises by 15% [6] when the device is cooled from RT to 77 K, yielding higher noise immunity.

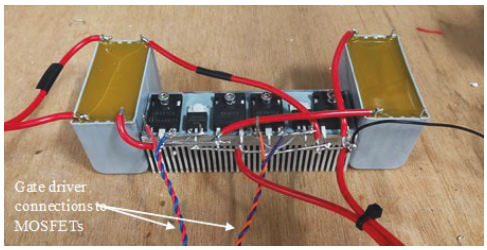


Fig. 10. Phase-leg used for cryogenic testing [23].

The circuit in Fig. 10 was connected as shown in Fig. 11 and run at a modulation index of 90%. The switching of SW1 and SW2 was done in the same manner as in Sections 2 and 3.

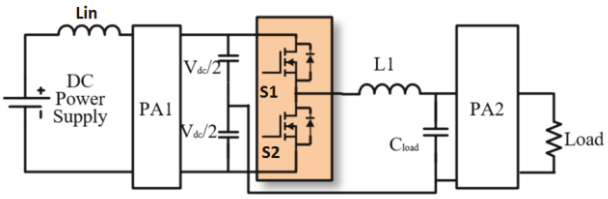


Fig. 11. Electrical test connections. Positions S1 and S2 in the bridge leg are each occupied by Module (c), and then by Module (d) in Fig. 3.

As seen in Fig. 11, two PM100 power analysers, PA1 and PA2, were used to measure the input power and output power. An input inductor Lin was included to reduce the high-frequency ripple current drawn from the supply, and thereby enable a more accurate input power measurement to be obtained from PA1.

Initially, the circuit was run at RT before immersing it in LN2 for cryogenic testing. Plots of efficiency against switching frequency with Vdc = 270 V at both RT and CT are shown in Figs. 12-15. Importantly, it is noted that, unlike the measurements in Section 3, losses in the 1-mH output choke inductance (L1) are included here. The phase-leg was tested at loads of 250, 500, 750 and 1000 W. The performance of the circuit using the Si diode improves at CT. However, the highest efficiencies are attained when a SiC diode is used at CT which validates the simulation results that this is the best performing circuit.

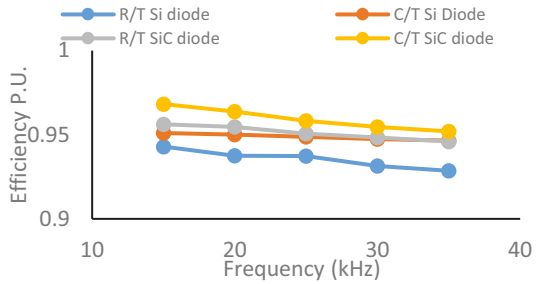


Fig. 12. Efficiency against switching frequency at RT and CT for 1000 W.

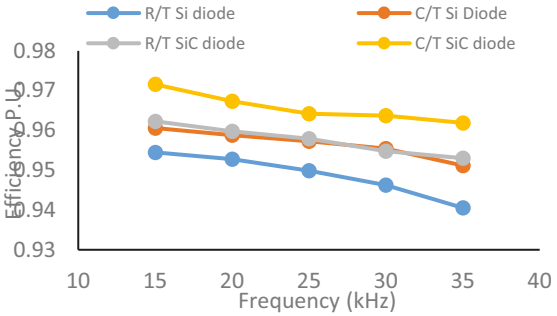


Fig. 13. Efficiency against switching frequency at RT and CT for 750 W.

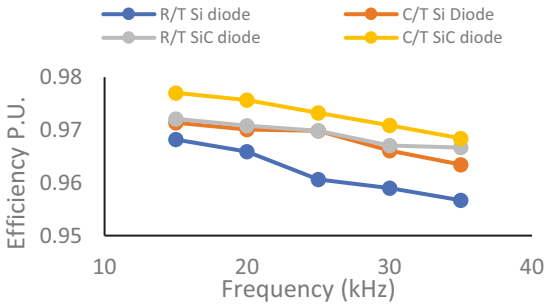


Fig. 14. Efficiency against switching frequency at RT and CT for 500 W.

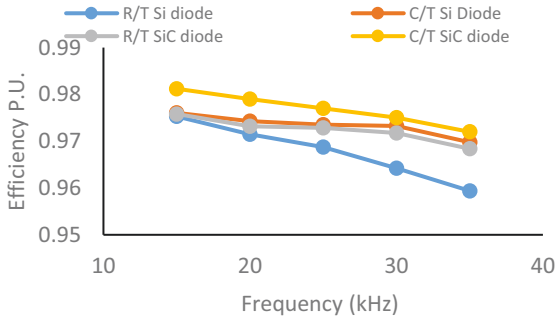


Fig. 15. Efficiency against switching frequency at RT and CT for 250 W.

5. Discussion

As expected from the literature, the performance of the phase leg at cryogenic temperature has improved efficiency compared to room temperature. This is mainly attributed to the decrease of the SJ MOSFET's on-resistance. The difference in the efficiency between the two temperatures becomes less pronounced at higher loads; mainly due to the larger current emphasising the conduction losses more.

The power semiconductor losses at RT were ascertained in Section 3 by using thermal superposition for a more accurate assessment. This is relatively simple to do at RT, but becomes more challenging when immersed in LN2. A feature of loss measurement using the power analyser method is that the choke loss is included. For experimental purposes, the devices being tested were in standard TO-247 and TO-220 packages, and appropriate packaging for low temperatures would normally be needed.

It is highlighted that there are discrepancies between the efficiencies calculated from the simulation and the ones extracted from the experiment, Fig. 16 shows the difference between the simulated and the measured efficiencies of the phase leg at cryogenic temperature while using the SiC Schottky diode at 1000 W. These can be mainly due to 1) measurement accuracies, 2) losses in the choke, 3) large ripple components in current waveforms, especially at lighter loads and lower switching frequencies.

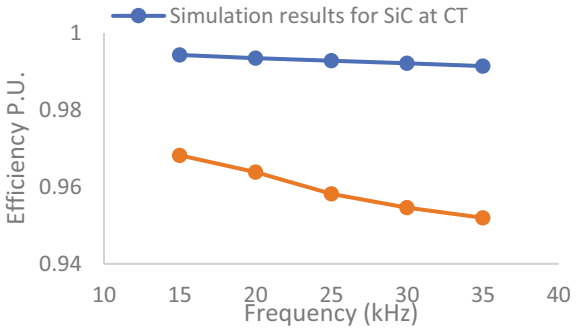


Fig. 16. Efficiency against switching frequency at CT showing experimental versus simulation results at cryogenic temperature for 1000 W.

6. Conclusion

A two-level voltage source converter phase-leg designed around SJ MOSFETs has been tested at room temperature and cryogenic temperature of 77 K. To address the problems presented by the MOSFET's intrinsic diode and output capacitance, ancillary power components are used in conjunction with a bespoke control technique. Four different permutations of ancillary components are experimentally evaluated at room temperature. Based on the results, two permutations were selected for further evaluation at room temperature and at 77 K. Both the simulation and experimental results have shown the usage of SiC Schottky diode for reverse recovery of the phase-leg exhibits lower losses than using a Si diode at cryogenic temperature.

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