Iberdrola Innovation Middle East &

University of Strathclyde

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Distributed ReStart: Non-conventional Black-Start Resources

RTDS Based Network Energization from Grid Forming Converters: Part 2

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GENERAL NOTES

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CONTENTS

1. Introduction

This report summarizes the results achieved in investigating the use of grid-forming converters (GFC) control for black-start applications, as part of the Distributed ReStart project collaboration between SPEN and Iberdrola Innovation Middle East. The experiments reported here are carried out in collaboration with the state-of-the-art Dynamic Power Systems Laboratory (DPSL) at the University of Strathclyde.

The previous deliverable, published as Chapter 9 of "Power Engineering Trials Demonstration of Black Start from DERs Live Trials Report Part 1 - December 2021" report, demonstrated the use of a modified virtual synchronous machine (VSM) grid-forming control to energize networks simulated in a real-time digital simulation environment. The energized networks ranged from simplified test networks to segments of the Chapelcross network. Results demonstrated successful energization using a voltage ramp with significantly mitigated transformers inrush current, as well as block loads pickup and grid synchronization. Preliminary results were also presented to test power hardware in the loop (PHiL) technique capabilities, where a hardware GFC is used to energize a simulated network in a real-time digital simulation environment such as the Real-Time Digital Simulator (RTDS).

This report builds on the results presented earlier, and expands them to extended PHiL tests and investigations through a complete black-start scenario that successfully demonstrates the hardware GFC use for network energization. This paves the way for similar experiments in the future that allow for repetitive and non-destructive testing of hardware grid-forming converters through a hybrid environment that takes into account practical aspects such as communication delays and limitations existing in the real network, while allowing for testing black-start scenarios in different simulated network configurations and connections. Key limitations of PHiL technique are also identified in the report for reference. Finally, the GFC control used throughout this report is illustrated in Figure 1, where its main functionalities are soft energization, voltage support and grid synchronization capabilities.

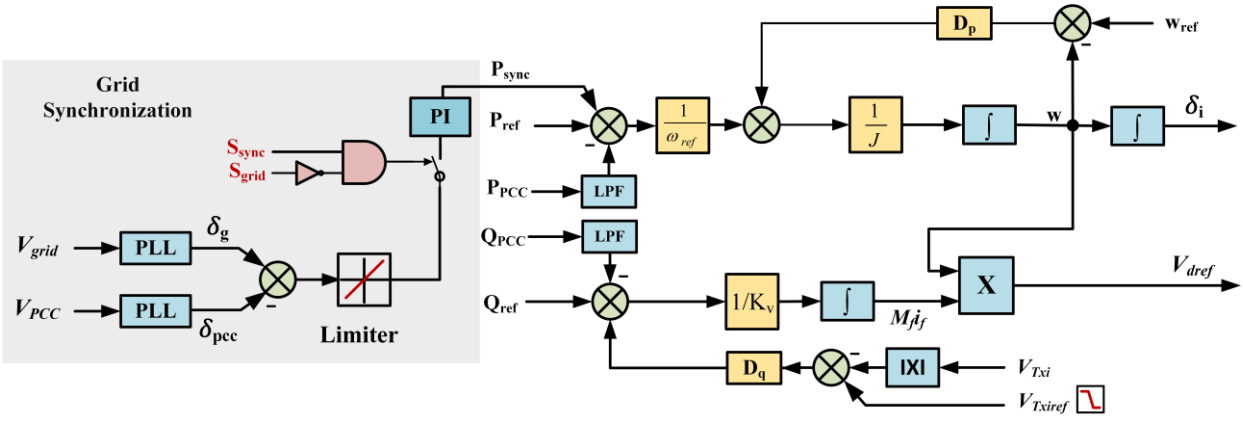

Figure 1: High-level VSM control block diagram for the GFC loop used in this study.

2. Test Network: Overview & Parameters

Black-start service provision through grid-forming converters is validated in this study through a simplified test network that consists of the energizing converter, interface transformer, transmission line, loads and a grid connection point for post black-start synchronization. The network block diagram used is illustrated in Figure 2. The components are selected to reflect a common configuration in distribution networks, and to be closely correlated to the Chapelcross network in Scotland. For instance, the used transformer model maintains the same parameters from the Chapelcross RSCAD model developed at The National HVDC Centre [1], with a similar 53 MVA rating and saturation characteristics. A π-section line is also used with default MATLAB/Simulink library RLC parameters. The network loads are divided into a main (initially closed) 20 MW load, and a 10 MW disturbance load. The VSM control utilizes inertia and damping factors that maintain minimum frequency variations at rated power disturbances. Inner voltage and current loops are integrated in all the experiments presented in this report. For the PHiL test, the hardware part of the network (converter & LC filter) and the real-time simulated software part (L_2 and rest of the network) are highlighted in Figure 3.

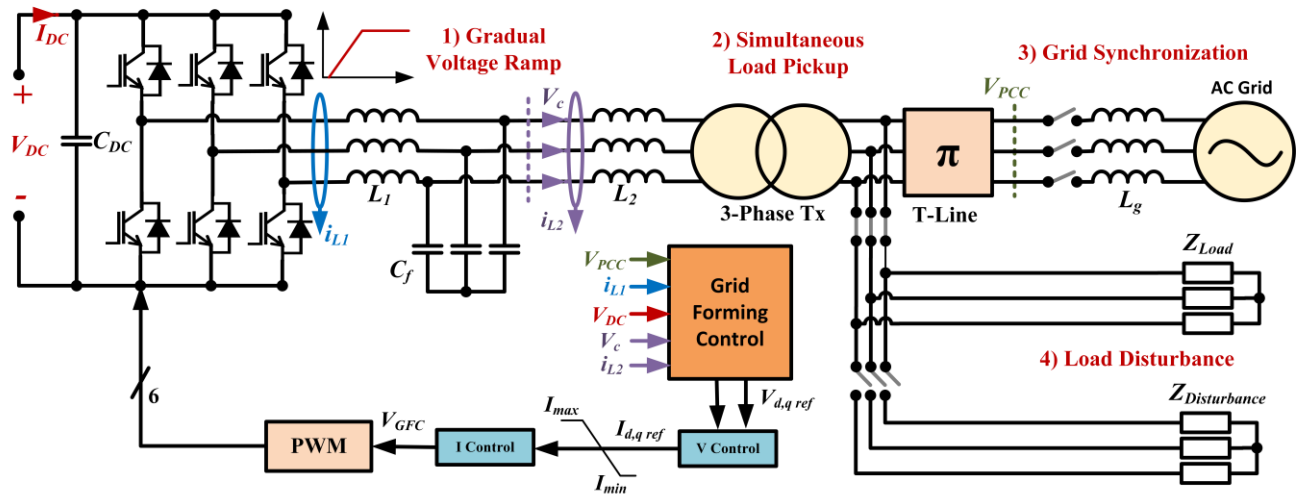

Figure 2: Test network block-diagram used for black-start experiments.

The main test network parameters are summarized in Table 1. It should be noted that the converter MVA rating is selected to resemble a value close to operating steady-state conditions. Whereas this rating can be decreased when combined with appropriate energization techniques if its main purpose is to perform black-start.

To mitigate transformer and line energizing inrush currents, a soft energization technique is used with a ramp duration of 10 seconds. This ramp duration can be shortened (or prolonged) depending on the network and transformer conditions. A study on the ramp-rate influencing factors by the authors is reported in [2]. Local load pickup (20 MW) is performed simultaneously to the transformer and line energization. Considering that load energization through a ramping voltage may not be compatible with all load types, the loads requiring 1 pu voltage supply for connection are integrated at a later stage as a disturbance. Grid synchronization is performed

using the modified controller in Figure 1, where it aims to drive the phase angle difference between point-of-common-coupling (PCC) and grid voltages to zero. Beyond synchronization, the grid-forming VSM continues to operate in voltage-control mode and capable of reactive power injection/absorption as a possible ancillary service. The VSM maintains the voltage required to exchange power with the grid after synchronization (i.e., power tracking mode) within its rating and capabilities.

Table 1: Key Test Network Parameters.

Grid-forming Converter Ratings			
Power Rating	40 MVA	Output Voltage	11 kV_{LL}
Transformer Parameters ($\Delta - Y$)			
Power Rating	53 MVA	Voltage Ratio V_o/V_i	$33/11\ kv$
Knee-Voltage	1.25 pu	Air-core Inductance	0.265 pu
Steady-State i_m	1%	Phases Residual Flux	[0.25, -0.1, -0.15] pu
Transmission Line Parameters ($\pi - model$)			
(R, L, C) per km	12.73 $m\Omega$, 0.93 mH, 12.74 nF	Length	30 km
Network Loads			
Main Load	20 MW	Disturbance Load	10 MW
Grid Parameters ($33\ kV_{LL}$)			
Short-Circuit Power	500 MW	X/R Ratio	14.5

The modified VSM capabilities were demonstrated in MATLAB/Simulink and RTDS simulations in previous reports and studies [1, 3, 4] Whereas here, the control is implemented using a scaled hardware grid-forming converter (typically with kW rating), which is interfaced to the simulated network in Figure 2 through a power amplifier. The network itself is simulated in RTDS (with MW ratings) and is used to receive and supply references to the external converter and power amplifier in a closed-loop configuration. A complete black-start scenario including energization, loads connection and grid synchronization is executed in this configuration. The following section provides more description of the used PHiL interface technique.

3. Power Hardware in the Loop

Power hardware in the loop simulation, as an advanced real-time simulation methodology, has been extensively leveraged for the repeated and non-destructive experimental assessment of emerging power apparatus [5]. Figure 3 presents the equivalent circuit diagram of the PHiL setup that consists of a real-time emulated network to be energized by GFC, and a current-mode power amplifier that is coupled with the GFC power converter. A current-type (I-ITM) interface is utilized to define the PHiL configuration in this study.

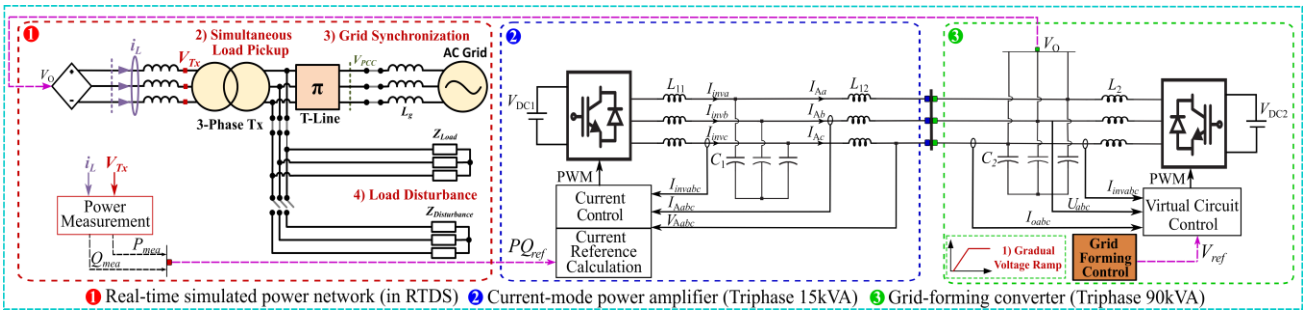

Figure 3: Equivalent circuit diagram of the PHIL setups.

The power amplifier source or sink current to the GFC under test and the GFC output voltage is transmitted to the software side as a reference value that energizes a controllable voltage source inthe real-time simulated network. By doing so, the GFC is incorporated into the closed-loop configuration with its power behaviors replicated in the simulated network while the dynamics at the GFC interfacing point in the simulated network are also replicated to the hardware GFC.

Figure 4 shows the configuration of the experimental setup with its cells corresponding to these as illustrated in Figure 3. Grid forming control schemes are implemented in Triphase 90kVA (TP90kVA) power converter to regulate its output voltage, which is utilized by Triphase 15kVA (TP15kVA) for output current regulation through a Phase-Locked Loop (PLL) unit. The voltage and power signals transmission are realized by the Aurora protocol and Giga-transceiver analog output (GTAO) card in RTDS.

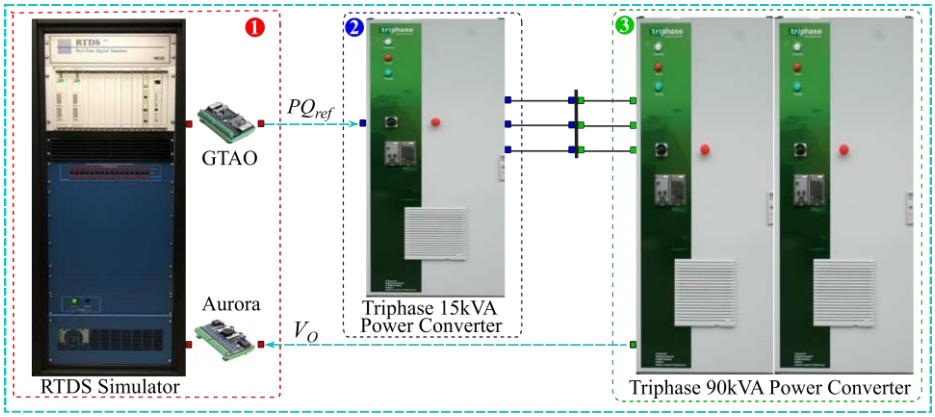

Figure 4: PHIL experimental setup representation.

Due to the limited voltage levels of the TP90kVA converter, a voltage scaling ratio ($v_{scale} = 27.5$) is employed to scale up the TP90kVA output voltage to a higher level to enable MW-scale emulation in the real-time simulated network. In terms of the current replication by TP15kVA, the scaled-down active and reactive power readings from RTDS ($P_{scale} = 4125$) are transmitted to the power amplifier interface to improve P/Q tracking accuracy and mitigate the impact of small phase drifts. These measurements are then converted to scaled current references when divided by the TP90kVA voltage that is also applied at TP15kVA terminals. The active and reactive power scaling ratio scales down the calculated current reference within the constraint of TP15kVA

($i_{scale} = 150$). This established interface leads to a closed-loop dual system operation in hardware and software, where the hardware feeds the voltage reference into the software and receives back a current or power reference. The voltage and power signals transmission are realized by the Aurora protocol and the Giga-transceiver analog output (GTAO) card in RTDS, respectively.

4. PHiL Results

The results presented in this section show a combination of hardware and software results obtained from the black-start experiment. Initially, the grid-forming VSM implemented in TP90kVA unit is activated with a 10 seconds voltage ramp between 0 and 325 V_{peak} (400 V_{LL} equivalent). This voltage is sensed and sent to RTDS, and scaled up by 27.5 to represent 8981 V_{peak} (11 kV V_{LL} equivalent). The scaled-up voltage is fed into the RTDS simulation network to energize the 53 MVA transformer, line and 20 MW load. Then the restored island is synchronized to the grid after the angle error is driven to zero, followed by power reference variation and a load disturbance. The synergy in trends between hardware and software sides is illustrated here, starting by GFC output voltage waveforms as illustrated in Figure 5.

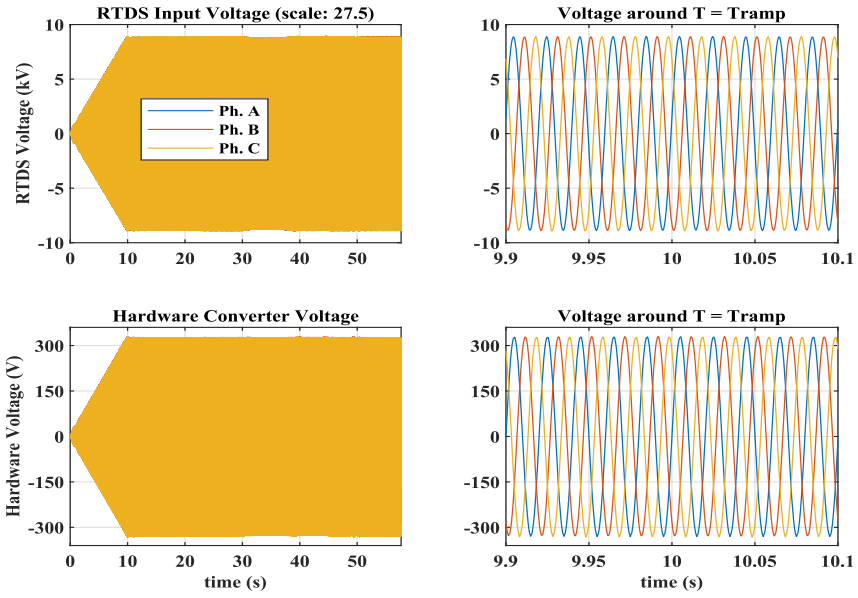

Figure 5: RTDS vs. Hardware Input Voltage Measurements.

After the voltage ramp is completed at t = 10 s, the synchronizing control continues to operate to drive the synchronizing voltages phase difference to zero, and the smooth grid-connection takes place around t = 22.75 s. After synchronization is done, the VSM tracks the power reference which is initially set to 20 MW (equivalent to pre-synchronization load demand) to avoid sudden jumps. At t = 29.75 s (after 7 seconds), the power reference ramps to 35 MW using a 7.5 MW/s slope. After 7 seconds, the reference is ramped down with a similar slope to 10 MW, before ramping up again to the initial 20 MW point around t = 43.75 s. Finally, a load disturbance

is applied at t = 48.75 s where an additional 10 MW load is connected ($Z_{disturbance}$ in Figure 2. The impact of these events on both hardware and RTDS VSM currents is illustrated in Figure 6, where similar trends can be observed between the RTDS input current and the measured hardware converter current, showing successful reference tracking and coordinated operation of both hardware and software using PHiL.

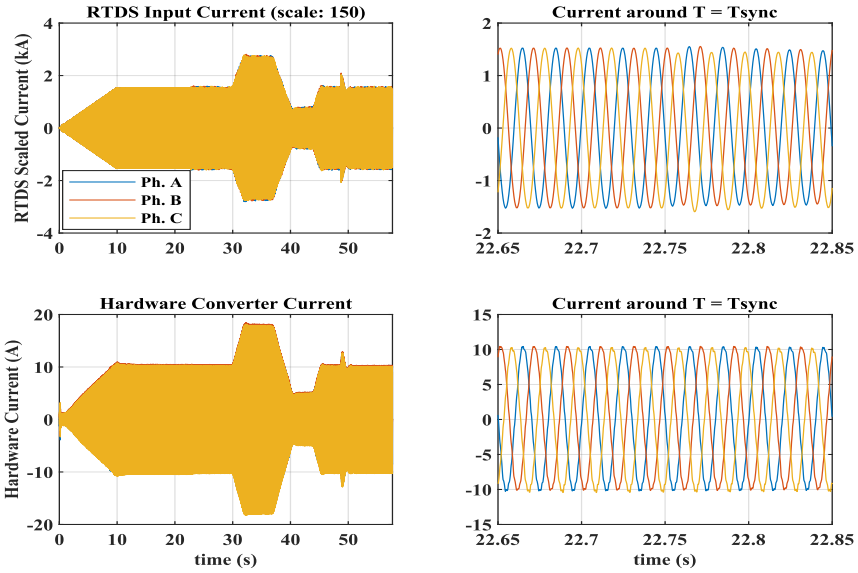

Figure 6: RTDS vs. Hardware Input Current Measurements.

The software vs. hardware active and reactive power tracking performance is also benchmarked for the PHiL application as illustrated in Figure 7. For this comparison, the hardware power is scaled up by 4125 to match the RTDS network power scale. The illustrated P/Q traces are passed through low-pass filters. The same filtered measurements are used for the VSM control power and voltage loops. The power reference tracking performance is satisfactory between hardware and software, with the applied time TP15kVA time-delay compensation of around 94 μs.

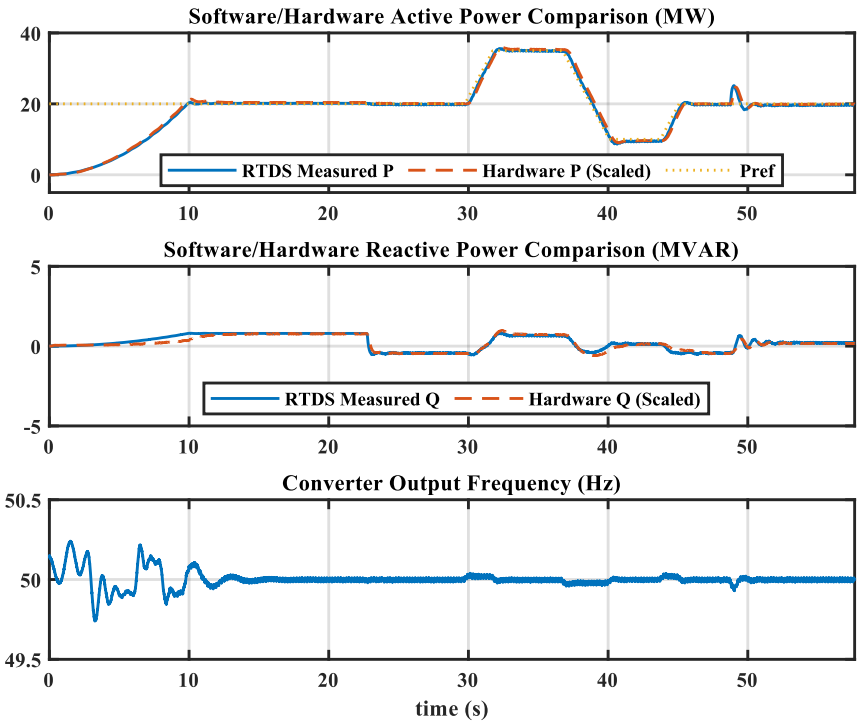

Figure 7: PHiL Active and Reactive Power Tracking Performance (Software vs. Hardware), and GFC frequency.

Figure 7 also illustrates the VSM voltage frequency trace throughout the simulation, showing slight variations around the steady 50 Hz points during the ramp and synchronizing control action, and small changes as a result of the power reference adjustments. The converter output voltage frequency value remains within an acceptable band throughout the experiment.

Finally, the synchronizing control action is also illustrated in Figure 8. The control is activated during the ramp to accelerate the phase-matching. Initially, an evident phase-shift is observed. As the synchronizing PI control tracks the zero-angle point error, the phase-angle between PCC and grid voltages approaches zero. The second panel shows both voltages around the moment of controlled synchronization, where the process is done smoothly. From here, the power exchange between the VSM and the grid is initiated following the VSM power reference. It is worth noting that the implemented synchronization technique requires access to the phase angle error at the PCC, which can be sent using high-speed communication infrastructure to the VSM control. Alternatively, synchronizing relays can be used when the system is ready to go into grid-connected mode. Overall, a successful black-start demonstration through PHiL has been presented in this report, showing the technique capabilities and potential. The next section identifies some of the lessons learned from these experiments, highlighting some PHiL limitations and points to be considered for testing.

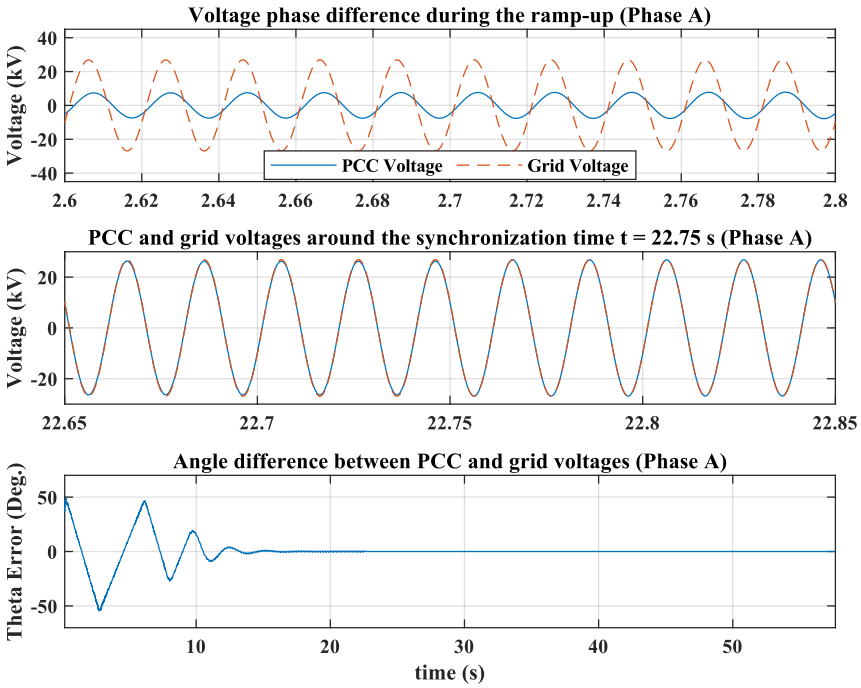

Figure 8: Synchronizing control impact in reducing the phase shift between PCC voltage and grid before synchronization.

5. Lessons Learned

This section summarizes the lessons learned from PHiL and GFC experiments and aims to provide some tips and tricks for readers interested in working on similar experiments.

- PHiL-GFC Control Implementation: Two options can be adopted to implement the GFC control. a) in the RTDS itself, where all the control functions are performed there, and the output reference is then sent for the hardware converter to replicate and share back with the RTDS software to drive its scaled voltage source. b) directly in the external hardware converter through its dedicated software interface (e.g., MATLAB/Simulink, dSPACE or a vendor specific software). Both options were investigated, and it is found that direct control implementation in the external hardware provides improved performance as it directly utilizes hardware measurements and mimics the realistic case since vendors typically implement the control software in the converter itself.
- PHiL Time-Delay Compensation Impact: Appropriate compensation of the communication links time-delay is essential for proper PHiL operation. Different compensation magnitudes were tested as part of this study (e.g., between zero and 180 degrees), and the impact of improper delay compensation is evident in terms of deviation in active and reactive power readings, which can cause more adverse tracking issues when combined with grid synchronization. Large mismatches in real-networks may lead to accuracy deviations, and in some cases, even stability issues especially when the communication signal is used for sensitive parameters control.

- PHiL Network Impedance and Ratios: It is observed that the nature of network impedance impacts the PHiL performance under certain conditions (e.g., grid-synchronization). Selecting an inductive impedance for appropriate power transfer between the GFC and the grid was observed to increase the system power tracking accuracy. Selecting proper voltage and current scaling ratios is also observed to impact stability. Further investigation is recommended on these points to generalize the observed trends.
- Unbalanced Reference Replication Capability: In I-ITM interface technique, the power amplifier receives its current reference from RTDS. In black-start and network energization studies, inrush currents are likely to be involved in some scenarios, which means the current reference can be highly unbalanced and rich in harmonics due to the inrush current nature. If the physical power amplifier control is unable to replicate this reference due to its implemented control, then the hardware will not be able to track currents that correspond in shape to the irregularities generated in RTDS, and the hardware VSM will not see similar conditions to that in RTDS. Understanding the control type implemented in the power amplifier interface thus becomes important if accurately studying such phenomenon is of an experimental interest.
- Impact of VSM tuning on tracking accuracy: The selection of VSM damping and virtual inertia parameters influence the control performance against disturbances. Proper tuning is required to maintain fast frequency response after any disturbance, while also being able to track the power references in grid-connected mode. The damping and inertia parameters should thus be balanced to take both objectives into consideration.

6. Remarks

Being one of the first attempts in the literature to investigate the use of PHiL technique for grid-forming converters testing in black-start, the results presented in this report serve as a reference to showcase the potential of using power hardware in the loop for network energization tests. The experiments demonstrated a successful PHiL utilization, allowing an external hardware converter to interact with and energize a simulated blacked-out network in a complete scenario. The scenario included transformers energization, loads pickup and grid-synchronization. This preliminary testing success paves the way to more extensive testing that can utilize industrial-scale converters in similar environments under appropriate software/hardware scaling ratios. These converters can then be tested under different network configurations, without being restricted to a particular network topology, while also being exposed to communication delays and limiting conditions that would exist in real networks.

That said, PHiL technique limitations should also be considered, such as using a power amplifier interface that is able to replicate unbalanced and/or harmonics-rich current references received from RTDS. PHiL stability margins is another important identified point that is impacted by factors such as simulated network impedances and scaling ratios. Understanding such sources of error is important for accurate behavior replication between software and hardware, and for accurate results interpretation in relation to the studied phenomenon.

From an application standpoint, the main study objective was to investigate networks energization with minimum inrush current during black-start from grid-forming converters. The modified VSM control implemented in the hardware converter was able to achieve this aim through applying soft energization. The soft-ramp voltage duration is an important factor to consider to avoid fast ramps that can still lead to significant inrush. Combining this aspect with PHiL allows for testing the hardware converter capability under different ramp speeds and ancillary services provision requirements. Expanding the presented results into larger network simulations should, in principle, be feasible with similar methodology to the one presented in this report.

Recommended routes for relevant future PHiL research include investigating different disturbances such as various active and reactive load combinations, or the use of multiple converters (e.g., from a wind farm) for black-start PHiL testing and synchronizing between a larger number of network segments.

7. References

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