Current-Type Power Hardware-in-the-Loop Interface for Black-Start Testing of Grid-Forming Converter

Zhiwang Feng$^1$, Abdulrahman Alassi$^{1,2}$, Mazheruddin Syed$^1$, Rafael Peña-Alzola$^1$, Khaled Ahmed$^1$, and Graeme Burt$^1$

$^1$ Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom
$^2$ Iberdrola Innovation Middle East, Doha, Qatar
Email: {zhiwang.feng, a.alassi, mazheruddin.syed, rafael.pena-alzola, khaled.ahmed, graeme.burt}@strath.ac.uk

Abstract—Grid-forming converter establishes a stable and controllable voltage at its output terminal without requiring external angle reference, which enables the GFC to be a candidate for providing black-start services. However, this attribute poses significant challenges to the conventional power hardware-in-the-loop (PHIL) simulation, which incorporates the physical power converter by regulating its voltage angle to be synchronized with that of an interfacing power amplifier mimicking the real-time emulated power grid. The lack of voltage synchronization at the coupling point of GFC and interfacing power amplifier leads to instability. To address this challenge, the current-type interfacing method with compensation and scaling scheme is proposed to interface a GFC with soft black-start capability into a PHIL setup. Analytical assessment and experimental results involving interfacing a 90 kVA power converter implemented with grid-forming control are presented to verify the methodology.

Index Terms—Power hardware-in-the-loop (PHIL), grid-forming converter, soft black-start, current-type power interface.

I. INTRODUCTION

Power converters used for the grid-connection of key distributed energy resources (DERs) such as solar PV, wind turbines and battery systems are typically operated in grid-following mode. The converter in this case latches to a strong grid voltage using a phase-locked-loop (PLL) and acts as a current source exchanging active and reactive power [1]. That said, the increasing DER penetration is necessitating a review of this classical paradigm to exploit the power converters grid-support and restoration capabilities. The use of grid-forming converters (GFC) is gaining high research and industrial traction due to the wide range of associated benefits [2]–[4]. One of the key benefits of operating converters in grid-forming mode stems from the name, i.e., due to its ability to ‘form’ a grid by generating its own AC voltage without the need of an external PLL. This makes it an attractive option to participate in black-start applications [5]–[8].

Comprehensive and in-depth investigations of the dynamic limitations of the candidate GFC controls schemes designed for black-start service provision under a broad spectrum of operating conditions are crucial prior to their final deployment and systemic application in the power industry. For this reason, the application of power hardware-in-the-loop (PHIL) simulation for GFC testing has attracted significant interest from academic researchers and industrial engineers. PHIL incorporates a real-time emulated network and hardware power converter into a closed-loop setup, which enables repeated and non-destructive testing of the dynamic behaviours of the candidate power converter or control strategies. This can be adopted for the GFC testing to address the computation limitations of pure software simulation and de-risk the hardware experiments in a more realistic manner.

The voltage-type PHIL simulation setup has been extensively employed for the real-time testing of grid-following converters. The grid-following converters regulate their voltage angle to be synchronized with that of the interfacing voltage-type power amplifier (i.e., a grid simulator) by employing a dedicated synchronization unit (e.g., a PLL) [9]–[13]. However, the voltage-type interface is not capable of incorporating a GFC in the PHIL setup for black-start testing. GFC regulates output voltage by using the angular frequency reference generated by its internal dedicated unit. The direct coupling of the GFC and interfacing power amplifier may lead to stability issues arising from their independent and inherent voltage regulation and the lack of voltage angle synchronization at their coupling point. To address this issue, a physical linking impedance insertion and a digital-twin emulated impedance based interfacing method was proposed in [14]. The applicability of this method is limited by the availability of the physical impedance and the necessity of precise power measurement before enabling the closure of a physical contactor. Furthermore, the accuracy of this setup is highly dependent on the consistency between the physically inserted linking impedance and the emulated impedance on the simulation side.

To address these limitations of the conventional voltage-type interfacing method and the interfacing method developed in [14], the current-type interfacing method is proposed to incorporate the GFC into a PHIL setup for black-start testing. Scaling and compensation schemes are developed for a robust and high-fidelity PHIL simulation guaranteeing an accurate replication of the dynamics of the emulated power network at the physical GFC interfacing point. To support its adoption, stability analysis of this PHIL setup is presented.
This paper is organized in the following way: Section II presents an overview of GFC control techniques to support black-start service provision. The proposed current-type PHIL setup is presented in Section III, detailing the topology, system modelling, scaling, delay compensation, and stability analysis. In section IV, analytical assessment and simulation results are presented to verify the proposed interfacing method. In Section V, experimental results are presented to demonstrate the applicability of the interfacing method. Section VI concludes this paper and recommends future directions for research.

II. GRID-FORMING CONTROL TECHNIQUES

An anchor black-start source is required to energize network segments, connect to loads, and in some cases synchronize to neighboring networks. Network restoration typically involves power transformers energization, a process that can cause very high inrush currents, up to 7-10 times the transformer rating [15]. On the other hand, power converters are also known for their limited overcurrent capabilities. Using GFCs for large transformers energization should thus be combined with inrush current mitigation techniques.

Given the GFCs voltage control flexibility, soft transformer energization technique can be integrated into the voltage control loop. This can be achieved through adjustment of the voltage reference to a ramp between 0 and 1 pu within a suitable duration that results in inrush current mitigation [7]. A sample scenario incorporating voltage ramp for black-start using a voltage source converter is shown in Fig. 1(a), and the corresponding GFC control diagram based on the virtual synchronous machine (VSM) is illustrated in Fig. 1(b). This control technique emulates the swing equation of a synchronous machine as in [16]:

\[
J \frac{d\omega}{dt} = \frac{1}{\omega_{ref}} (P_{ref} - P) + D_p (\omega_{ref} - \omega)
\]

where \( J \) is the virtual inertia, \( D_p \) is the damping factor, \( \omega_{ref} \) and \( \omega \) are reference and measured angular frequencies, with similar analogy for the active power \( P \). The VSM voltage loop is inspired by the synchronous generator (SG) analogy as:

\[
|V| = \frac{\omega}{K_v} (D_q \Delta|V| + \Delta Q)
\]

where \( 1/K_v \) is the integrator gain, \( D_q \) is the voltage damping factor, \( \Delta|V| \) and \( \Delta Q \) are the voltage magnitude and reactive power errors, respectively. Finally, when soft energization is used, the voltage reference is defined as:

\[
|V_{ref}| = \begin{cases} \frac{t}{T_{ramp}} |V_{nom}| & t < T_{ramp} \\ |V_{nom}| & t \geq T_{ramp} \end{cases}
\]

where \( T_{ramp} \) is the ramping time, \( t \) is the elapsed time since ramping initialization, and \( V_{nom} \) is the desired steady-state voltage amplitude.

Loads connected at the point of common coupling (PCC) can be energized with the same voltage ramp, or after a 1 pu voltage is established at the PCC. The former technique is applied in this paper while taking into account the sensitivity of some load types to a ramped voltage startup as reported in [6]. Overall, robust system response to disturbances and transients is crucial for a successful black-start process. During the network energization sequence, the GFC output voltage is controlled by following the amplitude and angular frequency setpoints generated by the grid-forming control loop.

III. STATE-OF-THE-ART OF PHIL SYSTEM

A. PHIL System Topology

Power hardware-in-the-loop simulation combines the real-world physical hardware and the digital real-time simulation system into a closed-loop setup emulating a monolithic system of interest (SOI) as in Fig. 2(a) (representative of network such as the simplified power network in Fig. 1(a)). As illustrated in Fig. 2(b), the monolithic SOI that is represented in the form of a lumped voltage divider topology in Fig. 2(a) is divided into two cascaded subsystems \( S_1 \) and \( S_2 \). System \( S_1 \) represents the emulated power network in the digital real-time simulator and comprises a Thévenin equivalent voltage source \( V_S \) cascaded with an equivalent impedance \( Z_1 \). System \( S_2 \) represents the grid-forming converter that is modelled as a voltage source in series with an output impedance \( Z_2 \).
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As shown in Fig. 2(b), systems $S_1$ and $S_2$ are coupled through a dedicated power interface that consists of a power amplifier, sensors, and signal conversion units (i.e. Giga-transceiver analogue output (GTAO) card, Giga-transceiver analogue input (GTAI) card, and Aurora protocol). The configuration of these components and the signal transmission manner among the systems $S_1$ and $S_2$ are defined by the interface algorithms (IAS) [17], among which the ideal transformer model (ITM) interface has been extensively adopted for its simplified structure and acceptable stability and accuracy.

B. Ideal Transformer Model Interface

Distinguished by the power amplification mode and the types of the controllable power source in simulation side, ITM interface can be classified into voltage-type and current-type.

As shown in Fig. 3, a voltage-type ITM interface is configured as a voltage-mode power amplifier that is coupled with hardware and a controllable current source on the software side. This setup has been extensively employed for grid-following converter testing, in which the converter under test regulates its current to be synchronized with the power amplifier output voltage [9], [12]. However, owing to the inherent voltage amplitude and angular frequency regulation of GFC, this setup is not suitable for interfacing GFC into a PHIL setup. The direct coupling of GFC and voltage-mode power amplifier leads to instability stemming from the lack of voltage synchronization at their coupling point.

On the contrary, a current-type ITM interface is configured as a current-mode power amplifier sinking or sourcing current to the coupled hardware and a controllable voltage source on the software side. Fig. 4 illustrates the equivalent circuit diagram of the PHIL setup comprising a real-time emulated power network, current-mode power amplifier, and power converter implemented with grid-forming control. The inductive filter of the current-mode power converter tackles the voltage synchronization issue of the voltage-type ITM interface and the dynamics in the simulated power network can be replicated to the GFC under test through the current-mode power amplifier. Despite the feasibility of this interface to incorporate GFC in a PHIL setup, its practical implementation is constrained by the limited capability of the power amplifier in terms of its power rating, and by the stability and accuracy issues arising from the loop time delay. From an application point of view, comprehensive system modeling, optimized design (proper scaling), stability assessment, and time delay compensation are crucial for accurate replication of the behaviours of physical GFC in the emulated grid.

C. Interface Design and Modelling

The equivalent block-diagram of the PHIL setup in Fig. 4 is presented in Fig. 5(a). As shown in Fig. 5(b), the interface components, equivalent impedance, and interface signals are represented in the equivalent block diagram as a single-input-single-output (SISO) closed-loop system. The scaling ratio design and component modelling are presented below:

1) Voltage and Current Scaling Ratio: The power capacity and voltage level of the network to be energized in the black-
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Fig. 6: Block diagram of the current feedback control of the current-mode power amplifier.

start sequence is higher than that of the candidate GFC power converter in the laboratory and the current in the energized network is much higher than the current constraint of the current-mode power amplifier. Voltage scaling ratio \( r_v \) is introduced to scale up the output voltage \( (V_A) \) of the physical GFC to a higher voltage \( (V_D) \) in the emulated power network. Current ratio \( r_i \) is utilized to scale the digital current \( (I_D) \) in the power network down to a lower command for regulating the output current \( (I_A) \) of the power amplifier. The voltage ratio and current ratio are given by:

\[
\begin{align*}
  r_v &= \frac{V_{D\text{nom}}}{V_{A\text{nom}}} , \quad r_i = \frac{I_{A\text{nom}}}{I_{D\text{nom}}} \\
  S_D &= r_v, \quad S_A = r_i \tag{4}
\end{align*}
\]

where \( V_A \) and \( V_D \) are the nominal voltage of the physical GFC and the emulated GFC at the simulation side, respectively. \( I_A \) and \( I_D \) are the nominal current of the power amplifier and the rated current of the emulated power network, respectively. \( S_A \) and \( S_D \) are the power rating of the physical GFC and the emulated GFC at the simulation side, respectively.

2) Current-Mode Power Amplifier: The cell 2 of Fig. 4 represents the circuit diagram of the switched-mode power converter with \( LCL \) output filter. Fig. 6 presents the grid side current feedback control diagram of this three-phase voltage source converter. The system open-loop transfer function is:

\[
T_{OCA}(s) = \frac{i_A}{i_a} = \frac{(k_p s + k_i) K_{PWM} e^{-s T_{d-P-A}}}{L_{11} L_{12} C_1 s^4 + (L_{11} + L_{12}) s^2} \tag{5}
\]

where \( k_p \) and \( k_i \) are the proportional gain and integral gain of the current controller, respectively. \( K_{PWM} \) is the gain (i.e., half of the DC-link voltage) of PWM converter and \( T_{d-P-A} \) is the PWM control delay that is a sum of one time step \( T_s \) for computation and half time step for PWM generation.

Applying the Taylor series expansion, the PWM control delay is approximated as:

\[
e^{-s T_{d-P-A}} = e^{-s 1.5 T_s} \approx \frac{1}{1 + 1.5 T_s s} \tag{6}
\]

Grid-side voltage feedforward is implemented to mitigate the impact of GFC output voltage on the grid-side current regulation. The voltage feedforward term \( T_{ff}(s) \) is given by:

\[
T_{ff}(s) = \frac{1}{K_{PWM} e^{-s T_{d-P-A}}} (L_{11} C_1 s^2 + 1) \tag{7}
\]

Substituting (6) into (5), the closed-loop transfer function of the current-mode power amplifier is obtained as:

\[
T_{CA}(s) = \frac{(k_p s + k_i) K_{PWM}}{1.5 T_s L_{11} L_{12} C_1 s^5 + 1.5 T_s (L_{11} + L_{12}) s^3 + (k_p s + k_i) K_{PWM}} \tag{8}
\]

3) Signal Measurement, Conversion and Processing Units: As shown in Fig. 5, the signal conversion units (i.e., the GTAO card in the feedforward path and the Aurora serial protocol in the feedback path) are modelled as units with unity gain and one digital real-time simulation (DRTS) time step delay \( T_{o} \). \( V_{M}(s) \) represents the voltage measurement unit with unity gain. \( T_{FW}(s) \) and \( T_{FB}(s) \) represent the low-pass filter in the feedforward path and the feedback path with a cut-off frequency \( f_{c1} \) and \( f_{c2} \), respectively. These signal processing units are modelled as:

\[
T_{FW}(s) = \frac{1}{2 \pi f_{c1}} + 1, \quad T_{FB}(s) = \frac{1}{2 \pi f_{c2}} + 1 \tag{9}
\]

D. PHIL System Stability Assessment

Based on the interface modelling, the open-loop transfer function of the SISO closed-loop PHIL system in Fig. 5(b) is:

\[
T_O(s) = r_v r_i T_{FW}(s) T_{CA}(s) T_{FB}(s) \frac{Z_2(s)}{Z_1(s)} e^{-s 2 T_o} \tag{10}
\]

The closed-loop stability is determined by the time delay, the non-ideal power amplifier and signal processing unit in the power interface, and the variable impedance at different black-start stages on the simulation side. Nyquist stability criteria can be applied to determine the closed-loop system stability by assessing the eigenvalues of the system characteristics equation that is given by:

\[
1 + T_O(s) = 0 \tag{11}
\]

Correspondingly, based on the system open-loop transfer function, gain margin (GM) and phase margin (PM) can be adopted to quantitatively assess the PHIL closed-loop stability.

E. Time Delay Compensation for Accuracy Improvement

As demonstrated in [18], [19], the time delay stemming from the signal conversion units (e.g., GTAO and GTAI cards) and the digital control of the power amplifier inevitably introduces phase offsets between the power signals transmitted within the closed-loop setup and deteriorates the power transfer transparency between the software and hardware side. Since the VSM control is dependent on accurate voltage signal synchronization and power measurement, time delay compensation is crucial for a high-fidelity replication of the emulated grid behaviours to the hardware GFC. The sliding DFT based time delay compensation scheme as presented in [19] is employed to compensate for the time delay in the PHIL setup by adding an additional phase shift to the power amplifier command signal and measured hardware voltage signal at the fundamental frequency. On the other hand, the time delay compensation of the current-mode power amplifier can be achieved by adding an additional phase shift to the hardware GFC output voltage phase angle that is utilized to convert the current control loop dq output component to the modulating signal. By doing so, accurate voltage or current signal synchronization and transparent power transfer between the real-time emulated power network and the hardware GFC can be achieved.
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IV. ANALYTICAL ASSESSMENT AND SIMULATION

This section presents a comparison between the voltage-type and current-type PHIL interfaces regarding their feasibility and capability of incorporating GFC into a PHIL setup. Analytical assessment of the current-type PHIL stability is presented.

A. Voltage-Type PHIL for Interfacing GFC

For black-start application, a grid-forming converter has its internal control loop to regulate voltage and frequency to energize the power network. Since the direct coupling of GFC and voltage-mode power amplifier leads to instability and potential damage to the physical apparatus, Matlab/Simulink simulation is employed to assess this setup. The emulated voltage-mode power amplifier and hardware GFC are based on the parameters of TP90kVA in Table I. The parameters of the remainder PHIL setup in Fig. 3 are given in Table I.

In the monolithic system of interest (SOI), a GFC is directly coupled with the power network without an interfacing power amplifier. Fig. 7(a) presents the GFC output voltage. A voltage reference with a ramp-up between $0 \sim 0.3$s and a step-down at $t = 0.6$s is emulated and the GFC output voltage presents good tracking performance.

In terms of the voltage-type PHIL setup as presented in Fig. 3, GFC regulates its output voltage by following its inherent angle while the power amplifier regulates its output voltage by following the reference signal from DRTS. These attributes lead to the angle mismatch at the coupling point between the GFC and the power amplifier. As shown in Fig. 7(b), the GFC output voltage (i.e., the voltage at the coupling point between GFC and power amplifier) presents significant oscillations. It is evident in Fig. 7(c) that the voltage angle of GFC presents significant discrepancy from that of the power amplifier.

B. Stability Assessment of Current-Type PHIL Interface

According to the virtual circuit control theory as presented in [20], the output impedance of TP90kVA is modelled as:

$$Z_2(s) = \frac{s5.5e^{-4} + 6.842}{s^25.5e^{-4} + s3.216e^{-4} + 1}$$

(12)

The system open-loop transfer function in (10) can be calculated by utilizing the system parameters tabulated in Table I and its corresponding frequency response is shown in Fig. 8. The open-loop transfer function of the current-type PHIL setup with parameters in Table I has positive GM and PM and the closed-loop setup is stable. The impact of the scaling ratios employed to facilitate the hardware GFC power

![Fig. 7: (a) GFC voltage of monolithic SOI (b) GFC voltage of voltage-type PHIL, and (c) voltage angle of voltage-type PHIL.](image)

![Fig. 8: Bode diagram of the open-loop transfer function of current-type PHIL setup.](image)

**TABLE I: PHIL setup parameters in Fig. 4.**

<table>
<thead>
<tr>
<th>Description</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PHIL setup</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage scaling ratio</td>
<td>$r_v$</td>
<td>27.5</td>
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<tr>
<td>Current scaling ratio</td>
<td>$r_i$</td>
<td>0.0133</td>
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<td>Cut-off frequency of $T_{PW}(s)$ in (9)</td>
<td>$f_{c1}$</td>
<td>8 kHz</td>
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<tr>
<td>Cut-off frequency of $T_{PH}(s)$ in (9)</td>
<td>$f_{c2}$</td>
<td>500 Hz</td>
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<tr>
<td>Transformer power rating (3 phase)</td>
<td>$S_{TR}$</td>
<td>53MVA</td>
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<td>Transformer turns ratio ($kV_{L1,L2}/kV_{L1,L2}$)</td>
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<td>11/33</td>
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<tr>
<td>Equivalent load in emulated power network</td>
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<tr>
<td>Real-time digital simulator (RTDS) time step</td>
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<td><strong>Current-type power amplifier (TP15kVA)</strong></td>
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<td></td>
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<td>DC voltage</td>
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<td>Grid side filter inductance</td>
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<td>$k_p$</td>
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<tr>
<td>PI controller integral gain</td>
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<td><strong>Hardware converter under test (TP90kVA)</strong></td>
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<td>DC voltage</td>
<td>$V_{DC2}$</td>
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<td>PWM switching frequency</td>
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<td>Emulated virtual inductance [20]</td>
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rating and to limit the power amplifier current reference is assessed. A higher power rating of the emulated GFC on the real-time simulation side can be achieved by implementing a high voltage ratio. However, as illustrated in Fig. 8, such a PHIL system can be unstable as the increment of the voltage ratio degrades the system gain margin. The cyan curve represents the PHIL system with the highest voltage ratio and power rating among the example systems, this PHIL system is unstable and presents negative GM and PM. The gain margin of the PHIL system is a factor by which the scaling ratio can be raised before breaching the system stability. A stability assessment of the PHIL system with pre-designed scaling ratios is crucial prior to the final system implementation.

V. EXPERIMENTAL VALIDATION

This section is dedicated to the experimental validation of the current-type interface regarding its ability to incorporate GFCs with black-start capability into a PHIL setup. This experiment was undertaken in the Dynamic Power Systems Laboratory at the University of Strathclyde.

Fig. 9 illustrates the experimental setup, the cells of which are corresponding to that as presented in Fig. 4. The simplified power network model is emulated in the real-time digital simulator (RTDS) and Triphase 90 kVA (TP90 kVA) power converter operates in grid-forming mode. These are coupled by a Triphase 15 kVA (TP15 kVA) power converter acting as a current-type power amplifier that sinks or sources current to the TP90 kVA converter, thus enabling the PHIL closed-loop configuration and mimicking the relative power behaviors in the emulated power network. The parameters of the emulated power network, power amplifier, and power converter are given in Table I. The scaling ratio $r_v$ and $r_i$ as tabulated in Table I are employed to represent the power converter that is emulated in the RTDS with higher power rating and voltage levels than that of the actual GFC (TP90 kVA) and to scale down the RTDS reference current signal within the current constraint of TP15 kVA power converter, respectively. By doing so, the power rating of the emulated GFC at the RTDS side is 2062 ($r_v/r_i$) times that of the physical one (TP90 kVA).

To validate the effectiveness of the current-type PHIL interface in realizing a stable and accurate testing of the hardware GFC integration throughout the black-start process, voltage-mode VSM control with a 5-second ramping time of the hardware GFC is utilized to realize a soft energization of the power transformer together with the load connected at the PCC point in the emulated power network. The voltage and current at the interfacing point in RTDS, the output voltage of TP90 kVA, and the command and output current of TP15 kVA are recorded by RTDS and Triphase datalogger, respectively, and are replotted by Matlab.

The voltage at the hardware GFC power converter output terminal is presented in Fig. 10(a) with a zoomed section

Fig. 9: A representation of the experimental PHIL setup with physical grid-forming converter.

Fig. 10: Experimental results of the voltage and current of the power amplifier and GFC power converter within the PHIL setup.

Fig. 11: Experimental results of the voltage and current at the interfacing point within the real-time emulated power network.
around the end of ramping time. This illustrates a successful hardware GFC output voltage tracking from 0 to the rated value without any measurable delay during the voltage ramp period. Correspondingly, the voltage at the interfacing point of the real-time emulated power network in RTDS is illustrated in Fig. 11. The scaled-up voltage at the interfacing point presents the same trend as the hardware GFC during the soft energization with voltage ramp period. Through the implementation of time delay compensation and scaling, the hardware GFC voltage behaviour is replicated in the emulated power network.

The current at the interfacing point of the real-time emulated power network in RTDS, as shown in Fig. 11, is transmitted to the current-mode power amplifier as its command signal through proper scaling. Fig. 10(b) and Fig. 10(c) present the command signal received from RTDS and the output current of the TP15 kV A power converter, respectively. The scaled-down \( r_i = 0.0133 \) three-phase current is accurately transmitted to TP15 kVA and is well-tracked by the output current of TP15 kVA. As shown in the zoomed version of the command and output current around the end of the ramping time, the actual output current is more harmonic-rich than the command signal. Despite the minor distortion of the output current, the phase of the power amplifier output current is aligned with that of the command signal. This is achieved by implementing the delay compensation method as presented in Section III-E, through which the current behavior in the emulated power network can be replicated by the power amplifier and be applied to the hardware GFC.

Through proper scaling and delay compensation, a high-fidelity simulation can be achieved by applying the current-type interface to incorporate a hardware GFC into a PHIL closed-loop. This can effectively tackle the stability issue of the voltage-type interface as presented in Section IV-A.

VI. CONCLUSIONS

This paper presents a comprehensive assessment and evaluation of the voltage-type and current-type PHIL interfaces regarding their suitability and applicability for incorporating grid-forming converter with black-start capability into PHIL closed-loop simulation. The in-depth modelling of the current-type PHIL interface has been presented along with stability analysis. In addition, interface optimization including proper scaling and time delay compensation has been proposed to facilitate the testing capability and to improve the simulation accuracy. Simulation results demonstrated the interfacing point voltage angular synchronization issue of the voltage-type interface. The experimental results involving the employment of a hardware GFC to energize a power network with a ramping voltage reference for the VSM control loop were illustrated. These outcomes indicate the capability of a current-type interface in incorporating hardware GFC into PHIL. Recommended future work includes expanding the testing of this interface to cover all the black-start scenarios and further stability analysis of this interface with the variable impedance over each black-start stage taken into account.

REFERENCES