

Low hardware consumption, resolution-configurable gray code oscillator time-to-digital converters implemented in 16nm, 20nm and 28nm FPGAs

Yu Wang, Wujun Xie, Haochang Chen, and David Day-Uei Li

Abstract—This paper presents a low-hardware consumption, resolution-configurable, automatically calibrating gray code oscillator time-to-digital converter (GCO-TDC) in Xilinx 16nm UltraScale+, 20nm UltraScale and 28nm Virtex-7 field-programmable gate arrays (FPGAs). The proposed TDC utilizes LUTs as delay elements and has several innovations: 1) a sampling matrix structure to improve the resolution. 2) a virtual bin calibration method (VBCM) to achieve configurable resolutions and automatic calibration. 3) hardware implementation of the VBCM in standard FPGA devices. We implemented and evaluated a 16-channel TDC system in all three FPGAs. The UltraScale+ version achieved the best resolution (least significant bit, LSB) of 20.97 ps with 0.09 LSB averaged peak-to-peak differential nonlinearity (DNL_{pk-pk}). The UltraScale and Virtex-7 versions achieved the best resolutions of 36.01 ps with 0.10 LSB averaged DNL_{pk-pk} and 34.84 ps with 0.08 LSB averaged DNL_{pk-pk} , respectively.

Index Terms—Gray code oscillator (GCO), field-programmable gate array (FPGA), low hardware consumption, automatic calibration, resolution-adjustable, time-to-digital converter (TDC).

I. INTRODUCTION

Time-to-digital converters (TDCs) are simply high-precision time-interval meters, converting a time interval (TI) into a digital code. (R2, comment 1) They are widely used in industrial and scientific applications, including light detection and ranging (LiDAR) for automatic vehicles and robotics [1]–[3], 3-D imaging [4]–[6], surveying [7], Raman spectroscopy [8], [9], hardware trojan detection [10], temperature sensing [11], [12], random number generation [13], [14], particle physics [15]–[17], positron emission tomography (PET) [18], fluorescence lifetime imaging microscopy (FLIM) [19] and space sciences [20].

The primary metric of a TDC is the resolution (the minimum TI that can be measured, also called the least significant bit, LSB). Ideally, all bins in a TDC should have the same width. The ideal bin width can be defined as $Q = T/n$, where T is the period of the sampling clock and n is the number of bins, respectively. However, bin widths are not uniform. The variations of bin widths caused by uneven delay elements [21]

are usually characterized by differential nonlinearity (DNL) and integrated nonlinearity (INL). They are respectively defined as $DNL[k] = (W[k] - Q)/Q$ and $INL[k] = \sum_{n=0}^k DNL[j]$, where $W[k]$ is the k -th bin's width, and it can be evaluated by code density tests [22]. With recent advances in CMOS manufacturing technologies, FPGA-TDCs and ASIC-TDCs can achieve picosecond-level resolutions. However, FPGA-TDCs are cheaper and have shorter developing cycles. These characteristics make FPGA-TDCs popular in prototype designs.

Industrial applications utilizing time-of-flight (TOF) information (such as LiDAR) concern not only the resolution but also linearity. In time-resolved LiDAR systems, a resolution of 66.6 ps corresponds to a distance of 1 cm [23]. Therefore, LiDAR systems for automatic vehicles and robotics require TDCs with a 35-500 ps resolution and high linearity [24]. Besides, PET and Raman spectroscopy also require TDCs with an acceptable resolution of 50 ps [8], [9], [25], [26]. Similar requirements make it possible to design general-purpose TDCs for these applications.

Interpolations in TDCs use the elements' delay to obtain a higher resolution. The tapped delay line TDC (TDL-TDC) is the mainstream for FPGA-TDCs because cascaded carry-chains are available in modern FPGAs, for example, CARRY4 modules in Xilinx 6-series and 7-series FPGAs [27] and CARRY8 modules in UltraScale and UltraScale+ FPGAs [28]. The TDL-TDC's resolution is determined by the carry module's propagation delay and can achieve 10 ps or better [29], [30] in 7-series FPGAs and 5 ps or better [31], [32] in UltraScale FPGAs. Due to the small propagation delay of carry modules, a TDL often requires more than 200 carry modules to

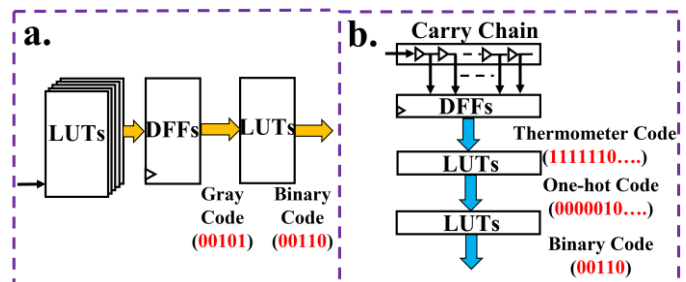


Fig. 1. The coding comparison between the (a) GCO-TDC and (b) TDL-TDC.

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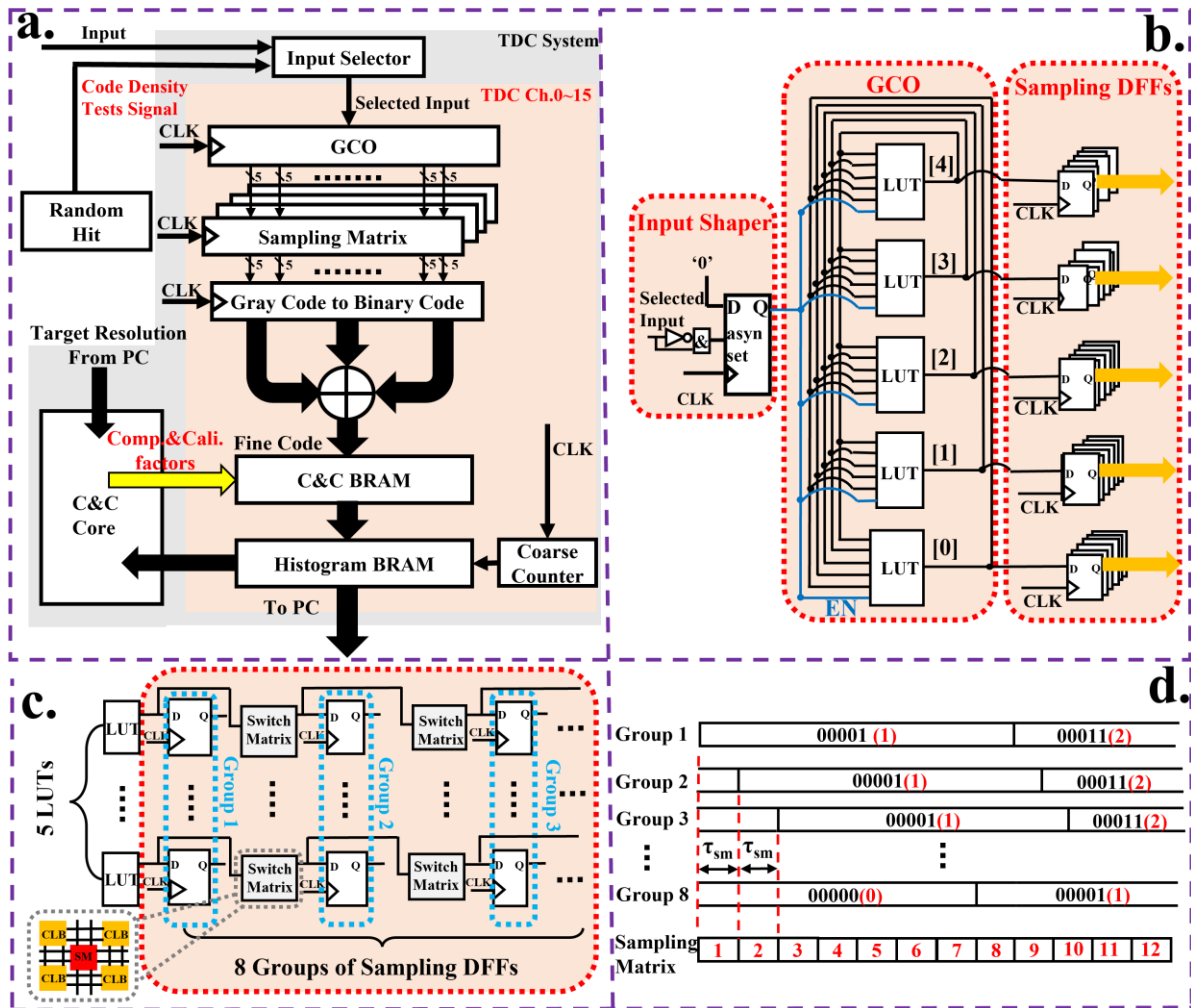


Fig.2. (a) The block diagram of the proposed TDC system. (b) The block diagram of the GCO-TDC (c) The block diagram of the sampling matrix. (d) The concept of the sampling matrix (R2 comment 2 and comment 3; R3, comment 9).

cover a sampling period. For example, it requires 50 CARRY4s (200 carry modules) in the 7-series FPGA (with a 710MHz sampling clock) [33] and 74 CARRY8s (592 carry modules) in the UltraScale FPGA (with a 500MHz sampling clock) [23]. When implementing multichannel designs, the consumption of carry modules would be significant (31.26% of CARRY8s are used for 128 channels in Ref. [23]). Besides, in highly-integrated systems, for example, in LiDAR applications [34], [35], multichannel TDCs are integrated with processing modules in FPGAs. Hence, as a basic unit for arithmetic operations, carry modules should be utilized efficiently rather than being largely utilized as delay elements. (R2, comment 6; R3, comment 1)

Recently, Wu and Xu [36] proposed a gray code oscillator (GCO)-TDC. Compared with TDL-TDCs, this design uses look-up tables (LUTs) rather than carry modules as delay elements. Through outputting gray codes directly, the GCO-TDC avoid tedious coding that uses many logic resources in TDL-TDCs (the comparison is shown in Fig.1). Hence, the GCO-TDC have high efficiency in hardware utilization and uses only eight LUTs and eight D-type flip-flops (DFFs) to build one TDC [36]. (R2, comment 6; R3, comment 1) However, the GCO-TDC's resolution (256 ps) is to be further improved, and it has a 1.25 LSB peak-to-peak differential nonlinearity

(DNL_{pk-pk}). (R3, comment 6) For better linearity, Machado *et al.* [37] adopted manual routing for the GCO-TDC and improved DNL_{pk-pk} to 0.76 LSB, but the resolution (380.9 ps) significantly increased. To enhance the resolution, Araújo *et al.* [38] proposed a double-sampling GCO-TDC. This work utilized the double-sampling method to improve the resolution to 69 ps. However, the linearity deteriorates to 1.76 LSB DNL_{pk-pk} . (R3, comment 7)

Besides, aforementioned GCO-TDCs [36], [38], [39] and most previously reported FPGA-TDCs [29], [30], [40] are designed with fixed resolutions. It is not friendly if application requirements change. For broader applications, TDCs in Ref. [23], [36] and [37] offer flexible resolutions. However, they all need manual configuration channel-by-channel and chip-by-chip when resolution requirements change. This process is time-consuming and difficult for users unfamiliar with FPGA-TDCs. TDCs in Ref. [38] and [39] achieve automatic calibration. But their resolutions are fixed. Hence, an automatic calibration TDC with flexible resolutions is desirable for general applications.

Based on the GCO structure, we proposed a high linearity multichannel TDC with configurable resolutions and automatic calibration. Although we aim for a resolution of 20~100 ps in this paper, it can be extended if needed. The main contributions

of this work are:

- 1) We propose a new sampling matrix structure and dramatically improve the GCO-TDC's resolution.
- 2) We propose a virtual bin calibration method (VBCM) for online resolution configuration and automatic calibration.
- 3) We implemented the VBCM by the hardware description language (HDL). Through multiplexing critical components, this core is hardware-efficient.
- 4) To show our methods, we developed and evaluated 16-channel TDCs in 16nm UltraScale+ XCZU7EV, 20nm UltraScale XCKU040 and 28nm Virtex-7 XC7V690T FPGAs.

This article is structured as follows: Section II describes the architecture and design of the proposed TDC. Section III presents the experimental results, Section IV compares with other designs, and Section V summarizes our TDC.

II. ARCHITECTURE AND DESIGN

The architecture of the proposed TDC is shown in Fig. 2a. The GCO is the cornerstone of the proposed TDC, and it is responsible for measuring TIs with a coarse counter. For each channel, it also contains a sampling matrix, a gray-code-to-binary-code converter, a compensation&calibration BRAM (C&C BRAM in Fig. 2a), and a histogram BRAM. Besides, the proposed TDC system contains a compensation&calibration core (C&C Core in Fig. 2a) for calculating compensation&calibration factors (comp.&cali. factors in Fig. 2a) for all 16 channels. The C&C core only works after system launching and configuring the resolution. After calculating, the C&C core loads comp.&cali. factors into the C&C BRAM. With the C&C core and the C&C BRAM, the proposed TDC achieves multi-resolution and high linearity without manual intervention.

A. GCO-TDC

The GCO is shown in Fig. 2b. Unlike the binary code, only one bit experiences transition between two contiguous states in the gray code. So, the GCO is robust against the "race and competition" phenomenon and can be structured with combinational logic resources only [36]. In our design, the GCO is implemented with LUTs. In 7-series and more advanced Xilinx FPGAs, each LUT has up to 6 inputs[28], [45]. One of these inputs is connected to "EN" (highlighted in blue

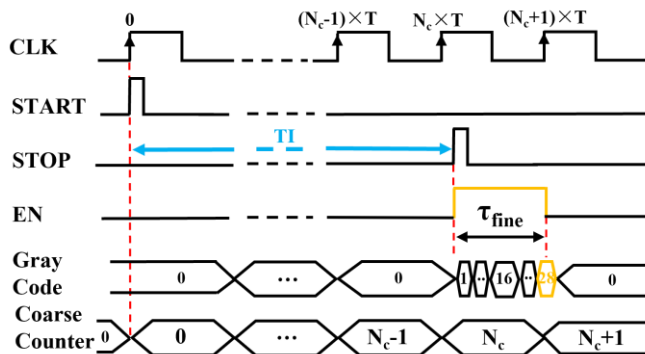


Fig. 3. The timing diagram of the GCO-TDC.

in Fig. 2b) to start/reset the GCO, and the other five inputs are used to get feedback from LUTs' outputs. By instantiating LUTs and DFFs with Vivado primitives [28], [45], five-bit gray code can be output from five LUTs and then sampled by DFFs.(R4, comment 2-ii) According to the sampled gray code, TI between the GCO launching and DFFs sampling can be evaluated. Hence, the GCO can be used to measure TI even it is less one clock period.

To reset the GCO after sampling and work with a coarse counter, as shown in Fig. 2b, an "Input Shaper" is designed to generate the control signal for the GCO. (R3, comment 2) The timing diagram of the proposed GCO-TDC is shown in Fig. 3. In the proposed system, the "START" is synchronous with the sampling clock (CLK in Fig. 3), and the "STOP" is asynchronous with it. When a rising edge of "STOP" comes ("STOP" is the input signal for the "Input Shaper"), the signal "EN" changes to "1"(high-logic level) and keeps this state until the rising edge of the sampling clock. Meanwhile, the GCO launches, and then it resets after being sampled by DFFs. With every rising edge of "STOP", a fine code from the GCO and a coarse code from the coarse counter can be latched. (R3, comment 8) By combining the fine code and coarse code, the proposed GCO-TDC can easily extend the measurement range without increasing gray code bits.(R3, comment 2) The TI (highlighted in blue in Fig. 3) can be calculated as $TI = (N_c + 1) \times T - \tau_{fine}$, where N_c is the coarse code and τ_{fine} is the time interval corresponding to the fine code.

B. Sampling Matrix

In the plain GCO-TDC [36], each LUT is sampled by a single DFF. Although this structure is hardware-efficient, it can only deliver a lower resolution. Therefore, a sampling matrix structure (shown in Fig. 2c) is proposed to improve the resolution.

In Fig. 2c, each LUT is sampled by eight DFFs. With eight

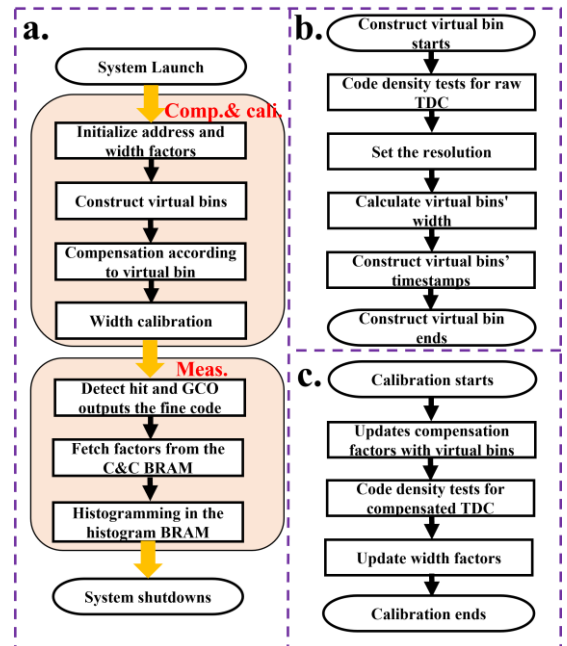


Fig. 4. (a) The workflow the proposed TDC system. (b) The workflow of the virtual bin construction. (c) The workflow of calibration.

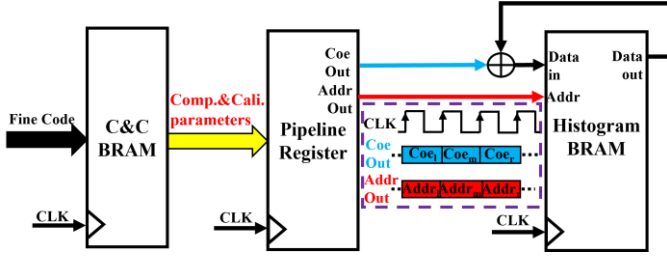


Fig. 5. Hardware implementation of the real-time histogram with the VBCM.

groups of DFFs, the TDC conducts eight measurements for the same TI in one clock period. Fig. 2d shows this method's concept, where τ_{sm} is the delay of the switch matrix. In plain GCO-TDCs, the resolution is defined as $Q = T/n$. For the GCO-TDC with a sampling matrix, each plain bin is sub-divided with τ_{sm} . (R2, comment 4) Hence, the resolution with a sampling matrix is defined as:

$$LSB_{sm} = \frac{T}{n} \times \frac{1}{M} = \frac{Q}{M}, \quad (R2, \text{comment } 4) \quad (1)$$

where M is the amount of DFF groups.

TABLE I compares raw TDCs' resolutions and hardware consumption (without the C&C core) with different sampling factors (M) in all three FPGAs. According to the utilization percentage, LUTs are mainly consumed in our design. So, we use the consumption of LUTs to evaluate hardware consumption in Eq (2). To find a balance between the resolution and hardware consumption when we increase M , the normalized efficiency of resolution improvement is proposed and calculated as:

$$E_M = \frac{LSB_{M[i-1]} - LSB_{M[i]}}{LSB_{plain}} / \frac{LUT_{M[i]} - LUT_{M[i-1]}}{LUT_{plain}}, \quad M=2^i \quad (2)$$

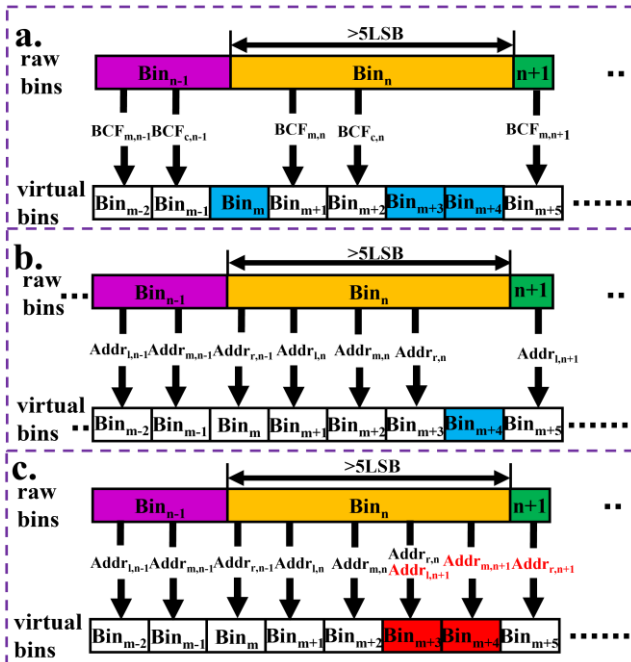


Fig. 6. Compensation in (a) the mixed calibration, (b) the weighted histogram calibration and (c) the virtual bin calibration methods.

TABLE I
COMPARISONS OF PERFORMANCES AND HARDWARE UTILIZATION WITH DIFFERENT SAMPLING FACTORS (M) (R3, comment 3)

M	E_M	LSB (ps)	Used LUTs (%) ¹	Used DFFs (%) ²
<i>UltraScale+</i>				
1	N/A ³	158.03	117 (0.05%)	177 (0.04%)
2	2.56	79.01	139 (0.06%)	194 (0.04%)
4	0.96	40.23	170 (0.07%)	221 (0.05%)
8	0.31	19.41	222 (0.10%)	268 (0.06%)
16	0.08	10.51	295 (0.13%)	354 (0.08%)
<i>UltraScale</i>				
1	N/A ³	267.09	146 (0.06%)	233 (0.05%)
2	6.50	136.39	157 (0.06%)	238 (0.05%)
4	1.76	68.93	178 (0.07%)	248 (0.05%)
8	0.44	35.42	220 (0.09%)	268 (0.06%)
16	0.15	19.02	279 (0.12%)	380 (0.08%)
<i>Virtex-7</i>				
1	N/A ³	256.41	146 (0.03%)	233 (0.03%)
2	5.73	125.69	159 (0.04%)	238 (0.03%)
4	11.69	64.10	162 (0.04%)	248 (0.03%)
8	0.43	32.54	204 (0.05%)	268 (0.03%)
16	0.11	17.05	281 (0.06%)	380 (0.04%)

¹ Percentage of LUTs' utilization; ² Percentage of DFFs' utilization;

³ Not available.

where LSB_M and LUT_M are, respectively the TDC's resolution and consumption of LUTs with an M -order sampling matrix, and LSB_{plain} and LUT_{plain} are the resolution and LUTs' consumption of the plain GCO-TDC ($M = 1$). When M increases, E_M decreases in UltraScale and UltraScale+ FPGAs. However, it shows a different trend in the Virtex-7 FPGA. E_M in the Virtex-7 FPGA reaches its peak value when $M = 4$ due to a different FPGA architecture. Overall, E_M is close to 0 when $M = 16$ in all three FPGAs, meaning the efficiency of resolution improvement is low when M increases from 8 to 16. Hence, we choose $M = 8$, considering the trade-off between performances and hardware consumption. (R3, comment 3)

C. Virtual Bin Calibration Method

Our previous work [44] presented a PS-based architecture to achieve automatic calibration. However, this design is device-dependent and its resolution is fixed. Here we propose a virtual bin calibration method for automatic calibration and online resolution configuration in common FPGA devices. For this work, we will demonstrate the proposed method in three different FPGA devices manufactured in 16nm, 20nm, and 28nm CMOS processes.

The workflow of the VBCM is shown in Fig. 4a. After launching the system and configuring the resolution, the C&C core calculates compensation factors ($Addr_l$, $Addr_m$ and $Addr_r$) and width calibration factors (Coe_l , Coe_m and Coe_r), then loads them to the C&C BRAM in the compensation/calibration stage (Comp.&cali. in Fig. 4a). In the measurement stage (Meas. in Fig. 4a), indexed by a fine code, factors are delivered from the C&C BRAM to the histogram BRAM. During this procedure, width calibration factors (Coe_l , Coe_m and Coe_r) are seriatim added to corresponding bins of the histogram BRAM indexed by compensation factors ($Addr_l$, $Addr_m$ and $Addr_r$) shown in Fig.5. Through this, real-time calibration and resolution configuration can be achieved.

Calculations of compensation and width calibration factors contains: 1) construction of virtual bins and 2) calculations according to virtual bins. These two steps are both based on code density tests. Figure 4b shows the workflow of virtual bins


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start_point=max[Addrr[k-1], Addrm[k-1], Addrr[k-1]];
if (Traw[k] ≤ Tvir[start_point])
    Addrr[k]= start_point;
elseif (Traw[k] ≤ Tvir[start_point+1])
    Addrr[k]= start_point;
    Addrm[k]= start_point+1;
elseif (Traw[k] ≤ Tvir[start_point+2])
    Addrr[k]= start_point;
    Addrm[k]= start_point+1;
    Addrr[k]= start_point+2;
else
    Addrr[k]= start_point+1;
    Addrm[k]= start_point+2;
    Addrr[k]= start_point+3;
    
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Fig. 7. The pseudo-codes of compensation in virtual bins calibration.

construction. With the target resolution R_{conf} , the number of hits collected at a virtual bin should be:

$$hit_{vir} = \frac{R_{conf}}{T} \times \tilde{N} = \frac{\tilde{N}}{n_{vir}}, \quad (3)$$

where n_{vir} ($n_{vir} \leq n$) is the number of virtual bins in a sampling period and \tilde{N} is the number of random hits for code density tests. Hence, the ‘‘timestamp’’ of the m -th virtual bin (number of hits collected until the m -th virtual bin) and the ‘‘timestamp’’ of the k -th raw bin can be defined, respectively, as:

$$T_{vir}[m] = hit_{vir} \times m, \quad m \in [1, n_{vir}], \quad (4)$$

$$T_{raw}[k] = \sum_1^k hit_{raw}[j], \quad k \in [1, n], \quad (5)$$

where $hit_{raw}[j]$ is the number of hits at the j -th raw bin.

With T_{vir} and T_{raw} , like the mixed calibration [32] and weighted calibration methods [44], the compensation factors can be calculated. However, both the mixed calibration method [32] and weighted calibration methods [44] have a limited compensation range, causing ‘‘missing bins’’ (highlighted in blue in Fig. 6a and Fig. 6b). Hence, this work proposes a new missing-bin-free compensation strategy. With three compensation factors ($Addr_r$, $Addr_m$ and $Addr_r$), the concept of the proposed compensation strategy is shown in Fig. 6c. In most cases, ultra-narrow bins (< 1 LSB, highlighted in green in Fig. 6c) and regular bins ($1 \sim 2$ LSB, highlighted in purple in Fig. 6c) could neighbor ultra-wide bins (highlighted in yellow in Fig. 6c). However, earlier studies [32], [44] did not utilize all compensation factors of ultra-narrow bins (only $BCF_{m,n+1}$ is used in Fig. 6a and only $Addr_{r,n+1}$ is used in Fig. 6b). To utilize ‘‘idle’’ compensation factors, in Fig. 6c, $Addr_{r,n+1}$ and $Addr_{m,n+1}$ are used to remap to virtual bins covered by Bin_n (Bin_{m+3} and Bin_{m+4} , highlighted in red in Fig. 6c). The pseudo-codes for compensation factor calculations are shown in Fig. 7. After updating compensation factors according to virtual bins, the width calibrations factors can be calculated as shown in Fig. 4c. Code density tests are conducted again for the compensated TDC. (R3, comment 10) Then, with the number of hits collected at each bin, width calibration factors can be calculated as:

$$Coe_{l,m,r}[k] = \frac{\tilde{N}}{n_{vir}} \times \frac{1}{hit_{com}[i]} \quad i = Addr_{l,m,r}[k], \quad (6)$$

comment 11)

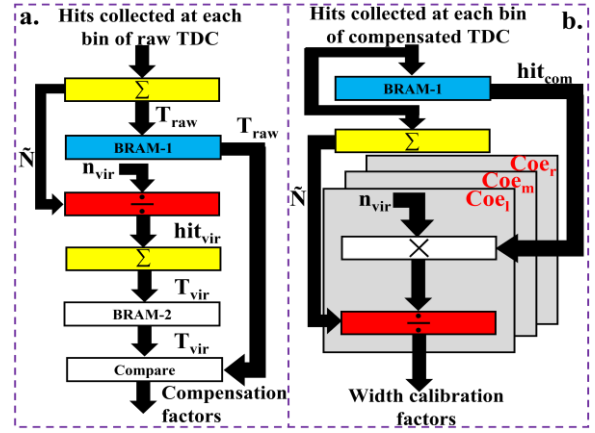


Fig. 8. Hardware implementation of (a) compensation factor calculations, and (b) width calibration factor calculations.

where $hit_{com}[i]$ is the number of hits collected at the i -th bin of the compensated TDC.

D. Hardware implementation of the VBCM

The hardware implementation of the VBCM contains: 1) the implementation of the real-time histogram and 2) the implementation of the C&C core. The implementation of the real-time histogram is shown in Fig. 5. For low BRAM-consumption, a pipeline structure is utilized. In the C&C BRAM, three groups of factors are merged and stored in an address to reduce hardware consumption. With pipeline registers, merged factors are separated and delivered to the histogram BRAM within three system clock periods. (R3, comment 12) Compared with consuming two histogram BRAMs in the mixed calibration method [32] and three histogram BRAMs in our previous work [44], only one histogram BRAM is required in this design.

The C&C core is responsible for calculating compensation and width calibration factors. It is composed of two modules: 1) a compensation factor calculation (CFC) module, and 2) a width calibration factor calculation (WCFC) module. The WCFC module works after the CFC module. Hence, we multiplex some components in these two modules to achieve low resource-consumption. The hardware implementation of the CFC module is shown in Fig. 8a. After code density tests, T_{vir} and T_{raw} are calculated according to Eqs (4) and (5) and stored in BRAM-2 and BRAM-1, respectively. When all T_{vir} and T_{raw} are calculated, they are output from respective BRAMs and compared following pseudo-codes shown in Fig. 7 to calculate compensation factors ($Addr_r$, $Addr_m$ and $Addr_r$). After

TABLE II
SIMULATION RESULTS WITH DIFFERENT \tilde{M} (Reviewer 4, comment 2 i)

	16nm UltraScale+					
\tilde{M}	1	2	3	4	5	6
DNL _{pk-pk} (LSB)	0.68	0.39	0.20	0.12	0.10	0.08
INL _{pk-pk} (LSB)	3.21	1.39	0.50	0.42	0.49	0.31
	20nm UltraScale					
\tilde{M}	1	2	3	4	5	6
DNL _{pk-pk} (LSB)	0.68	0.38	0.20	0.16	0.12	0.12
INL _{pk-pk} (LSB)	2.56	0.95	0.77	0.48	0.36	0.35
	28nm Virtex-7					
\tilde{M}	1	2	3	4	5	6
DNL _{pk-pk} (LSB)	0.65	0.36	0.20	0.16	0.09	0.10
INL _{pk-pk} (LSB)	3.11	1.35	0.73	0.62	0.26	0.34

TABLE III
LINEARITY OF THE PROPOSED TDC WITH DIFFERENT RESOLUTIONS

		LSB (ps)	DNL_{pk-pk} (LSB)	σ_{DNL} (LSB)	INL_{pk-pk} (LSB)	σ_{INL} (LSB)	ω_{eq} (ps)	σ_{eq} (LSB)
UltraScale+ 16nm	Raw-TDC	19.41 ($n = 228$)	3.98	0.96	7.17	1.39	43.11	0.64
		20.97 ($n_{vir} = 211$)	0.09	0.01	0.20	0.04	20.98	0.29
	VBCM-TDC	29.90 ($n_{vir} = 148$)	0.05	0.01	0.12	0.02	29.91	0.29
		39.86 ($n_{vir} = 111$)	0.05	0.01	0.12	0.03	39.86	0.29
		50.28 ($n_{vir} = 88$)	0.05	0.01	0.11	0.02	50.29	0.29
		80.45 ($n_{vir} = 55$)	0.03	0.01	0.09	0.02	80.46	0.29
UltraScale 20nm	Raw-TDC	35.42 ($n = 181$)	4.76	0.93	12.38	2.92	76.94	4.72
		36.01 ($n_{vir} = 178$)	0.08	0.01	0.14	0.03	36.02	0.29
	VBCM-TDC	40.06 ($n_{vir} = 160$)	0.07	0.01	0.12	0.03	40.07	0.29
		50.08 ($n_{vir} = 128$)	0.05	0.01	0.13	0.03	50.09	1.00
		80.13 ($n_{vir} = 80$)	0.05	0.01	0.08	0.02	80.15	0.29
		100.16 ($n_{vir} = 64$)	0.04	0.01	0.11	0.03	100.18	0.29
Virtex-7 28nm	Raw-TDC	32.54 ($n = 197$)	5.48	0.95	11.23	2.35	72.96	0.65
		34.84 ($n_{vir} = 184$)	0.07	0.02	0.29	0.08	34.85	0.29
	VBCM-TDC	40.06 ($n_{vir} = 160$)	0.07	0.01	0.18	0.04	40.07	0.29
		50.08 ($n_{vir} = 128$)	0.07	0.01	0.16	0.04	50.09	0.29
		80.13 ($n_{vir} = 80$)	0.04	0.01	0.15	0.03	80.15	0.29
		100.16 ($n_{vir} = 64$)	0.05	0.01	0.11	0.03	100.18	0.29

compensation is complete, compensation factors are updated into the C&C BRAM. Then code density tests are conducted again for the compensated TDC, and results are stored in BRAM-1 as shown in Fig.8b. With bin-widths of the compensated TDC, width calibration factors (Coe_i , Coe_m and Coe_r) can be calculated according to Eq (6). In the WCFC module, we reuse the BRAM-1, the accumulator and the divider (highlighted in blue, yellow and red in Fig.7) previously used in the CFC module. Moreover, three width calibration factors are calculated similarly. Therefore, the multiplier-divider component (highlighted in gray) is also multiplexed in the WCFC module.

In our design, all data is presented and calculated in the fixed-point format to reduce hardware consumption. Considering errors when the decimal parts are discarded, we use the last \bar{M} bits of Coe to present decimals. Then, calibration factors can be calculated as:

$$Coe_{i,m,r}[k] = Coe_{i,m,r}[k] \times 2^{\bar{M}} = \frac{N}{n_{vir}} \times \frac{2^{\bar{M}}}{hit_{com}[i]}, i = Addr_{i,m,r}[k]. \quad (7)$$

For selecting an appropriate \bar{M} , we used MATLAB to simulate the VBCM with a different \bar{M} (setting $n_{vir} = n$). Results in TABLE II indicate that when \bar{M} increases from 5 to 6, linearity cannot be further improved in UltraScale and Virtex-7 FPGAs, but only peak-to-peak INL (INL_{pk-pk}) is enhanced in the

UltraScale+ FPGA. Hence, we choose $\bar{M} = 5$ for all three FPGAs for an optimized design. (Reviewer 4, comment 2 i)

III. EXPERIMENTAL RESULTS

We implemented the proposed TDC in ZCU104 [46] (16nm UltraScale+), KCU105 [47] (20nm UltraScale) and NetFPGA SUME [48] (28nm Virtex-7) evaluation boards, respectively. Random hits for code density tests were generated by an SRS CG-635 (Stanford Research Systems), and TDCs' clocks are from low-jitter crystal oscillators on the boards (IDT-8T49 in ZCU104, SI-570 in KCU105 and DSC-1103 in NetFPGA SUME). The frequencies of TDCs' clocks are 226MHz (ZCU104), 156MHz (KCU105) and 156MHz (NetFPGA SUME) respectively, due to different GCOs' oscillation frequencies in three FPGAs. The temperature and voltage were maintained in experiments.

A. Resolution configuration and linearity

We evaluated our configurable TDCs with different resolution options. The linearity is characterized by DNL, INL and their standard deviations (σ_{DNL} and σ_{INL}). Besides, Wu [49] also proposed the equivalent bin-width (ω_{eq}) and its deviation (σ_{eq}) to evaluate the TDC's linearity. They are:

$$\sigma_{eq}^2 = \sum_{i=1}^n \left(\frac{W[i]^2}{12} \times \frac{W[i]}{W_{total}} \right), \quad (8)$$

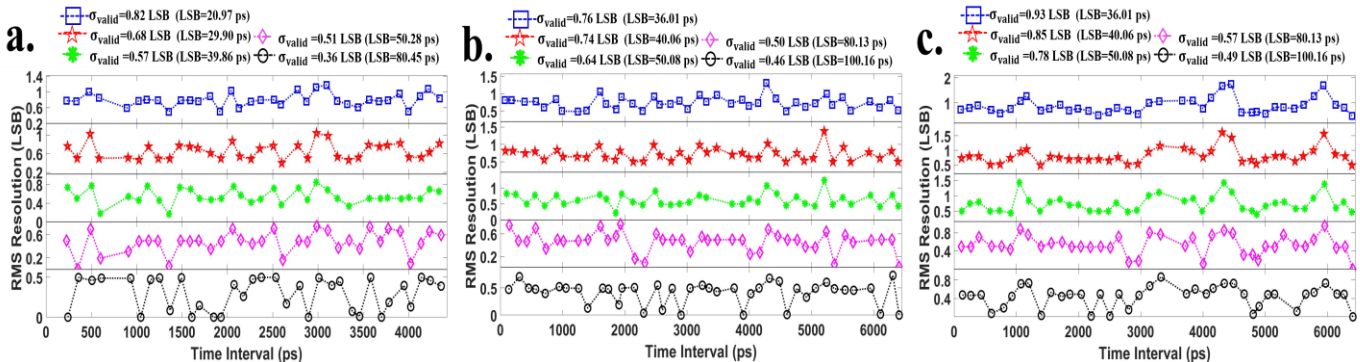


Fig.9. RMS resolutions with different resolution configurations in (a) 16nm UltraScale+, (b) 20nm UltraScale, and (c) 28nm Virtex-7 FPGAs.(R3, comment 13)

$$\omega_{eq} = \sigma_{eq} \times \sqrt{12} = \sqrt{\sum_{i=1}^n \frac{W[i]^3}{W_{total}}}, \quad (9)$$

where $W_{total} = \sum_{i=1}^n W[i]$. The experimental results are summarized in TABLE III. With the VBCM, the proposed TDC's linearity is improved significantly. The 16nm UltraScale+ TDC has DNL_{pk-pk} enhanced by more than 44-fold (from 3.98LSB to less than 0.09 LSB), and INL_{pk-pk} enhanced by more than 35-fold (from 7.17 LSB to less than 0.20 LSB). Besides, we have also achieved significant improvements in 20nm UltraScale and 28nm Virtex-7 FPGAs, with DNL_{pk-pk} respectively improved by more than 59-fold (from 4.76 LSB to less than 0.08 LSB) and 78-fold (from 5.48 LSB to less than 0.07 LSB), and INL_{pk-pk} respectively improved by more than 88-fold (from 12.38 LSB to less than 0.14 LSB) and 38-fold (from 11.23 LSB to less than 0.29 LSB). Results indicate the proposed TDC has high linearity in different resolutions.

B. Time Interval Tests

The RMS resolution can be evaluated by the standard deviation of measurements for the same TI. It is defined as $\sigma^2 = \sum_{i=1}^{N_T} \frac{(x_i - \mu)^2}{N_T}$, where x_i is the i -th output and μ is the averaged value for N_T measurements when TI is fixed.

To avoid jitter introduced by input signals, we utilized programmable input delay elements inside FPGAs (IDELAY3

in UltraScale+ and UltraScale FPGAs, and IDELAY2 in the Virtex-7 FPGA) to generate controllable delays.

The RMS resolutions for different resolution configurations are shown in Fig. 9. We conducted time interval tests with different intervals (less than one system clock period). However, for each resolution option with different intervals, the averaged RMS resolution or the maximum RMS resolution cannot represent the RMS resolution because they overestimate or underestimate it [23]. Hence, the valid RMS resolution (σ_{valid}) is used, and it is defined as $\sigma_{valid}^2 = \sum_{i=1}^H \frac{\sigma_i^2}{H}$ [23], where σ_i is the standard deviation of measurements for the i -th fixed time interval and H is the number of different time intervals. With the resolution improved, the valid RMS resolution deteriorates in all three FPGAs. The UltraScale+ version achieves the best valid RMS resolution of 0.36 LSB when LSB=80.45 ps. The UltraScale and Virtex-7 versions, respectively, can achieve valid RMS resolutions of 0.46 LSB and 0.49 LSB when LSB=100.16 ps. (R3, comment 13)

C. Multichannel Design

We implemented the proposed TDCs in all three FPGAs. In each channel, an 18k-BRAM is used as the histogram BRAM, and a 36k-BRAM is used as the C&C BRAM. Besides, less than 230 LUTs and 270 DFFs are required to build the GCO-TDC with a sampling matrix. For the C&C core, two 18k-BRAMs, no more than 3800 LUTs and 1600 DFFs are used to calculate

TABLE IV
HARDWARE RESOURCES UTILIZATION (R2, COMMENT 5)

		LUT	DFF	CARRY ¹	BRAM ²
UltraScale+ 16 nm	Available	230400	460800	28800	312
	1-ch.	222	268	9	1.5
	16-ch.	3548	4288	144	24
	C&C core	3719	1596	310	1
UltraScale 20 nm	Available	242400	484800	30300	600
	1-ch.	220	268	9	1.5
	16-ch.	3518	4288	144	24
	C&C core	3725	1569	310	1
Virtex-7 28 nm	Available	433200	866400	108300	1470
	1-ch.	204	268	18	1.5
	16-ch.	3263	4288	288	24
	C&C core	3753	1597	574	1

¹ CARRY8s in UltraScale+ and UltraScale FPGAs, and CARRY4s in Virtex-7 FPGA; ² 36K-BRAM.

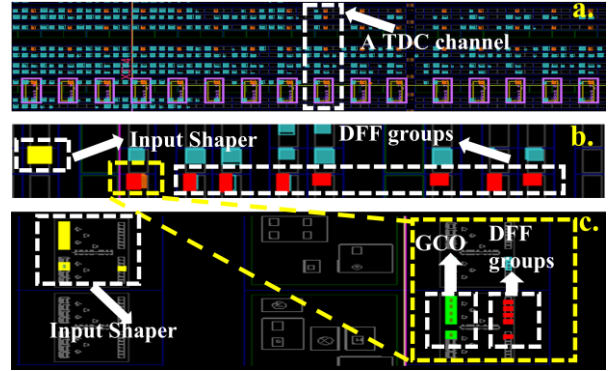


Fig. 10. Implementation layouts of (a) 16 channels, (b) a single channel, and (c) an input shaper and a GCO.

TABLE V
DNL_{PK-PK} OF 16-CHANNEL TDCs IN 16NM, 20NM, AND 28NM FPGAs

LSB (ps)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Ave.
	LSB																
UltraScale+																	
20.97	0.09	0.07	0.10	0.08	0.07	0.18	0.08	0.07	0.11	0.06	0.07	0.07	0.07	0.13	0.07	0.08	0.09
29.90	0.05	0.06	0.06	0.06	0.05	0.08	0.06	0.07	0.06	0.06	0.06	0.07	0.06	0.06	0.06	0.05	0.06
39.86	0.05	0.04	0.05	0.04	0.05	0.05	0.06	0.05	0.05	0.06	0.05	0.05	0.04	0.05	0.05	0.06	0.05
50.28	0.05	0.04	0.04	0.04	0.05	0.05	0.04	0.04	0.04	0.04	0.04	0.05	0.05	0.05	0.04	0.05	0.04
80.45	0.03	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04	0.04
UltraScale																	
36.01	0.08	0.16	0.08	0.13	0.08	0.08	0.08	0.09	0.07	0.18	0.09	0.07	0.08	0.08	0.21	0.09	0.10
40.06	0.07	0.11	0.10	0.20	0.10	0.02	0.06	0.12	0.09	0.10	0.07	0.09	0.09	0.10	0.25	0.16	0.11
50.08	0.05	0.15	0.14	0.05	0.17	0.07	0.06	0.05	0.07	0.06	0.07	0.09	0.06	0.09	0.06	0.05	0.08
80.13	0.05	0.06	0.05	0.08	0.05	0.15	0.05	0.05	0.05	0.05	0.05	0.05	0.09	0.06	0.05	0.06	0.06
100.16	0.04	0.18	0.05	0.06	0.04	0.16	0.05	0.04	0.05	0.05	0.05	0.04	0.06	0.04	0.05	0.05	0.06
Virtex-7																	
34.84	0.07	0.07	0.06	0.06	0.10	0.07	0.07	0.06	0.05	0.11	0.06	0.15	0.09	0.07	0.07	0.10	0.08
40.06	0.07	0.11	0.09	0.07	0.09	0.08	0.08	0.08	0.09	0.15	0.08	0.08	0.07	0.09	0.06	0.09	0.09
50.08	0.07	0.07	0.06	0.06	0.05	0.06	0.06	0.07	0.05	0.06	0.06	0.07	0.06	0.06	0.06	0.07	0.06
80.13	0.04	0.04	0.05	0.05	0.05	0.05	0.04	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
100.16	0.05	0.04	0.05	0.04	0.05	0.05	0.05	0.04	0.04	0.04	0.04	0.04	0.05	0.04	0.04	0.05	0.04

TABLE VI
COMPARISON OF RECENTLY PUBLISHED FPGA-TDCs (R3, COMMENT 14)

Ref-year	Methods	Devi. Proc. (nm)	LSB (ps)	ω_{eq} (ps)	RMS Resol. (ps)	DNL(LSB)	INL(LSB)	LUT (%) ¹	DFF (%) ¹	Carry (%) ¹	36K-BRAM	Auto/manual Cali.
TDL-TDCs												
[29]-17	Tuned-TDL, Direct Histogram, Bin-width Cali.	28	10.50	10.55	4.42	[-0.04,0.04]	[-0.09,0.04]	N/S ²	N/S ²	N/S ²	N/S ²	Manual
[32]-19	Tuned-TDL, Sub-TDL, Mixed Calibration	28	10.54	10.55	14.59	[-0.05, 0.08]	[-0.09, 0.11]	1145	1916	N/S ²	1.5	Manual
		20	5.02	5.03	7.80	[-0.12, 0.11]	[-0.18, 0.46]	703	1195	80 ¹⁰		
[43]-21	Slide Scale, Gain & Error cal., Moving Ave.	28	4.88	N/S ²	2.90~8.03	[-0.10, 0.15]	[-0.23, 0.28]	2962	4157	N/S ¹	N/S ¹	Auto
[23]-21	Mixed-binning	20	51.28	51.29	15.89	[-0.018, 0.021]	[-0.019,0.035]	663	1124	74 ¹⁰	2.5	Manual
			83.33	83.34	21.67	[-0.017, 0.016]	[-0.028,0.003]	0.27	0.23	0.24		
			105.26	105.26	26.32	[-0.008, 0.008]	[-0.009,0.007]					
[44]-21	Sub-TDL, AC-WU	28	9.83	9.85	13.86	[-0.14, 0.16]	[-0.25, 0.42]	764	1095	50 ¹¹	2	Auto
[42]-21	Half single-chain, real States-based Coding	16	5	N/S ²	19 ³	[-0.99, 1.44]	[-2.84, 1.62]	N/S ²	N/S ²	N/S ²	N/S ²	N/S ²
			21.56	N/S ²	30.18 ³	[-0.16, 0.19]	[-0.50, 0.33]	N/S ²	N/S ²	N/S ²	N/S ²	
			87.74	N/S ²	105.29 ³	[-0.07, 0.05]	[0.00, 0.11]	N/S ²	N/S ²	N/S ²	N/S ²	
Other TDCs												
[40]-20	Bidirectional, RO Vernier	65	24.50	N/S ²	28.00	[-0.20,0.25]	[0.03,0.82]	172	986	N/S ²	N/S ²	N/S ²
[41]-21	NUMMP, Timing Scale Marking	28	1.87	N/S ²	2.79	[-0.54,1.30]	[-2.21,3.51]	1679	1103	N/S ²	12	N/S ²
			11.24	N/S ²	8.07	[-0.43,0.26]	[-0.55,0.30]	0.82	0.27	1328	857	
			20.00	N/S ²	12.81	[-0.05,0.06]	[-0.15,0.08]	0.65	0.2	634	828	
								0.41	0.16	N/S ²	12	
GCO-TDCs												
[36]-2019	GCO, Bin-by-bin Cali.	28	256	N/S ²	155	[-0.53,0.72] ⁶	N/S ²	8	8	N/S ²	N/S ²	Manual
[39]-2020	GCO, Manual Routing	28	380.9	N/S ²	290	[-0.38,0.38]	[0.01,0.70]	6	10	N/S ²	N/S ²	Manual
[38]-2021	GCO, Double Sampling	16	69	N/S ²	54.99	[-0.95,0.81]	[-1.01,0.49]	5	19	N/S ²	N/S ²	Manual
This TDC	GCO, Sampling Matrix, VBCM	16	20.97⁴	20.98	17.11⁵	[-0.055, 0.034]	[-0.196, 0.000]	222⁸	268⁸	9¹⁰	1.5¹²	Auto
						0.087⁷	0.224⁷	0.10	0.06	0.03		
								455⁹	368⁹			
								0.20	0.08			
								220⁸	268⁸			
								0.09	0.06	9¹⁰		
		20	36.01⁴	36.02	27.37⁵	[-0.036, 0.046]	[-0.057, 0.081]	453⁹	367⁹	0.03	1.5¹²	
						0.102⁷	0.262⁷	0.19	0.08			
								204⁸	268⁸			
								0.05	0.03	18¹¹	1.5¹²	
		28	34.84⁴	34.85	32.33⁵	[-0.033, 0.034]	[-0.016, 0.277]	437⁹	368⁹	0.02		
						0.078⁷	0.203⁷	0.10	0.04			

¹ Percentage of resource utilization for target device; ² N/S=not specified; ³ FWHM of the residual; ⁴ Proposed TDCs' best resolution in this device; ⁵ Valid RMS resolution; ⁶ Approximate values from figures presented in literature; ⁷ Averaged peak-to-peak DNL or INL of multichannel TDCs. ⁸ Logic resource consumption without the C&C core per channel; ⁹ Averaged logic resource consumption with the C&C core; ¹⁰ CARRY8s; ¹¹ CARRY4s; ¹² BRAM consumption per channel.

comp.&cali. factors.(R2, comment 5) The resources required for the proposed TDCs are summarized in TABLE IV. It indicates our design is more hardware-effective compared with TDL-TDCs presented in Ref. [23], [39] and [42], and has similar logic resource consumption compared with the RO-TDC presented in Ref. [40] (a comparison shown in Table VI).

Implementation layouts in the UltraScale+ FPGA are shown in Fig. 10. Each "Input Shaper" is constrained near the corresponding GCO to minimize jitters introduced by routing resources. Moreover, DFFs are manually placed to enhance linearity. In the UltraScale+ FPGA, DFF groups are placed contiguously (SLICE XnYm and SLICE X(n+1)Ym) in a row.

In UltraScale and Virtex-7 FPGAs, DFF groups are placed at a fixed distance (SLICE XnYm and SLICE X(n+2)Ym).

Code density tests were conducted for 16-channel TDCs in three FPGAs. The linearity with different resolutions is summarized in TABLE V, showing the proposed TDC has high linearity and good uniformity.

IV. COMPARISONS AND DISCUSSIONS

TABLE VI summarizes recently published FPGA-TDCs and the proposed TDC. As shown in Table VI, the TDL-TDC is the mainstream design. Other advanced architectures like the ring-oscillator-based (RO-based) Vernier [40] and the nonuniform monotonic multiphase (NUMMP) architectures [41] were also

well-developed. However, we have further developed the new GCO-TDC architecture (firstly published in Ref. [36] by Xu and Wu).

Unlike high resolution (<10 ps) TDCs aimed for scientific applications, our design aims for multichannel industrial LiDAR applications with variable resolutions and high linearity. Compared with TDL-based and NUMMP-based TDCs for similar specifications (for example, a 20 ps resolution or high linearity), the proposed TDC is more efficient in hardware consumption. Our design uses only one-third LUTs and one-fifth DFFs compared with Ref. [23], and one-third LUTs and one-third DFFs compared with Ref. [41]. Although the RO-TDC in Ref. [40] has similar hardware consumption, its dead time is significant (maximum 602 ns). Although our GCO-TDC consumes slightly more logic resources than previously published GCO-TDCs [36], [38], [39], it is acceptable since the proposed TDC significantly improves both the resolution and linearity.

Although calibration methods like bin-by-bin calibration [50], bin-width calibration [29] and mixed calibration methods [32] can improve linearity and precision, they all need manual calibration. To achieve automatic calibration, gain and error calibration [43] and weighted calibration [44] methods are proposed. However, these designs only offer fixed resolutions. TDCs in Ref. [23], [41] and [42] provide flexible resolutions, but they all need manual configuration when resolution requirements change. To our knowledge, the VBCM is the first to achieve online resolution configuration and automatic calibration simultaneously in FPGA-TDCs. The C&C core serves 16 channels in this report but can serve more channels if required. Hence, the number of channels can be easily extended, and each channel's averaged logic resource consumption (with the C&C core) can be reduced. (R2, comment 6)

We use Verilog to implement the proposed TDC. As the GCO-TDC's resolution and linearity are sensitive to placing and routing strategies, it requires a few constraints to guarantee that GCO's placements and routes are immobile. Firstly, we used Vivado Tcl commands "set_property BEL" and "set_property LOC" to place LUTs and DFFs [51] manually and then used commands "set_property LOCK_PINS" and "set_property FIXED_ROUTE" to lock LUTs' input pins and fix routing resources, respectively [51]. We can verify the "Input Shaper", GCO and sampling matrix by post-implementation simulations and the C&C core by behavior simulations. Although the design of the proposed TDC is slightly more complex than TDL-TDCs, it is acceptable since our TDC with automatic calibration is hardware cost-effective, highly linear and resolution-configurable. (R1, comment 1; R4, comment 2-ii)

V. CONCLUSION

We proposed a new sampling structure, the sampling matrix, to enhance resolutions of GCO-TDCs. With this new structure, GCO-TDCs achieve excellent performances and low hardware consumption simultaneously. We also proposed the VBCM to achieve automatic calibration and online resolution configuration. Besides, the hardware implementation of this method is detailed in this paper, and it is hardware-efficient through multiplexing critical components.

To evaluate our design, we implemented the proposed 16-channel TDC in UltraScale+, UltraScale and Virtex-7 FPGAs, respectively. Experimental results indicate that the proposed TDCs have competitive linearity and excellent uniformity. Due to online resolution configuration, they can have broader applications in TOF-LiDAR, PET-CT, or time-resolved spectroscopy (such as Raman spectroscopy). It can also be utilized as a TDC-core in prototype designs or commercial products, benefiting from automatic calibration and low resource consumption.

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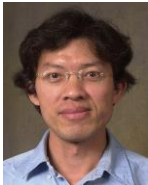


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