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A secure system integrated with DC-side energy storage for renewable generation applications

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ABSTRACT

Massive energy storage capability is tending to be included into bulk power systems especially in renewable generation applications, in order to balance active power and maintain system security. This paper proposes a secure system configuration integrated with the battery energy storage system (BESS) in the dc side to minimize output power fluctuation, gain high operation efficiency, and facilitate fault ride through, which is suitable for unidirectional renewable power generation systems (power transfer from renewable sources to the grid). The system utilizes robust diode units (DUs) to protect receiving-end devices against dc faults. Also, the BESS and half-bridge modular multilevel converter (MMC) at the receiving end can operate safely and flexibly to achieve stable and high-quality power transfer, in both source power intermittency and dc-link fault cases. Depending on BESS sizing, the source system power fluctuation can be reduced (absorbed by the receiving-end BESS) when a receiving-end grid fault occurs. Topological configuration and control design of the proposed system are presented. Simulation results show the effectiveness of the proposed system in both dc and ac fault cases, with power fluctuation elimination functionality highlighted. The receiving-end operation losses are investigated, showing a high-efficiency system. In addition, key system implementation considerations regarding the proposed system are elaborated.

1. Introduction

Development of energy storage systems (ESSs) is desirable for power system operation and control given the increasing penetration of renewable energy sources [1,2]. With the development of battery technology, the battery ESS (BESS) becomes one of the most promising and viable solutions to promptly compensate power variations of larger-scale renewables for a predetermined duration [3]. Also, manufacturing advances are enabling more massive storage integration into the power converter station with proper isolation and protection [4].

However, integrating the BESS into a grid for high-voltage/power applications is challenging, not only due to capacity and cost concerns, but also uncertainty of integration schemes [5,6]. First, large voltage and power differences between a single energy storage cell and the high-voltage systems should be addressed [7]. Energy storage cells can be scaled up to form larger packages, where management systems are essential. However, such scalability has limitations and package-level design/management is critical in order to meet requirements of higher voltage/power applications [8]. In addition, although conventional power electronic converters enable direct and centralized dc-side integration of the energy storage packages (such as applications in [9]), the limited voltage rating of single semiconductor switch is posing challenges on the realization of high power/voltage dc-ac conversion systems. Second, the battery energy storage cells have tight operation condition requirements (in terms of temperature, current, etc.), which should be met by the management/regulation systems to avoid performance degradation and safety issues [10].

Therefore, designing the overall ESS in a modular way is desirable, as modularization can, not only solve the voltage mismatch issue, but effectively provide redundancy and achieve submodule (SM) level management of the key factors, such as state of charge (SoC), state of health (SoH), and even package faults. Various approaches of massive ESS construction and integration have been proposed based on different modular converter topologies, for both ac and dc high-voltage systems. However, there are still research gaps regarding the suitable topology for ESS integration.

The cascaded H-bridge (CHB) converter allows its full-bridge (FB) SMs (integrated with energy storage packages) to be connected in series in order to synthesize a multi-level ac voltage for its tied ac system [11].

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Nomenclature

C_{BESS}	Battery energy storage system (BESS) submodule (SM) interfacing circuit capacitor, F
C_{MMC}	Modular multilevel converter (MMC) SM capacitor, F
E_{off}	Generic semiconductor turn-off energy losses, J
E_{on}	Generic semiconductor turn-on energy losses, J
E_{rec}	Generic diode recovery losses, J
f_s	BESS/MMC equivalent switching frequency, Hz
i_{ac}	Point of common coupling (PCC_2) current, A
$I_{ac\text{-}d}$	PCC_2 *d*-axis current in *dq*-frame, A
$I_{ac\text{-}q}$	PCC_2 *q*-axis current in *dq*-frame, A
i_{ARM}	MMC arm current, A
I_{dcA}	Sending-End station dc current, A
I_{dcBESS}	BESS dc current, A
I_{dcD}	Receiving-End station dc current, A
I_{dcMMC}	MMC dc-side current, A
i_{SEMI}	Generic semiconductor on-state current, A
L_{Bat}	BESS SM interfacing circuit inductor, H
L_{BESS}	Receiving-End station BESS filtering inductor, H
L_{LLC}	Line-Commutated converter (LCC) dc inductor, H
L_{MMC}	MMC arm inductor, H
M	BESS SM number
$m_{BESS}^{(*)}$	BESS modulation index
M_P	BESS parallel battery cell number per SM
M_{P1}	BESS parallel battery cell number per SM determined by power rating
M_{P2}	BESS parallel battery cell number per SM determined by energy capacity rating
M_S	BESS series battery cell number per SM
N	MMC SM number per arm
N_{ARM}	MMC SM selection profile/number
N_{DU}	Diode unit (DU) series diode number
P_{DU}	DU power losses, W
P_{BESS1}	BESS battery power losses, W
P_{BESS2}	BESS semiconductor conduction losses, W
P_{BESS3}	BESS semiconductor switching losses, W
$P_{DIODE1C}$	MMC arm HB SM upper diode conduction losses, W
$P_{DIODE1S}$	MMC arm HB SM upper diode switching losses, W
$P_{DIODE2C}$	MMC arm HB SM lower diode conduction losses, W
$P_{DIODE2S}$	MMC arm HB SM lower diode switching losses, W
P_{IGBT1C}	MMC arm HB SM upper IGBT conduction losses, W
P_{IGBT1S}	MMC arm HB SM upper IGBT switching losses, W
P_{IGBT2C}	MMC arm HB SM lower IGBT conduction losses, W
P_{IGBT2S}	MMC arm HB SM lower IGBT switching losses, W
P_{MMC1}	MMC semiconductor conduction losses, W
P_{MMC2}	MMC semiconductor switching losses, W
P_{SEMIS}	Generic semiconductor switching losses, W
R_{Bat}	BESS battery cell internal resistor, Ω
R_{SEMI}	Generic semiconductor on-state voltage drop constant, Ω
SOC_{BESS}	BESS state of charge value, %
T	AC grid fundamental period, s
v_{ac}	PCC_2 ac voltage, V
V_{ac}	PCC_2 voltage amplitude, V
V_{Bat}	BESS SM battery package voltage, V
V_{Batmax}	BESS SM maximum battery package voltage, V
V_{Batmin}	BESS SM minimum battery package voltage, V
V_{BESSSM}	BESS SM battery package voltage for losses estimation, V
V_{dcA}	Sending-End station dc terminal node A voltage, V
V_{dcC}	Receiving-End station node C voltage, V
V_{dcD}	Receiving-End station node D voltage, V
V_{DU}	DU forward-biased voltage, V
V_{DIODE}	IGBT's diode conduction voltage, V
V_{IGBT}	IGBT conduction voltage, V
v_{MMC}	MMC ac-side voltage, V
V_{MMCSM}	MMC SM rated voltage, V
V_{SEMI}	Generic semiconductor on-state voltage drop, V
V_{SEMI0}	Generic semiconductor on-state voltage drop constant, V

Greek letters

α	LCC firing angle, °
ω	Rotational speed, rad/s

However, the CHB SMs suffer from large ac current fluctuation in the normal operation, as the instantaneous power of each phase is a dc value (average power input/output) plus a second-order harmonic, which will either require bulky and costly interfacing circuits or significantly increase operation losses and reduce lifetime of the integrated energy storage cells [12].

The modular multilevel converter (MMC) is another popular candidate for such split energy storage deployment [13,14]. By integrating energy storage packages into the MMC SMs, the concept of an energy storage static synchronous compensator emerges, with both active and reactive power provision capabilities for the ac network. However, from the perspective of batteries, low-order harmonic components exist in each leg/arm/SM during the MMC normal operation, leading to high power ripple and jeopardizing the energy storage cells [14]. Similarly, tackling the low-frequency ripple issue requires extra interfacing circuits (either passive or active power filters) and additional design margin [6].

To avoid the design complexity related to instantaneous power fluctuation of ac systems, ESSs can be shunt-connected to the dc bus via series half-bridge (HB) SMs in scenarios where a dc link is available/created. In this way, the merits of modularity (in terms of SM-based battery management) is maintained, whilst the output voltage can still be scaled up to high levels [15,16].

On the other hand, the dc system (at medium and high voltage levels) provides an attractive way to integrate and transfer renewable energy sources. Nevertheless, the dc link may suffer from faults especially when overhead lines are used. Due to the low dc impedance and the lack of voltage/current zero-crossing points, addressing dc faults is challenging in dc transmission applications. DC breakers can isolate the fault but are costly and require mechanical switches [17]. Most dc-fault tolerant MMCs have lower efficiency than the HB SM based type [18]. Thyristor-based line-commutated converters (LCCs) have dc-fault resilience capability but are susceptible to commutation failure if used as an inverter [19].

Some research focuses on a unidirectional hybrid HVDC system where LCC and HB SM based MMC systems are deployed at the sending and receiving ends respectively [19]–[21]. As evaluated in [20], the series-connected diodes in the dc link can not only clear the dc fault current but also eliminate the danger of overcurrent at the receiving-end MMC (conventional HB SM based MMCs suffer from dc faults due to the topological characteristics). However, although the unidirectional hybrid HVDC system, without ESS integration, can successfully ride through the dc fault, negative effects on the receiving end in terms of intermittent renewable generation and active power interruption are not addressed, which could result in huge power variation for the grid. For the load systems, such sudden power fluctuation is detrimental to system safety and security [22].

Therefore, considering both the ESS integration challenges and the dc system characteristics, this paper proposes a unidirectional dc system integrated with an independent dc-side shunt-connected BESS at the receiving end, to improve system security for renewable energy integration applications. At the sending end, a fault-tolerant converter (such as the LCC) can be used to transmit low-cost and high-efficiency

renewable power of the source system. At the receiving end, dc-link series diode units (DUs) can ensure simple and effective dc-fault resiliency, while the dc-ac conversion (active power injection and ac grid support) is achieved by the HB SM based MMC. Importantly, the proposed HB SM based BESS, with high scalability and modularity, can smooth active power flow in both renewable generation intermittency and connected-system ac/dc fault cases. Uninterruptable active power provision (from either the renewables or BESS, depending on system circumstances) to the load system (grid) can be ensured. Thus, not only the system itself can be protected, but the power supply security can be significantly improved, against the external operation factors (generation fluctuation, source-side system fault, dc link fault and load-side system fault). As the BESS is integrated in the dc side, no low-frequency ac power oscillation should be considered; thereby simplifying BESS design/management and improving operation efficiency. Time-domain simulation verifies the proposed system; whereas major part losses under the rated operating conditions and system operation efficiency under different power-sharing conditions are analyzed. System implementation and operational features are also discussed.

The remainder of this paper is organized as follows. In Section 2, the system configuration is discussed, including specific considerations of BESS management and sizing. Typical operation cases and control system design are presented in Section 3. Section 4 details a design case, and illustrates simulated performance during dc-link and ac grid faults, verifying the proposed system effectiveness. Section 5 presents operation efficiency of the receiving-end converter system, considering different operational conditions, and Section 6 gives a discussion on system implementation and operation features. Conclusions are given in Section 7.

2. System configuration and BESS sizing

The proposed dc transmission system is illustrated in Fig. 1. Typical unipolar (positive pole to ground) dc system configuration is adopted in line with [23]; whereas different dc system grounding configurations are feasible, as detailed in [24]. The renewable source power is transmitted via a sending-end rectifier. The dc link can be realized by overhead lines or cables depending on various factors. Normally, with higher fault current rating and lower investment, overhead lines are utilized, however, this means that the system has to tolerate dc faults. The receiving-end station has three major parts, namely, the DU, the BESS, and the MMC, which can operate coordinately to inject smooth active power into the grid.

A. Sending-end station (rectifier)

Various high-power converter systems based on LCCs [20], MMCs [25] and diode rectifiers [26], can be utilized as the sending-end station to transmit dc current I_{dcA} by regulating the dc terminal voltage V_{dcA}. LCC technology could be justified due to its maturity, lower cost, dc-fault resiliency, and high efficiency [22]. MMCs are a competitive alternative but a dc-fault protection/tolerant configuration should be considered, such as those in [27,28]. Given this analysis, this research takes the LCC as an example, where the dc-fault current would be simply controlled by the firing angle, even during the faults.

B. Receiving-end DU

The DU in the receiving-end station is used to protect the BESS and MMC against dc-link faults as in [20]. The diode anode is connected to station dc port (point C), and cathode is connected to node D, with BESS and MMC.

In normal operation, the DU is forward-biased, carrying the rated a dc current with minor conduction losses ($V_{DU} \times I_{dcD}$). When dc fault occurs in the dc transmission line, the series DU goes through a negligibly short reverse recovery period (the duration is mainly determined by diode characteristics and external current flow) and becomes reverse-biased, thereby gaining the reverse blocking capability to effectively maintain node D voltage V_{dcD} and stop the dc fault propagation. Thus, the steady-state DU current (I_{dcD}) cannot be negative, whereas BESS and MMC are protected against a dc-link fault. Basic voltage relationship regarding DU operation is:

$$V_{DU} + V_{dcD} = V_{dcC} \tag{1}$$

During dc faults, the reverse-biased DU should be able to withstand the voltage different between the node D (V_{dcD}, which would be maintained) and the point C (V_{dcC}, which would be induced by transmission link de-energization and oscillates towards zero). Also, parallel resistors and snubber circuits are used to equalize the high voltage, and surge arresters are to absorb stray energy for transient protection.

C. Receiving-end MMC

An HB MMC is used in the receiving end to inject decoupled active and reactive powers into the grid and ride through the ac grid fault, exactly as the normally deployed MMCs. The MMC dc-side positive port is connected to point D and its ac side is connected to the grid point of common coupling (PCC_2) via an interfacing transformer (T_2). Each arm of the MMC consists of N SMs (with HB and C_{MMC}) and an arm inductor L_{MMC}. With the MMC ac-side voltage source characteristics, it has black-start and grid-forming functions, which are helpful for the grid. This will be the case especially when the dc-side power generation becomes controllable, which is achieved by the BESS.

D. Receiving-end BESS

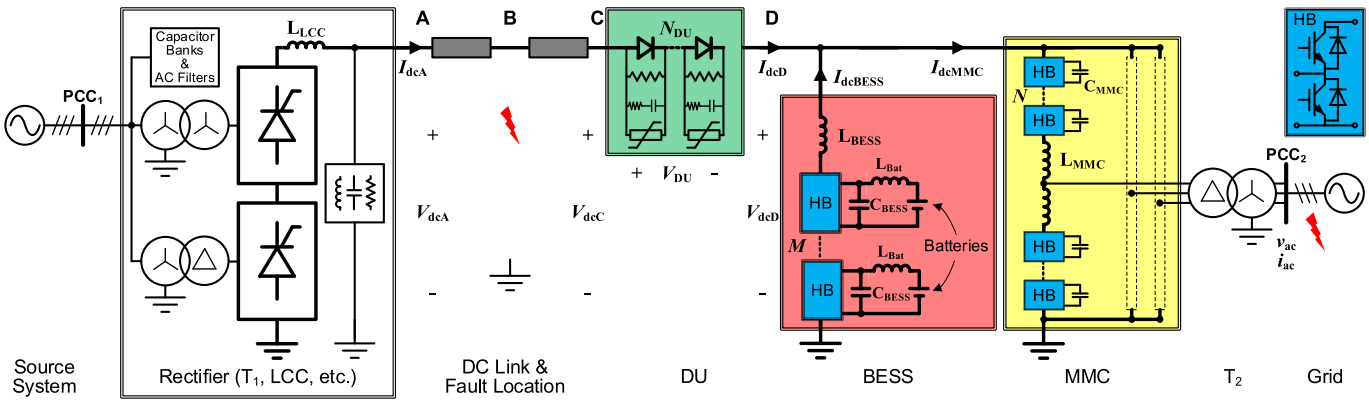

Fig. 1. Schematic diagram of the proposed system (rectifier converter topology is optional).

Being rail-to-rail shunt-connected with the node D of the dc bus, the BESS in the receiving-end station mainly consists of M HB-based SMs and a filtering reactor L_{BESS}. Within each HB SM, an interfacing circuit based on a capacitor and an inductor (C_{BESS} and L_{Bat}) is used between the HB SM and the integrated battery (package) to suppress transient voltage/current over/through the battery, which is desirable in terms of both safety and longevity. As the interfacing circuit is for high-frequency oscillation suppression during transients, C_{BESS} and L_{Bat} values/volumes could be much smaller than those used for low-order harmonic power smoothing [6]. Therefore, depending on the engineering circumstances, L_{Bat} could be stray or an air-core inductor, and C_{BESS} serves as a snubber. Also, all critical inner-SM variables can be locally measured and transmitted to the higher-layer controller(s), with no common-mode voltage involved. The main functions of BESS chain inductance L_{BESS} are to reduce high-frequency current ripples caused by pulse width modulation (PWM) action, and to control the dc current I_{dcBESS}. Various PWM techniques applicable to multilevel converter topologies can be used to synthesize the required dc terminal voltage for its tied dc system, while SM-level voltage balancing can be assured [16].

The high modularity provided by the HB SM based configuration enables not only scalable design/sizing for the targeted dc system, but flexible and effective BESS management.

In terms of BESS design/sizing, the battery within one SM is constructed by connecting small battery cells, and the series and parallel cell numbers per HB SM (M_S and M_P) are highly dependent. It is assumed that the battery cells within one HB SM battery package can be properly balanced and managed by manufacture. Essential aspects regarding BESS sizing are as follows:

1) *Battery voltage range and SM number (BESS voltage)*

The SM voltage (SM-level battery package) is constructed by M_S series-connected battery cells and is usually further defined by the manufacture with the main concern of consistency. During operation, the battery package voltage varies within an allowable range for performance and safety purposes. The maximum and minimum battery package voltages (V_{Batmax} and V_{Batmin} respectively) must be within the range between the battery charge and discharge cut-off voltages, whereas conservative margins are suggested considering measurement error, SoC, battery condition, etc. Also, the predefined minimum voltage V_{Batmin} is chosen to quantify the BESS minimum output voltage ($V_{Batmin} \times M$, without considering redundancy), which should be at least equal to the dc-link voltage (the rated V_{dcD}) to meet the basic BESS voltage requirement.

2) *Battery charge and discharge currents (BESS power)*

Battery cells have different charge and discharge currents, and the maximum limits should be strictly obeyed in order to achieve safe operation and expected lifetime. The parallel-connected battery cells per HB SM M_P can be partially determined by the power rating, as M_{P1}. Usually, discharge current is higher than charge current, indicating that the BESS has higher active power compensation ability in the proposed system. In particular, in order to fully compensate the rated power (receiving-end MMC remains rated power injection even when the source system power output is zero), the BESS discharge current should be at least equal to the rated dc current.

3) *Battery stored energy (BESS capacity)*

Battery stored energy should be monitored to determine BESS capacity. Both source and grid power profiles should be analyzed or estimated to determine the expected BESS operation boundaries (power and duration). Sizing optimization approaches for specific applications involve quantization of objective identification and short and long term characterization, as studied in [3,29]. Such required BESS energy capacity gives another quantitative factor when calculating the parallel-connected battery cells per HB SM, as M_{P2}.

Thus, to achieve normal operation, the minimum values of series cell and SM numbers (M_S and M) mainly depend on the rated BESS voltage requirement as above; whereas redundant SMs can be added for purposes of managing energy storage packages and increasing overall reliability. Besides, the selection of the minimum value of M_P mainly depends on the required BESS power and energy capacity, as $M_P = \max(M_{P1}, M_{P2})$, indicating an acceptable BESS sizing consideration.

From the perspective of BESS management, the proposed modular structure is beneficial for inner-SM battery regulation, inter-SM consistency, and redundancy configuration. Firstly, measurement of critical variables of the large amount of battery cells can be realized in a hierarchical manner, therefore monitoring all cells is achievable (divided by different SMs). Also, with such an SM-based configuration, SM-level battery states (such as voltage, SoC, SoH, etc.) can be summarized. As activating, bypassing and blocking the SMs are flexibly achieved by manipulating the HB semiconductors, individual HB SM/battery can be easily selected/bypassed to attain high (voltage and/or SoC) consistency among different SMs/packages. Thirdly, redundancy design and operation can be easily implemented (similar to the MMC configuration, with SMs adopted/selected/bypassed for hot or semi-hot standby [30]), therefore the overall BESS reliability can be significantly improved. Conclusively, modularity feature of the proposed system is attractive for battery-oriented applications especially considering the operational safety.

Currently, the lithium iron phosphate ($LiFePO_4$) battery is mainstream in massive energy storage applications [14], whereas either new or repurposed batteries can be utilized theoretically as long as sizing and consistency requirements are met.

3. System operation and control

In this section, operation modes of the proposed system are discussed with highlighted characteristics in terms of security. Also, control system of the major parts within proposed system is presented, including both normal and fault cases.

A. Operation cases and system security

The receiving-end system operation can be illustrated by the simplified model in Fig. 2, where the operation cases are as follows:

1) *Normal case*

The sending-end rectifier controls its dc-side current I_{dcA}, flowing through the DU as I_{dcD}, whereas the BESS injects current I_{dcBESS}. Thus, the MMC dc-side current I_{dcMMC} is:

$$I_{dcMMC} = I_{dcD} + I_{dcBESS} \tag{2}$$

Also, the MMC can generate a controlled dc-side voltage while its ac-side output voltage v_{MMC} is synthesized to control the current injected into the grid. As the dc-link voltage is controlled by the MMC, I_{dcBESS} can also be flexibly adjusted to regulate battery SoC.

2) *Power-fluctuation case*

Given a controlled dc-link voltage (V_{dcD}), the intermittent renewable sources will lead to fluctuating power and dc-link current (I_{dcA} and I_{dcD}). The integrated BESS is able to compensate the power curtailment and ensure a constant I_{dcMMC} (thereby active power) for the MMC, ensuring the security of its connected grid.

3) *Source-system fault case*

Any installed sending-end rectifier should ride through this fault

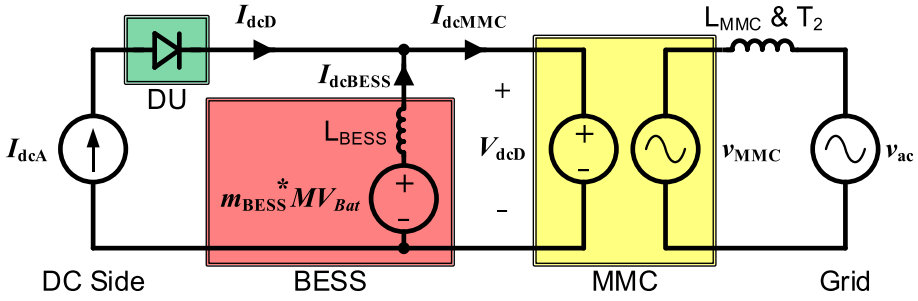

Fig. 2. Receiving-end analytical model.

before the fault is cleared. In such a case, the source output power might be reduced, which is similar to the previous power-curtailment case, and the proposed system is therefore able to maintain the grid security.

4) *DC-link fault case*

Sending-end rectifier should ride through the fault with corresponding approaches as the requirements aforementioned. For the receiving end, a solid dc fault can be viewed as an extreme case of source power fluctuation, due to the protective DU. Thus, the proposed system can ride through the dc fault, and the protected BESS is also required to provide the rated dc current for the MMC, thereby maintaining secure power supply for the load system.

5) *AC-grid fault case*

When an ac fault occurs in the ac network, the injectable ac power into the grid might be reduced to some extent, mainly depending on the ac voltage drops and MMC current capacity. The MMC is able to ride through the ac fault and even provide reactive current to support the grid. However, load-side faults may affect the normal power flow of source-side system and pose challenges on the source and dc system regulation. Optionally, the BESS can be controlled to absorb some or all of the non-transferable source/dc power (relying on the battery charge capacity) to minimize fluctuation at the sending end under this condition.

Therefore, the proposed secure system can not only ride through all kinds of faults (both ac and dc faults), but ensure an uninterrupted active/dc power provision/compensation for its connected systems during the faults.

B. Control design

Based on the operation analysis previously mentioned, control systems for each installed equipment can be designed as follows:

1) *Sending-end rectifier*

The dc current I_{dcA} is controlled by the sending-end rectifier through the terminal voltage V_{dcA}. Taking an LCC as an example, the V_{dcA} is changed by adjusting its firing angle. During dc faults, the LCC (with the firing angle shifted to be much greater than 90°) can operate as an inverter to quickly reduce the dc current.

2) *Receiving-end BESS*

The BESS controller is illustrated in Fig. 3, where a mode switch is used to change the BESS between MMC dc-current control and SoC control modes and the mode-switching action is mainly determined by BESS SoC. Both modes are based on a BESS dc current controller, which regulates the output current I_{dcBESS} via the modulation index m_{BESS}^{*}. To avoid over-current, reference saturation setup for both charge and discharge currents is needed. When the BESS SoC is within a predetermined range (for example, 5%–95%), the BESS operates in MMC dc-current control mode, where the BESS regulates its dc current contribution based on Eq. (2) to allow a controlled MMC power injection, while an ac voltage level detection mechanism enables fast injected power reduction during ac grid faults. In this mode, the reference I_{dcMMC}^{*} is determined by various system-wise factors such as the grid frequency, mission profiles, renewable prediction, etc., which can be managed and optimized by the system operator. The BESS SoC control mode can be triggered when the SoC is out of the predetermined range, indicating that the BESS is not able to participate into system regulation (insufficient energy capacity to supply or store the power). In this mode, the BESS is controlled by the BESS SoC PI controller with low gains to sink or source a minor dc current to regulate SoC in a closed-loop

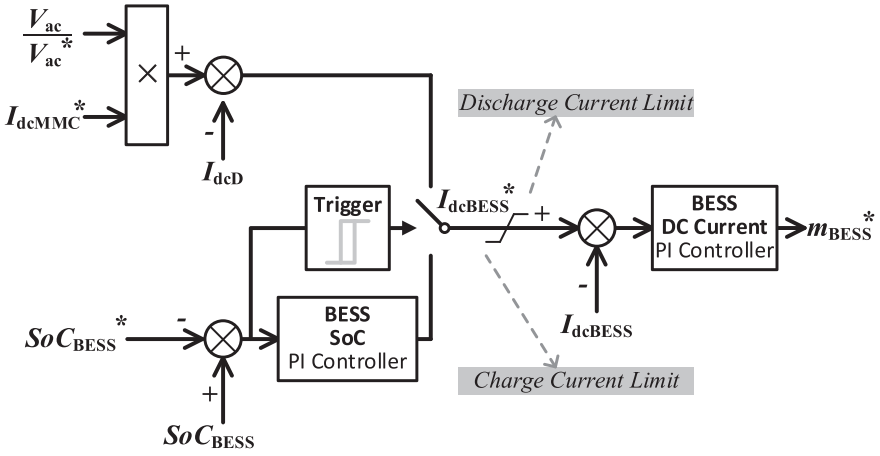

Fig. 3. BESS control system diagram.

manner. This mode can be used for BESS initialization, reactivation and restoration from extreme cases. Normally, the system operator can employ the BESS in the MMC dc-current control mode properly while keeping the BESS SoC within the limits. More detailed operation rules are beyond the scope of this paper.

3) *Receiving-end MMC*

The basic MMC control is shown in Fig. 4, where the vector current control based on *dq*-frame is used to regulate the PCC_2 currents. The MMC can control its dc-side and PCC_2 voltages (V_{dcD} and V_{ac}) with the *dq*-axis currents respectively. MMC internal control, which involves capacitor voltage control, circulating current control, etc., can be referred to [31]. Given the changeable reference I_{dcMMC}^*, advanced control (such as grid-forming functionality) is applicable.

Thus, with the installed BESS, the MMC connected to PCC_2 can inject smooth and uninterrupted active power into the grid, with optionally advanced frequency management function by manipulating I_{dcMMC}^*. Also, the grid voltage can be supported by reactive current provision.

4. Case study and time-domain simulation

To verify the proposed system, a practically oriented case study is investigated, with components and parameters listed in Table I. Positive power flow is defined from the source system to the grid, whilst system configuration and voltage/current directions are indicated as in Fig. 1. The MATLAB/Simulink-based model is built to verify the system time-domain performance.

The source system is assumed to be a strong grid given the sufficiency sources and conventionally nearby-deployed reactive power compensator (and harmonic filters), whereas the load grid is assumed to be weak with a SCR = 3. At the sending end, an LCC is used as the rectifier, with its dc current controlled by a PI controller in a closed-loop manner (based on Section 3-A). The series-connected diode number within the DU in the dc link is mainly determined by the required voltage level during extreme system dc fault cases and the diode supportable reverse voltage [32], with a relatively large margin adopted given its criticalness in the dc fault cases. The BESS HB SM is rated at 550 V, thus 1.2 kV IGBT types can be selected with sufficient current capacity, as given in [33]. The equivalent PWM frequency for the aggregated BESS is 5 kHz considering system dynamics and ripple. The BESS is sized based on the discussion in Section 2-D, with design margins included. The BESS battery is modelled based on the MATLAB/Simulink battery (Lithium-ion) block library with parameters from the manufacture of the selected type [34]. The BESS control system adopted for simulation is based on the structure presented in Section 3-B. Given the 2 kV rated voltage of the MMC HB SM, 4.5 kV IGBTs are utilized with current capacity considered [35]. Similarly, the equivalent PWM frequency for the MMC is chosen to be 5 kHz, with average MMC arm modelled. The modelled

Table I
Parameters of the studied system.

Part	Item	Value
Source System & Rectifier (LCC)	Source system frequency	50 Hz
	Source voltage (L-L rms)	33 kV
	Source system SCR and X/R	10, 10
	T_1 power rating	55 MW
	T_1 voltage (Y/Y/D)	33/21/21 kV
	T_1 leakage inductance	0.18 pu
	T_1 resistance	0.01 pu
	DC inductance L_{LLC}	200 mH
	DC filter (capacitance)	1 μF
DC Link	DC (pole-to-ground) voltage rating	50 kV
	Rated dc power P	50 MW
	Line length A to B (5 π-sections)	25 km
	Line length B to C (5 π-sections)	25 km
	Resistance	12.73 mΩ/km
	Inductance	0.9337 mH/km
	Capacitance	12.74 nF/km
DU	Diode part No.	D2601NH90T [32]
	Series diode No. N_{DU}	25
BESS	Power rating (output/discharge)	50 MW
	filtering reactor inductance L_{BESS}	8 mH
	HB SMs No. per BESS M	110
	Equivalent switching frequency f_s	5 kHz
	HB SM IGBT Part No.	FF1400R12IP4 [33]
	HB SM capacitance C_{BESS}	40 μF
	HB SM inductance L_{Bat}	1 μH
	Battery cell type	PSL-FP-IFP36130200EC [34]
	Series battery cell No. per HB SM M_S	157
	Parallel battery cell No. per HB SM M_P	5
	Energy capacity	27.6 MWh
MMC & Grid	MMC HB SM No. per arm N	25
	Equivalent switching frequency f_s	5 kHz
	HB SM IGBT Part No.	FZ1200R45KL3_B5 [35]
	MMC HB SM rated voltage	2 kV
	MMC HB SM capacitance C_{MMC}	5 mF (30 kJ/MVA)
	MMC arm inductance L_{MMC}	25.9 mH
	T_2 power rating	55 MW
	T_2 voltage (D/Y)	27.5/33 kV
	T_2 leakage inductance	0.18 pu
	T_2 resistance	0.01 pu
	Grid frequency 1/T	50 Hz
	Grid voltage (L-L rms)	33 kV
	Grid SCR and X/R	3, 10

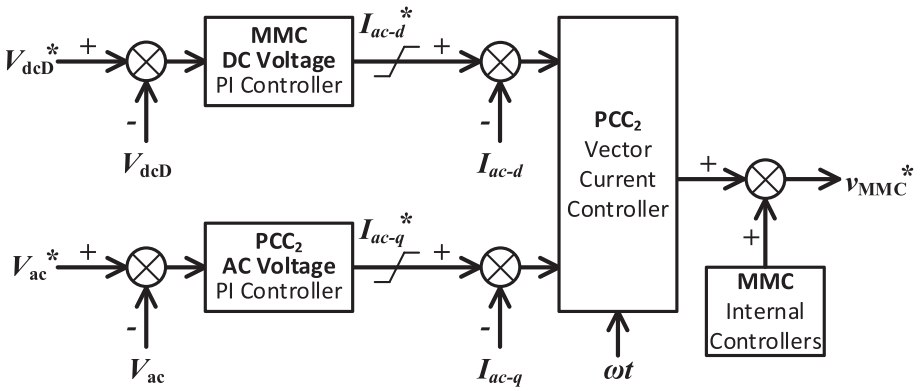

Fig. 4. MMC control system diagram.

MMC control system is in line with that presented in Section 3-C.

A. DC-link fault

The resiliency against source/dc-side contingencies (including source power fluctuation, source system fault and dc-link fault) is critical for system security. A solid dc-link fault is the most extreme case (as power transfer is nullified in a very short period) with the most severe system dynamics; therefore, the dc-link solid fault case is used to verify the effectiveness of system security against source/dc-side contingencies.

In the simulation, a pole-to-ground dc fault caused by 0.1 Ω fault resistance occurs at point B marked in Fig. 1, from 1 s to 1.2 s. Fig. 5 shows the system performance.

For the sending-end rectifier, the dc fault causes slight overcurrent (I_{dcA}) for a short duration, and the LCC firing angle α is rapidly changed to 150° to reduce the dc current I_{dcA}, as shown in Fig. 5(a) and (b). After the fault is cleared, the I_{dcA} is controlled to rise to the rated value in about 0.1 s, whereas the LCC α returns back to around 14°, as in the normal case.

The receiving-end dc voltage at point C V_{dcC} collapses dramatically with damped oscillations due to the dc lines, while the DU withstands a reverse voltage of about 1.5 pu (due to the dc link stray parameters) after a short reverse recovery period, thereby preventing dc voltage at point D V_{dcD} from collapsing in all cases, see Fig. 5(c)–(e). The fault current from the receiving end is eliminated quickly while the related energy could be absorbed by arrestors/snubbers. During the fault, all components remain safe and operative.

As the dc-link power from the sending end is not available during the fault, point D dc current I_{dcD} is nullified. The MMC dc current I_{dcMMC} is then rapidly compensated by the BESS based on the control system in Fig. 3, as shown in Fig. 5(f)–(h). Thus, during the fault, the BESS outputs near 1 pu dc power to the MMC, with its measured SM average voltage reduced slightly, due to battery internal resistance. When the fault is cleared, BESS SM voltage recovers and the BESS SoC decreases slightly indicating a minor stored energy reduction, as displayed in Fig. 5(i) and (j). Basically, the BESS compensates the lost power from the dc link and maintains a near constant MMC active power output for the grid, while the MMC ac output current and SM voltage are marginally affected during the dc fault.

In conclusion, the proposed system can ride through dc faults with on negative effect on the normal active power provision into the grid; thus, the grid security is achieved. It can be projected that the BESS can support the system for longer durations, mainly depending on its SoC (and predetermined capacity). Also, as the dc-link fault is the most extreme generation nullification case, the BESS can support the grid in a similar way during renewable power-fluctuation and source-system faults, which are less severe cases for both the proposed system and the load grid.

B. AC grid single-phase fault

AC faults that occur at the grid will result in dropped voltage, thereby reducing system transferrable power from the receiving-end MMC into the load system. The proposed system can minimize the active power variation by compensating dc power, in order to reduce regulation challenges on the source system.

In the simulation, a single-phase ac fault with a 0.1 Ω fault resistance occurs at PCC_2 in Fig. 1, from 1 s to 1.2 s. Fig. 6 shows the performance of the proposed system.

At the grid side, the fault impairs MMC normal active power transfer, and causes higher ac current (limited by MMC control), as shown in Fig. 6(l)–(n). Also, the MMC capacitor voltages are regulated during the fault, see Fig. 6(o). The MMC dc-side current is controlled by the BESS and maintained in line with the ac positive-sequence voltage amplitude, whereas the BESS participates in power balancing by absorbing a certain amount of dc current (within the absolute charge current limit), as shown in Fig. 6(g) and (h). When the BESS absorbs power during the fault, its SM average voltage increases due to the internal resistance, and the SoC increases slightly, see Fig. 6(i) and (j). The negative BESS power output during the fault indicates that it sinks extra power that cannot be injected into the grid. Thus, the receiving-end of the dc transmission system maintains its dc-side voltage (V_{dcD}) and current (I_{dcD}), with the DU conduction status unchanged, as shown in Fig. 6(c)–(f). For the sending-end LCC rectifier, the dc output current is dynamically regulated, see Fig. 6(a) and (b).

In conclusion, the MMC, which is limited by its current capacity, cannot inject more power to support the grid during ac grid faults,

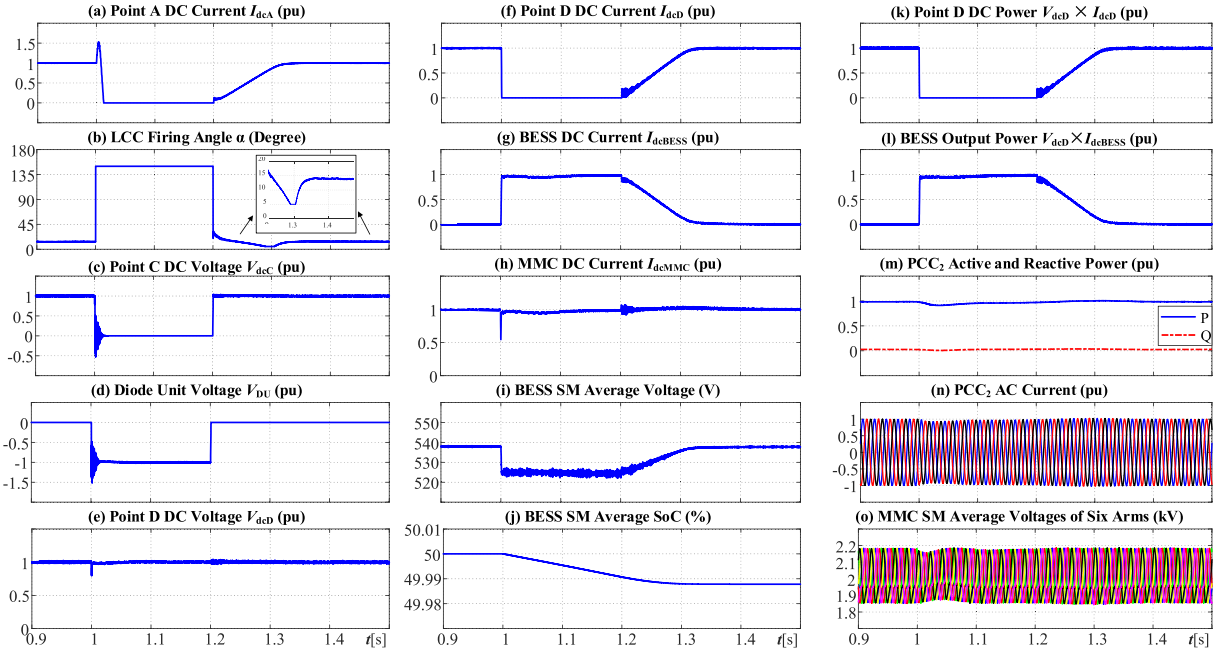

Fig. 5. System performance in the dc-link fault case.

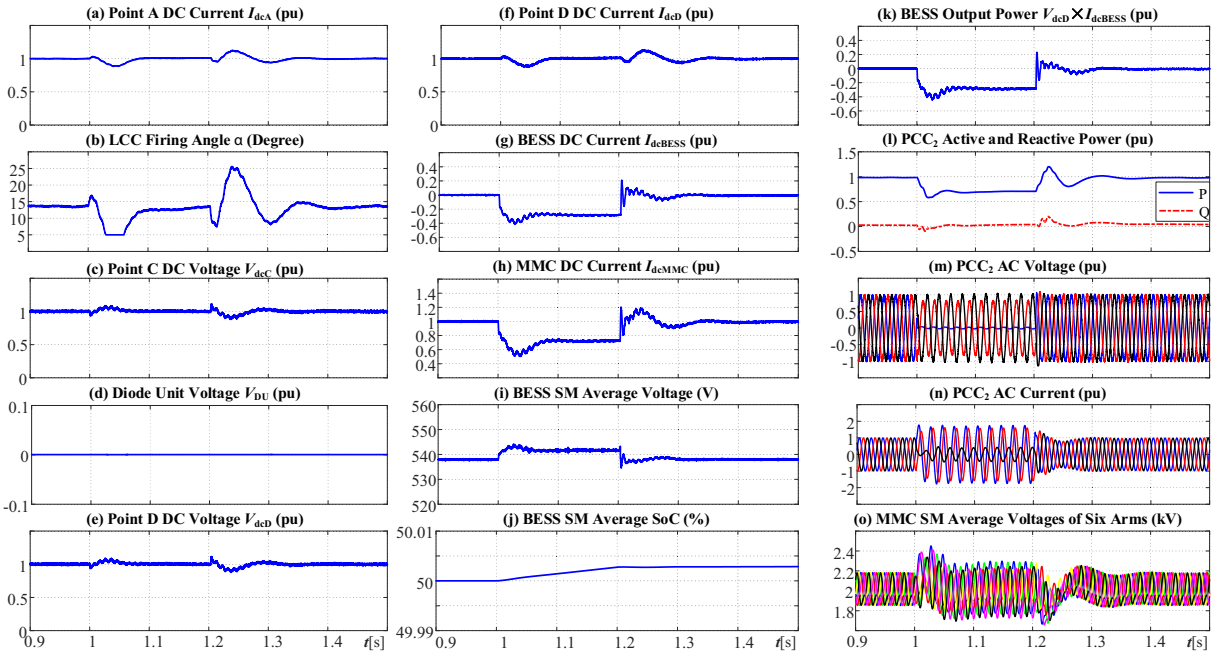

Fig. 6. System performance in the ac grid single-phase fault case.

whereas grid security is maintained by well-established ac circuit breaker based protection. The proposed system can ride through the grid fault case, while the BESS can mitigate the impact of the reduced grid-side power consumption on the sending end by charging its integrated batteries. Also, it can be anticipated that the BESS can store source generation for a longer duration, mainly depending on SoC.

5. Receiving-end operation efficiency analysis

The sending-end terminal of the proposed system can be either a mature or customized converter, wherein the operation efficiency varies. The transmission link losses are also highly dependent. This section focuses on loss estimation and the case study based efficiency analysis for the receiving end of the proposed system.

A. Loss estimation method

For loss estimation of power converter systems, it can be reasonably assumed that: 1) System operates with constant dc voltage/current and sinusoidal ac voltage/current; 2) Modulation signals are linear; 3) Losses are equally distributed within each part; 4) Semiconductor characteristics are linearly and piecewise represented under the typical condition; 5) Battery condition is as initial; and, 6) Minor losses of auxiliary/protective circuits are not considered [6,18].

First, in order to calculate the generic semiconductor (IGBT or diode) conduction losses, on-state voltage drop is required and can be expressed as:

$$V_{SEMI}(i_{SEMI}) = V_{SEMI0} + R_{SEMI}\, i_{SEMI} \tag{3}$$

where, V_{SEMI0} and R_{SEMI} are the constants obtained from the piecewise on-state characteristics of the generic IGBT/diode; and i_{SEMI} is the on-state current, which varies in different devices and operation cases (details are referred to [36]). Also, the switching loss of the a generic IGBT semiconductor device can be estimated based on the average switching energy losses (mainly determined by the IGBT voltage V_{SEMI} and current i_{SEMI}) as:

$$P_{SEMIS}(V_{SEMI}, i_{SEMI}) \approx f_s \left[E_{on}(V_{SEMI}, i_{SEMI}) + E_{off}(V_{SEMI}, i_{SEMI}) + E_{rec}(V_{SEMI}, i_{SEMI})\right] \tag{4}$$

where, f_s is the switching frequency; E_{on}, E_{off} and E_{rec} indicate the turn-on, turn-off and diode recovery energy losses, determined by the IGBT characteristics and operation conditions during switching (details are referred to [37,38]).

For the studied case, three major parts, viz., DU, BESS and MMC, are considered as follows:

1) *DU*

The DU switching loss is zero in normal operation. Thus, the dc-link current I_{dcD} and DU on-state characteristics determine the DU total power (conduction) loss P_{DU} [36] as:

$$P_{DU} \approx V_D(I_{dcD})\, I_{dcD}\, N_{DU} \tag{5}$$

where V_D indicates the conduction voltage drop of the adopted diode as given in Eq. (3). DU reverse blocking occurs mainly in dc-fault cases; it therefore has marginal effects on the system operation efficiency.

2) *BESS*

Ignoring the battery self-discharging losses, the BESS loss sources are battery internal resistance (P_{BESS1}), and SM conduction and switching action (IGBT conduction and switching losses, P_{BESS2} and P_{BESS3} respectively). First, the power loss due to battery internal resistance P_{BESS1} can be estimated by:

$$P_{BESS1} \approx {m_{BESS}}^{*}\, {I_{dcBESS}}^{2}\, R_{Bat}\, M\, M_S / M_P \tag{6}$$

where R_{Bat} is the internal resistance of the selected battery cell. The HB SM IGBT (plus its diode) conduction loss P_{BESS2} (dependent on the BESS current direction) is calculated as:

$$P_{BESS2} \approx \begin{cases} \left[\begin{matrix} {m_{BESS}}^{*} V_{IGBT} + \\ (1 - {m_{BESS}}^{*}) V_{DIODE} \end{matrix}\right] M I_{dcBESS}, I_{dcBESS} > 0 \\ \left[\begin{matrix} (1 - {m_{BESS}}^{*}) V_{IGBT} \\ + {m_{BESS}}^{*} V_{DIODE} \end{matrix}\right] M I_{dcBESS}, I_{dcBESS} < 0 \end{cases} \tag{7}$$

where V_{IGBT} and V_{DIODE} are conduction voltages of the selected IGBT and

its diode respectively as given in Eq. (3). Also, the total switching loss P_{BESS3} can be estimated by summing up all related semiconductor switching losses (turn-on, turn-off and recovery) according to Eq. (4) [37], as succinctly expressed by:

$$P_{BESS3} \approx f_s \left[\sum E_{on}(V_{BESSSM}, |I_{dcBESS}|) + \sum E_{off}(V_{BESSSM}, |I_{dcBESS}|) + \sum E_{rec}(V_{BESSSM}, |I_{dcBESS}|) \right] \quad (8)$$

where, f_s indicates the BESS IGBT equivalent switching frequency, and V_{BESSSM} is the BESS SM voltage.

3) *MMC*

The MMC power losses are mainly caused by semiconductor conduction and switching losses (P_{MMC1} and P_{MMC2} respectively), whereas the estimation method has been well established in the literature [18, 36–39]. Collective conduction losses of the IGBTs and diodes within one arm (P_{IGBT1C}, P_{IGBT2C}, $P_{DIODE1C}$, and $P_{DIODE2C}$ respectively) can be calculated based on the MMC arm current $i_{ARM}(t)$ (assumed consisting of a dc component and a fundamental frequency ac component) and SM selection profile $N_{ARM}(t)$ (indicating the selected SM number), as (detailed derivation can be referred to [18,39]):

$$P_{IGBT1C} \approx {}^1\!/\!_T \int_0^T [V_{IGBT1}\, i_{ARM-}(t)\, N_{ARM}(t)]\, dt \quad (9)$$

$$P_{IGBT2C} \approx {}^1\!/\!_T \int_0^T \{V_{IGBT2}\, i_{ARM+}(t)\, [N - N_{ARM}(t)]\}\, dt \quad (10)$$

$$P_{DIODE1C} \approx {}^1\!/\!_T \int_0^T [V_{DIODE1}\, i_{ARM+}(t)\, N_{ARM}(t)]\, dt \quad (11)$$

$$P_{DIODE2C} \approx {}^1\!/\!_T \int_0^T \{V_{DIODE2}\, i_{ARM-}(t)\, [N - N_{ARM}(t)]\}\, dt \quad (12)$$

where, V_{IGBT1}, V_{IGBT2}, V_{DIODE1} and V_{DIODE2} are conduction voltages of the BESS HB SM IGBTs and its diodes respectively, as given in Eq. (3); $i_{ARM+}(t) = i_{ARM}(t)$ when $i_{ARM}(t) > 0$, and $i_{ARM+}(t) = 0$ when $i_{ARM}(t) \leq 0$; and $i_{ARM-}(t) = -i_{ARM}(t)$ when $i_{ARM}(t) < 0$, and $i_{ARM-}(t) = 0$ when $i_{ARM}(t) \geq 0$. Thus, the MMC overall conduction loss P_{MMC1} is calculated by:

$$P_{MMC1} \approx 6\,(P_{IGBT1C} + P_{IGBT2C} + P_{DIODE1C} + P_{DIODE2C}) \quad (13)$$

Also, MMC one arm semiconductor switching losses (P_{IGBT1S}, P_{IGBT2S}, $P_{DIODE1S}$, and $P_{DIODE2S}$ respectively) can be estimated by adding up all related semiconductor device switching losses according to Eq. (4) [37,38], as succinctly expressed by:

$$P_{IGBT1} \approx f_s \left\{ \sum E_{on}[V_{MMCSM}, i_{ARM-}(t)] + \sum E_{off}[V_{MMCSM}, i_{ARM-}(t)] \right\}, i_{ARM}(t) < 0 \quad (14)$$

$$P_{IGBT2S} \approx f_s \left\{ \sum E_{on}[V_{MMCSM}, i_{ARM+}(t)] + \sum E_{off}[V_{MMCSM}, i_{ARM+}(t)] \right\}, i_{ARM}(t) > 0 \quad (15)$$

$$P_{DIODE1S} \approx f_s \sum E_{rec}[V_{MMCSM}, i_{ARM+}(t)], i_{ARM}(t) > 0 \quad (16)$$

$$P_{DIODE2S} \approx f_s \sum E_{rec}[V_{MMCSM}, i_{ARM-}(t)], i_{ARM}(t) < 0 \quad (17)$$

where, f_s indicates the MMC IGBT equivalent switching frequency, and V_{MMCSM} is the MMC SM rated voltage. Thus, given the HB SM switching behavior, the MMC overall switching loss P_{MMC2} can be estimated by:

$$P_{MMC2} \approx 6\,(P_{IGBT1S} + P_{IGBT2S} + P_{DIODE1S} + P_{DIODE2S}) \quad (18)$$

B. Major parts losses under rated operating conditions

This subsection aims to analyze the losses of the major parts (DU, BESS and MMC) of the receiving-end system, therefore rated operating conditions (where the 1 pu power is transferred/converted) are adopted for different parts. Specifically, the DU loss is estimated by assuming that 1 pu dc current is transmitted from the dc link through the DU; the BESS losses is obtained assuming 1 pu current is provided by the BESS; and, for MMC, it is assumed that 1 pu active power with unity power factor is transferred to the grid.

Thus, according to the aforementioned loss estimation method and parameters in Table I, the operation losses of DU, BESS and MMC are presented in Fig. 7, where the percentage results are calculated based on the system rated power (50 MW). The DU accounts for a small amount of losses (approximately 0.1%), indicating an efficient dc-fault protection measure. The internal resistance within the BESS batteries results in relatively high power losses as anticipated, whereas the lower BESS switching loss is mainly due to a high number of SMs (thus lower switching frequency for each SM) and the lower BESS SM voltage level than those of the MMC. Also, the rated operation efficiency of the single BESS is calculated to be approximately 96.5%, and the resultant MMC operation efficiency is about 99.4%.

C. System efficiency variation with different power sharing

Assuming 1 pu active power is transferred into the MMC, the different conditions of power-sharing between the dc link (renewable generation) and the BESS (stored energy), as described by Eq. (2), will lead to different receiving-end operation efficiency. This subsection presents the receiving-end system efficiency variation with the different power-sharing ratios. Fig. 8 shows the loss and efficiency characteristics under different power-sharing conditions, where the value of I_{dcBESS}/I_{dcMMC} indicates BESS power contribution ratio (assuming a constant and rated dc-link voltage, 0% means that the renewable source provides the rated active power while 100% represents that the BESS provides the rated active power). As shown in Fig. 8(a), the DU loss decreases from 45.5 kW to 0 with the reduced dc-link current, whereas BESS loss increases from 0 to less than 2 MW with the increased BESS current. The overall receiving-end station efficiency decreases from the highest 99.3% to the lowest 95.9%, with the utilization of the BESS, see Fig. 8 (b).

Conclusively, with integrated DU and BESS, both high operation efficiency in long term and effective fault resiliency without complex operation are maintained with the proposed system.

6. Implementation discussion

Considering the proposed system's resiliency against renewable source intermittency and dc-faults, the sending-end rectifier can be cost-effective and dc-fault interruption requirements (such as response speed or fault-current interruption) are not high. Therefore, LCCs and HB SM

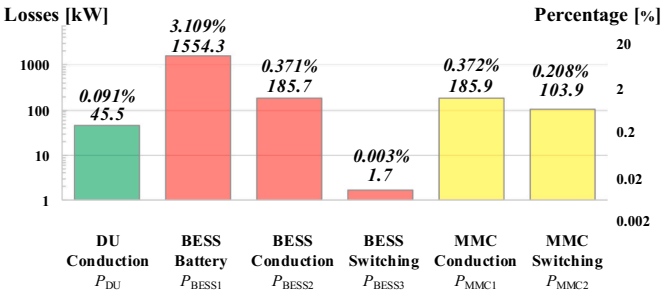

Fig. 7. Receiving-end major part (DU, BESS and MMC) losses under the rated operating conditions of the studied case.

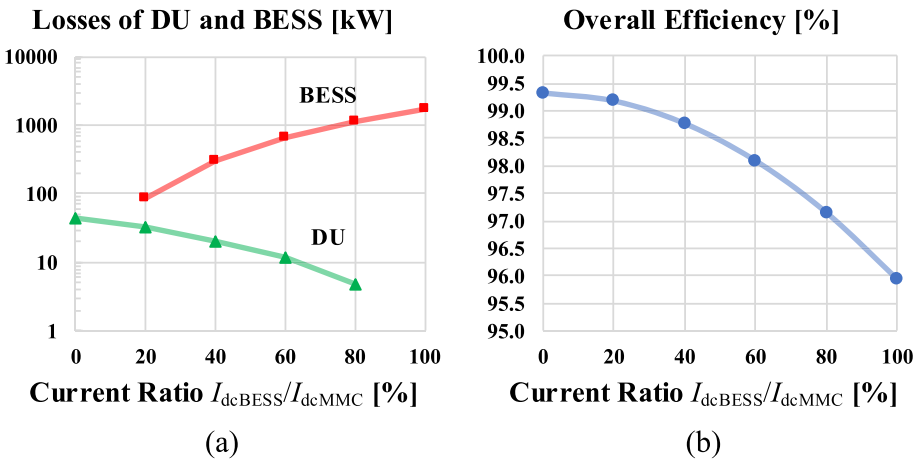

Fig. 8. DU and BESS losses, and overall system efficiency under different power-sharing conditions of the receiving end. (a) DU and BESS loss profiles with different current (power-sharing) ratios. (b) Relationship between overall efficiency and current (power-sharing) ratio.

based MMC with ac circuit breakers are applicable while other factors such as renewable source system characteristics, rectifier station volume and weight can be taken into account.

In terms of the receiving-end configuration, the configuration can be optional as well. Topologically speaking, parallel connection of multiple independent power converters in either ac or dc systems may feature a back-up mechanism, where the power fluctuation/exhaustion of one unit can be compensated by others. It has been established that such an independent dc-side ESS can avoid low-frequency ac current oscillation of the battery, leading to high performance and low cost [6]. Also, this ESS integration approach can be used to retrofit/enhance the existing MMC-based converter stations in order to obtain smoother power output. However, a fault-resilient concept is highly needed in such BESS-integrated systems to avoid power transfer interruption. Thus, the proposed receiving-end system intends to address the renewable intermittency and fault-related interruption collectively, thereby achieving higher system security.

A promising alternative is to replace the DU with a dc circuit breaker (DCCB), which obviously features a bidirectional power flow. Assuming the DCCB configuration proposed in [40] is used and fault detection delay is negligible (thus, breaking current can be low), a basic DCCB can then be implemented for the previously studied case. Similar to Eq. (3), the steady-state IGBT/diode conduction losses of the DCCB can be calculated as around 5.4 kW, which is much lower than that of the DU (45.5 kW). However, in this most efficient case, system overall efficiency is 99.4%, which is just slightly higher the DU-based solution. A comparison of the estimated costs based on the major components of the two options is given in Table II, where the DCCB-based solution is much costly due to the significantly large amount of IGBTs. Besides, the DU-based solution is more attractive in terms of simplicity (hardware and software) and fault isolation performance (response time, fault current interruption, etc.). Thus, the proposed DU-based concept could be more suitable for the renewable energy generation.

Furthermore, the proposed concept can be adopted in the multi-terminal dc system (MTDC) construction with the feature of high security inherited, as shown in Fig. 9, where three different envisaged scenarios are illustrated. The three-terminal system with two sending ends in Fig. 9(a) can harvest and transmit power from different locations, resulting in even less intermittency (power compensation happens among the BESS and two sources). Also, the receiving-end inverter (such as an MMC) can be protected against faults at both sources and dc links.

Table II
Cost estimation of DU and DCCB based protection solutions.

Part	Components	Price	Total
DU	Diode (D2601NH90T)	≈\$1k × 25 = \$25k	≈\$30k
	MOV, resistor, heat sink etc.	≈\$5k	
DCCB	IGBT (FZ1200R45KL3_B5)	≈\$2.5k × 52 = \$130k	≈\$150k
	Disconnector	≈\$10k	
	Gate driver, MOV, heat sink, etc.	≈\$10k	

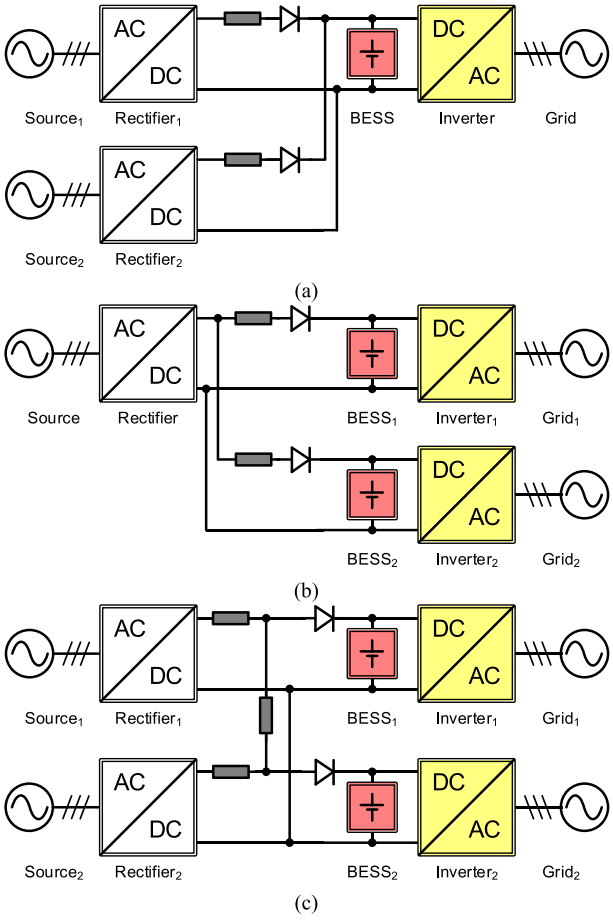

Fig. 9. Three envisaged multi-terminal dc systems (MTDCs) with BESSs based on the proposed concept. (a) A three-terminal system with two sending ends and one receiving end. (b) A three-terminal system with one sending end and two receiving ends. (c) A four-terminal system with two sending ends and two receiving ends.

In Fig. 9(b), the sending end of the three-terminal system can transfer power to the two receiving ends simultaneously, while both $Grid_1$ and $Grid_2$ can be supported by the respective BESS. The operational flexibility of the four-terminal system shown in Fig. 9(c) would be even more desirable and flexible in terms of system management. Conclusively, all scenarios above can achieve smooth power injection into their tied grids, with the system security ensured.

7. Conclusion

In this paper, a secure system integrated with battery energy storage has been proposed mainly for applications of massive renewable energy transfer via dc link(s). The proposed system has the following technical characteristics:

1) With the adoption of diode units (DUs) in the dc-link, dc link faults can be readily tolerated without involving complicated manipulation for system protection;
2) The grid-connected MMC at the receiving end station can be achieved by the half-bridge (HB) submodule (SM) based topology, leading to a lower system cost and higher operation efficiency;
3) The battery energy storage system (BESS) is integrated into the secure (protected by the DU) dc link at the receiving-end station, with only dc current going through during its normal operation, thereby extending lifetime and reducing losses;
4) For the BESS, scalable design/sizing and effective management are feasible due to the modular structure;
5) With the integrated BESS, receiving-end station is able to inject smooth and uninterrupted active power into the load grid, in both renewable fluctuation and source/dc fault cases; and
6) The BESS can also provide active power consumption support for the source system, when an ac fault occurs at the load grid and the transferrable active power is limited.

System configuration, operation, and control were presented in detail, while the BESS design/sizing considerations were given in terms of both basic functionality and BESS management aspects. System performance during dc-link and ac-grid faults were simulated, whereas the major parts of the receiving-end system losses were estimated and system efficiencies under different power-sharing conditions were analyzed. Also, major implementation considerations and potential multi-terminal dc system applications have been discussed. The proposed concept would be applicable for renewable energy transfer/integration and secure system construction, especially for critical and/or isolated systems.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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