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ORIGINAL RESEARCH

Evaluation of HVDC system's impact and quantification of synchronous compensation for distance protection

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Abstract

This paper presents a comprehensive evaluation of the HVDC system's impact on distance protection via systematic and realistic experimental tests, along with theoretical analysis of the root causes of the identified compromised protection performance. A methodology for quantifying the impact of Synchronous Compensation (SC) in supporting the distance protection operation is also established. In this work, the performance of two widely used physical distance protection relays have been evaluated using a realistic Hardware'In'the'Loop (HIL) testing environment, where a total of 480 cases have been tested under a wide range of system scenarios. Representative cases with compromised protection performance are selected, where issues of under/over'reach, faulted phase selection and impedance measurement are identified and analysed. Furthermore, a method for quantifying the required SC level to address the under/over'reach issues resulting from HVDC systems is presented. The method establishes the relationship between the angle difference of the two'end fault current infeeds of the protected line and the SC level. Based on this relationship, the required SC capacity to constrain the angle difference within a targeted limit can be estimated, which offers a useful tool for system operators to appropriately size the SC's capacity with additional valuable insights from the distance protection perspective.

1 | INTRODUCTION

Driven by the target of net-zero carbon emission, a massive amount of Converter-Based Resources (CBRs), for example, HVDC system and renewable generation, have been connected to the GB transmission network. Unlike Synchronous Generators (SGs), which has natural responses during faults that are well known, the behaviour of CBRs is governed by their embedded controllers, which can vary significantly by the different grid codes and vendors [1]. Furthermore, as the weak thermal capability of power electronic devices, the CBRs can only provide very limited fault currents compared with SGs (typically less than 1.5 pu) [2]. These aforementioned features of CBRs pose severe challenges to the existing protection devices in the transmission network.

Distance protection is one of the main protection schemes widely used in transmission networks, playing a critical role in ensuring the safe operation of transmission systems. As reported in [3], an additional reactance will be introduced to the measured reactance of the distance relay owing to the combined effect of the phase angle difference between the local and remote-end infeed and the fault resistance. In a conventional transmission system dominated by SGs, the phase angle difference is typically small (e.g. in the range of a few degrees). Therefore, the observed under-reach and over-reach in an SG-dominated network is insignificant [4]. However, this assumption does not hold true in a converter-dominated network, as the converters' fault responses are determined by the embedded controllers, where the phase difference may experience a significant increase, thus posing the risk of maloperation of distance protection [5]. Relevant research on the aforementioned reach issues are also reported in [6–9].

The phase selection issues of distance protection are discussed in [10–12], where the performance of the sequence

component-based phase selector is evaluated. The sequence component-based phase selection algorithm works by comparing the angle relations between the negative and positive-sequence currents, and the negative and zero-sequence currents. It was found that the connection of CBRs can lead to the incorrect angle relations among the sequence components, thus resulting in incorrect identification of fault types. However, in these papers, the performance of the superimposed content-based phase selector, which is another widely used phase selection algorithm, has not been discussed. The impact of different controllers, that is, the constant active power, constant reactive power and balanced current controllers, on the distance protection are considered in [13]. In this publication, the authors suggest that careful consideration should be made if the constant reactive power controller is used as it could introduce numerical instability problems to the impedance measurement elements of distance relay in the event of the phase-to-phase faults. However, the study only considers the impact of converter's control modes on impedance measurement, but its impact on the phase selection has not been fully investigated, leading to some further risks that could be neglected. This is particularly important as negative sequence current injection is starting to be considered by some countries' Grid Codes [14], and inadequate consideration of control modes' impact on phase selection could lead to the underestimation of the risk of compromised protection performance.

Although there are various existing publications on the topic of converters' impact on distance protection as discussed above, there are three main key limitations of existing work: (1) These papers only focus on one specific issue without the consideration of the inter-dependency of various elements within the protection system, for example the potential consequences when there is a conflict between the phase selection element and impedance measurement element due to the changed fault characteristics from the converters; (2) most of these activities have been conducted based on simulation models or only focus on specific scenarios without realistic and systematic verification via HIL studies using actual devices from different relay manufacturers with different protection designs and implementations under a comprehensive range of system operating conditions; (3) the existing work has only considered a specific protection characteristic or algorithm, without studies to compare the performance with different protection characteristics/algorithms, for example, comparison of the performance of MHO and QUAD characteristics; comparison of the performance with different phase selection algorithms, for example, the delta-quantities and sequence components-based strategies. The aforementioned limitations represent major technical gaps, which lead to the significant remaining challenges for industry to fully understand the nature and extent of the protection issues, and the level of risks to anticipate with the massive integration of converters.

In this paper, systematic tests of 480 cases with two physical relays from different manufacturers are presented, covering different fault conditions, HVDC control strategies, levels of system strength and protection characteristics. Based on the testing results, a clear view of key factors and the overall trend of relays' performance with varied testing conditions are identified and analysed. Representative cases are selected for detailed analysis to illustrate the root cause of compromised performance of two relays, providing valuable insights for network operators on the cause, scale and nature of potential protection failure due to the integration of CBRs.

Synchronous Condensers (SC) is a type of synchronous machines without the mechanical loads and prime mover, which have conventionally been mainly used for supporting the system voltage by injecting or absorbing reactive power [15]. Recently, SC solutions have been reintroduced to the power system to assist the system operation and protection. As reported in [16], the connection of SCs can increase the system strength, therefore, it can be used to mitigate the HVDC operating issues in a weak system, for example, loss of synchronisation [17], resonant issues [18] etc. Furthermore, they are also beneficial to the healthy operation of the protection devices owing to the large currents generated during faults [19]. Additionally, SCs are also capable of improving system voltage and frequency stability and increasing the maximum active power transfer capability between the HVDC converter and the interconnected transmission network [20–22]. Conventionally, the size of the SC is only selected from the system and converter operation perspectives, but the quantification from the protection point has not been fully considered. In [23], it was revealed that the SC connected to the same bus as the protective relay could reduce the phase difference between the currents from the local and remote-end sources. However, the work does not establish the mathematical relation between the introduced synchronous compensation level and the phase difference of current infeed, and it does not provide any methods for quantifying the required level of synchronous compensation for enhancing the performance of protection relays.

In this paper, the mathematical relation between the phase difference of current infeed from both ends of the protected line and the level of synchronous compensation at HVDC side are derived, based on which, the required level of synchronous compensation from the distance protection perspective is estimated, for example, connecting certain amounts of synchronous compensation to achieve the desired phase difference of current infeed from both ends of protected line. Therefore, it provides an additional insight on the optimal sizing of SCs during the planning stage of the system. It should be noted that the authors are not proposing the deployment of more SCs in the power system purely for improving the distance protection performance, but the presented method is more for supporting the understanding of the SCs' impacts on distance protection and providing additional insight when sizing the SC from the distance protection perspective.

The contributions of this paper are summarised as follows:

1. Systematic evaluation of the impact of the HVDC system on distance protection performance using the realistic HIL testing platform. The tests are performed on two commercially available relays and the root causes of the found protection issues are determined and analysed, that is, dis-

tance under-reach/over-reach, phase selection issues, and impedance measurement issues.
2. The impact of CBRs on both delta quantities and sequence-based faulted phase selection algorithms are investigated, compared and analysed in this paper, which, to the authors' best knowledge, has not been reported in existing literature.
3. Establishment of the mathematical relation between the synchronous compensation and the angle difference between the current phasors feeding from the two ends of the protected line, based on which, a methodology for quantifying the required level of synchronous compensation from protection perspective, that is, to address the under-reach/over-reach problems, is developed.

In this paper, the analysis of the compromised distance protection due to CBRs and the quantification of required capacity of SC are both based on the systematic tests conducted on the relays. Therefore, the test setup and test results will be presented first, which are followed by the detailed analysis and the method for SC quantification. The rest of paper is organised as follows: Section 2 presents the network model and the setup of HIL platform; Section 3 presents the systematic HIL tests of distance relays; Section 4 discusses the detail HIL tests of distance relays; Section 5 derives the equations used to quantify the required level of synchronous compensation from protection perspective and evaluates the performance of the derived equation by the designed cases; the conclusions of the paper are provided in Section 6.

2 | NETWORK MODEL AND HIL TEST SETUP

2.1 | Overview of the network used for the study

A simplified equivalent network model in RTDS specifically designed for evaluating distance protection performance with high penetration of CBRs as reported in [24] is used for this study, which is represented in Figure 1. Equivalent SG1 and SG2 represent the connected AC network at the remote and local-end of the protected line, which are modelled as the ideal AC voltage sources with a serial impedance; MMC-HVDC represents the Modular Multi-level Converter (MMC)-based HVDC system, where a flexible controller discussed in Section 2.2 is developed to emulate different control strategies of the HVDC system, for example, constant reactive power control to suppress the ripples on the reactive power, balanced current control to mitigate the negative sequence output current and constant active power control to suppress the ripples on the active power; SC represents the synchronous condenser installed at the HVDC site with an AVR controller; NSG represents the equivalent non-synchronous generation at the remote end of the network, for example, wind, solar etc., whose control structure can be found in [25]; Z_{eq1} and Z_{eq2} represent the equivalent impedance between the connected AC sources and the protected line, which determine the fault levels of Bus B and Bus A.

2.2 | Controller design of MMC-HVDC model

In the designed MMC-HVDC model, the dual-sequence current controller in Figure 2 is employed to control the positive and negative-sequence components independently. The fault response of the developed MMC-HVDC model is governed by its outer power controller, which is designed following the control objectives listed below:

1. Emulate various control strategies in asymmetrical faults, for example, constant reactive power control to suppress the ripples on the output reactive power, balanced current control to generate symmetrical fault currents and constant active power control to suppress the ripples on the output active power.
2. Inject certain amounts of the positive-sequence reactive currents based on the injection curve defined in the GB Grid Code [26], that is, the equation of $I_{qr}^{+}\ (pu) = -3.28\,|v^{+}| + 2.64,\ 0 \le I_{qr}^{+} \le 1$ is used in this study.
3. Limit the fault currents to 1.2 *pu* to avoid the over-current issues of converter.

After considering above requirements, the outer power controller in Figure 3 is developed in the MMC-HVDC model, where the equations (1)-(7) in this diagram are presented below. The detail derivation process can be found in the modelling report of the HVDC project supported by the National HVDC centre [27]. In those equations, all variables are represented as per-unit values with the bases of $S_{base} = S_{rated}$, $V_{base} = \frac{\sqrt{2}V_{LL}}{\sqrt{3}}$ and $I_{base} = \frac{2S_{base}}{3V_{base}}$, where S_{rated} is the rated power of MMC-HVDC system and V_{LL} is the nominal line-to-line voltage at the measuring point.

$$I_{dr,nor}^{+} = \frac{2}{3}\left(\frac{v_d^{+}}{{v_d^{+}}^2+{v_q^{+}}^2}P_r + \frac{v_q^{+}}{{v_d^{+}}^2+{v_q^{+}}^2}Q_r\right) \tag{1}$$

$$I_{qr,nor}^{+} = \frac{2}{3}\left(\frac{v_q^{+}}{{v_d^{+}}^2+{v_q^{+}}^2}P_r + \frac{-v_d^{+}}{{v_d^{+}}^2+{v_q^{+}}^2}Q_r\right) \tag{2}$$

$$I_{dr\_ini}^{+} = \sqrt{{I_{max}}^2 - \left(I_{qr\_ini}^{+}\right)^2} \tag{3}$$

$$\begin{aligned} I_{qr\_ini}^{+} &= -3.28\left|v^{+}\right| + 2.64, 0 \le i_{qr\_ini}^{+} \le 1\ I_{qr\_ini}^{+} \\ &= -3.28\left|v^{+}\right| + 2.64, 0 \le i_{qr\_ini}^{+} \le 1 \end{aligned} \tag{4}$$

$$I_{dr\_ini}^{-} = K_{mode}\left(\frac{v_d^{+}v_d^{-}-v_q^{+}v_q^{-}}{v_d^{+2}+v_q^{+2}}\right)I_{dr\_ini}^{+} + K_{mode}\left(\frac{v_d^{+}v_q^{-}+v_d^{-}v_q^{+}}{v_d^{+2}+v_q^{+2}}\right)I_{qr\_ini}^{+} \tag{5}$$

$$I_{qr\_ini}^{-} = K_{mode}\left(\frac{v_d^{+}v_q^{-}+v_d^{-}v_q^{+}}{v_d^{+2}+v_q^{+2}}\right)I_{dr\_ini}^{+} + K_{mode}\left(\frac{v_q^{+}v_q^{-}-v_d^{+}v_d^{-}}{v_d^{+2}+v_q^{+2}}\right)I_{qr\_ini}^{+} \tag{6}$$

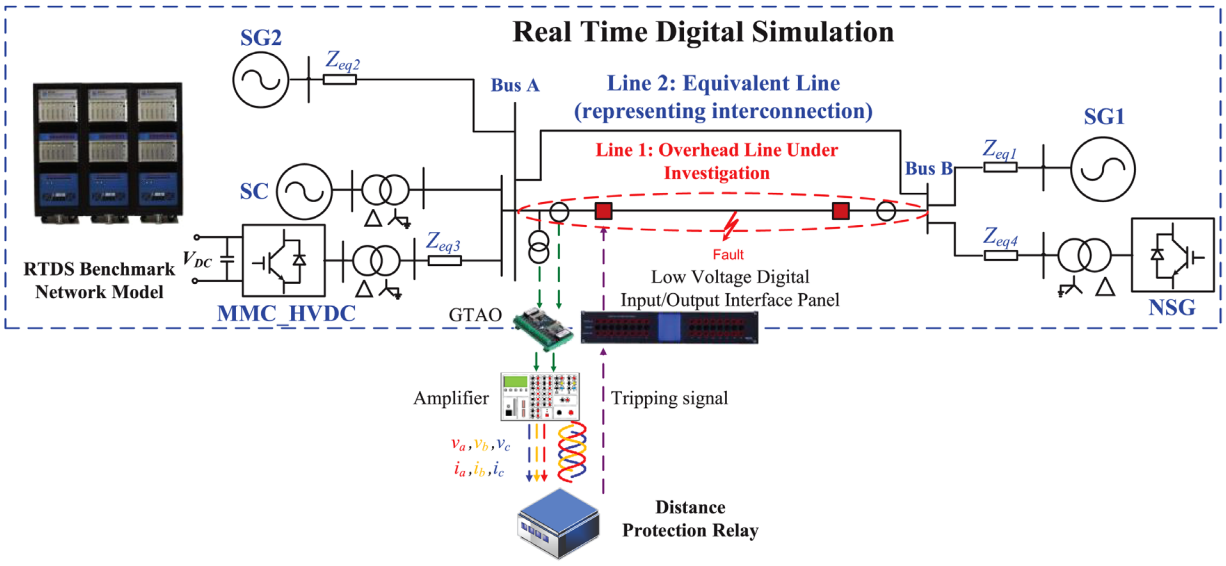

FIGURE 1 Diagram of the studied network and HIL setup

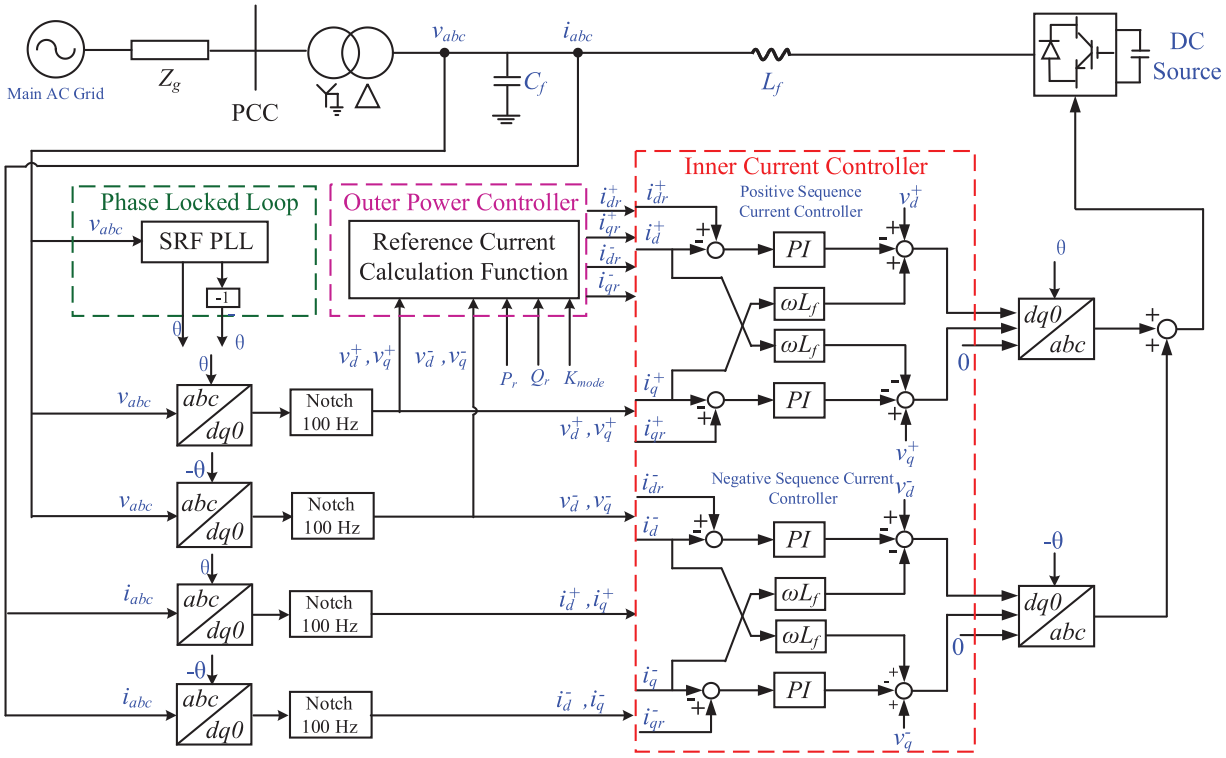

FIGURE 2 Control structure of the designed HVDC system with dual-sequence current control loop

$$SF = \frac{\sqrt{I_{dr\_ini}^{+2} + I_{qr\_ini}^{+2}} + \sqrt{I_{dr\_ini}^{-2} + I_{qr\_ini}^{-2}}}{I_{max}} \quad (7)$$

where $I_{dr,nor}^{+}$, $I_{qr,nor}^{+}$ are the positive-sequence current references in the normal operating condition; $I_{dr\_ini}^{+}$, $I_{qr\_ini}^{+}$, $I_{dr\_ini}^{-}$ and $I_{qr\_ini}^{-}$ are the initial positive and negative- sequence current references without the fault current limitation; I_{max} is the maximum current of MMC-HVDC system, for example, 1.2 pu used in this study; SF is the calculated Scaling Factor used to limit the fault current; v_d^+, v_d^-, v_q^+ and v_q^- are the positive and negative-sequence voltages in the dq frame; $|v^+|$ is the magnitude of the positive-sequence voltage, which is calculated by $|v^+| = \sqrt{v_d^{+2} + v_q^{+2}}$; K_{mode} is the variable used to realise the different operating modes of the MMC-HVDC system, for example, constant reactive power control mode ($K_{mode} = 1$),

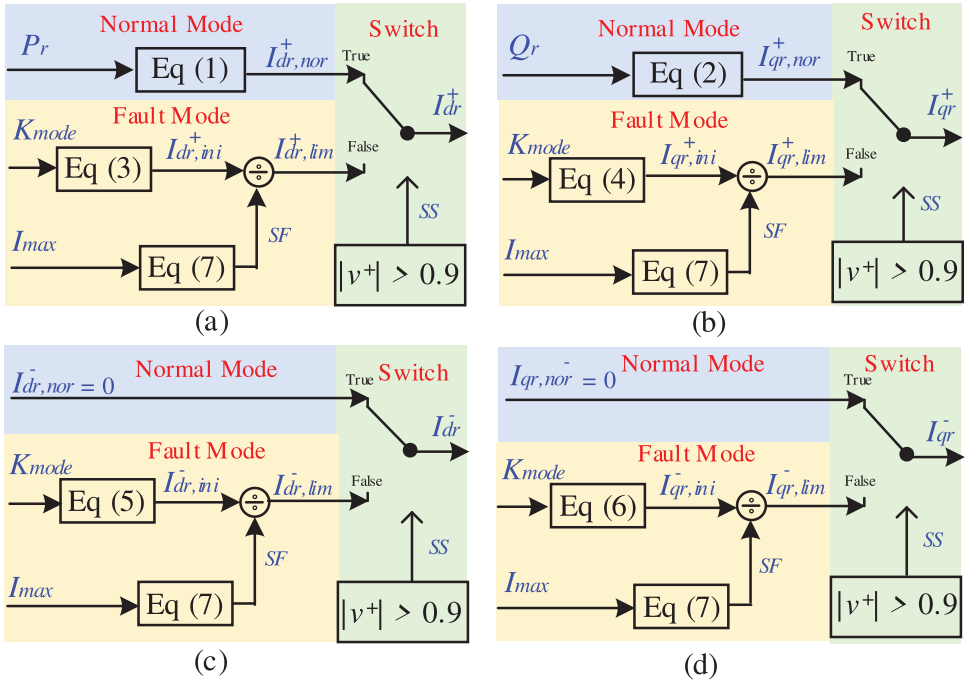

FIGURE 3 Calculation of the current references of outer power controller, (a) I_{dr}^{+}, (b) I_{qr}^{+}, (c) I_{dr}^{-} and (d) I_{qr}^{-}

balanced current control mode ($K_{mode} = 0$) and constant active power control mode ($K_{mode} = -1$).

Based on Figure 3, there are two operating modes of the developed MMC-HVDC system, that is, the normal mode and fault mode, which is controlled by the Switching Signal (*SS*) from the voltage comparison block, where the magnitude of the positive-sequence voltage is compared to the voltage threshold, that is, 0.9 pu in this model. If the voltage is larger than 0.9 pu, the current references calculated by (1) and (2) will be used in the converter. However, if the voltage depresses lower than 0.9 pu, then the converter will employ the current references from (3)to (6). Considering the weak thermal capability of converter, the Scaling Factor, *SF*, depicted in (7) is introduced to scale down the maximum phase current during faults. Through implementing the proposed control structure in Figure 2 and using current references from (1) to (7), the aforementioned three control objectives can be realised.

2.3 | Overview of the HIL setup

The arrangement of the HIL test platform is presented in Figure 1. In this test, the network model developed in RSCAD, a software designed for RTDS, is simulated in real time by the RTDS simulator. The secondary side voltages and currents at Bus A, where the distance relay being tested is installed, are measured by the Voltage Transformer (VT) and Current Transformer (CT) models [28] provided by RSCAD. Additionally, given that the voltage range of the analogue GIGA -Transceiver Analogue Output (GTAO) card is ±10 V [29], the voltages and currents from VT and CT models need to be further scaled down by the defined factor in RSCAD, so that they are within the required range and can be output by the GTAO card. After that, the scaled voltages and currents from the GTAO card will be amplified by a physical amplifier to the same level as the outputs of VT and CT. Those amplified voltages and currents are injected to the physical distance relay, and the tripping signal of the relay is transmitted back to the RTDS through the digital input ports in the front of the RTDS rack, which will be monitored and recorded for evaluating the performance of the investigated distance relay.

3 | SYSTEMATIC HIL TESTS OF DISTANCE RELAYS

3.1 | Overview of the network used for the study

The parameters of the studied system are displayed in Table 1. In this study, the performance of two commercially-available relays, named as 'Relay 1′ and 'Relay 2. are evaluated in a systematic manner, where two commonly used protection characteristics with the settings in Tables 2 and 3 are applied to both relays. In Table 2, the memory-polarised technology is employed to the MHO based distance relay to avoid the protection failure in close-up fault scenarios. The developed vectors, S_1 and S_2, used in the phase comparator are depicted in (8) and (9) and the tripping condition is defined in (10) [30].

$$S_1 = V + pV_{mem} \tag{8}$$

TABLE 1 Parameters of the studied network

Elements	Description	Value
Nominal voltage	–	275 kV
MMC-HVDC	Rated power	839 MVA
	Transformer voltage	275 kV / 360 kV
Rated DC-side voltage	640 kV	
Protected line	Length	12.1 km
	Positive- and zero-sequence resistance per km	$r_1 = 0.0378\ \Omega$/km, $r_0 = 0.159\ \Omega$/km.
	Positive- and zero-sequence inductance per km	$l_1 = 1.324$ mH/km, $l_0 = 3.202$ mH/km.
	Positive- and zero-sequence capacitance per km	$C_1 = 8.964$ nF/km, $C_0 = 6.48$ nF/km.

TABLE 2 Settings with MHO characteristic of both relays

Parameter name	Relay settings
Protection characteristic	Memory-polarised MHO
Polarising factor	Relay 1: $p = 1$; Relay 2: Positive-sequence voltage used
Reach setting	Zone 1: 80%; Zone 2: 120%
Residual compensation factor	$K_0 = 0.48\angle -6.4°$
Delay setting	Zone1: 0 ms; Zone 2: 400 ms

TABLE 3 Settings with QUAD characteristic of both relays

Parameter name	Relay settings
Protection characteristic	QUAD based
Reach setting	Zone 1: 80%; Zone 2: 120%
Residual compensation factor	$K_0 = 0.48\angle -6.4°$
Delay setting	Zone1: 0 ms; Zone 2: 400 ms
Right resistive reach	6.72 Ω
Left resistive reach	1.68 Ω
Directional angle	30°
Tilt angle	−3°

$$S_2 = V - IZ_R \tag{9}$$

$$\theta = ang\left(\frac{S_1}{S_2}\right) > 90° \tag{10}$$

where V is the relay input voltage; I is the relay input current; p is the polarising factor; V_{mem} is the memory-polarised voltage, which is typically the voltage several cycles before the faults. Apart from the use of the pre-fault phase voltage, the positive-sequence voltage during faults can also be used directly to polarise the voltage in some physical relays and in that case, the vector S_1 will equal to the measured positive-sequence voltage during faults and Z_R is the reach settings of the distance relay.

TABLE 4 Information of systematic HIL cases

Parameters	Values
FL_{SG1}: Fault level of SG1	3000 MVA / 1372 MVA
FL_{SG2}: Fault level of SG2	0 MVA / 1836 MVA
SC capacity	0 MVA / 300 MVA
HVDC capacity	839 MVA ($Pf = 1$);
HVDC control modes	CP, BI, CQ
Fault conditions	AG, AB; 2 Ω; 20 %, 70 %, 75 %, 80%, 85%
NSG	839 MVA ($Pf = 0.93$)

3.2 | Information of the studied cases

In the systematic HIL tests, the network in Figure 1 is used to test the cases in Table 4, where pf refers to the power factor; CP, BI, CQ refer to the constant active power, balanced current and constant reactive power modes respectively. All cases in Table 4 will be applied to both relays to evaluate and compare their performance under different system scenarios. In total, there are 480 tests, with 240 tests for each relay. In this work, a script [31] was developed to automate the simulation of the cases in RTDS and record the tripping signal of both relays after every injection, along with the MATLAB codes for analysing the tripping time of those recorded tripping signal, thus assessing the tripping performance, which minimizes the need of human intervention.

3.3 | HIL systematic test results

Based on the relays' tripping actions and operating time as defined in (11) during the tests, the performance of relays can be categorized into four groups, that is, 'Healthy Trip', 'Delayed Trip', 'Trip in False Zone' and 'Failed Trip (Not Trip)'.

$$t_{op} = t_{trip} - t_{incep} - t_{zone} \tag{11}$$

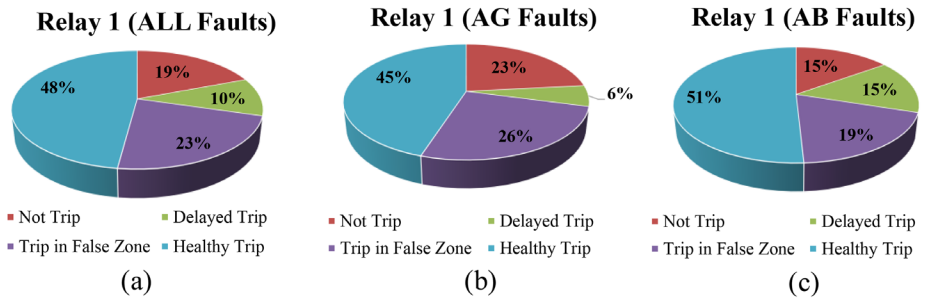

FIGURE 4 Overall performance of Relay 1 with, (a) AG and AB faults, (b) AG faults, (c) AB faults

where t_{trip} is the tripping time of relay; t_{incep} is the fault inception time and t_{zone} is the configured intentional zone delay (e.g. 0 s for zone 1).

The detailed criteria for classifying the relays performance into these four tripping groups are presented below:

1. Healthy Trip: relay trips in the correct zone with the operating delay less than 90 ms.
2. Delayed Trip: relay successfully trips in the correct zone but with the operating delay longer than 90 ms.
3. Trip in False Zone: relay trips in a false zone (e.g. trip in zone 2 for the zone 1 fault).
4. Failed Trip: relay does not trip for the faults in the protective zone.

The selection of the tripping time of 90 ms as the criteria for healthy tripping is based on the grid code [26], which requires short-circuit faults in the super-voltage transmission networks should be isolated no more than 140 ms, which includes the relay tripping time, the circuit breaker (CB) operating time and other potential delays. Assuming a CB operating time is approximately 50 ms, thus the relay operating time is defined as 90 ms. However, in practice, some other delays will be introduced in the fault isolation process and the operating time of CB may be larger than 50 ms, so the required time of 90 ms is intentionally set at the high end, thus when the operating time is longer than this value, it will indeed indicate compromised performance that is not acceptable for transmission system protection.

3.3.1 | Overview of distance protection performance

A high-level view of the statistics of the two relays' performance in the tests is provided in Figures 4 and 5 receptively. These figures include test results from all cases with different faults, HVDC control modes, fault levels etc. Therefore, it provides a high-level comparison of the two relays' performance and initial indicator for the scale of the potential compromised protection performance. It can be seen from the figures that, both relays manage to provide desirable performance for around 50% of the tested cases. Additionally, the two relays have different performance for the tested cases, where relay 2 has slightly higher number of desirable operation cases. Notably, both relays suffer from the 'failed trip' issues and 'delayed trip' issues, which are particularly alarming as it indicates both relays could fail to meet protection requirements in some scenarios. In conventional networks (i.e. dominated by SGs), distance protection is expected to be highly dependable and secure. From the above test results, in future scenarios involving integration of HVDC systems and more renewable based generation, the protection system performance is indeed concerning as it appeared that it could be compromised significantly.

3.3.2 | Impacts of local and remote-end fault level

The results indicating the impact of the local and remote-end fault level are shown in Figures 6 and 7. It can be seen that, the performance of both relays has degraded significantly when the FL_{SG2} decreases to 0 MVA and the FL_{SG1} rises to 3000 MVA, compared to the cases with FL_{SG1} = 1372 MVA and FL_{SG2} = 1832 MVA (the present system fault level data from actual substations in Scotland). This problematic scenario is caused by the increased angle difference and current magnitude ratio between the remote and local-end infeed, which will be analysed later in Section 4.2.2.

3.3.3 | Impacts of HVDC control strategies

In this section, three typically used control strategies during faults, including balanced current control, constant active power control and constant reactive power control, are applied to the developed HVDC model. Figures 8 and 9 present a summary of the results to evaluate the HVDC control strategies on the distance protection. From the results, it can be seen that while both distance relays have compromised performance in some cases with all HVDC control modes, there is a clear difference in the overall performance when different modes are used. It appears that the most problematic control mode is the constant reactive power control, where the severe faulted phase selection and impedance measurement issues are observed from both investigated relays, which is explained later in Section 4.2.1 and Section 4.2.2. Additionally, as discussed in Section 4.2.1, the connection of HVDC systems with balanced current

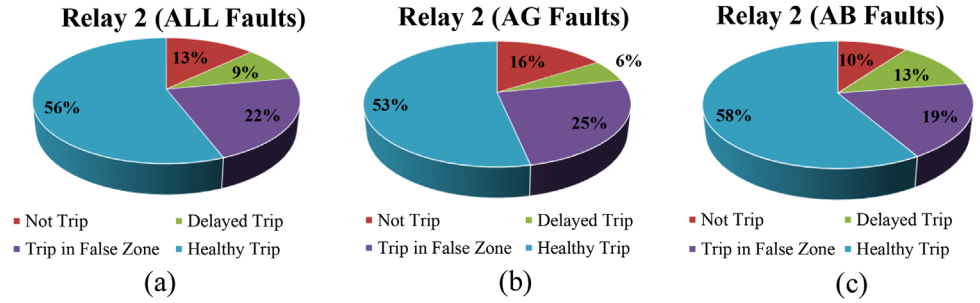

FIGURE 5 Overall performance of Relay 2 with, (a) AG and AB faults, (b) AG faults, (c) AB faults

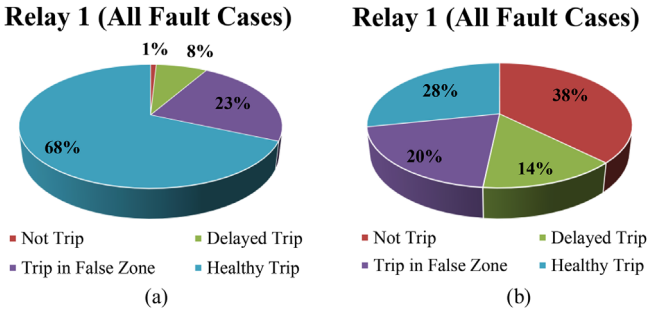

FIGURE 6 Performance of Relay 1 with, (a) FL_{SG1}= 1372 MVA; FL_{SG2}= 1832 MVA; (b) FL_{SG1}= 3000 MVA; FL_{SG2}= 0 MVA

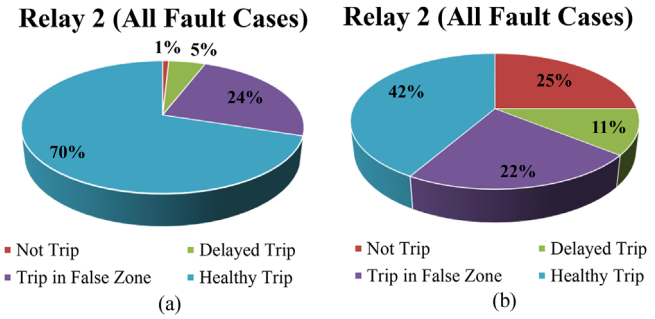

FIGURE 7 Performance of Relay 2 with, (a) FL_{SG1}= 1372 MVA; FL_{SG2}= 1832 MVA; (b) FL_{SG1}= 3000 MVA; FL_{SG2}= 0 MVA

controllers, can result in the phase selection failure of Relay 1 with the superimposed phase-to-phase current based selection algorithm, while the Relay 2 can avoid that failed tripping issues but an undesired delay will be introduced to the phase selection. Therefore, the failed tripping risk of Relay 1 is higher than Relay 2, while the delayed tripping risk of Relay 1 is lower than Relay 2 when balanced current controllers are adopted by the HVDC system.

3.3.4 | Impacts of distance protection characteristics

In this part of the study, both MHO and QUAD characteristics with the settings in Tables 2 and 3 are applied to both relays for the evaluation of the impact of the protection characteristics. The test results are shown in Figures 10 and 11. Examining the results, for Relay 1, the MHO and QUAD characteristics have the similar performance, while for relay 2, the QUAD characteristic appears to perform better overall performance (from the perceptive of the percentage of healthy trip and not trip cases).

4 | DETAILED ANALYSIS OF THE REPRESENTATIVE HIL CASES

Section 3 provides the high-level insights of the distance protection performance under various testing conditions. This section will further investigate the detailed causes behind the identified protection issues with a number of representative cases that lead to compromised protection performance.

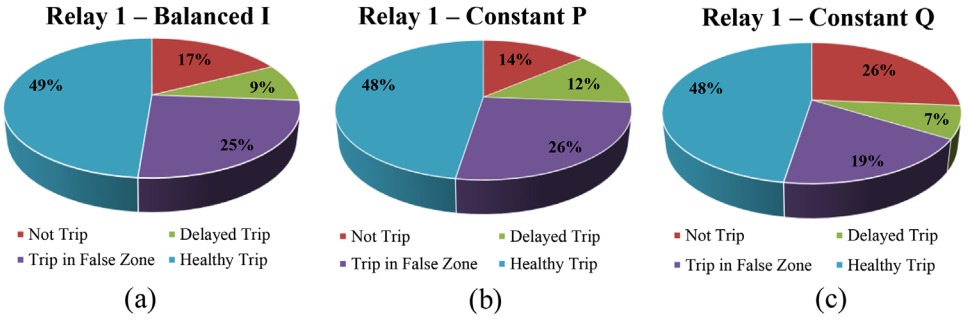

FIGURE 8 Performance of Relay 1 with, (a) balanced current control; (b) constant active power control; (c) constant reactive power control

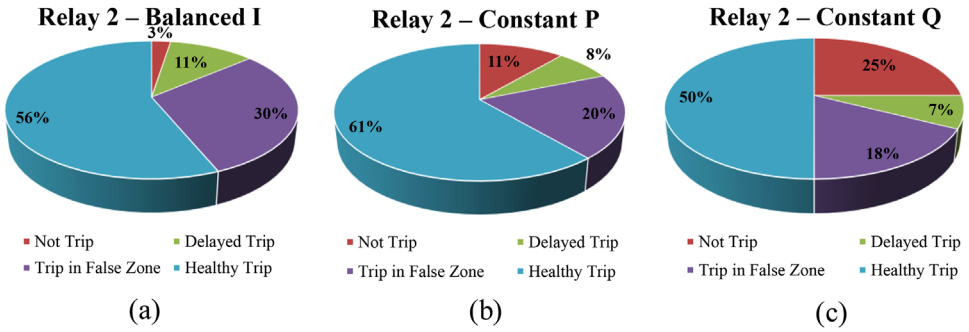

FIGURE 9 Performance of Relay 2 with, (a) balanced current control; (b) constant active power control; (c) constant reactive power control

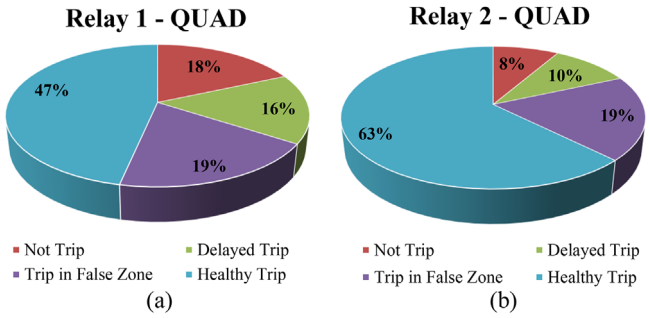

FIGURE 10 Performance of relays with QUAD characteristics, (a) Relay1, (b) Relay 2

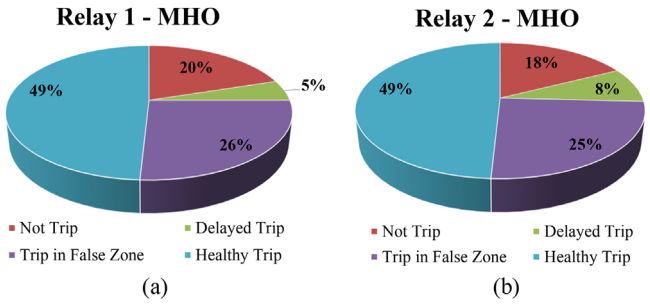

FIGURE 11 Performance of relays with MHO characteristics, (a) Relay1, (b) Relay 2

4.1 | Information of the representative HIL cases

The information of the selected cases for the detailed investigation is presented in Table 5. The fault infeed of 0 MVA from SG2 represents the worst-case scenario, where the magnitude ratio of remote-end (SG1 side) and local-end (HVDC side) infeed is largest. Additionally, based on the previous systematic test results and analysis, the sources of protection issues are similar for the relay with QUAD and MHO characteristics in most cases, so the analysis of relay with the QUAD characteristic will be presented as the example in the following discussion.

4.2 | Results of the representative HIL tests

The results of test cases in Table 5 are presented in Table 6, where the relay tripping conditions, for example, 'YES' and 'NO' refer to the successful and failed trips respectively, and the tripping time is the time between the fault occurrence to the tripping of the relay.

4.2.1 | Protection issues during single-phase-to-ground faults (Cases 1–3)

The HIL test results of AG faults from Cases 1 to 3 are presented in Table 6. Based on the results, it can be concluded that Relay 1 fails to trip when the HVDC uses the balanced current and constant reactive power controller. Relay 2 experiences a severe tripping delay of 100 ms in Case 2, and it fails

TABLE 5 Information of the representative HIL cases

Cases	FL_{SG1}	FL_{SG2}	HVDC control	Fault condition
1	3000 MVA	0 MVA	CP	AG, 15 %, 2 Ω
2	3000 MVA	0 MVA	BI	AG, 15 %, 2 Ω
3	3000 MVA	0 MVA	CQ	AG, 15 %, 2 Ω
4	3000 MVA	0 MVA	CP	AB, 15 %, 2 Ω
5	3000 MVA	0 MVA	BI	AB, 15 %, 2 Ω
6	3000 MVA	0 MVA	CQ	AB, 15 %, 2 Ω

TABLE 6 Results of the representative HIL tests

Cases	Tripping condition		Tripping time	
	Relay 1	Relay 2	Relay 1	Relay 2
1	YES	YES	68 ms	40 ms
2	NO	YES	NA	100 ms
3	NO	NO	NA	NA
4	YES	YES	87 ms	61 ms
5	NO	YES	NA	43 ms
6	NO	NO	NA	NA

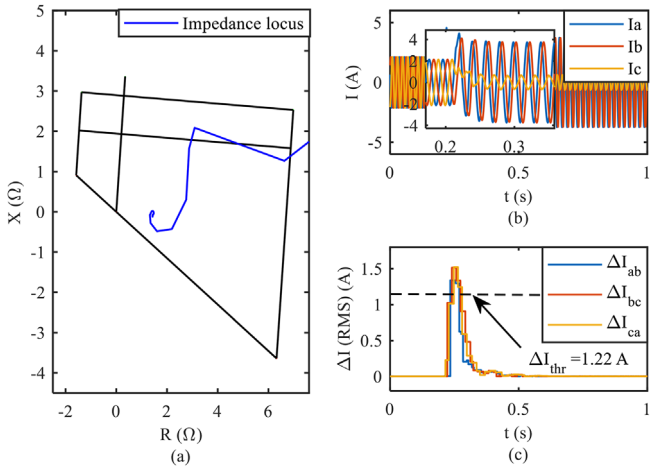

FIGURE 12 Test results of case 2, (a) impedance locus, (b) relay input currents, (c) phase-to-phase superimposed currents

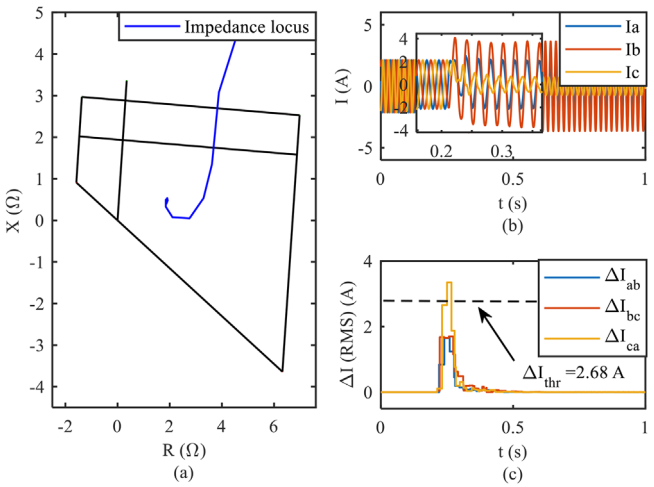

FIGURE 13 Test results of case 3, (a) impedance locus, (b) relay input currents, (c) phase-to-phase superimposed currents

to trip in Case 3. An investigation of the causes of these problematic cases, that is, Case 2 and Case 3, are conducted. Relay 1 selects the faulted phases based on the magnitude relations of the phase-to-phase superimposed currents, that is, ΔI_{ab}, ΔI_{bc} and ΔI_{ca}, while Relay 2 uses the angle relations of the sequence-based components, that is, the angle relations of the negative and positive-sequence currents and voltages, and the angle relations of the negative and zero-sequence currents and voltages [32].

The impedance locus, input currents and the RMS values of phase-to-phase superimposed currents measured by the Relay 1 for Case 2 and Case 3, are presented in Figures 12 and 13 respectively. For Relay 1, any superimposed currents that are greater than 80% of the largest superimposed current will be considered to contain the faulted phase. For example, in the event of the investigated AG faults, the relay is capable of detecting the fault type when the values of ΔI_{ab} and ΔI_{ca} are both greater than the threshold while the values of ΔI_{bc} is lower than the threshold. However, by observing the RMS values of the superimposed phase-to-phase currents in Figure 12, it is clear that all values of the ΔI_{ab}, ΔI_{bc} and ΔI_{ca} are larger than the current threshold, ΔI_{thr}, which results in the relay incorrectly identifying the fault as a balanced fault. Additionally, it can be confirmed that similar phase selection issues are also experienced by Relay 1 when the HVDC uses the constant reactive power controller as shown in Figure 13, where the relay detects the fault as the phase-A-to-phase-C-to-ground fault since only the value of ΔI_{ca} is greater than the calculated threshold and other two phase-to-phase superimposed currents are both lower than the threshold. For the above reasons, the outputs of the phase selection algorithm of the distance relay will be inconsistent with the faulted phase detected by the impedance measuring elements, which cause the blocking of Relay 1 tripping action (although the impedance locus is presented in the protective zone in Case 2 and Case 3).

The sequence-based phase selection plane shown in Figure 14 is used in Relay 2 to identify the faulted phases. For instance, in the event of AG faults, the angles of I_2/I_1 and I_2/I_0 should be in the zones of $-15°$ to $15°$ and $-30°$ to $30°$ respectively. Additionally, to increase the dependability and avoid the maloperation in some specific operating conditions, for example, weak-infeed conditions, the phase selection logics in Figure 14 are also applied to analyse the sequence-contents of the system voltages if the current-based phase selection cannot recognise the type of the fault. The simulated angles of the I_2/I_1, I_2/I_0, V_2/V_1 and V_2/V_0 in Case 2 and Case 3 are presented in Table 7. From the results in Table 7 of Case 2, the angle of

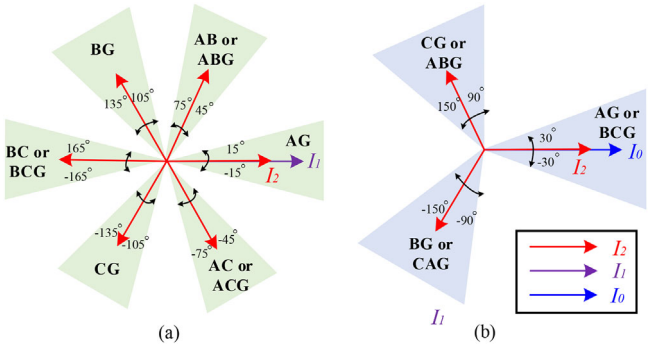

FIGURE 14 Sequence-based phase selection plane, (a) relations of the negative-sequence current and the positive-sequence current, (b) relations of the negative-sequence current and the zero-sequence current

TABLE 7 Angle information in Case 2 and Case 3

Angles	Case 2	Case 3
I_2/I_1	117.2°	−167.5°
I_2/I_0	176.7°	−98.5°
V_2/V_1	9.2°	12.42°
V_2/V_0	6.4°	26.92°

I_2/I_1 and I_2/I_0 are in the zones of 'BG' and 'out of the zone' respectively, therefore, the relay fails to detect AG faults by the relations of the sequence contents of the measured currents. In such conditions, the relay will further use the voltage phasors, which can recognise the AG faults successfully. However, in this case, an undesired delay, that is, 100 ms (refer to Table 6), will be introduced. The above analysis can also be applied to explain the results of Case 3, where the angles of I_2/I_1 and I_2/I_0 are in the incorrect zones but the V_2/V_1 and V_2/V_0 are in the AG zones. Given the internal functional blocks and signals of the physical relay are largely inaccessible, the simulated angles in Table 7 are calculated from an analysing tool developed in the RSCAD software based on the relay manual. Therefore, there could be some errors between the actual angle values used in the physical relays and the corresponding simulated angles. Additionally, the angle of V_2/V_0 of Case 3 in Table 7 reaches to 26.92°, which is close to the upper boundary of AG zone, that is, 30°. Therefore, it is considered that this is the potential cause that leads to the failed tripping issue of Relay 2.

4.2.2 | Protection issues during phase-to-phase faults (Cases 4 to 6)

Based on the results in Table 6, the Relay 1 fails to trip for the fault when the HVDC system uses the balanced current controller (Case 5) and the constant reactive power controller (Case 6). The simulation results of Case 5 and Case 6 are presented in Figures 15 and 16 respectively. As reported in [3], the connection of CBRs will cause a large angle difference of the current infeed from the two ends of the protected line,

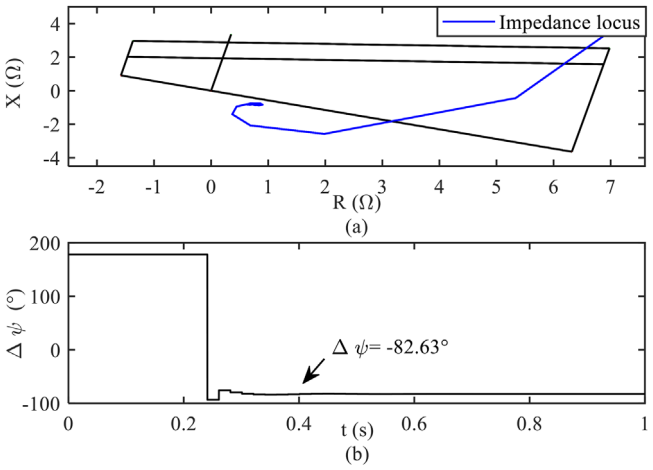

FIGURE 15 Test results of case 5, (a) impedance locus, (b) angle difference of the current infeed from both ends of the protected line

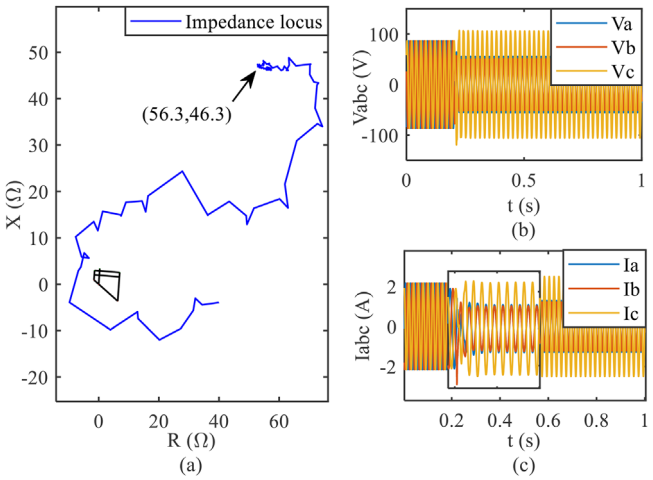

FIGURE 16 Test results of case 6, (a) impedance locus, (b) relay input voltages, (c) relay input currents

which further results the protective reach issues, that is, over/under-reach issues, of distance relay. According to Figure 15b, the angle difference of the current infeed contributed from two ends of the protected line, $\Delta\psi$, is −82.63° in the fault scenario of Case 5, which results the over-reach issues of distance protection. Additionally, owing to the limited current contribution of HVDC system, those observed over-reach issue become more apparent, which results in the impedance locus appearing at the reverse side of the protective zone. Therefore, the fault cannot be detected by distance relay and further lead to the failed trip issues. However, Relay 2 successfully trips for the fault in Case 5. Presently, it is unclear the reason of that tripping behaviour of Relay 2 owing to the lack of information about the detailed internal implementation of Relay 2, which will be part of the future research with support from the relay manufacturer.

The impedance locus of Case 6 is plotted in Figure 16a, where the measured impedance does not enter the protective zone and increase to a large value during the faults. This scenario can be explained by Figure 16c, where the phase A and phase B cur-

rents are almost identical. Therefore, the denominator value in (12) will close to zero, which leads to a significant increase on the impedance measured by the distance relay. More information of the issue in case 6 can be found in [13].

$$Z_{AB} = \frac{V_A - V_B}{I_A - I_B} \tag{12}$$

where Z_{AB} is the impedance measured at phase-A-to-phase-B fault; V_A and V_B are phase A and phase B voltages; I_A and I_B are the phase A and phase B currents.

5 | QUANTIFICATION OF SYNCHRONOUS COMPENSATION FOR DISTANCE PROTECTION

As discussed in Section 4.2.2, a key contributor to the compromised distance protection performance is associated with the inaccurate impedance measurement (thus the under/over-reach issues) due to the connection of HVDC system. In this section, the benefits of SC on distance protection in perspective of addressing the under-reach and over-reach issues will be discussed and a method for quantifying the required level of synchronous compensation at the HVDC side from the protection perspective is presented.

5.1 | Theoretical analysis to quantify the required level of synchronous compensation

As the objective of this section is to quantify the required level of the synchronous compensation from distance protection perspective, the NSG, SG2 in Figure 1 are disconnected to simplify the analysis. Additionally, given that the fault currents contributed by the SC is determined by multiple factors, for example, the internal impedance, capacity, etc., the exact specification of the installed synchronous condenser is not the focus of this work. Therefore, the model of SC is also simplified as an AC voltage source with an equivalent impedance in this study. In this case, the quantified level of synchronous compensation required will be in the form of fault level contribution in MVA, which aligns with the approach adopted in the Stability Pathfinder 2 for procuring fault level as an ancillary service by National Gird ESO [33].

With the connection of SC, the impedance measured by the distance relay can be represented as (13), which is derived by applying the Kirchhoff Voltage Law (KVL) from the fault point to the relay point.

$$Z_M = Z_L + \left(1 + \frac{\overbrace{I_{SG1}}^{A}}{I_{SC} + I_{HVDC}}\right) R_F \tag{13}$$

where Z_M is the measured impedance of relay; Z_L is the line impedance between the fault point and relay location; R_F is the faulted loop resistance and I_{SG1}, I_{SC}, I_{HVDC} are the fault currents contributed by the SG1, SC and MMC-HVDC respectively.

According to [3, 7], the under-reach and over-reach issues are mainly determined by the angle difference of the current infeed from both ends of the protected line (represented as $\Delta\psi$), which is determined by the phase of the part A in (13). Therefore, the phase of part A will be specially analysed in this section. Additionally, as reported in [5, 6], the angle difference of the fault currents contributed by the synchronous generators at both ends are only a few degrees owing to the requirements of the voltage stability at two ends of protected line, thus the imaginary part of $\frac{I_{SC}}{I_{SG1}}$ can be neglected. Therefore, the results of $\frac{I_{SC}}{I_{SG1}}$ is regarded as a real number in the following derivation, then (14) is derived.

$$A = \frac{1}{\frac{I_{SC}}{I_{SG1}} + \frac{I_{HVDC}}{I_{SG1}}} = \frac{1}{C_1 + C_2 \angle \theta_{C2}} \tag{14}$$

where $C_1 = |\frac{I_{SC}}{I_{SG1}}|$; $C_2 = |\frac{I_{HVDC}}{I_{SG1}}|$ and $\theta_{C2} = \angle(\frac{I_{HVDC}}{I_{SG1}})$.

With further mathematical operation, the (14) can be extended to (15):

$$A = \frac{1}{\sqrt{C_1^2 + C_2^2 + 2C_1C_2\cos(\theta_{C2})}} \left(-\angle \arctan\left(\frac{C_2 \sin(\theta_{C2})}{C_1 + C_2\cos(\theta_{C2})}\right)\right) \tag{15}$$

based on (15), the representation of $\Delta\psi$, which is the phase of $\frac{I_{SG1}}{I_{SC}+I_{HVDC}}$ part in (13), is displayed in (16):

$$\Delta\psi = -\angle \arctan\left(\frac{\overbrace{C_2 \sin(\theta_{C2})}^{B}}{C_1 + C_2\cos(\theta_{C2})}\right) \tag{16}$$

From (16), the value of $\Delta\psi$ is dependent on the value of part B, and to minimise the under-reach and over-reach issues, the value of B should be as close to zero as possible. Additionally, the following conclusions can be derived based on (16).

1. For the magnitude difference of I_{SC} and I_{SG1}: a higher value of I_{SC}, that is, a higher level of synchronous compensation, will lead to a larger value of C_1 and a smaller value of B, thus the angle difference value of $\Delta\psi$ will be smaller.
2. For the magnitude difference of I_{HVDC} and I_{SG1}: this is determined by the current limiting strategy and the capacity of the HVDC system and the fault infeed of SG1. If the value of I_{HVDC} is small, for example, with a small HVDC system, then C_2 will be small, so the values of B and $\Delta\psi$ will be small. Therefore, it will have the small impact on the impedance measurement of distance relay.
3. For the angle difference of I_{HVDC} and I_{SG1}: a large θ_{C2} will lead to a large $\Delta\psi$, thus contributing more to the impedance measurement error.

TABLE 8 Cases studies to quantify the required level of synchronous compensation

Case no	HVDC capacity (MVA)	FL_{SG1} (MVA)	Fault condition	Target angle $\Delta\psi^*$ (°)
1	839	3000	ABCG, 5 Ω, 50 %	10°
2	839	3000	ABCG, 5 Ω, 50 %	15°
3	839	3000	ABCG, 5 Ω, 50 %	20°
4	839	3000	ABCG, 5 Ω, 50 %	25°
5	839	3000	ABCG, 5 Ω, 50 %	30°

Based on (16), the required magnitude of fault currents contributed by SC can be quantified by (17).

$$|I_{SC}| = -\left(\frac{C_2 \sin\theta_{C2}}{\tan\Delta\psi^*} + C_2\cos\theta_{C2}\right)|I_{SG1}| \quad (17)$$

where $\Delta\psi^*$ is the target angle difference of the currents contributed from the two ends of the protected line, which can be set by the system operator, that is, to quantify the required level of synchronous compensation, the system operator should identify the acceptable impedance measurement error first, which will then have a corresponding $\Delta\psi^*$, based on which, the corresponding value of $|I_{SC}|$ can be calculated. A detailed example is presented later in Section 5.2. It should be noted that, as mentioned above, the quantification of $|I_{SC}|$ has mainly considered the impedance measurement error in distance protection relays, and other protection elements, for example, faulted phase selection, signal filtering and processing, are not considered as they are highly dependent on the vendor-specific design. Furthermore, another assumption made in the quantification is the remote end fault infeed is mainly supplied by SGs and largely have voltage source behaviour. If the remote side is also dominated by converters, the current $|I_{SC}|$ will also be dependent on the control of remote-end connected NSGs and their penetration level, which can change significantly, thus further dedicated analysis will be required.

5.2 | Cases to evaluate the proposed SC quantification method

5.2.1 | Information on the studied cases

As proposed in Section 5.1, the level of synchronous compensation is represented by the fault level contributed by the SC in this study. In practice, the fault level at a busbar should consider both single-phase-to-earth (Ph-E) and three-phase faults [24]. As reported in [4], the impedance measurement of distance relay does not have significant risk in the Ph-E faults because the magnitude of zero-sequence current is typically much larger than the fault current contributed by the HVDC system. Therefore, the three-phase fault level is selected in this study as the main criteria for the quantification of the SC required. The information of the studied cases is presented in Table 8.

5.2.2 | Quantification of the required level of synchronous compensation

In this section, the cases in Table 8 are used to present the quantification of the level of synchronous compensation based on (17), where three-phase faults are at the middle point of the protected line as shown in Figure 1.

The quantification procedure comprises the following steps:

1. Step I: Set the objective angle, $\Delta\psi^*$: Smaller $\Delta\psi^*$ introduces less under/over-reach issues but needs a higher level of synchronous compensation.
2. Step II: Run simulation to acquire the variables in the investigated fault scenario without the connection of SC, including $|I_{SG1}|$, $|I_{HVDC}|$ and θ_{C2} ($\theta_{C2} = \angle(\frac{I_{HVDC}}{I_{SG1}})$)
3. Step III: Calculate $C_2 = |\frac{I_{HVDC}}{I_{SG1}}|$.
4. Step IV: Substitute $\Delta\psi^*$, C_2, θ_{C2} and $|I_{SG1}|$. into (17) to quantify the required fault current from SC.
5. Step V: Configure the Z_{SC} to deliver the required fault current $|I_{SC}|$. As the SC can contribute a high level of fault current (even reach 6 to 8 pu as reported in [34]), the required capacity of SC will be much lower than the calculated fault level.
6. Step VI: Run the simulation in RTDS by inputting the Z_{SC} in step V to the system model in Figure 1 and compare the $\Delta\psi$, which is obtained from the RTDS simulation, with the target angle, $\Delta\psi^*$.

It should be noted that based on the derivation procedure in Section 5.1, the actual values for the variables $|I_{SG1}|$, $|I_{HVDC}|$ and θ_{C2} in (17) should be the ones after the synchronous compensation is installed. However, as the level of synchronous compensation is unknown at the beginning, which is the target value to be quantified, an approximation is made, where the values of $|I_{SG1}|$, $|I_{HVDC}|$ and θ_{C2} without the SC is used for calculation. This will result in a small error between the target angle $\Delta\psi^*$ and the actual $\Delta\psi$ ($\Delta\psi$ being more desirable than the designed targets, which will be demonstrated with the case

TABLE 9 Results of quantification of required synchronous compensation level

Case number	C_2	θ_{C2} (°)	$\lvert I_{SG1}\rvert$ (kA)	$\lvert I_{SG2}\rvert$ (kA)	$\lvert FL_{SG2}\rvert$ (MVA)	$\Delta\psi^*$ (°)	$\Delta\psi_{RTDS}$ (°)	X_{RTDS} (Ω)	X_{Err} (%)
1	0.37	−50.03°	5.74	7.87	3746.93	10°	5.5°	1.31	4.36
2	0.37	−50.03°	5.74	4.71	2243.44	15°	12.0°	1.48	11.41
3	0.37	−50.03°	5.74	3.11	1481.34	20°	16.8°	1.64	18.05
4	0.37	−50.03°	5.74	2.13	1014.54	25°	21.7°	1.80	24.69
5	0.37	−50.03°	5.74	1.45	690.66	30°	26.8°	1.97	31.74

studies presented later in the paper. As the type of the investigated fault scenarios is balanced fault, the impedance measured by the earth fault group (including AG, BG and CG elements) and phase-to-phase fault group (including AB, BC and CA elements) will be same. In this case, the parameters measured by AG elements are employed to display the results, whose measured impedance after the connection of SC is depicted in (18).

$$Z_M^{AG} = Z_L + \left(1 + \frac{I_A^{SG1} - K_0 I_G}{I_A^{HVDC} + I_A^{SC} + K_0 I_G}\right) R_{AG} \tag{18}$$

where Z_M^{AG} is the impedance measured by the AG elements; I_A^{SG1}, I_A^{SC} and I_A^{HVDC} are the phase A currents contributed by SG1, SC and HVDC respectively; K_0 is the residual compensation factor; I_G is the grounding current measured by the relay and R_{AG} is the fault resistance of phase-A impedance loop. As in balanced fault scenarios, the grounding current I_G in (18) becomes zero, therefore, (18) can be represented as (19).

$$Z_M^{AG} = Z_L + \left(1 + \frac{I_A^{SG1}}{I_A^{HVDC} + I_A^{SC}}\right) R_{AG} \tag{19}$$

Based on (19), the inputs of (17), for example, C_2, θ_{C2} and $|I_{SG1}|$, should be represented as $C_2 = \left|\frac{I_A^{HVDC}}{I_A^{SG1}}\right|$; $\theta_{C2} = \angle\left(\frac{I_A^{HVDC}}{I_A^{SG1}}\right)$ and $|I_{SG1}| = |I_A^{SG1}|$ respectively. The results of the cases in Table 8 are displayed in Table 9. In this table, the error of measured reactance, X_{Err}, in Table 9 is defined as (20).

$$X_{Err}\ (\%) = \left|\frac{X_{RTDS} - X_{act}}{X_{line}}\right| \times 100\% \tag{20}$$

where the X_{RTDS} is the reactance measured by the distance relay model in RTDS [29]; X_{act} is the actual reactance, which is $50\% \times X_{line} = 1.205\ \Omega$ in the studied cases and X_{line} is the total reactance of the protected line, which is 2.41 Ω ; $\Delta\psi^*$ is the target angle given by system operator; $\Delta\psi$ is the angle difference of the current infeed from both sides of the protected line observed in RTDS simulation.

Based on the results in Table 9, the proposed SC quantification method can estimate the required SC to control the impedance measurement error within the defined limit. The error of estimation is introduced by the changes of the system dynamics caused by the connection of SC, which has been discussed earlier in the section. Additionally, the calculated fault level can be further transformed to the capacity of SC if the fault capability of SC is known. For example, in this study, if ψ^* is set to be 15°, the quantified SC capacity will be around 280 MVA (assuming SC can contribute a fault level of 8 pu).

It should be noted that, the aforementioned sizing approach only considers protection performance. In practice, the system operators should quantify the SC capacity from multiple perspectives, for example, system stability, inertia level, fault level etc. The ultimate optimum level of SC required will need to consider all of the aforementioned factors and associated costs, but this is outside the scope of this paper.

6 | CONCLUSIONS

This paper has presented systematic tests for evaluating the impact of HVDC systems on the performance of two physical relays using a specifically developed HIL plasstform and an RTDS network model. In total, there are 480 cases tested for two relays, and the test scenarios cover different fault conditions, HVDC control strategies, levels of system strength and protection characteristics. From the results, compromised protection performance was observed in both relays, including failed operation, delayed tripping, and zone reach issues, when the conventional voltage sources are replaced by the converter based HVDC system. While the relays appear to have different performance in some individual cases, it was observed that both relays have compromised performance in 29% and 22% of the tested cases respectively with either delayed or failed tripping. Detailed analysis and investigation of the observed compromised protection performance has been conducted, and it was found that the main observed issues and causes are: under/over-reach issue due to the angle difference of the current infeed contributed from both ends of the protected line; faulted phase selection issues in AG fault with the balanced current and constant reactive power controller of the HVDC system; numerically unstable impedance measurement in AB fault with constant reactive power control used by the HVDC system. It should be highlighted that although the paper

discusses the AC protection issues caused by HVDC systems, the proposed HIL results and the analysis are generally also applicable for evaluating the distance protection performance in the transmission network with other converter-interfaced renewables.

Additionally, a method for quantifying the required level of synchronous compensation from the protection perspective has also been presented and validated, which allows the estimation of the SC capacity to limit the angle difference of the fault current from the two ends of the line within a certain value, thus ensuring the impedance measurement error of distance protection is within an acceptable range. The proposed SC quantification method provides additional insights for network operators to appropriately size the SC at HVDC sites from the distance protection perspective.

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CONFLICT OF INTEREST

The authors have no conflicts of interest to this work.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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