Energy Reports 6 (2020) 3346–3356

Contents lists available at ScienceDirect

Energy Reports

journal homepage: www.elsevier.com/locate/egyr

A computationally efficient robust voltage control for a single phase dual active bridge

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ARTICLE INFO

Article history:
Received 7 September 2020
Received in revised form 30 October 2020
Accepted 26 November 2020
Available online 4 December 2020

Keywords:
Dual active bridge converter
DC–DC converters
Fractional order systems
Rapid control prototyping
Single phase shift modulation
Sliding mode controller

ABSTRACT

This paper proposes fractional and integer order sliding mode controllers (SMC) for the high voltage (HV) bridge control in a bidirectional dual active (DAB) converter. The proposed controllers are derived based on nonlinear model of DAB converter and the closed loop stability is ensured using integer and fractional order Lyapunov theorems. Fractional order controllers offer more degree of freedom to adjust the desired response of the system, however the implementation issues of such controllers are rarely explored. Both variants of control schemes are implemented on a DSP control card, and hardware-in-the-loop (HIL) and processor-in-the-loop (PIL) experiments are conducted using rapid control prototyping technique. In order to choose the most suitable robust controller, experimental data for the two performance indices namely robustness and computational resources utilization is compared for both integer and fractional order control schemes. The experimental results demonstrate that the integer order SMC utilizes reduced computational resources as compared to the fractional order SMC. Moreover it is further verified that integer order SMC exhibits comparable robustness as fractional order SMC under all test conditions.

1. Introduction

In modern power grids, the isolated bidirectional DC–DC converters are finding interesting applications. An enormous attention has been paid to the bidirectional dual active bridge (DAB) converters, because of its inherent advantages such as zero voltage switching, galvanic isolation, and high power density (Xue et al., 2015; Riedel et al., 2017; Shi et al., 2015; Zhao et al., 2017; Engel et al., 2015). Fig. 1 shows a general layout of a microgrid system that includes AC–DC and DC–DC converters. DAB integrated battery storage system is an integral part of the microgrids, thus bidirectional DAB converters are utilized to store or supply power from battery storage system depending on the mode of operation.

The performance of battery storage system depends on several factors that include the robustness of closed-loop control algorithms, fast dynamic response of the system in the event of fluctuations at the source or load sides, and the dynamics of DC link. To ensure the robust performance of battery storage system, a lot of work has been reported on the closed-loop control of the DAB converters. Both linear control schemes and nonlinear control paradigms have been reported and applied for the voltage and current control of the DAB converters (Kheraluwala et al., 1992; Tiwari et al., 2019; Segaran et al., 2013; Zumel et al., 2016; Dutta et al., 2016; Liu et al., 2016; Farooq et al., 2019; Talbi et al., 2015; Carrizosa et al., 2013). Proportional, integral and derivative (PID) controllers are the most commonly used linear control method, that are easy to implement and have a simple structure. In Kheraluwala et al. (1992) and Tiwari et al. (2019), the authors reported conventional PI controllers to stabilize the output voltage of a DAB converter. However, the conventional PI controllers show poor and unsatisfactory performance when the system is

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https://doi.org/10.1016/j.egyr.2020.11.246

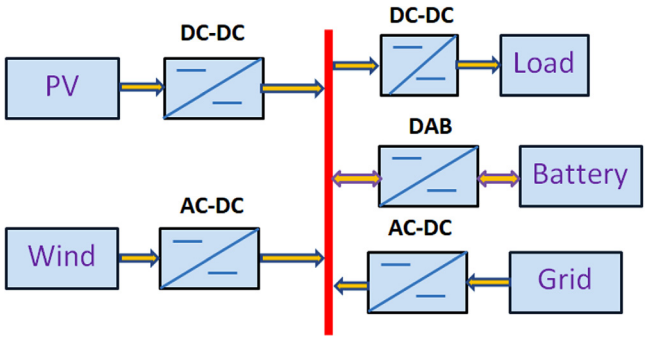


Fig. 1. DC micro-grid configuration.

subject to uncertainties and parameters variations. In Segaran et al. (2013), a feed forward control method based on lookup table is presented for the current control of a DAB converter. However, the lookup table is calculated based on the nominal parameters of the DAB converter, thus the control performance of the system will degrade with parametric uncertainties. To overcome the bandwidth limitation of the PI controllers, a boundary control method is presented in Zumel et al. (2016). In Dutta et al. (2016), a method based on the transformer's current samples is proposed for the DAB converter. The samples are taken at every switching cycle, based on current samples, the control signal is generated for the next switching cycle. In the above mentioned work, the control signal is generated based on the instantaneous current instead of the average current, thus the control signal can suffer from large spikes and it can lead the system to instabilities in the absence of proper filtration. In Liu et al. (2016), a fuzzy logic based control system is proposed for the current loop of the DAB converter. Fuzzy system based method does not require any prior knowledge about the system parameters; however such controllers require cumbersome tuning efforts and need high computational resources over the processor. Moreover there is no formal method to prove the closed-loop stability when it is controlled using fuzzy logic systems. Similarly an adaptive weighted artificial neural controller is proposed in Farooq et al. (2019). The method is simple in structure and as robust as any other control method.

In addition to the linear and model free controllers, different nonlinear control techniques based on the system's nominal parameters have been reported in the existing literature. The nonlinear controllers provide fast dynamic response and possess the capability for compensating the disturbances and system uncertainties. The classical sliding mode controller (SMC) is reported for the current loop of the bidirectional DAB converter in Talbi et al. (2015), Carrizosa et al. (2013). With linear sliding surface and without integral term, the controller showed steady state error and large overshoots. In Jeung and Lee (2018), Jeung et al. (2016), a double integral SMC is proposed for the voltage and current control of a DAB converter. With the application of double integral SMC , the steady state error is compensated using double integral terms; however, the "signum" function is replaced with its continuous approximation that caused poor performance of the controller. In the above literature all the discussed control methods are integer order. Fractional order controllers (FOSMC) have been widely applied in different fields such as biomedical engineering, numerical analysis, chaotic systems and Mechatronic engineering applications (NasimUllah et al., 2017; Ullah et al., 2015; Ibeas et al., 2017; Miller and Ross, 1993). Several interesting applications of FOSMC includes power converters, aerospace and biomedical engineering applications (NasimUllah et al., 2017; Ullah et al., 2015; Ibeas et al., 2017; Miller and Ross, 1993). These include the generalized fractional order sliding mode control (FOSMC) (Vinagre and Calderon, 2006), hybrid fractional order fuzzy sliding mode controller (fuzzy-FOSMC) (Delavari et al., 2010) and novel FOSMC for a DC–DC power converter (Calderón et al., 2006). The fractional calculus based SMC controller can be formulated based on the mathematical model of DAB. An introductory theory of fractional order (FO) derivatives and integration is explained in Miller and Ross (1993), Matignon (1998). Generally, fractional calculus based controllers provide more degree of freedom as compared to the integer order controllers (IOC's) (Aghababa, 2014). Therefore; for optimal dynamic response of the system, the controller can be tuned without losing the robustness. In addition, the stability analysis of fractional calculus based controllers is briefly discussed by the author in Li and Deng (2007), Zhang and Li (2011), Gao and Liao (2012). The stability of FOSMC controllers using integer and fractional order Lyapunov theorems is reported in Burton et al. (2011), Kiruthiga (2015), Lima et al. (2011), Mechter et al. (2015), Patton et al. (2000), Segaran et al. (2010), Zhao et al. (2014), De Doncker et al. (1988), Podlubny (1999), Oldham and Spinier (1974), Ullah et al. (2019), Zhang and Li (2011), Prasanna and Rathore (2014), Sun et al. (2017), Rahmani et al. (2016a,b), Rahmani (2018), Rahmani and Rahman (2018). The application of fractional calculus based controllers is limited to the basic topologies of power converters such as buck and boost converters. To the author's best knowledge, FOSMC have rarely been applied to DAB integrated systems, thus its utilization in the advanced DC–DC converter topologies have not been exploited well. Inspired by the precedent research work, this proposal aims to fill the research gap by investigating the fractional calculus based SMC controllers and its application to the bidirectional DAB converters. In addition, the motivation behind this work is to investigate the computational resources required by FOSMC controllers when programmed to a processor (Prasanna and Rathore, 2014; Sun et al., 2017). Overall the computational resources will give us an idea if FOSMC controllers are feasible for practical applications such as DAB integrated systems.

Based on the above literature survey, this paper formulates fractional and integer order sliding mode controllers for HV bridge voltage regulation problem of a DAB converter connected in a DC micro-grid configuration. A large signal nonlinear model of DAB converter is used to derive the proposed controller. To get a relation between the control performance and fractional orders α of the controllers, two variants of the proposed FOC ($\alpha = 0.99$ and $\alpha = 0.95$) are implemented on a Texas Instrument (TI) DSP processor (TMS320F28379D). The performance of FOSMC and SMC is tested under source, reference and load variations.Main contributions of this paper are given as follows

1. FOSMC controllers are rarely exploited for DAB converters. More specifically the computational resource utilization of FOSMC controllers is never reported for its practical implementation over processors. In this paper PIL experiment is performed to get an idea of the computational resources for both FOSMC and integer order SMC control schemes.

2. Based on nonlinear model of DAB converter, fractional and integer order robust voltage controllers are derived and implemented using rapid prototyping method

3. Based on the two performance indices, a best controller which exhibits robustness and utilizes less computational resources is chosen.

4. Stability of the closed-loop controllers is verified using fractional and integer order Lyapunov theorems .

The rest of the paper is organized as follows. Section 2 explains the basic topology of DAB converter, its operating wave forms,

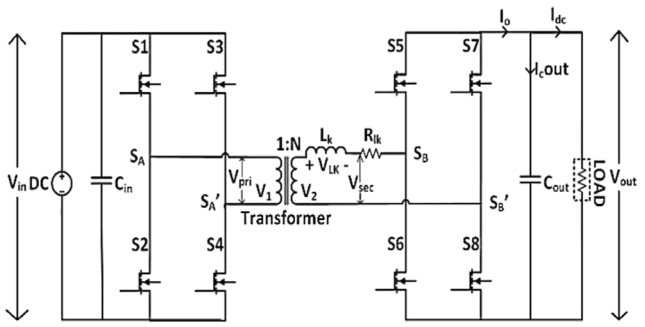


Fig. 2. Circuit configuration of DAB converter.

and the mathematical modeling. Section 3 discusses basic theory of fractional calculus. Section 4 formulates the proposed controller. Section 5 discusses the experimental results and Section 6 concludes the rest of the paper.

2. The bidirectional dual active bridge converter

2.1. Circuit configuration

The circuit configuration of the bidirectional DAB converter is shown in Fig. 2. The system consists of two H-bridges converter configuration connected to the high frequency transformer's primary and secondary side. Filtering capacitors are connected at high and low voltage side of the bridges to smooth out the ripples. The desired power flow is achieved through an auxiliary inductor, connected to the transformer secondary side (Podlubny, 1999). The parameter L represents the sum of leakage inductance of the high frequency transformer and auxiliary inductor. The primary and secondary turns of transformer are represented by N_P and N_S respectively. The high voltage (HV) bridge of the converter is connected to battery storage system, whereas the low voltage (LV) side is connected to variable source DC supply.

2.2. Operating wave forms

Fig. 3 illustrates the operating wave forms of the DAB converter using single phase shift (SPS) modulation scheme. Using SPS method, the duty cycle of both the bridges is kept at 50%, whereas, the phase angle between them determines the quantity and direction of the power flow. The voltage across the inductor is the difference of transformer primary voltage referred to secondary side (v_{sec}), and terminal voltage of the bridge (v_{h2}) operated with leading phase shift. The positive phase shift enables the flow of power from the low to high voltage side and vice versa. The expression of average power is given as follows (Oldham and Spinier, 1974).

$$Pout = \frac{n\,|v_1|\,|v_2|}{2f_s L_k}\,\frac{\delta(1-\delta)}{\pi^2} \tag{1}$$

Here v_1 and v_2 refer to transformer's primary and secondary voltages, δ represents the phase shift angle between the two bridges and f_s corresponds to the switching frequency, whereas L_k is the equivalent inductance of auxiliary inductor and transformer itself. From Eq. (1), the relation between output power and phase shift is evidently nonlinear and subject to parameter variations.

2.3. Mathematical modeling of DAB converter

The mathematical model of DAB converter is derived based on Fourier series switching harmonics of a square wave function (Segaran et al., 2013; Jeung and Lee, 2018). The developed

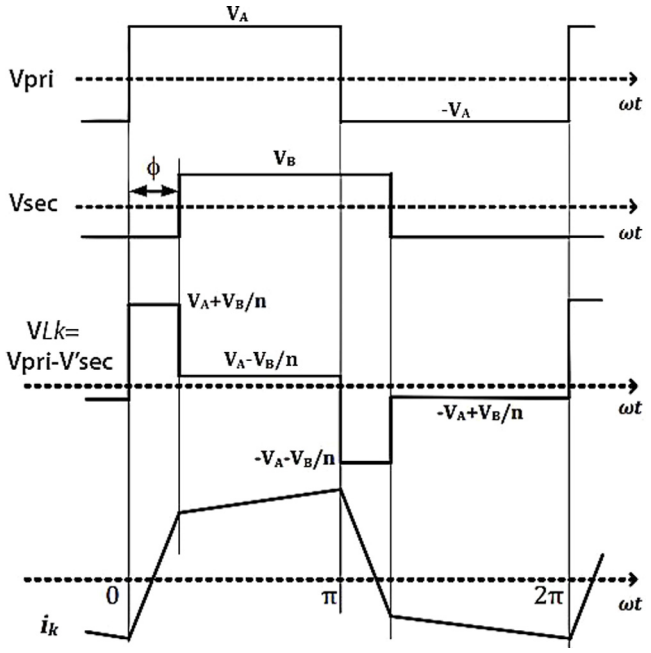


Fig. 3. SPS modulation of DAB converter for power flow from low to high voltage side (a) primary voltage of transformer referred to secondary side v_{sec} (b) secondary voltage v_{h2} (c) voltage across inductor v_{LK} (d) inductor current i_{LK}.

low harmonic model characterizes the output voltage of the DAB converter at HV bridge. A square wave represented by the basic switching function is expressed as follows (Rahmani et al., 2016b).

$$S_A = \frac{1}{2} + \frac{2}{\pi}\sum_{n=0}^{\infty}\frac{sin\,(2n+1)\,(\omega_s t)}{2n+1} \tag{2}$$

Primary side voltage can be obtained and expressed as follows:

$$v_{prim} = V_{source}\left\{\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{sin\,(2n+1)\,(\omega_s t)}{2n+1}\right\} \tag{3}$$

Similarly for HV bridge, MOSFET, s switching phenomena is expressed as follows:

$$V_{\sec} = V_{load}\left[S_B - S_B^{"}\right] \tag{4}$$

$$v_{\sec} = V_{load}\left\{\frac{4}{\pi}\sum_{n=0}^{\infty}\frac{\sin\,(2n+1)\,(\omega_s t-\delta)}{2n+1}\right\} \tag{5}$$

Here, δ refers to the phase shift of the modulating signal. Referring to Fig. 3, the power is transferred to the HV bridge, and therefore the modulation scheme of the secondary bridge is operated with phase delay of δ with respect to the primary bridge. Using basic Kirchhoff voltage laws at the HV side of the circuit yields the following expression:

$$R_{Lk} i_{Lk}(t) + L_k \frac{d}{dt} i_{Lk} = N v_{prim}(t) - v_{sec}(t) \tag{6}$$

Here, N refers to the transformer turns ratio i.e. $Ns : Np$. By combining Eq. (3) and Eq. (5) with Eq. (6), the inductor current and impedance are characterized as follows:

$$i_{Lk}(t) = \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{1}{(2n+1)}\begin{bmatrix}\frac{N v_{prim}}{|Z(n)|}\sin\left[(2n+1)\,\omega_s t\right] \\ -\varphi_Z(n) - \frac{v_{\sec}}{|Z(n)|} \\ \sin\begin{bmatrix}(2n+1) \\ (\omega_s t-\delta)\end{bmatrix} \\ -\varphi_Z(n)\end{bmatrix} \tag{7}$$

$$|Z\,(n)| = \sqrt{{R_{Lk}}^2 + [(2n+1)\,\omega_s L_k]^2} \tag{8}$$

$$\varphi_Z\,(n) = tan^{-1}\left(\frac{(2n+1)\,\omega_s L_k}{R_{Lk}}\right) \tag{9}$$

Here $Z(n)\angle\phi_z(n)$ refers to the impedance and its corresponding angle. By applying Kirchhoff current law at HV side of the converter yields the following expression;

$$C_{out}\frac{dv_{cout}}{dt} = i_{out} - i_{load} \tag{10}$$

The current i_{out} can be expressed in-terms of inductor current and switching states i.e.; $i_{out} = i_{Lk}(S_B - S_B{}^*)$. By combining Eq. (10) with the inductor's current expression and replacing Eqs. (5) and (7) in the final expression yields the following formulation.

$$\begin{aligned}\frac{d}{dt}v_{out} &= -\frac{v_{out}\,(t)}{R_{load}} \\ &+\frac{1}{C_{out}}\left[\frac{4}{\pi}\sum_{n=0}^{m}\begin{matrix}\dfrac{NV_{in}}{(2n+1)\,|Z\,(n)|} \\ \times\sin\left(\begin{matrix}(2n+1)\,\omega_s t \\ -\varphi_z\,(n)\end{matrix}\right)\end{matrix} - V_{out}\sin\left(\begin{matrix}(2n+1)\,\omega_s t-\delta \\ -\varphi_z\,(n)\end{matrix}\right)\right] \\ &+\frac{4}{\pi}\sum_{r=0}^{1}\frac{1}{(2r+1)}\sin\left((2r+1)\,(\omega_s t-\delta)\right)\end{aligned} \tag{11}$$

By simplifying Eq. (11), the final expression for the output voltage can be obtained as follows: (Jeung and Lee, 2018).

$$\begin{aligned}\frac{dv_{load}}{dt} &= \frac{-8}{C_{out}\pi^2}\sum_{n=1,3,5,..}^{\infty}\frac{\cos\left(\varphi_z\,(n)\right)}{n^2\,|Z\,(n)|}v_{load} \\ &+\frac{8}{C_{out}\pi^2}\sum_{n=1,3,5,..}^{\infty}\frac{\cos\left(n\delta-\varphi_z\,(n)\right)}{n^2\,|Z\,(n)|}NV_{source} \\ &-\frac{i_{load}}{C_{out}}\end{aligned} \tag{12}$$

Eq. (12) shows the nonlinear relation between the phase shift (δ) and the voltage dynamics of the HV bridge for the odd harmonics states i.e. $n = 1, 3, 5\ldots$. Further, Eq. (12) can be represented in state space model as follows:

$$\dot{x}_v = A(x_v) + B(x_v)u + D \tag{13}$$

Here, $A(x_v)$ and $B(x_v)$ represent state matrices. Where, $x \in R^r$ is state of the system and u is the controls signal that will be expressed in-terms of phase shift signal. Additionally, the state matrices are expressed as follows:

$$A(x_v) = \frac{-8}{C_{out}\pi^2}\sum_{n=1,3,5,..}^{\infty}\frac{cos\left(\varphi_z\,(n)\right)}{n^2\,|Z\,(n)|}V_{load}$$

$$B(x_v) = \frac{8}{C_{out}\pi^2}\sum_{n=1,3,5,..}^{\infty}\frac{1}{n^2\,|Z\,(n)|}NV_{source}$$

$$D = -\frac{i_{load}}{C_{out}}.$$

It is assumed that the system parameters vary in a small range, therefore the disturbance term D can be further extended by including the uncertainties and parametric uncertainties. The lumped disturbance term can be written as follows;

$$\begin{aligned}G &= D + \Delta d_{load} + \Delta d_{source} + \Delta A(x_v) \\ &+\frac{-8}{C_{out}\pi^2}\sum_{n=3,5,..}^{\infty}\frac{\cos\left(\varphi_z\,(n)\right)}{n^2\,|Z\,(n)|}v_{load} \\ &+\frac{8}{C_{out}\pi^2}\sum_{n=3,5,..}^{\infty}\frac{1}{n^2\,|Z\,(n)|}NV_{source}\end{aligned} \tag{14}$$

Here the source and load side disturbances are represented as Δd_{source} and Δd_{load} respectively. The parameter uncertainties are represented as: $\Delta A(x_v)$. With the above definitions, Eq. (13) is expressed as follows:

$$\dot{x}_v = A(x_v) + B(x_v)u + G \tag{15}$$

Eq. (15) represents the nonlinear model of the DAB converter. In the next section fractional calculus and basic mathematical preliminaries are discussed briefly.

3. Fractional calculus

This section presents the basic concepts of fractional calculus that are necessary to understand for formulation of the FOSMC control scheme.

3.1. Preliminary definition of fractional calculus

This section gives an overview of fractional integrator and derivative operators. The fractional operator in generalized form is expressed as follows: (Ullah et al., 2019; Zhang and Li, 2011)

$${}_aD_t{}^{\alpha} \cong \begin{cases}\frac{d^{\alpha}}{dt^{\alpha}} & R(\alpha) > 0 \\ 1 & R(\alpha) = 0 \\ \int_a^t d\tau^{\alpha} & R(\alpha) < 0\end{cases} \tag{16}$$

Here α represents the order of fractional operator. The general definition is extended further to formulate the α^{th} order Riemann–Liouville (RL), Caputo definition and Grundwald-Letnikov definitions (Ullah et al., 2019; Zhang and Li, 2011). Mapping of fractional order systems is performed differently then the integer order system on **S** plane. Apart from the left half region of **S** plane, half of its positive plane is also included in the stable region for fractional order systems when $\alpha = (0 \rightarrow 1)$ (Prasanna and Rathore, 2014). Oustaloup recursive algorithm is used to approximate the fractional operator (Lima et al., 2011), and it is expressed in form of a rational transfer function. This transfer function has poles and zeros that depend on the specific values of α.

4. Formulation of closed loop control

This section describes the formulation of both FOSMC and integer SMC with details. Further the stability proof of the closed loop system with both fractional and integer order dynamics is also presented in the subsections given below.

4.1. Fractional order sliding mode control

In this section, a fractional order closed loop voltage controller is derived for the DAB converter system. The derived model of DAB converter given in Eq. (15) is used to design the controller. In order to design the control scheme, the error term is formulated as follows:

$$e_v = x_v - x_{vd} \tag{17}$$

Time derivative of the error is expressed as follows:

$$\dot{e}_v = \dot{x}_v - \dot{x}_{vd} \tag{18}$$

Based on the error dynamics presented above, a fractional order sliding surface is selected as follows (Ullah et al., 2015):

$$s_v = k_{v1} D^{-\alpha} e_v + k_{v2} \int \dot{e}_v \tag{19}$$

Where k_{v1}, k_{v2} represent the sliding surface constants. By multiplying fractional operator D^{α} on both hand sides of Eq. (19), one obtains the following relation.

$$D^{\alpha} s_v = k_{v1} e_v + k_{v2} D^{\alpha-1} \dot{e}_v \tag{20}$$

Using Eq. (15), the expression of Eq. (20) can be modified in the following form:

$$D^{\alpha} s_v = k_{v1} e_v + k_{v2} D^{\alpha-1} (A(x_v) + B(x_v)u + G - \dot{x}_{vd}) \tag{21}$$

By re-arranging the terms in Eq. (21), the desired control law u is derived as follows:

$$u = (k_{v2} B(x_v))^{-1} \begin{bmatrix} -k_{v2} A(x_v) + k_{v2} \dot{x}_{vd} - k_{v1} D^{1-\alpha} e_v \\ -k_s D^{1-\alpha} \mathrm{sgn}(s_v) \end{bmatrix} \tag{22}$$

Here k_s represents switching gain of the proposed control law u.

Fractional order Lyapunov theorem is used to prove the stability of the derived controller of Eq. (22) (Prasanna and Rathore, 2014).

Theorem 1. *The proposed control paradigm of Eq. (22) stabilizes the system given in Eq. (15). Once the system becomes stable, the error defined in Eq. (17) converges to zero. Thus for the proposed sliding surface of Eq. (19), following inequality holds true (Prasanna and Rathore, 2014):*

$$\left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^{j} s_v D^{\alpha-j} s_v \right| \leq \Omega_1(s_v) \tag{23}$$

Here s_v represents the voltage sliding surface and $\Omega_1(.)$ is a positive constant. The Lyapunov candidate function is defined as follows:

$$V_V = \frac{1}{2} s_v^2 \tag{24}$$

By applying D^{α} to Eq. (24), one obtains the following expression (Prasanna and Rathore, 2014):

$$D^{\alpha} V_V = s_v D^{\alpha} s_v + \left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^{j} s_v D^{\alpha-j} s_v \right| \tag{25}$$

Eqs. (21)–(23) are combined and then simplified to acquire the following expression:

$$D^{\alpha} V_V \leq s_v (k_{v1} e_v + k_{v2} D^{\alpha-1} (A(x_v) + B(x_v)u + G - \dot{x}_{vd})) + \left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^{j} s_v D^{\alpha-j} s_v \right| \tag{26}$$

By combining Eq. (26) and Eq. (22), and by setting $D^{\alpha-1} D^{1-\alpha} = D^0 = 1$, one obtains the following expression

$$D^{\alpha} V_V \leq -k_s |s_v| + G + \Omega_1(s_v) \tag{27}$$

By letting $k_s > G_{\max} + \Omega_1(s_v)$, it is easy to show that $D^{\alpha} V_V \leq 0$ which means that the reaching condition of the sliding surface is satisfied and $s_v = 0$. Furthermore, the control signal from Eq. (22) can be written more precisely in terms of phase shift as follows:

$$u = cos\,(n - \varphi_z\,(n)) \tag{28}$$

Therefore by using basic trigonometric laws, Eq. (28) can be generalized and expressed as follows:

$$\delta = \sin^{-1}(u) \tag{29}$$

By replacing Eq. (22) in Eq. (29) one obtains the following control expression:

$$\delta = \sin^{-1} \left[(k_{v2} B(x_v))^{-1} \begin{bmatrix} -k_{v2} A(x_v) + k_{v2} \dot{x}_{vd} \\ -k_{v1} D^{1-\alpha} e_v - \\ k_s D^{1-\alpha} \mathrm{sgn}(s_v) \end{bmatrix} \right] \tag{30}$$

By utilizing Eq. (30), the nonlinear dynamics of the system can be expressed in terms of phase shift. From Eq. (1) it is obvious that for maximum power transfer the phase shift should be $\delta \rightarrow \frac{\pi}{2}$. Therefore, the phase shift amount of $\frac{\pi}{2}$ is equal to 250 counts of the PWM register of the control board.

4.2. Integer order sliding mode control

In this sub-section integer order sliding mode controller is derived based on the nonlinear state space model of Eq. (15). Let the integral sliding surface is defined as follows:

$$S_v = C_1 e_v + C_2 \int e_v \tag{31}$$

Here C_1 and C_2 represent gains of the sliding surface. Differentiating Eq. (31) and by combining it with Eq. (15) yields the following equation.

$$\dot{S}_v = C_1 (A(x_v) + B(x_v)u + G - \dot{x}_{vd}) + C_2 e_v \tag{32}$$

From Eq. (32), the control law becomes:

$$u = -C_1 B {x_v}^{-1} [\ -C_1 A x_{vd} - C_2 e_v + C_1 \dot{x}_{vd} - k_v sgn S_v\ ] \tag{33}$$

For the stability proof, the Lyapunov function is chosen as follows:

$$V = \frac{1}{2} S^2 \tag{34}$$

Therefore, by combining Eq. 32, 33 and first derivative of Eq. 34, the stability of the closed system is ensured subject to the following condition: $k_v > G_{max}$.

5. Experimental results and discussion

HIL and PIL experiments are performed for robustness and computational resource utilization test of the discussed controllers. Block diagrams of HIL and PIL experimental setups are shown in Fig. 4 and Fig. 5 respectively. The derived controllers are tested for three different conditions. In the sub-section below, the experimental test bench and collection of experimental data via high speed serial port of the control board is explained.

5.1. Experimental test bench and serial data logging

The test bench for HIL experiment is shown in Fig. 4. In HIL, a hardware DAB converter system is physically integrated to the DSP control card. The control board consists of a dual core processor TMS320F379D which is programmed through rapid prototyping method from Simulink environment. The control board exchanges real-time data with both the DAB hardware test bench and Simulink. Data received and recorded from DAB converter is exchanged through analog to digital (ADC) converters and pulse width modulation (PWM) modules respectively. While the experimental data collected from DAB converter is logged into the Simulink environment through a high speed serial port of the control board. In PIL experiment, DAB converter is not physical rather it is a software model in Simulink environment interfaced to the hardware DSP control card. Data is exchanged between the DSP control card and the software DAB converter using high speed serial port.

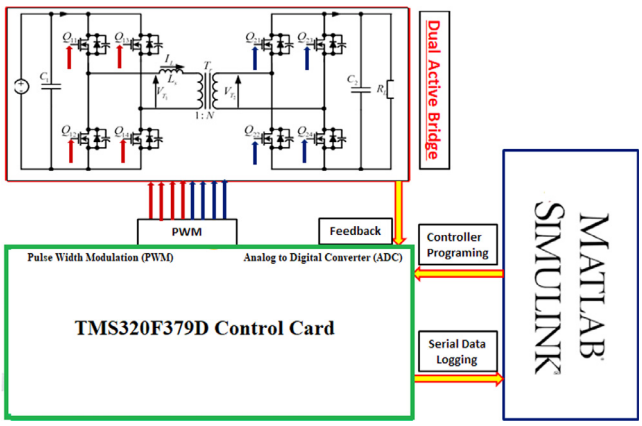


Fig. 4. HIL experimental setup diagram.

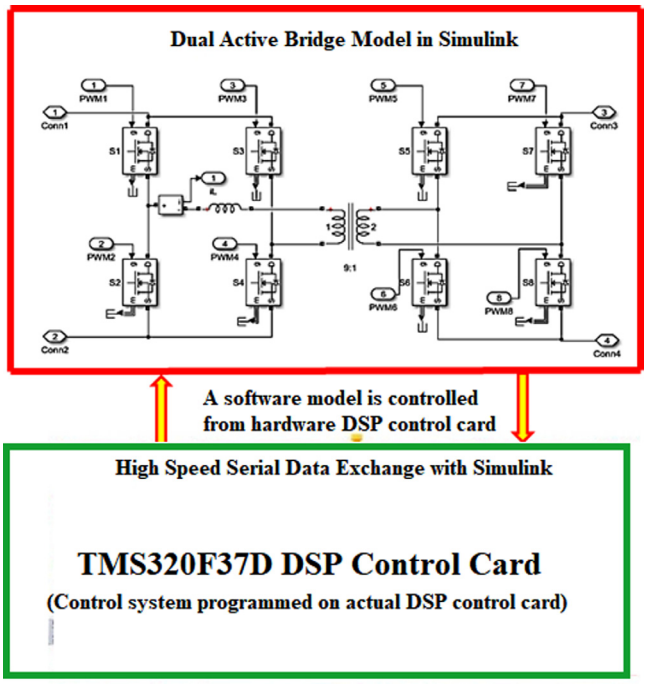


Fig. 5. PIL experimental setup diagram.

5.2. System and control parameters

System parameters are listed in Table 1 and control gains are given in Table 2. As shown in Table 2, the PI control gains are selected based on the author's previous work reported in Farooq et al. (2019). Moreover for integral SMC, the parameters of equivalent control are the same as PI controller and the switching gain is adjusted based on the maximum limit of signal variations in all test conditions. In order to choose the fractional controller with best performance, two non-integer orders controllers of orders $\alpha = 0.99$ and $\alpha = 0.95$ are tested.

5.3. Implementation of fractional order controller

Fractional order controllers are robust and flexible as compared to integer order control schemes. The fractional order integrator and derivative add complexities to the practical implementation of such controllers as compared to integer order control paradigms. In this work, fractional order integrator and derivatives are approximated using Oustaloup filter. Poles and zeros

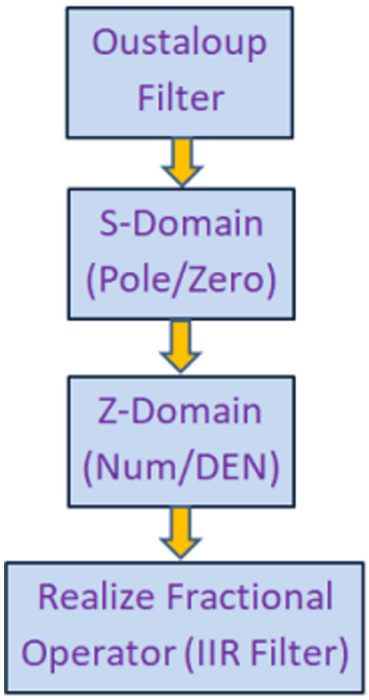


Fig. 6. Implementation of fractional operator.

Table 1
System parameters.

Parameters	Value
Rated power	150 Watts
Input voltage v_{source}	12 to 16 V
Output voltage v_{out}	20 to 24 V
f_s	200 Khz
C_{in}, C_{out}	100 uF, 200 uF
Transformer's turn ratio	1:2
Leakage inductance(L_k)	50 uH
Variable load	35–65 watts

are extracted from the Oustaloup filter in continuous domain and then transformed into z-domain. After converting it to z-domain, infinite impulse response (IIR) filter is used to implement the fractional operators practically. The rest of the process is explained in Fig. 6. As mentioned above the FOSMC control method is tested with two variants, i.e. $\alpha = 0.99$ and $\alpha = 0.95$. Goal of the experimentation is to control the output voltage of the high voltage bridge (HV) and to verify the robustness of the derived FOSMC and SMC controllers under three different test conditions; that include the source voltage, load and reference command variations (Farooq et al., 2019). The experimental results are compared to choose the best performing controller. Single-phase shift modulation scheme is used in the experiment (Tiwari and Sarangi, 2019). The collected results are discussed in the subsections given below.

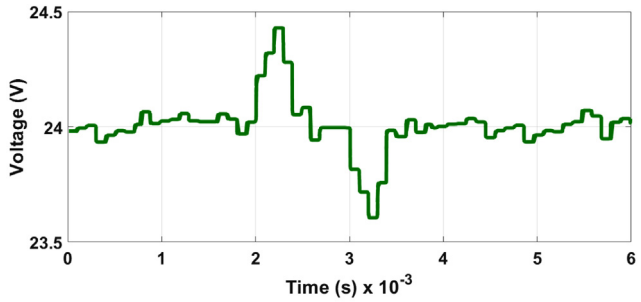
6. HIL testing

6.1. Test Case 1

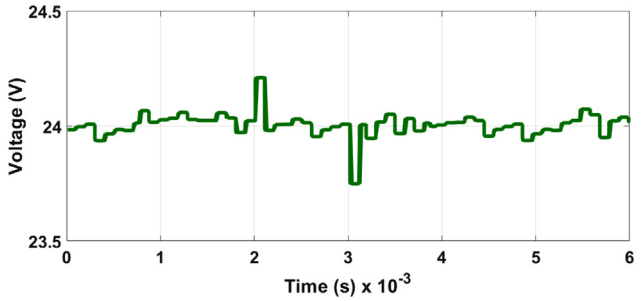
A constant reference voltage of 24 V is given in the first test case to analyze the performance of the derived control schemes. A variation between 12 V $\rightarrow$ 16 V in the input source voltage at various instances is carried out. Initially it is kept constant to 12 V during (1$\rightarrow$2) ms and then varied abruptly to 16 V from 12 V during (2$\rightarrow$3) ms and finally it is made constant for the rest

Table 2
Control system parameters.

Controller	Parameters	Value
Integral SMC	C_1	1.5
	C_2	1.2
	k_s	0.5
FOSMC	αth order	0.99, 0.95
	k_{v1}	1.5
	k_{v2}	1.2
	k_s	0.5
	w_b, wh	0,500 Hz



(a) With α= 0.99

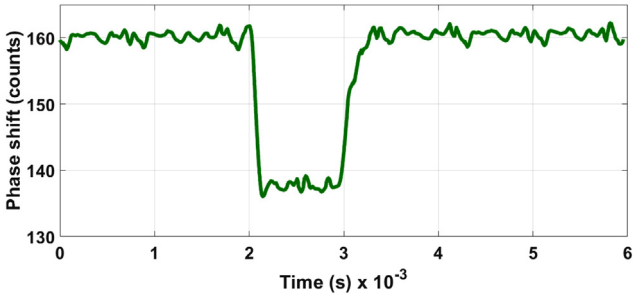


(b) With α= 0.95

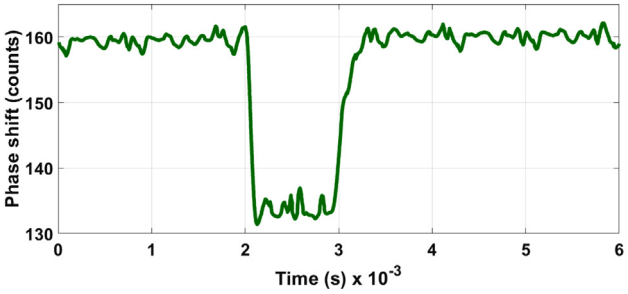
Fig. 7. Voltage tracking response of system with FOSMC controllers under source variations.

of time. In presence of the mentioned source voltage variations, the HV bridge voltage response with FOSMC control variants is shown in Fig. 7a and 7b. By comparing the experimental results of Fig. 7a and 7b, it is noted that the FOSMC controller with $\alpha = 0.95$ shows superior performance in terms of overshoot, undershoot and convergence time . The results shows that the for $\alpha = 0.95$, the total time for voltage convergence to its reference is 0.2 ms with an overshoot of 0.2 V and undershoot of -0.2 V and with $\alpha = 0.99$ it takes 0.8 ms with an overshoot of 0.4 V and undershoot of -0.4 V.

The corresponding phase shifts generated by FOSMC controllers are shown in Fig. 8a and 8b. The results depict that for the change in source voltage from 12 V to 16 V during $(2\rightarrow3)$ *ms*, the phase shift decreases to a lower level. The phase shift settles to a constant value after the subject variations. For both variants of FOSMC control scheme, the phase shift count is initially fixed at approximately 160 counts. With the mentioned variations of source voltage, the phase counts are observed to decrements from 160 to 136 when $\alpha = 0.99$. On the other side, the noted decrements is from 160 to 132 counts with $\alpha = 0.95$. The phase shift envelop of the fractional order control scheme with $\alpha = 0.95$ is bigger as compared to the second variant of the FOSMC method, and thus the superior performance of the first



(a) With α= 0.99



(b) With α= 0.95

Fig. 8. Phase shift of fractional order controllers with source variations.

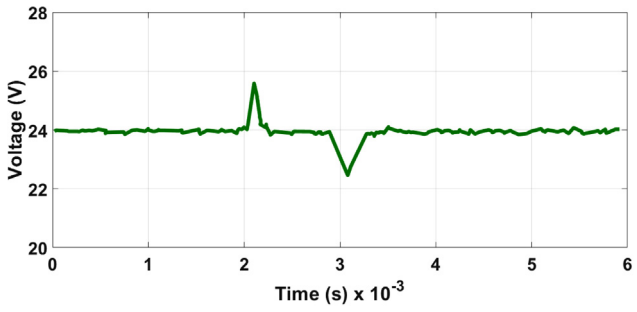
variant fractional control scheme is already evident from Fig. 7b in comparison to Fig. 7a.

Fig. 9a and 9b show the voltage tracking response and corresponding phase shift of the system with integral SMC. As mentioned above, the same source voltage variations are applied to the system. By comparing the experimental results of Fig. 9a and 9b with Fig. 7a and 7b, it is noted that the system under integral SMC controller shows better steady state response. The results show improved convergence time for the output voltage tracking and the observed convergence time is 0.1 ms. Similarly voltage overshoot of 1.5 V and an undershoot of -1.5 V is noted in the system with integral SMC. The corresponding phase shift is shown in Fig. 9b. When the source voltage is changed from 12 V to 16 V during time interval $(2\rightarrow3)$ *ms*, the phase shifts decreases to a lower level respectively. At $t = 3$ ms, the phase shift settles to a constant value. Under the variable source voltage scenario, the phase shift counts of integral SMC show a decrement from 170 to 130 in the same time interval of the subject variations.

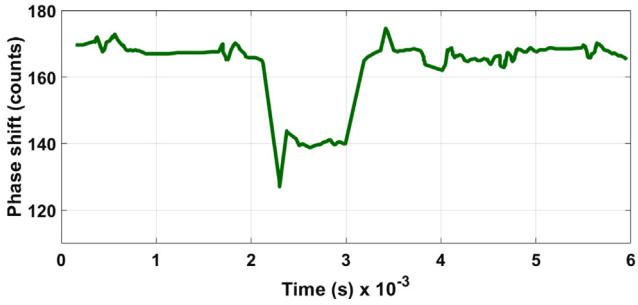
So from the above discussion and the presented results in Figs. 7–9, FOSMC controller with $\alpha = 0.95$ ensures the best transient performance while the integral SMC exhibits superior steady state performance. By comparing the transient performance of all variants of the controllers, the difference is not that significant between the FOSMC and integral SMC.

6.2. Test Case 2

In this case source voltage is fixed at 12 V while the reference command is varied between 20 V $\rightarrow$ 24 V at various instances. Initially it is kept constant at 24 V during time interval $(1\rightarrow2)$ *ms* and then it is varied abruptly to 20 V during time interval $(2\rightarrow3)$ *ms*. In presence of reference command variations, the voltage tracking response of the system with two variants of FOSMC and integral SMC controllers is shown in Figs. 10a, 10b and 10c respectively. The experimental results are presented to evaluate



(a) Voltage tracking response with integral SMC

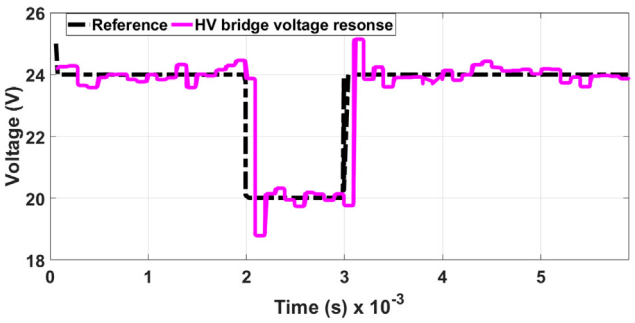


(b) Phase shift response with integral SMC

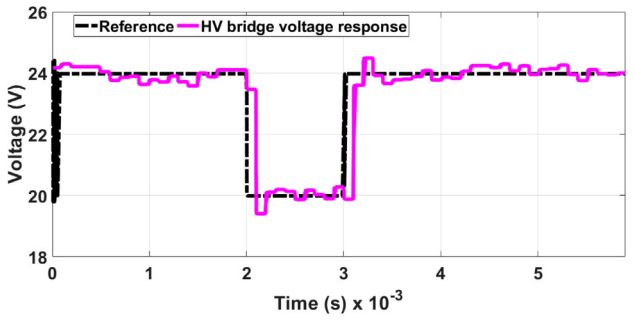
Fig. 9. Voltage tracking and phase shift response of integral SMC with source variations.

the performance of the derived control schemes with reference to the undershoot and overshoot in the tracking signal. FOSMC controller with $\alpha = 0.95$ shows improved performance as compared to the other two control schemes in terms of undershoot and overshoot. The results show that the for FOSMC controller with $\alpha = 0.95$, the time for voltage to converge to its reference is 0.1 ms with an overshoot of 0.5 V and an undershoot of -0.5 V. While FOSMC with $\alpha = 0.99$ takes 0.8 ms with an overshoot of 1.1 V and undershoot of -1.1 V. Fig. 10c shows the voltage tracking response of the system under the action of integral SMC. As mentioned above, the same reference command variations are applied to the DAB converter. By comparing the experimental results of Fig. 10c with Fig. 10a and 10b, it is noted that system under integral SMC controller shows better steady state performance. From the results presented, it is noted that the output voltage converges to its reference command in 0.4 ms with integral SMC. Similarly voltage overshoot of 1.2 V and undershoot of -1.2 V is noted with integral SMC.

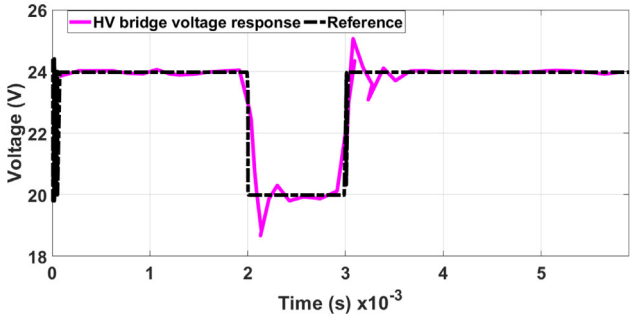
The corresponding phase shifts for test case 2 are shown in Fig. 11a and 11b. For the subject change in reference command during the time interval $(2 \rightarrow 3)$ *ms*, the phase shifts decrease to a lower level. At $t = 3$ ms, the phase shift settles to a constant value. Under the variable voltage scenario, the phase shift count shows a decrement from 160 to 130 With integral SMC. While for FOSMC with $\alpha = 0.99$ and $\alpha = 0.95$, the noted decrement is from 158 to 128. So from the above discussion and the presented results of Figs. 9–11, FOSMC controller with $\alpha = 0.95$ ensures best transient performance while the integral SMC exhibits superior steady state performance. Comparing the transient performance of all variants of controllers, the difference is not that significant between the FOSMC and integral SMC.



(a) With $\alpha = 0.99$



(b) With $\alpha = 0.95$

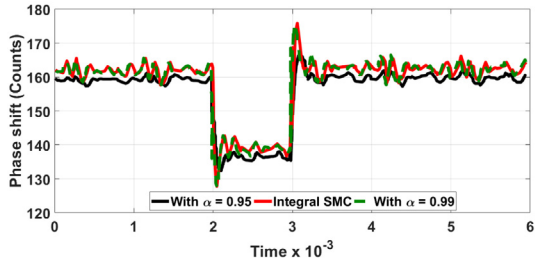


(c) With integral SMC

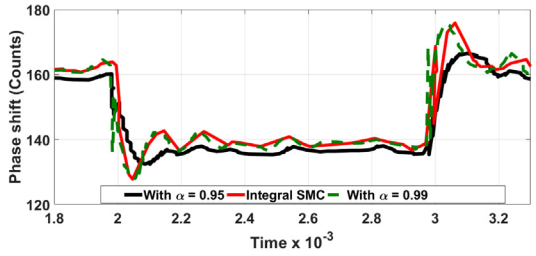
Fig. 10. Voltage tracking response with reference variations.

6.3. Test Case 3

In the case the source voltage is fixed at 12 V while the reference command is adjusted to a constant value of 24 V. Load is initially fixed at 11.5 Ω and then it is varied between 10 Ω to 14 Ω in the time interval $t = (2 \rightarrow 4)$ ms. In presence of the mentioned load variations, the voltage convergence time with both variants of FOSMC controllers and the integral SMC scheme is shown in Fig. 12a. The enlarged view of the voltage tracking response is shown in Fig. 12b. Similarly Fig. 12c shows the corresponding power changes in response to the voltage tracking errors. Fig. 12d shows the phase shift comparison under all variants of control schemes. By comparing the experimental results of Fig. 12a and 12b, it is noted that the FOSMC controller with $\alpha = 0.95$ shows superior performance in terms of overshoot, undershoot and convergence time. The results show that FOSMC controller with $\alpha = 0.95$, convergence time for voltage signal to its reference value is around 0.9 ms with an observed overshoot of 1.5 V and undershoot of -1.5 V. While for FOSMC control



(a)Phase shift variation comparison with all variants of controllers



(b)Enlarge view of Fig. 11a

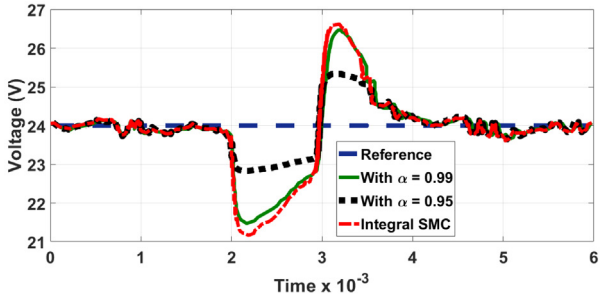
Fig. 11. Phase shift variations with reference command variations.

with $\alpha = 0.99$, it takes 0.9 ms with an overshoot of 2.4 V and undershoot of -2.4 V. For integral SMC, the time for voltage convergence to its reference value is recorded as 0.9 ms with an overshoot of 2.5 V and undershoot of -2.5 V.

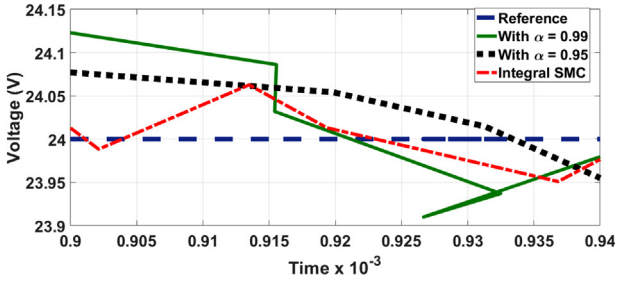
The corresponding changes in power are shown in Fig. 12c. As per specifications, DAB can deliver maximum power of 150 watts, however the tests are conducted in a low power range for the safety of the test bench. In the load test, initially the total load connected is kept fixed at 11.5 Ω and at 24 V, DAB delivers only (24/11.5)= 2.087*A*, and thus with constant load and constant voltage the amount of power consumed by the load is around 50 watts. As shown in Fig. 12c, with load changes the actual amount of power delivered also change. The load is switched at 2 ms to 10 Ω and then switched back to 14 Ω at 3 ms, while it is restored to 11.5 Ω at 4 ms. Now the power changes is due to the fact that voltage is controlled, and any changes in the current totally depends on the amount of voltage change across the load, so the power change is different under controllers. As shown in Fig. 12c, under FOSMC controller with $\alpha = 0.95$, the power change is minimum. This is due to the fact that the same controller ensures lesser voltage deviation. Under the variable load scenario, the phase shift count shows a increment from 160 to 178 in case of integral SMC, from 160 to 176 in case of FOSMC with $\alpha = 0.99$, while in case of FOSMC with $\alpha = 0.95$, the noted increment is from 160 to 172. So from the above discussion and the presented results in Fig. 12a–12d, FOSMC controller with $\alpha = 0.95$ ensures the best transient performance while the integral SMC exhibits superior steady state performance. The experimental results obtained from HIL experiments are tabulated in Table 3.

7. PIL testing

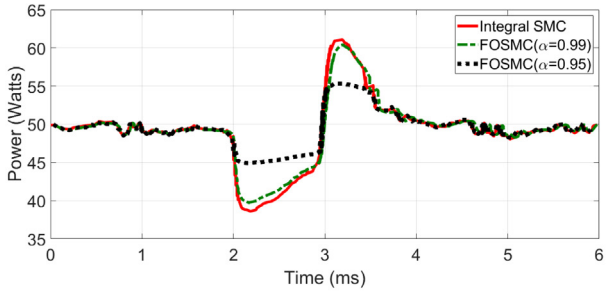
As discussed previously PIL experiment is performed to compute the time profiling of control schemes under discussion. This section presents the collected experimental results for all variants of control schemes. The PIL test results with integer and FOSMC schemes are shown in Table 4. From the presented experimental results, the recorded CPU loading is 19.02% with integral SMC and 29.28% with FOSMC controller.



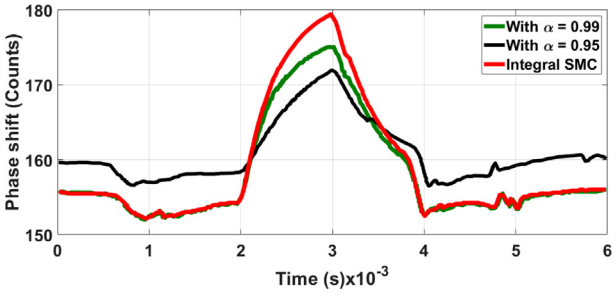
(a)Voltage tracking response comparison with all variants of controllers



(b)Enlarged view of voltage tracking



(c)Power consumed with load changes with all variants of controllers



(d)Phase shift variations comparison with all variants of controllers

Fig. 12. Voltage, power tracking and phase shift variations with applied disturbance.

8. Conclusions

In this paper two variants of robust control schemes namely integer and fractional order sliding mode controllers have been

Table 3
Performance comparison with all variants of control schemes.

Controller	Parameters	Test case 1	Test case 2	Test case 3
Integral SMC	Overshoot	1.5 V	1.2 V	2.5 V
	Undershoot	−1.5 V	−1.2 V	−2.5 V
	Settling time	0.1 ms	0.4 ms	0.9 ms
	error(t→ ∞)	Low	Low	Low
FOSMC $\alpha = 0.99$	Overshoot	0.4 V	1 V	2.5 V
	Undershoot	−0.4 V	−1 V	−2.5 V
	Settling time	0.8 ms	0.1 ms	0.9 ms
	error(t→ ∞)	Medium	Medium	Medium
FOSMC $\alpha = 0.95$	Overshoot	0.2 V	0.5 V	1.5 V
	Undershoot	−0.2 V	−0.5 V	−1.5 V
	Settling time	0.2 ms	0.1 ms	0.9 ms
	error(t→ ∞)	High	High	High

Table 4
Computational efficiency and time profiling of controllers.

Controller	Maximum execution time (ns)	Average execution time (ns)	Maximum CPU utilization (%)
SMC			
SMC initialize	3100	3100	19.02
SMC step($5e^{-5}$)	9510	9406	19.02
SMC terminate	520	520	19.02
FOSMC			
FOSMC initialize	3200	3200	29.28
FOSMC step($5e^{-5}$)	14640	14563	29.28
FOSMC terminate	500	500	29.28

analyzed for a DAB converter integrated energy storage system. Both variants of control schemes have been tested under source, load and reference command variations in the HIL and PIL experiments using rapid prototyping technique. The experimental data related to the two performance indices namely robustness and computational resources utilization is collected. System exhibits an overshoot/undershoot of 2.4/−2.4 V with integral sliding mode control, 1.5/−1.5 V with fractional order SMC (α = 0.95) and 2.3/−2.3 V with fractional order SMC (α = 0.99) respectively under variable load condition. For the other two test cases, same conclusion is true. With both variants of fractional order controllers, steady state error is large as compared to integral SMC. From the PIL test, maximum CPU utilization of 19.02% is recorded with integral SMC and 29.28% with both variants of fractional order SMC controller respectively. Keeping in view the performance indices and the CPU utilization data from the experiments, integral SMC is found to be the most suitable control scheme for the proposed system. Apart from the DAB converter system, the proposed method is applicable in several other areas such as aerospace, biomedical engineering and Mechatronic systems.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

The authors acknowledge the funding of Researchers Supporting Project number (TURSP-2020/144), Taif University, Taif, Saudi Arabia.

Funding

This research was supported by Taif University Researchers Supporting Project number (TURSP-2020/144), Taif University, Taif, Saudi Arabia.

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