A New Adaptive Instantaneous Average Current Sharing Technique for Circulating Current Minimization among Parallel Converters in a LV DC-Microgrid

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Abstract

This paper proposes a new adaptive instantaneous average current sharing technique for load current sharing and minimizing circulating current among parallel-connected converters in a LV islanded DC microgrid. This control technique is common for load current sharing among parallel inverters in AC systems, however, its use in DC networks has not been reported in the open literature. Unfortunately, the conventional controller does not come up with the expected improvements in terms of regulating the load voltage and minimizing circulating current among parallel DC-DC converters. Therefore, adaptive instantaneous average current sharing technique, based on the steepest descent method, is proposed to achieve this goal. A mathematical model is derived for n-parallel converters with the proposed controller. In addition, stability analysis of closed-loop controllers is carried out by studying locations of poles using the root locus plot. The analysis and simulation of the proposed system demonstrate that the proposed controller shows better performance for regulating the load voltage and achieving very low circulating current level. Matlab/Simulink model is implemented to verify the proposed controller performance under different operating conditions.

Keywords: Boost converter; circulating current; DC microgrid; adaptive control; load sharing, parallel converters, steepest descent method, voltage deviation

Nomenclature

V_{i1}	Converter-1 input voltage
V_{i2}	Converter-2 input voltage
V_{conv-1}	Converter-1 output voltage
V_{conv-2}	Converter-2 output voltage
i_1	Converter-1 output current
i_2	Converter-2 output current
R_1	Converter-1 line impedance
R_2	Converter-2 line impedance
I_{c12}	Circulating current passing from converter-1 to converter-2
R_{load}	Load resistance

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$V_{conv\text{-}i}$	Output voltage of converter *I* where *I* equals 1 to *n*
v_{load}	Load Volatge
v_{avg}	Average output voltage of all parallel connected converters
$V_{nominal}$	Nominal load voltage
$V_{ref\text{-}i}$	Reference voltage after adaptation
K_c	Gain of the inner capacitor current feedback loop
K	Outer current loop gain
I_{ci}	Capacitor current for I^{th} converter
$f(k)$	Cost function of the steepest descent algorithm
λ	Adaptive gain which controls convergence speed of *f(k)*
i_{li}	Inductor current of i^{th} boost converter
v_{ci}	Capacitor voltage of i^{th} boost converter
V_{ii}	Converter input voltage of i^{th} boost converter
T_s	Boost converter switching period
D	Boost converter duty cycle
C	Boost converter capacitor
L	Boost converter inductance
K_f	Gain of the voltage feedforward loop
G_c	Transfer function of the voltage loop PI-controller
k_{pv}	Proportional gain of the voltage PI-controller
k_{iv}	Integral gain of the voltage PI-controller
Z_p	Line impedance
Z_{load}	Load impedance
i_{dis}	Disturbance current
k_{pc}	Current controller proportional gain
k_{pc}	Current controller integral gain

1. Introduction

There are different types of microgrids: AC microgrid, DC microgrid or both together called a hybrid microgrid. AC microgrids are in service years ago and so its components and operation are well understood. It has a simpler voltage transformation and its AC circuit breaker protection is more mature technology [1]. The hybrid microgrid embraces the advantages of both AC and DC microgids, however, they require more complicated controllers [2]. LV DC microgrid as a promising candidate having clear advantages over AC microgrids such as lower power distribution loss and it requires simpler control system [3, 4]. It is easier to connect DC microgrids in parallel to increase power supply reliability. In DC systems, wires can handle more power. In addition, integrating energy storage with distributed generation such as Photovoltaic (PV) solar farm in a DC system results in greater end-use energy efficiency and reliability [5]. The study demonstrated that 350 VDC installation is more efficient than 230 VAC installation with 33% less use of the copper [5].

Having said that, LV DC mirogrids still have practical obstacles to replace the AC microgrids. For example DC microgrids have protection concerns as there is no natural zero crossing of the current. DC system requires new standard for voltage levels and products. DC microgrid includes many power electronic converters and this results in a complex system which may lead to power quality issues. Also, reliable communication infrastructure is required for connecting various DC microgrids [1, 6].

Connecting power converters in parallel has increasing interest for the reasons of increasing the output power capacity and system reliability, system modularity, facilitating system maintenance and reducing system design costs. Also, parallel converters can be applied for systems which require high current levels at a low voltage within a microgrid [7]. However, elimination of the circulating current arise among the parallel converters is a challenge. This current is due to an unequal output voltage of connected converters [8, 9]. Unless controlled, it can lead to higher losses and overloading of energy source, thereby causing source failure and system instability. For this reason, voltage

regulation and load power-sharing among energy resources based on their power ratings is a key research topic [7].

Many control schemes are proposed in the literature to solve this problem. These control techniques can be classified to passive load-sharing techniques such as droop control [9-23] and active load sharing techniques such as master-slave [24, 25], circular chain current programming[26], average current programming [27] and central limit control technique [28, 29]. Lastly, hybrid passive/active load sharing techniques which have the advantages of both control techniques [30].

The advantages of active load sharing techniques guarantee accurate power-sharing and good dynamic performance. However, due to their high dependency on high-speed communications, the system redundancy and expandability is reduced, the system costs are increased and system stability is not guaranteed [11]. For example, studies [24] and [31] proposed a master-slave control based on two layers controller to coordinate the operation of multiple wind turbines in isolated DC microgrid with no storage. Although the results show that the controller is successfully achieved power balance, controller dependency on communications and upper layer for providing power references to lower layer controllers degrades the system reliability in case of the failure of the upper layer.

On the other hand, as a communicationless technique, droop controller assures system stability and reliability. However, it has several drawbacks such as inaccurate load power-sharing and poor DC bus voltage regulation [9, 10]. For example, the study [12] proposed proportional droop index algorithm with droop shifting for improving the load voltage deviation and load sharing in a DC-microgrid. The controller successfully achieved proportional power-sharing among the converters, however, the study does not take into account the impact of the circulating current among the parallel converters. Also, the load voltage is not accurately regulated as it is varying with the input voltage and load current variations.

In this paper, Instantaneous Average Current Sharing (IACS) techniques is presented. Studies [27, 32-35] used IACS in order to achieve proper voltage regulation and load sharing among parallel inverters in AC-systems. IACS is never been used for controlling parallel converters in DC-systems. Applying the conventional IACS to parallel DC-DC converters shows good power-sharing and zero circulating current with equal line impedances. However, with different line impedance, there is a high circulating current depends on the difference between line impedances. This is due to a steady-state error between the reference voltage and the output voltage of converters. To eliminate this error, this paper proposed an adaptive reference voltage technique with zero-steady state error based on the Steepest Descent Method (SDM) to ensure the same output voltage of parallel converters. The contribution of this paper is

- Investigation of using IACS with DC system is provided.
- Modelling of a single boost converter and n-parallel connected converters with IACS is presented with stability analysis provided for both.
- Adaptive reference voltage using SDM is proposed to improve the performance of the IACS with stability analysis is held for this part.
- Matlab/Simulink based comparison study is held to show the advantages and performance of the proposed technique against the droop control technique of another study in literature.

2. System configuration

Fig. 1 shows two parallel DC-DC converters connected as interfaces between renewable energy sources (RES) and DC grid. The RES examined in this paper is solar photo-voltaic (PV) array. Considering the islanded mode of the DC microgrid, the PV generation could work in different operation modes such as Maximum Power Point Tracking (MPPT), droop mode and non-working mode [36]. The symbols V_{i1} and V_{i2} are the input voltage from the PV array. $V_{conv\text{-}1}$, $v_{conv\text{-}2}$, i_1, i_2, R_1 and R_2 refer to output voltages, output currents and line impedances of converter 1 and converter 2, respectively. While I_{c12} r epresent the circulating current passing from converter 1 to converter 2 and R_{load} is the load resistance.

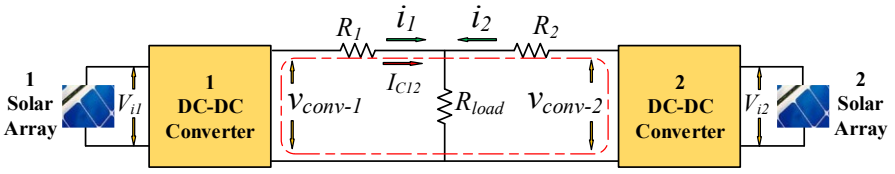

Fig. 1. Two parallel DC-DC converters connected between RES and DC-grid.

The circulating current between two parallel converters equals

$$I_{C12} = -I_{C21} = \frac{v_{conv-1} - v_{conv-2}}{R_1 + R_2} \tag{1}$$

3. The proposed controller scheme

Fig. 2 shows the conventional IACS associated with the parallel DC-DC converters. IACS includes four control loops (three feedback loops and one feedforward loop). The three feedback control loops are: voltage feedback loop for converter output voltage regulation, outer current sharing loop for proper current sharing among parallel-connected converters [27], and inner current feedback loop provide a fast dynamic response for the system during steady-state and transient. Lastly, the feedforward loop included for high tracking accuracy of the reference voltage [27]. To reduce the controller sensitivity for parameter variations, capacitor current is selected as a controlled variable. Two Proportional Integral (PI) controllers are used for current sharing and voltage regulation control loops.

The left part of Fig. 2 shows the proposed IACS with the adaptive reference voltage. $V_{conv\text{-}i}$ refers to the output voltages of parallel-connected converters where i equals 1 to n. v_{load} and v_{avg} are the load and average voltage, respectively. $V_{nominal}$ is the nominal load voltage. $V_{ref\text{-}i}$ is the reference voltage after adaptation. K_c and K refer to the gain of the inner capacitor current feedback loop and outer current loop gain, respectively. I_{ci} is the capacitor current for I converter.

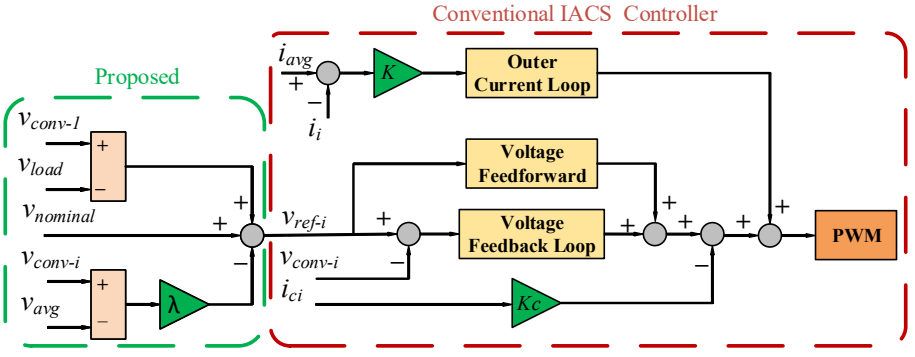

Fig. 2. Proposed and conventional IACS controller

Referring to (1), the magnitude of the circulating current depends on the difference between the output voltages of parallel converters $v_{conv\text{-}1}$ and $v_{conv\text{-}2}$. The converters output voltages could be varied due to line impedance mismatch or system parameters deviation. So, for circulating current minimization, it is required to control the converters output voltages to ensure they are equal even when there is line impedance mismatch or system parameter deviations as mentioned above. The proposed adaptive controller in Fig. 2 is doing this job. The reference voltage $V_{ref\text{-}i}$ of the

conventional IACS controller is not a fixed value and it is varying in order to ensure the converter output voltage is equal to the average voltage as shown in Fig. 2.

3.1. Steepest descent method

SDM is an iterative method which uses the gradient of the objective function to find a search direction through design space [37]. In this paper, SDM is used to adapt the reference voltage for individual converter such that the output voltage of all parallel-connected converters is the same. The idea of SDM is to select a search direction (by taking the gradient of the cost function) and then finds the minimum value of cost function based on that direction. Then, the process is repeated by selecting a new search direction and so forth until stop criteria has been satisfied. The error equation is given in (2) as this is the steady-state error to be eliminated.

$$e(k) = v_{conv-i}(k) - v_{avg}(k) \tag{2}$$

where $v_{conv-i}(k)$ is the output voltage of converter *i* and $v_{avg}(k)$ is the average output voltages of parallel-connected converters at instant *k*.
The adaptive steepest descent algorithm is

$$v_{ref-i}(k) = v_{ref}(k-1) - \lambda \nabla f(k) \tag{3}$$

where $f(k)$, $\nabla f(k)$ are the cost function and the gradient of the cost function with respect to the converter output voltage. The negative gradient in (3) refers to the direction of steepest descent (minimum value). λ is a positive adaptive gain which controls convergence speed of *f(k).* The quadratic cost function equals to

$$f(k) = \frac{1}{2} e^2(k) \tag{4}$$

by taking the gradient of *f(k)* in (4)

$$\nabla f(k) = \frac{\partial f(k)}{\partial v_{conv-i}(k)} = \frac{1}{2} \frac{\partial \left(v_{conv-i}(k) - v_{avg}(k) \right)^2}{\partial v_{conv-i}(k)} = e(k) \tag{5}$$

Replacing the value of $\nabla f(k)$ in (3) with (5), the adaptive steepest descent algorithm will be

$$v_{ref-i}(k) = v_{ref}(k-1) - \lambda e(k) \tag{6}$$

replacing $e(k)$ in (6) by (2), gives

$$v_{ref-i}(k) = v_{ref}(k-1) - \lambda \left(v_{conv-i}(k) - v_{avg}(k) \right) \tag{7}$$

where $v_{ref}(k-1)$ is the nominal voltage of the grid.

Although the algorithm in (7) gives excellent results regarding the circulating current minimization, however, there is load voltage deviation from the nominal voltage. To eliminate this deviation, the difference between the converter output voltage and load voltage is added to the algorithm in (7). Then, the adaptive steepest descent algorithm in the final form is

$$v_{ref-i}(k) = v_{ref}(k-1) - \lambda\left(v_{conv-i}(k) - v_{avg}(k)\right) + \left(v_{conv-i} - v_{load}(k)\right) \tag{8}$$

Referring to (6), the adaptive gain λ should be selected to achieve fast convergence while maintaining the system stable as there is tradeoff between them. The Lyapunov's direct method is used for analyzing the system stability with changing the adaptive gain. According to Lyapunov's stability theorem, a system is globally asymptotically stable if the Lyapunov function $V(k)$ satisfies the following conditions: $V(k) > 0$ and $\Delta V(k) < 0$. Thus, Lyapunov function must be always positive at any instant while change in this function must be negative to insure system stability. The proposed Lyapunov function is the quadratic of the error function which satisfies the first Lyapunov criteria

$$V(k) = e_i^2(k) \tag{9}$$

Change in Lyapunov function equals

$$\begin{gathered}\Delta V(k) = V(k+1) - V(k) \\ \Delta V(k) = e_i^2(k+1) - e_i^2(k) \\ \Delta V(k) = \Delta e_i^2(k) + 2\Delta e_i(k) e_i(k)\end{gathered} \tag{10}$$

Where $\Delta \mathrm{e}_i(\mathrm{k}) = \mathrm{e}_i(k+1) - \mathrm{e}_i(k)$ and using (2)

$$\begin{aligned}\Delta \mathrm{e}_i(\mathrm{k}) &= \left(v_{conv-i}(k+1) - v_{avg}(k+1)\right) - \left(v_{conv-i}(k) - v_{avg}(k)\right) \\ &= v_{conv-i}(k+1) - \frac{1}{n}\sum_{j=1}^{n} v_{conv-j}(k+1) - v_{conv-i}(k) + \frac{1}{n}\sum_{j=1}^{n} v_{conv-j}(k)\end{aligned} \tag{11}$$

where $v_{avg} = (\sum_{j=1}^{n} v_{conv-j})/n$
The discrete average model of a boost converter is

$$\begin{bmatrix} i_{li}(k+1) \\ v_{ci}(k+1) \end{bmatrix} = \begin{bmatrix} 1 & -\dfrac{(1-D)T_s}{L} \\ \dfrac{(1-D)T_s}{C} & 1 - \dfrac{T_s}{R_{load}C} \end{bmatrix} \begin{bmatrix} i_{li}(k) \\ v_{ci}(k) \end{bmatrix} + \begin{bmatrix} \dfrac{T_s}{L} \\ 0 \end{bmatrix} [V_{ii}] \tag{12}$$

Where i_{li} is the inductor current and it is assumed to equal the converter output current. v_{ci} is the capacitor voltage which equals the converter output voltage v_{conv-i}. T_s, D, C and V_{ii} are the switching time, duty period, capacitor capacitance and converter input voltage, respectively.
By replacing the value of v_{conv-i} from (12) into (11), one can get

$$\begin{aligned}\Delta \mathrm{e}_i(\mathrm{k}) = {} & \frac{(1-D)T_s}{C} i_{li}(k) + \left(1 - \frac{T_s}{R_{load}C}\right) v_{ci}(k) - v_{ci}(k) \\ & - \frac{1}{n}\sum_{j=1}^{n}\left(\frac{(1-D)T_s}{C} i_{li}(k) + \left(1 - \frac{T_s}{R_{load}C}\right) v_{ci}(k)\right) + \frac{1}{n}\sum_{j=1}^{n} v_{conv-j}(k)\end{aligned} \tag{13}$$

Assume same line impedance. i.e. $i_{i1} = i_{i2} = \cdots = i_{in} = \frac{v_{ci}}{2R_{load}}$ [9]

$$\begin{gathered}\Delta \mathrm{e}_i(\mathrm{k}) = \frac{(1-D)T_s}{C}\frac{v_{ci}(k)}{2R_{load}} + \left(1 - \frac{T_s}{R_{load}C}\right) v_{ci}(k) - v_{ci}(k) \\ -\frac{1}{n}\sum_{j=1}^{n}\left(\frac{(1-D)T_s}{C}\frac{v_{cj}(k)}{2R_{load}} + \left(1 - \frac{T_s}{R_{load}C}\right) v_{cj}(k)\right) + \frac{1}{n}\sum_{j=1}^{n} v_{conv-j}(k) = -\left(\frac{T_s(1+D)}{2R_{load}C}\right) e_i(k)\end{gathered} \tag{14}$$

By inserting (14) into (10), the change in Lyapunov function will be

$$\begin{aligned}\Delta V(k) &= \left[-\left(\frac{T_s(1+D)}{2R_{load}C}\right)e_i(k)\right]^2 + 2\left[-\left(\frac{T_s(1+D)}{2R_{load}C}\right)e_i(k)\right]e_i(k) \\ &= {e_i}^2(k)\left(\frac{T_s(1+D)}{2R_{load}C}\right)\left[\left(\frac{T_s(1+D)}{2R_{load}C}\right)-2\right]\end{aligned} \tag{15}$$

As per Lyapunov's second criteria above, $\Delta V(k)$ must be negative to ensure system stability. Using (15), it is clear that the first two terms are positive definite. Furthermore, change in Lyapunov becomes negative definite if

$$\lambda\left(\frac{T_s(1+D)}{2R_{load}C}\right) < 2 \quad i.e. \quad \lambda < \frac{4R_{load}C}{T_s(1+D)} \tag{16}$$

Choice of λ will be decided based on the load voltage quality after deriving the system model later on the next sections.

4. System model with IACS

The switching converter is a nonlinear system, so a small-signal ac model is required for stability analysis purposes [38]. Consider a single boost converter, it is has a line-to-output transfer function $G_{vd}(s)$ and the control-to-output transfer function $G_{vg}(s)$ as per (18) and (19), respectively [39]

$$G_{vd}(s) = G_{d0}\frac{\left(1-\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right)} \tag{17}$$

$$G_{vg}(s) = G_{g0}\frac{1}{\left(1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2\right)} \tag{18}$$

Where $G_{d0} = \frac{V}{(1-D)}$, $\omega_z = \frac{(1-D)^2R_{load}}{L}$, $\omega_0 = \frac{(1-D)}{\sqrt{LC}}$, $G_{g0} = \frac{1}{(1-D)}$ and $Q = (1-D)R_{load}\sqrt{C/L}$. L is the converter inductance. While V and D are the steady-state converter output voltage and duty cycle, respectively.
To get the output impedance of the boost converter, put $d(s)$ and $v_g(s)$ equals to zero in the canonical form of [39], the converter output impedance will be the equivalent of parallel impedances of R_{load}, sL_e and $\frac{1}{sC}$ which equals

$$Z_{out} = \frac{sL_e}{s^2CL_e + s\left(\frac{L_e}{R_{load}}\right)+1} \tag{19}$$

From (17), (18) and (19), the converter output voltage variation can be expressed as a linear combination of the independent inputs as follow:

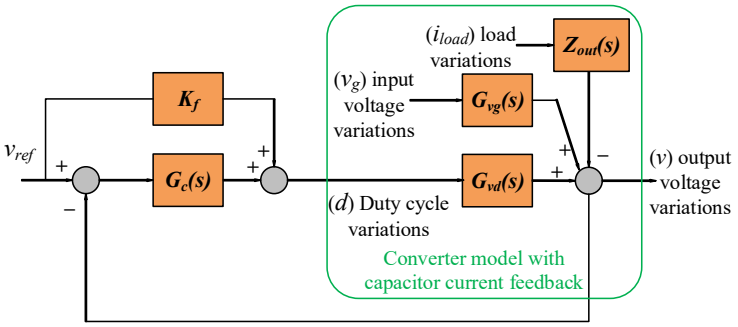

Fig. 3. Boost converter model with IACS controller

$$v(s) = G_{vd}(s)d(s) + G_{vg}(s)v_g(s) - Z_{out}(s)i_{load}(s) \tag{20}$$

Equation (20) represents the small signal linearized model for a single boost converter.
Boost converter model with IACS scheme can be modelled as per Fig. 3. K_f refers to the gain of the voltage feedforward loop. v_g is the variations in the converter input voltage and i_{load} is the output load current variations. v_{ref} is the adaptive reference voltage of parallel converters. G_c is the transfer function of the voltage PI-controller. G_c equals $k_{pv} + \frac{k_{iv}}{s}$ where k_{pv} and k_{iv} are the proportional and integral gains of the of this controller, respectively. From Fig. 3, output voltage variation of a single converter is derived as follow

$$v = \frac{G_{vd}\left[G_c + K_f\right]}{1 + G_{vd}G_C}v_{ref} + \frac{G_{vg}}{1 + G_{vd}G_C}v_g - \frac{Z_{out-i}}{1 + G_{vd}G_C}i_{load} \tag{21}$$

Equation (21) can be simplified to (22) for converter i^{th}

$$v = G_i v_{ref-i} + P_i v_{g-i} - Z_{CL-i}i_{load-i} \tag{22}$$

where G_i , P_i and Z_{CL-i} are the closed-loop transfer functions of control-to-output, line-to-output and output impedance, respectively.
To derive a model for parallel-connected converters, Thevenin theorem is used to obtain the equivalent circuit for a closed-loop converter with IACS in Fig. 3 [35]. The closed-loop converter of Fig. 3 can be represented by an equivalent circuit as a controlled voltage source Gv_{ref} in series with the converter closed-loop output impedance Z_{CL}. For the purpose of this paper which study the impact of line impedance on the circulating current among parallel converters, the variations of the input voltage will be assumed zero considering these converters are supplied from high capacitance DC-link. Also, it is assumed that all parallel converters are identical, i.e. it is assumed that

$$\begin{gathered} Z_{CL1} = Z_{CL2} = Z_{CLn} = Z_{CL} \\ Z_{p1} = Z_{p2} = Z_{pn} = Z_p \\ H_1 = H_2 = H_n = H \\ G_1 = G_2 = G_n = G \end{gathered} \tag{23}$$

Where Z_p is the line impedance. H is the current sharing PI-controller. However, practically, there is no identical converter as electrical components have always tolerances. These parameter deviations make the output current from individual converters different and mismatched line impedances do the same. For simplicity, the impact of parameter deviation and line impedance are combined together as a disturbance at the converter output current. As a result, line impedance will be the same for all converters as its impact is already considered in the disturbance current i_{dis}.
First, a model for n-converters is derived without considering the adaptive section for simplicity. Based on (23), a model for n-converters can be implemented as per Fig. 4. This model can be described by a set of equations as follow

$$(i_1 + i_2 + \ldots + i_n)Z_L = Z_L \sum_{j=1}^{n} i_j = v \tag{24}$$

$$\begin{aligned} G\{v_{ref-1} + (i_{avg} - i_1)H\} - v &= (i_1 - i_{dis-1})Z_e \\ G\{v_{ref-2} + (i_{avg} - i_2)H\} - v &= (i_2 - i_{dis-2})Z_e \\ &\vdots \\ G\{v_{ref-n} + (i_{avg} - i_n)H\} - v &= (i_n - i_{dis-n})Z_e \end{aligned} \tag{25}$$

where $Z_e = Z_{CL} + Z_P$, and i_{avg} is the average current of n-parallel converters.

$$i_{avg} = \frac{(i_1 + i_2 + i_n)}{n} = \frac{\sum_{j=1}^{n} i_j}{n} \tag{26}$$

by adding the group of equations of (25) together, one can get

$$G\sum_{j=1}^{n} v_{ref-j} + GH\left(ni_{avg} - \sum_{j=1}^{n} i_j\right) - nv = \left(\sum_{j=1}^{n} i_j - \sum_{j=1}^{n} i_{dis-j}\right)Z_e \tag{27}$$

by inserting i_{avg} from (26) and $\sum_{j=1}^{n} i_j$ from (24) into (27), the voltage regulation characteristic is obtained

$$v = \frac{G/n}{1 + \frac{Z_e}{nZ_L}} \sum_{j=1}^{n} v_{ref-j} + \frac{Z_e/n}{1 + \frac{Z_e}{nZ_L}} \sum_{j=1}^{n} i_{dis-j} \tag{28}$$

referring to (25), converter output current for k^{th} converter is obtained as follow

$$G\{v_{ref-k} + (i_{avg} - i_k)H\} - v = (i_k - i_{dis-k})Z_e \tag{29}$$

from (24) and (26), i_{avg} can be represented as

$$i_{avg} = \frac{v}{nZ_L} \tag{30}$$

by inserting v and i_{avg} from (28) and (30), respectively, into (29), current sharing characteristic is obtained

$$i_k = \frac{n_1}{d_1} v_{ref-k} + \frac{n_2}{d_2} \sum_{j=1}^{n} v_{ref-j} + \left(\frac{1}{n}\right)\frac{n_3}{d_2} \sum_{j=1}^{n} i_{dis-j} + \frac{1}{d_1} i_{dis-k} \tag{31}$$

where $n_1 = G/Z_e$, $n_2 = \left(\frac{G}{nZ_e}\right)\left(\frac{GH}{nZ_L} - 1\right)$, $n_3 = \left(\frac{GH}{nZ_L} - 1\right)$, $d_1 = \left(1 + \frac{GH}{Z_e}\right)$ and $d_2 = \left(1 + \frac{GH}{Z_e}\right)\left(1 + \frac{Z_e}{nZ_L}\right)$. It is important to confirm that voltage and current characteristic equations in (28) and (31) are derived without considering the adaptive reference voltage for simplicity.

The next section shows those equations with considering the adaptive part of the controller. Recall (8) which is

$$v_{ref-j} = v_{ref-nom} - \lambda\left(v_{conv-j} - v_{avg}\right) + \left(v_{conv-j} - v_{load}\right) \tag{32}$$

from Fig. 4, converter k^{th} output voltage is

$$v_{conv-k}(s) = v_{load}(s) + (i_k - i_{dis-k})Z_p \tag{33}$$

Replace $v_{conv-k}(s)$ in (32) with (33) and rearrange

$$v_{ref-k}(s) = v_{ref-nom}(s) - \lambda v_{load}(s) + (1 - \lambda)(i_k - i_{dis-k})Z_p + \lambda v_{avg}(s) \tag{34}$$

Consider n-parallel connected converters, then n of (34) will be added together to give (35)

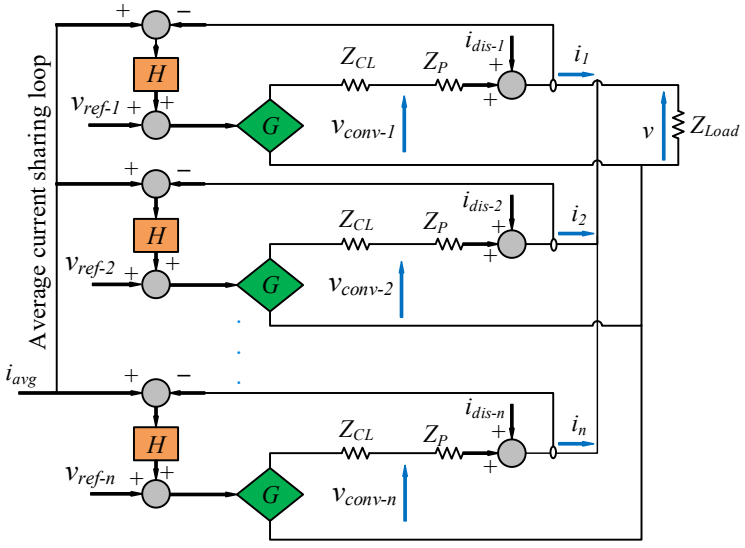

Fig. 4. *N*-parallel converter with IACS model

$$\sum_{j=1}^{n} v_{ref-j}(s) = nv_{ref-nom}(s) - n\lambda v_{load}(s) + (1 - \lambda)\left[\sum_{j=1}^{n} i_j - \sum_{j=1}^{n} i_{dis-j}\right]Z_p + n\lambda v_{avg}(s) \tag{35}$$

where $v_{avg}(s)$ equals

$$v_{avg}(s) = \frac{v_{c1} + v_{c2} + \cdots + v_{cn}}{n} = \frac{\sum_{j=1}^{n} v_{cj}}{n} \tag{36}$$

replace v_{cj} in (36) with (33), one can get

$$v_{avg} = v_{load} + \frac{1}{n}\sum_{j=1}^{n}(i_j - i_{dis-j})Z_p \tag{37}$$

replace v_{avg} in (35) by (37) yields

$$\sum_{j=1}^{n} v_{ref-j}(s) = nv_{ref-nom}(s) + rZ_p \sum_{j=1}^{n} i_j - rZ_p \sum_{j=1}^{n} i_{dis-j} \tag{38}$$

where $r = Z_p(1 - \lambda + n)$.
recall (24) $Z_L \sum_{j=1}^{n} i_j = v$, i.e. $\sum_{j=1}^{n} i_j = \frac{v}{Z_L}$. Insert this current into (38) gives

$$\sum_{j=1}^{n} v_{ref-j}(s) = nv_{ref-nom}(s) + rZ_p \left(\frac{v}{Z_L}\right) - rZ_p \sum_{j=1}^{n} i_{dis-j} \tag{39}$$

by inserting the value of $\sum_{j=1}^{n} v_{ref-j}(s)$ from (39) into (28), the voltage characteristic equation for the proposed controller will be

$$v = \frac{G}{1 + \frac{Z_e}{nZ_L} - \frac{Z_p}{Z_L}\left(\frac{G}{n}\right)r} v_{ref-nom} + \frac{\left(\frac{1}{n}\right)\left[Z_e - GZ_p r\right]}{1 + \frac{Z_e}{nZ_L} - \frac{Z_p}{Z_L}\left(\frac{G}{n}\right)r} \sum_{j=1}^{n} i_{dis-j} \tag{40}$$

The output voltage equals

$$v = \frac{G}{q_1} v_{ref-nom} + \left(\frac{1}{n}\right)\frac{p_1}{q_1} \sum_{j=1}^{n} i_{dis-j} \tag{41}$$

where $p_1 = (Z_e - Gr), q_1 = 1 + \frac{p_1}{nZ_L}$.
again, by inserting v from (41) and i_{avg} from (30) into (29), current sharing characteristic of k^{th} converter is obtained

$$i_{k-adp} = \frac{n_1}{d_1} v_{ref-k} + \frac{nn_2}{d_1 q_1} v_{ref-nom} + \left(\frac{1}{n}\right)\frac{n_3 w}{d_1 q_1} \sum_{j=1}^{n} i_{dis-j} + \frac{1}{d_1} i_{dis-k} \tag{42}$$

where $w = (1 - Gr/Z_e)$

5. Stability analysis

System stability analysis is achieved at different stages. Firstly, study the stability of the single converter with IACS as a unit base of the parallel system while the current sharing loop is open. Secondly, stability analysis of parallel converters with conventional IACS. Lastly, study the stability of parallel converters with adaptive IACS. shows parameter list for boost converter and system considered under this study. Matlab/ M-files are implemented for plotting the root loci for studying system stability at different stages as described. For the purpose of stability analysis, the boost converter duty cycle is fixed to 0.76.

For stability analysis of single boost converter with IACS, stability depends on the location of the roots of the denominators of (21). If there is any of the roots have positive real parts, the system will be unstable.

Table 1. Boost converter and system parameters list.

Description	Value
Boost converter parameters	
Input boost inductor ($\boldsymbol{L}$)	750 µH
Output boost capacitor ($\boldsymbol{C}$)	2220 µF
Feedforward gain($\boldsymbol{K_f}$)	1
Capacitor current gain ($\boldsymbol{K_C}$)	8
Load impedance($\boldsymbol{Z_L}$)	25 Ω
Number of converters ($\boldsymbol{n}$)	2
System parameters	
DC load voltage (v)	100 V
Input DC voltage (v_g)	24 V
Voltage controller proportional gain ($\boldsymbol{k_{pv}}$)	23
Voltage controller integral gain ($\boldsymbol{k_{iv}}$)	50
Current controller proportional gain ($\boldsymbol{k_{pc}}$)	.2
Current controller integral gain ($\boldsymbol{k_{pc}}$)	5
Switching frequency ($\boldsymbol{f_s}$)	10 kHz

By inserting the parameters in Table 1 into the closed-loop transfer functions of (21), one can get the root loci of closed-loop poles as per Fig. 5 which implies that closed-loop converter system with IACS is stable as all poles are on the left half-plane.

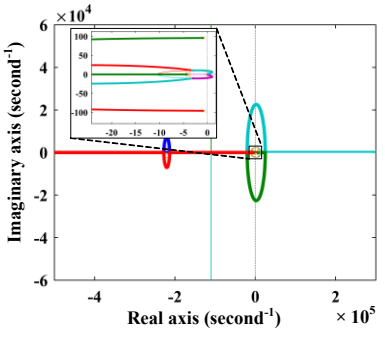

Fig. 5. Root locus plot of (13).

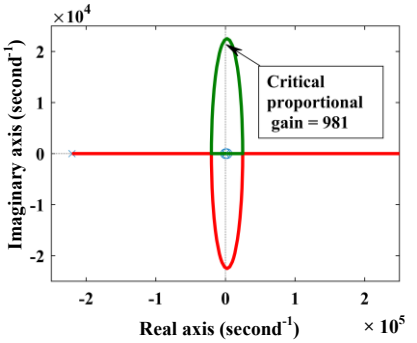

Fig. 6. Root locus of $G_{vd}G_C$.

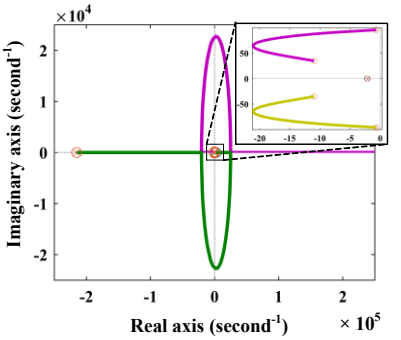

Fig. 7. Root locus of (28) at k_{pv}=23.

However, increasing the proportional gain of the controller threatens the system stability and k_{pv} should not exceed the critical value of 981 to guarantee a stable system as per the root locus plot of the open-loop transfer function ($G_{vd}G_C$) in Fig. 6. Now, studying the stability of the load voltage under n-parallel converters connected based on (28). Equation (28) shows the relationship among the load voltage, the reference voltages and the disturbance source. Referring to (28), it can be noted that the current sharing controller H has no impact on the load voltage since (28) is free of H. To ensure load voltage stability, all closed-loop poles of the two transfer functions of (28) must be on the left half-plane. The root locus plots for these transfer functions shown in Fig. 7 which illustrates that all poles are in the left half-plane.

It should be noted that applying proportional gain k_{pv} above the critical value ($k_{pv} = 981$) leads to an unstable load voltage. Also, by comparing (22) and (28), one can note that both equations depend on G and Z_e. In other words, stability of the load voltage for the parallel converters depends on the voltage regulation capability of the individual converters.

Stability of the current control loop of k^{th} converter depends on the denominator of (31) which has two terms $(1 + Z_e/nZ_L) = 0$ and $(1 + GH/Z_e) = 0$. The first term is similar to the denominator of (28) which studied in the previous section. The second term depends on the current controller H. To ensure output current stability, it is required to determine the critical value of the gain of H, where H is the transfer function for a PI controller (43).

$$H = k_{pc} + \frac{k_{ic}}{s} \tag{43}$$

Insert (43) into $(1 + GH/Z_e)$ and rearrange the equation to factor k_{pc} and k_{ic}, one can get

$$1 + \frac{k_{pc}G}{Z_e} = 0 \qquad and \qquad 1 + \frac{k_{ic}G}{Z_e s} = 0 \tag{44}$$

From (44), using root locus to plot G/Z_e as an open loop while the current sharing loop is open which gives the critical proportional gain of the current controller. It is found that this critical value of proportional gain equals $k_{pc-critical} = 98.2$ at $k_{pv} = 1$, and $k_{iv} = 1$ as per Fig. 8.

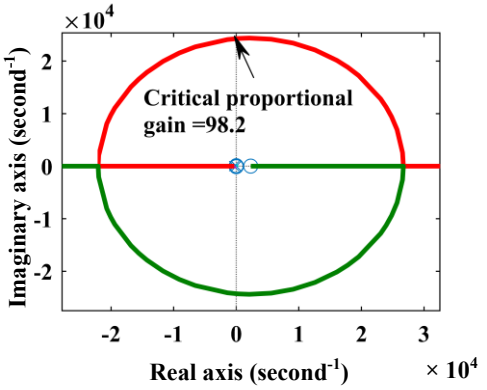

Fig. 8. Current controller critical gain estimation based on (44) at ($k_{pv} = 1$ and $k_{iv} = 1$).

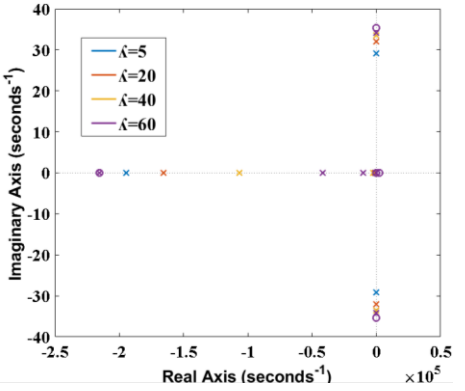

Fig. 9. Zero-pole map of the closed-loop transfer function of voltage equation (41) at various λ.

The choice of the adaptive gain is achieved based on the load voltage quality as increasing λ leads to a higher voltage overshoot and a higher voltage ripple. Referring to (16), the adaptive gain must be less than 630 to ensure global stability. Fig. 9 shows the zero-pole map for the closed-loop transfer function of (40) at ($\lambda = 5, 20, 40$ and 60). The figure shows that the load voltage is stable at these values of λ. However, increasing λ to 60 leads to higher overshoot and undershoot with load step change. Moreover, higher voltage ripple appears especially at light load as Fig. 10 shows from 2 to 4 s.

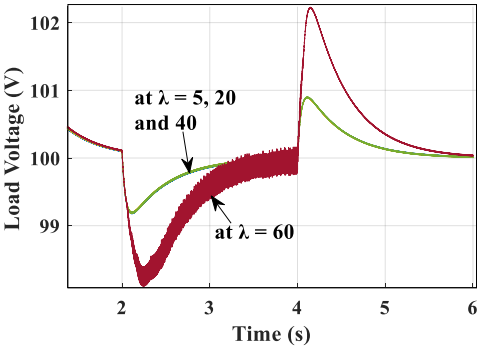

Fig. 10. Load voltage at the adaptive gain (λ = 5, 20, 40 and 60).

6. Simulation setup

Matlab/Simulink is used to investigate the performance of both conventional and proposed adaptive IACS for minimizing the circulating current among parallel-connected converters when line impedances among converters are varying.

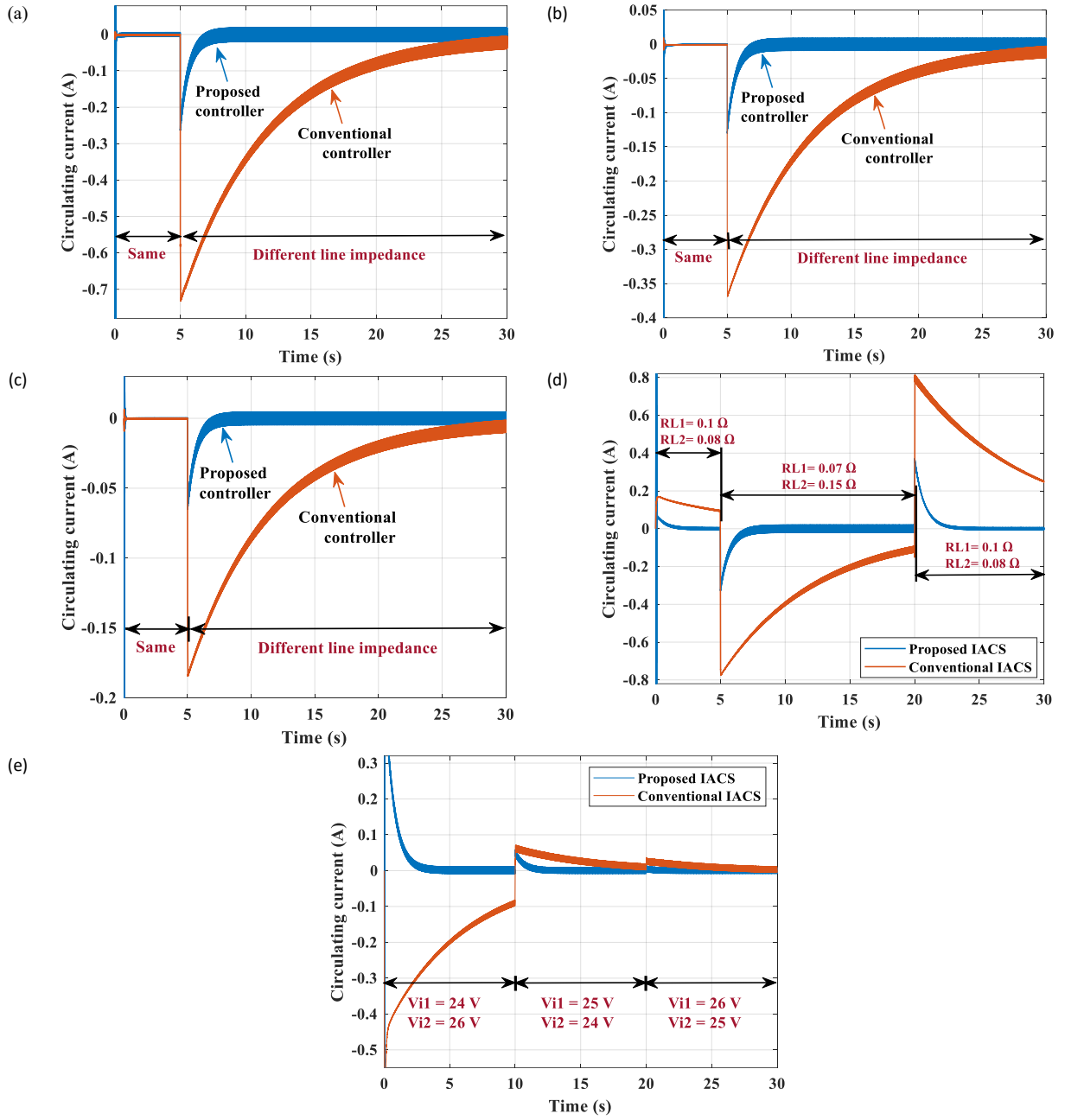

Fig. 11. Matlab/Simulink simulation results of circulating current for the conventional and proposed IACS at (a) $R_{load} = 12.5\ \Omega$, (b) $R_{load} = 25\ \Omega$, (c) $R_{load} = 50\ \Omega$, (d) line impedance variation at $R_{load} = 25\ \Omega$ and (e) converters input voltages variation at $R_{load} = 25\ \Omega$.

Simulation circuit is built based on 2-parallel converters as per Fig. 1 with system parameters as per Table 1. This simualtion section can be divided into two parts: Part 1 compares the performance of the conventional and proposed

controller at different operating conditions with focus on the circualting current in each case. Part 2 compares the simulation results of the proposed controller and the results of study [9] based adpative droop control, specifically for the level of circulating current minimisation achieved under both studies. As mentioned earlier similar converters are considered with different line impedances 0.1 Ω for converter-1 and 0.15 Ω for converter-2.

At first the circualting current among the parallel DC-DC converters is investigated at different operating conditions such as different load currents, different line impedances and different converters input voltages as shown in Fig. 11. The figure shows faster responses for the proposed controller comparing with the conventional controller at different load conditions as shown in cases (a), (b) and (c) of Fig. 11. Also, the circulating current is minimised faster with the proposed controller while the line impedances and the converters input voltages are varying as shown in Fig. 11 (d) and (e), respectively.

As per Fig. 12, the converters output currents show faster response with the proposed adpative IACS controller over the conventional controller.

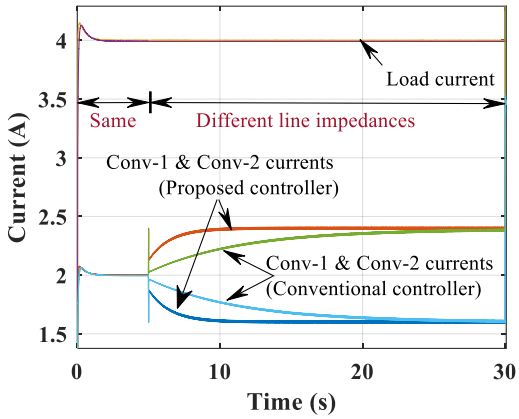

Fig. 12. Matlab/Simulink simulation results of the converters output currents and Load current when conventional and proposed IACS controller applied.

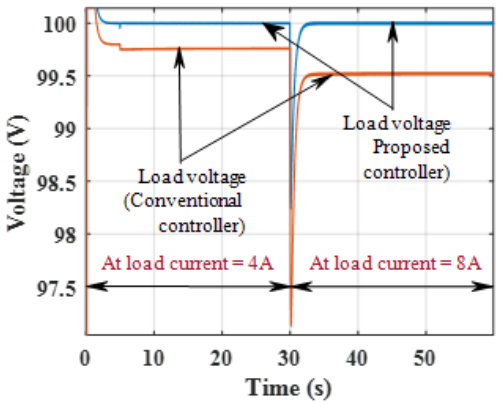

Fig. 13. The output load voltage under the conventional and proposed controller.

Fig. 13 shows the impact of varying the load current on the output load voltage for the proposed and conventional IACS controller while the load current step from 4 A to 8 A at 30 s. The figure shows a steady-state error for the load voltage when the conventional IACS controller is applied. This steady-state error is eliminated with the adaptive proposed controller. Also, the proposed IACS shows better voltage control capabilities over the conventional

controller with varying load current. This can be shown in Fig. 13 with varying the load current from 4A to 8A, the output voltage dropped with the conventional controller scheme. However, with the proposed IACS, the load voltage maintained at the desired voltage 100V when similar load step applied.

The performance results based on Fig. 12 and Fig. 13 are summarized in Table 2. The table shows better performance for the proposed controller scheme over the conventional in terms of fast transient response and accurate output voltage.

Table 2. Performance results of 2-parallel converters under conventional and proposed IACS control schemes.

Characteristics	Conventional IACS	Proposed IACS
Converter output current rise time (ms)	2811	92.1
Converter output current settling time (s)	24	3.619
Circulating current, mean value (mA)	-60.6	-5.6
Load voltage (V)	99.5	100

The following section compares the outcomes of this study and study [9] as both studies has the same goal of circulating current minimization among parallel-connected DC-DC converters. First, comparing the magnitude of circulating current achieved by adaptive droop control in study [9] and that obtained under this study. Second, investigating controller capability for regulating load voltage at different operating points based on both studies. The results of study [9] are reproduced in Matlab/Simulink as per Fig. 14 for the converters output voltages and load voltages.

Fig. 14 (a) is for study [9] which shows that the load voltage is changing with varying the line impedance of both converters. On the other hand, the output load voltage (see Fig. 14 (b)), based on the proposed adaptive IACS, is accurately regulated at the desired voltage with variable line impedance.

For circulating current, study [9] based on adaptive droop controller minimized the magnitude of circulating current to 0.03 A, while the adaptive IACS proposed under this study is able to reduce the magnitude of circulating current to 0.005A. Based on the above comparison, the proposed controller gives better controllability on the load voltage at different operating points and reduces the circulating current to very low values.

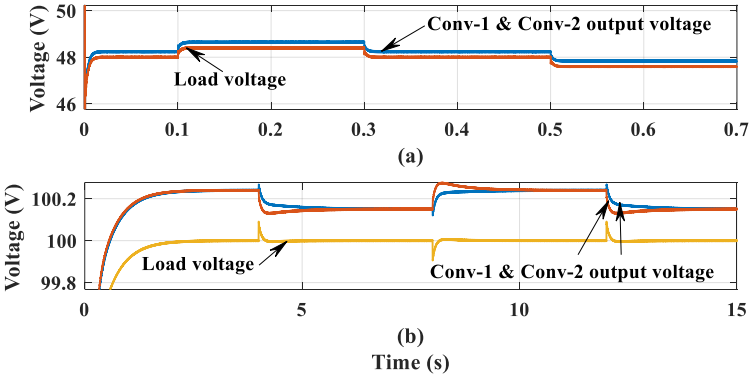

Fig. 14. Converters output voltages and load voltage for (a) Study [9] and (b) proposed IACS controller.

7. Conclusion

The paper proposed a new adaptive IACS control scheme based on SDM for accurate voltage regulation and minimizing circulating current among parallel DC-DC converters connected in a DC-microgrid. N-parallel connected converters model with the proposed controller is derived assuming identical converters. Stability analysis is used for designing the PI controllers of IACS to insure stable closed loops. From the analysis, it is concluded that the stability of the load voltage with parallel converters depends on the voltage regulation capability of the individual converters. Matlab/Simulink is used to investigate the performance of conventional and proposed adaptive IACS controllers based 2-parallel DC-DC boost converters supplying DC-load. The proposed controller overcomes the shortcomings of the

conventional IACS in terms of better voltage regulation with varying line impedances and in minimizing the circulating current. Also, it shows better performance comparing with one of the studies in the literature in terms of accurate voltage regulation and lower circulating current levels.

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