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New Fault Detection Algorithm for an Improved Dual VSM Control Structure With FRT Capability

AHMED ABDELRAHIM[1,2], MICHAEL SMAILES[3], KHALED H. AHMED[1], (Senior Member, IEEE), PAUL MCKEEVER[3], AND AGUSTÍ EGEA-ÀLVAREZ[1], (Member, IEEE)

[1]Electronic and Electrical Engineering Department, University of Strathclyde, Glasgow G1 1XW, U.K.
[2]Electrical and Control Department, Arab Academy for Science, Technology and Maritime Transport, Alexandria 1029, Egypt
[3]Offshore Renewable Energy Catapult, National Renewable Energy Centre, Blyth NE24 3AG, U.K.

Corresponding author: Ahmed Abdelrahim (ahmed.abdelrahim@strath.ac.uk)

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ABSTRACT Grid forming converters are a promising solution to enhance the stability of electrical networks with a high penetration of renewable generation. Virtual Synchronous Machines (VSM) are a particular type of grid forming converter, which can be implemented without an inner Current Control (CC) loop. This VSM implementation can provide a better inertial response than other grid forming structures with an inner CC. However, it cannot limit the current through the converter during a fault. A standard solution uses a VSM as the primary controller with a conventional inner CC acting as a backup controller during fault conditions, referred to here as a Dual VSM control structure. The switching action between the primary and the backup controllers is dependent on an accurate Fault Detection Algorithm (FDA). The conventional FDA mentioned in the literature has limitations in particular but not uncommon scenarios. The article shows the limitations of the conventional FDA in weak grids and unbalanced conditions and introduces a new FDA with improved performance. Two types of sensitivity analysis are used to study the dynamics of the proposed control approach. The First is the sensitivity of the proposed control structure to different fault locations in strong and weak grids. The Second is the sensitivity of the controller response to changing controller parameters. The second analysis is introduced as a reference for tuning and improvement of the control structure introduced.

INDEX TERMS Balanced faults, current control, fault detection algorithm, grid forming converters, grid following converters, parameter sensitivity analysis unbalanced faults, virtual synchronous machine, weak grids.

I. INTRODUCTION

In the UK, offshore wind generation is expected to increase from 9 GW to 83.1 GW by 2050 [1]. As the penetration of converter interfaced generation increases, new network operation and control challenges arise. Two of the future power network biggest challenges are the reduction of inertia that threatens the frequency stability of the network [2] and the connection of new converter based generation into weak networks [3].

There are a large variety of proposed solutions such as increasing the number of synchronous condensers [4], using Flexible Alternating Current Transmission System (FACTS) devices to enhance voltage support and fault current [4], new Fast Frequency Response (FFR) services [5], and upgrading the converter controllers to grid forming [5], [6]. Grid forming converters can create a voltage at the converter terminals without an external grid [7], [8]. One of the most known types of grid forming converter is the Virtual Synchronous Machine (VSM), which emulates the synchronous machine behaviour in different degrees of detail. It has been reported that VSMs can: provide an inertial response similar to a Synchronous Machine (SM) [9], achieve stable response in very weak grids [10], and provide black start capability [8]. However, the VSM structure requires further studies, including the assessment of converter-converter interactions and the requirement of adding new energy storage to support the inertial power provision [11].

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Fault Ride Through (FRT) capability for Voltage Source Converters (VSCs) can be provided using different approaches. The first approach is to add an external hardware components, such power electronic fault current limiters [12]. The second approach, which is adopted in this article, is to enhance the control structure, which can enable the FRT capability with lower cost as the same hardware is used. For the FRT capability enhancement of a VSC controlled as a VSM, the researchers tend to build a VSM structure with an inner positive sequence Current Control (CC) loop [13]–[23], or positive and negative (pn) sequence controllers [18], [24]. In addition to the use of the current loop, some ancillary controllers have been used to enhance the FRT performance such as virtual impedance [13], [15], [17], [19], [20], [25]–[27], current reference saturation [18], [28]–[31], and some structures merging both techniques [14], [16]. However, some authors reported instabilities regarding the virtual impedance [28], [29], and the current reference saturation [20], [32]. The authors in [33] reported that an inner CC loop within a VSM structure requires careful tuning to avoid instability, especially for low switching frequency. Another approach to building a VSM structure without a CC was proposed in [34], [35] that requires the solution of an optimization function, which is time-consuming and cannot be tuned in real-time.

Several solutions have been presented, which considered switching to another control mode during a fault including: switching the outer loops/adding extra loops [15], [17], [31], disabling the voltage controller [36], and switching to a grid following mode (referred to as Dual VSM structure in this paper) [24], [29], [37]. However, the issues associated with switching loops have not been widely assessed in the literature. Often studies do not assess for unbalanced faults [15], [24], [29], [36]–[39] or weak grids [17], [24], [29], [36] (particularly the algorithms used for switching the control loops).

The motivation of the article is to assess the algorithm responsible for switching between controllers. This has been largely neglected in the literature. Therefore, this article discusses in detail the limitations of the Dual VSM structure. First the article discusses the behaviour of a conventional Fault Detection Algorithm (FDA) inspired from [15], [36], [37], which is used in the Dual VSM structure to switch between controllers [18], [24], [36], [37]. Second a new FDA is proposed to mitigate the limitations of the conventional FDA in low SCRs and different types of faults. The limitation of directly controlling the CC references is presented. In addition, an outer loop is presented with a current reference saturation method inspired by [40], which is used to limit the current in both weak and strong grid conditions. The full proposed control structure is referred to here as the Improved Dual VSM.

Two types of analysis are conducted to determine the performance of the proposed controller: a fault location sensitivity and a control parameter sensitivity analysis. The first sensitivity analysis shows the response of the proposed structure to balanced and unbalanced faults in low and high SCRs. This analysis is used to verify the reliability and performance of the proposed structure. The second analysis demonstrates the difference in controller behaviour when each control parameter changes. This analysis is discussed for low and high SCR grid conditions, which can be used as a tuning reference for such a control structure.

The contribution of this article can be summarized as follows:

- Identification of the limitations of the Dual VSM structure with conventional FDA.
- Proposal of a new FDA to overcome the identified limitations.
- Usage of an outer loop controller to be grid compliant during faults in weak networks.
- A fault distance sensitivity analysis to validate the proposed structure.
- Further control parameter sensitivity analysis to show the tuning preference of the proposed structure.

The Dual VSM structure configuration is considered in Section II. Section III discusses the FRT capability of Dual VSM structure for high and low SCR. Section IV discusses the Improved Dual VSM structure, the new FDA, and the CC outer loop. Section V presents the verification of the Improved Dual VSM structure through fault location sensitivity analysis in low and high SCR. Section VI assesses the response sensitivity to control parameters with the paper's conclusion given in Section VII.

II. DUAL VSM STRUCTURE CONFIGURATION

The dual VSM structure [15], [18], [24], [41] studied in this paper consists of a primary VSM controller without CC and backup CC for fault conditions. When a fault is detected, the FDA switches from VSM to CC mode. The main parts of the controller are the voltage and current sequence calculation, the VSM controller, the back-up current control and FDA. The full converter control is presented in Fig. 1.

In this study, the grid is represented by a Thevenin equivalent as standard model used to assess the performance of VSC-FRT [15], [16], [23], [34], [42]. The grid equivalent voltage is represented by E_{grid}, R_n is the grid Thevenin resistance, and L_n the Thevenin inductance. The converter voltage is Vc_{abc}, and the line reactor resistance and inductance are R_c and L_c respectively. The Point of Common Coupling (PCC) measurements are the voltage U_{abc} and the current Ic_{abc}.

A. MEASUREMENT AND SEQUENCE CALCULATION

The Dual VSM structure uses the PCC measurements for all the control loops. A park transformation is applied to the PCC measurements to calculate the dq components. The q component is aligned to the active power and the d components lag by 90°.

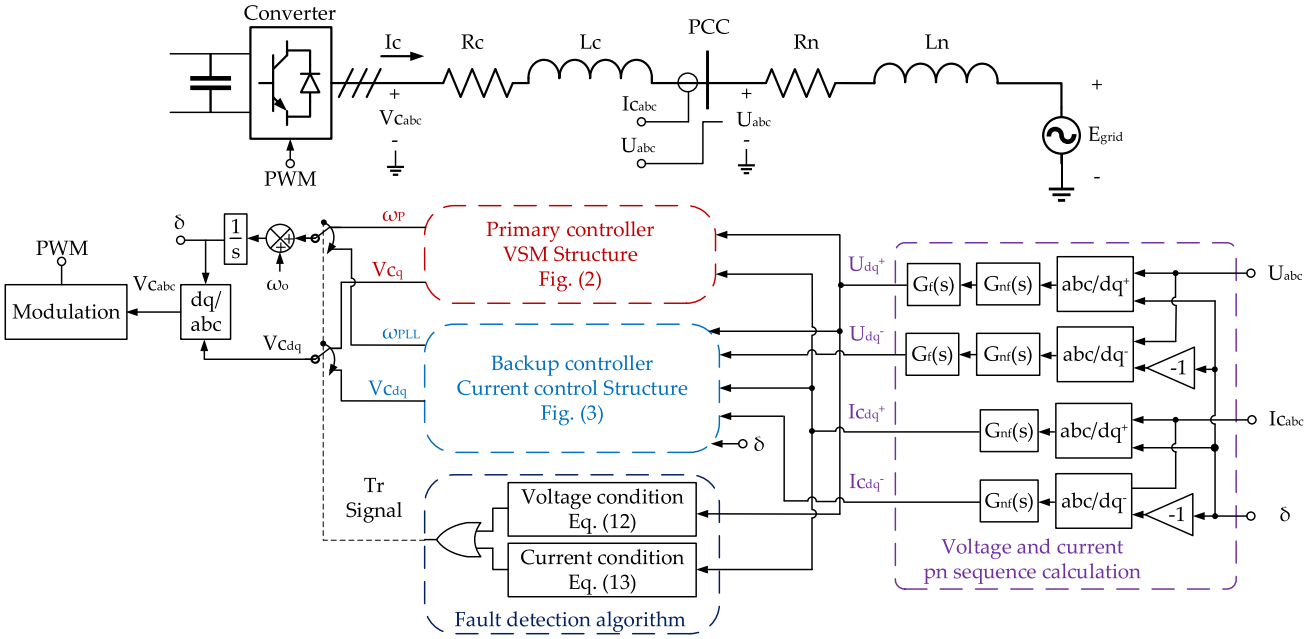

FIGURE 1. Dual VSM structure. (purple) positive and negative voltage and current calculation, VSM structure (red), current control structure (blue), and fault detection algorithm (navy).

A notch filter $G_{nf}(s)$ is used to decouple the pn sequence of the voltage and current, as in

$$G_{nf}(s) = \frac{s^2 + \omega_f^2}{s^2 + \frac{\omega_f}{Q_f}s + \omega_f^2} \tag{1}$$

where ω_f is the centre frequency of the filter, and Q_f is the filter quality factor.

An extra first order filter is used to filter the pn sequence voltage components to enhance converter's stability [43], which has τ_f as a time constant.

The pn sequence components are U_{qd}^{+}, Ic_{qd}^{+}, U_{qd}^{-}, and Ic_{qd}^{-} for the voltage and current.

B. VSM STRUCTURE DESCRIPTION AND TUNING

The VSM structure shown in Fig. 2 is a simplified version of SM emulation and is based on the power synchronization loop shown in [41]. This controller calculates the converter angle to exchange a particular amount of active power. Here, however, a PI controller is used instead of a P controller to emulate both the inertia and damping behaviours of the swing equation. The control structure consists of an active power loop PI controller represented by $G_P(s)$ and given by (2).

$$G_P(s) = k_{p-p} + \frac{k_{i-p}}{s} \tag{2}$$

where, k_{p-p} is the proportional gain and k_{i-p} is the integral gain of the PI controller.

The active power loop control gains tuning can be calculated from the SG swing equation. The first step to find the equivalency is to manipulate the SG swing

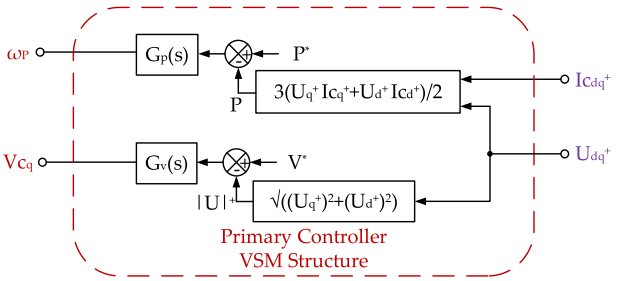

FIGURE 2. Schematic of the primary controller (VSM structure).

equation described as

$$\frac{\Delta\delta}{P_{mech} - P_{elec}} = \frac{1}{\frac{2HS_{rated}}{\omega_o}s^2 + Ds} \tag{3}$$

where H is the inertia constant, S_{rated} is the rated complex power, ω_0 is the rotor rated speed or rated frequency, D is the damping factor, δ is the angle of the rotor or the converter angle, P_{mech} is the mechanical power, and P_{elec} is the electrical power.

The swing equation can be used as a forward path in the closed-loop transfer function, and the gain k_m is the synchronizing torque coefficient. The natural frequency (ω_{n_1}) and the damping factor (ζ_1) of the synchronous machine can be expressed as

$$\omega_{n_1} = \sqrt{\frac{\omega_o}{2H}\frac{k_m}{S_{rated}}}, \quad \zeta_1 = \frac{D}{2}\sqrt{\frac{\omega_o}{2H\,S_{rated}k_m}} \tag{4}$$

A similar relationship can be found for the VSM active power loop, which represents the relation between the active

power loop and the converter angle. The closed-loop natural frequency (ω_{n_2}) and damping coefficient (ζ_2) for the VSM active power loop are expressed by

$$\omega_{n_2} = \sqrt{k_{i-p} k_m}, \quad \zeta_2 = \frac{k_{p-p}}{2}\sqrt{\frac{k_m}{K_{i-p}}} \tag{5}$$

Finally, both closed-loop transfer function parameters from equation (4) and equation (5) are equated so that $\omega_{n1} = \omega_{n2}$ and the damping factor $\zeta_1 = \zeta_2$.

Therefore, the integral coefficient K_{i-p} can be tuned using

$$K_{i-p} = \frac{\omega_o}{2H\ S_{rated}} \tag{6}$$

And the proportional coefficient K_{p-p} can be tuned using

$$K_{p-p} = \frac{D\omega_o}{2H\ S_{rated} k_m} = D\frac{K_{i-p}}{k_m} \tag{7}$$

The converter voltage magnitude is controlled using a PI controller represented by $G_v(s)$, which can be tuned as described in [41].

C. CONVENTIONAL POSITIVE AND NEGATIVE SEQUENCE CURRENT CONTROLLER

A conventional pn sequence CC is used as a backup controller during grid fault conditions. The pn sequence CC is based on [18], [24], [41], and can control the current during balanced and unbalanced faults. The control structure shown in Fig. 3 takes U^+_{qd}, Ic^+_{qd}, U^-_{qd}, and Ic^-_{qd} from the pn voltage and current components calculation. The references Ic^{+*}_{qd}, Ic^{-*}_{qd} of pn CC are used to set the current limit during faults. The converter voltage pn sequences are Vc^+_{qd}, and Vc^-_{qd}. The negative sequence converter voltage component is added to the positive sequence converter component using the conversion block (dq^-/dq^+), as per (8).

$$\begin{bmatrix} x^+_q \\ x^+_d \end{bmatrix} = \begin{bmatrix} \cos(2\delta) & -\sin(2\delta) \\ \sin(2\delta) & \cos(2\delta) \end{bmatrix} \begin{bmatrix} x^-_q \\ x^-_d \end{bmatrix} \tag{8}$$

The control structure consists of a current control loop PI controller represented by $G_{CC}(s)$ [44], which is expressed by

$$G_{CC}(s) = k_{p-CC} + \frac{k_{i-CC}}{s} \tag{9}$$

where, k_{p-CC} is the proportional gain of the PI controller, and k_{i-CC} is the integral gain of the PI controller. These controller parameters are tuned using internal model control as

$$k_{p-CC} = \frac{L_C}{\tau_{CC}}, \quad k_{i-CC} = \frac{R_C}{\tau_{CC}} \tag{10}$$

where, τ_{cc} is the CC loop time constant. The cross-coupling term $\omega_o L_c$ is the rated frequency multiplied by the converter filter inductance.

A PLL is used for synchronization with a PI controller G_{PLL} (S) represented by

$$G_{PLL}(s) = k_{p-PLL} + \frac{k_{i-PLL}}{s} \tag{11}$$

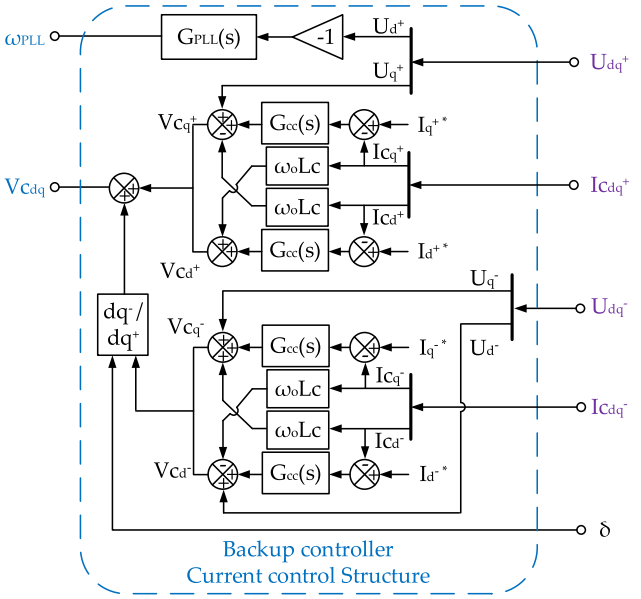

FIGURE 3. Schematic of the backup controller (pn sequence CC).

where, k_{p-PLL} is the proportional gain and k_{i-PLL} is the integral gain of the PI controller. The ratio between the control parameters k_{i-PLL}/k_{p-PLL} dictates the bandwidth of the controller [45]. Low PLL bandwidths have been suggested in [45] to stabilize the standard controller during faults in low and high SCRs.

D. CONVENTIONAL FDA

The conventional FDA uses the positive components to calculate the Tr signal which is the FDA output that determines the operating mode. The conventional FDA conditions are developed based on [15], [36], [41] and expressed by (12) and (13)

$$\sqrt{\left(U^+_q\right)^2 + \left(U^+_d\right)^2} < |U|_{min} \tag{12}$$

$$\sqrt{\left(I^+_{cq}\right)^2 + \left(I^+_{cd}\right)^2} > |I_c|_{max} \tag{13}$$

where, $|U|_{min}$ is the minimum voltage magnitude measured at the PCC (as specified by the Local grid code), and $|I_c|_{max}$ is the maximum current magnitude chosen below or equal to the maximum current capacity of the converter switches.

The primary operating mode is the VSM (when both (12) and (13) are false and Tr signal = 0), whose outputs are ω_P, the change in frequency related to the power, and the voltage loop output (Vc_{dq}). The backup operating mode is the CC (when either (12) and (13) is true and Tr signal = 1), whose outputs are ω_{PLL}, the change in frequency in relation to the change in the d voltage component, and Vc_{dq}, the CC voltage output. Then, the converter angle δ is derived after adding the change in frequency to the rated frequency ω_o.

III. DUAL VSM STRUCTURE FRT CAPABILITY STUDY

To show the limitation of the conventional Dual VSM structure a model was created in MATLAB/Simulink and

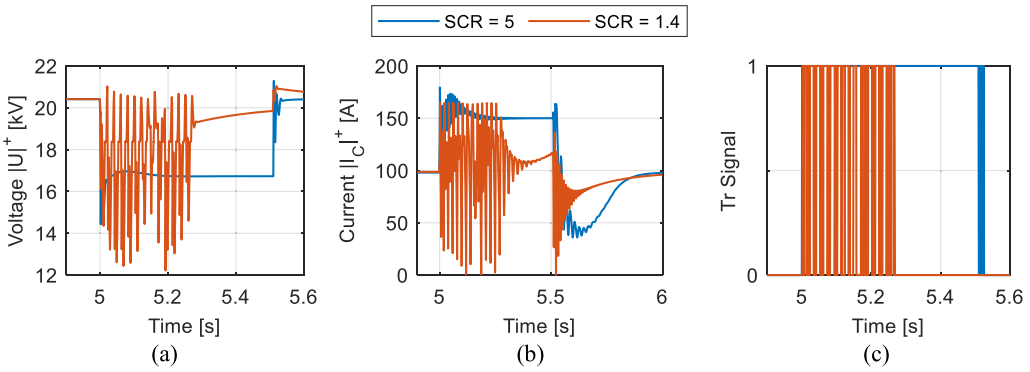

FIGURE 4. Comparison in low SCR (1.4) and high SCR (5), (a) positive sequence voltage magnitude |U|+ at the PCC, (b) positive sequence current magnitude |Ic|+, (c) FDA output signal (Tr signal).

TABLE 1. Power network simulation parameters.

Parameter Name	Parameter Value
S_{base}	5 MVA
$U_{nominal}$	25 kV
X_n/R_n	10
R_c	0.01 pu
x_c	0.1 pu

simulated under unbalanced fault conditions using a high SCR (5), and a low SCR (1.4). The parameters used for all test case scenarios are presented in Table 1. The notch filter in (1) was tuned for the simulations to have a centre frequency ω_f equal to 200π rad/s for all filters, and the quality factor Q_f is set to 1 for all filters except the positive sequence current, which was set to 10.

The first order filter time constant τ_f is set to 1 ms for the positive sequence voltage components, and is set to 10 ms for the negative sequence component. The fault is applied between 5 s and 5.5 s.

A test scenario is considered for the two SCR conditions where a converter that operates at 60% loading in steady-state conditions is subject to a single-phase to ground fault. During the fault, the converter injects 92% of its peak current. According to the simulation parameters in Table 1, this peak current is 163.3 A. The converter rating and references are designed to account for this peak plus a 20 % safety threshold [46], arriving at a peak current of 196 A (approximated to 200 A). The safety threshold accounts for overcurrent transients that are caused when switching between the controllers and are especially severe in weak networks. Inspired from the study in [47] and considering the converter rating, the reactive positive current component i_d^{+*} was set to 150 A, and all other current references were set to zero as per the local grid code.

Fig. 4(c) shows the conventional FDA output during the unbalanced fault in both low and high SCRs. The fault starts at $t = 5s$ and lasts 500 ms. Fig. 4(a) shows the positive sequence voltage, Fig. 4(b) shows the positive sequence current and Fig. 4(c) shows the output of the FDA.

The standard FDA detects the fault correctly for high SCR but disengages after some time for low SCR. The sub-optimal early FDA reset in the low SCR is driven by the higher grid Thevenin impedance, which requires the CC to apply a higher voltage to achieve the same current. The higher converter voltage increases the PCC voltage. For a single-phase to ground fault, the two remaining healthy phases voltages are increased by the higher converter voltage and the total voltage magnitude calculated by the FDA is within the specified nominal range as shown in Fig. 4(a), so the voltage appears to be healthy. Meanwhile, the fault detection current condition is not reliable, as the current decreases over time as a result of the current controller action. The combination of the voltage and current conditions makes the conventional FDA less effective in low SCRs. Furthermore, the injection of maximum current by the high voltage healthy phases drives the power transfer above the maximum complex power limit of the converter.

IV. IMPROVED DUAL VSM STRUCTURE

This section discusses a new improved FDA, and the enhancements added to support the faults in weak grids. A comparison between the conventional Dual VSM and the improved Dual VSM is presented.

A. NEW FDA AND CONTROLLER ENHANCEMENTS

The full schematic of the proposed structure is shown in Fig. 5. Moreover, an outer loop is added to the CC loop to deal with the weak network scenario and a bump-less transfer is added.

The new FDA is designed to operate effectively in different types of faults, and different SCR. The new FDA achieves better operation during unbalanced faults by considering the pn sequence voltage and current components, unlike the conventional FDA. The incorporation of the negative sequence is a key component to be added to the new FDA, especially in weak networks. The voltage condition is considered as

$$G_{fv}(s)\left(|U|^{+} - |U|^{-/+}\right) < |U|_{min} \tag{14}$$

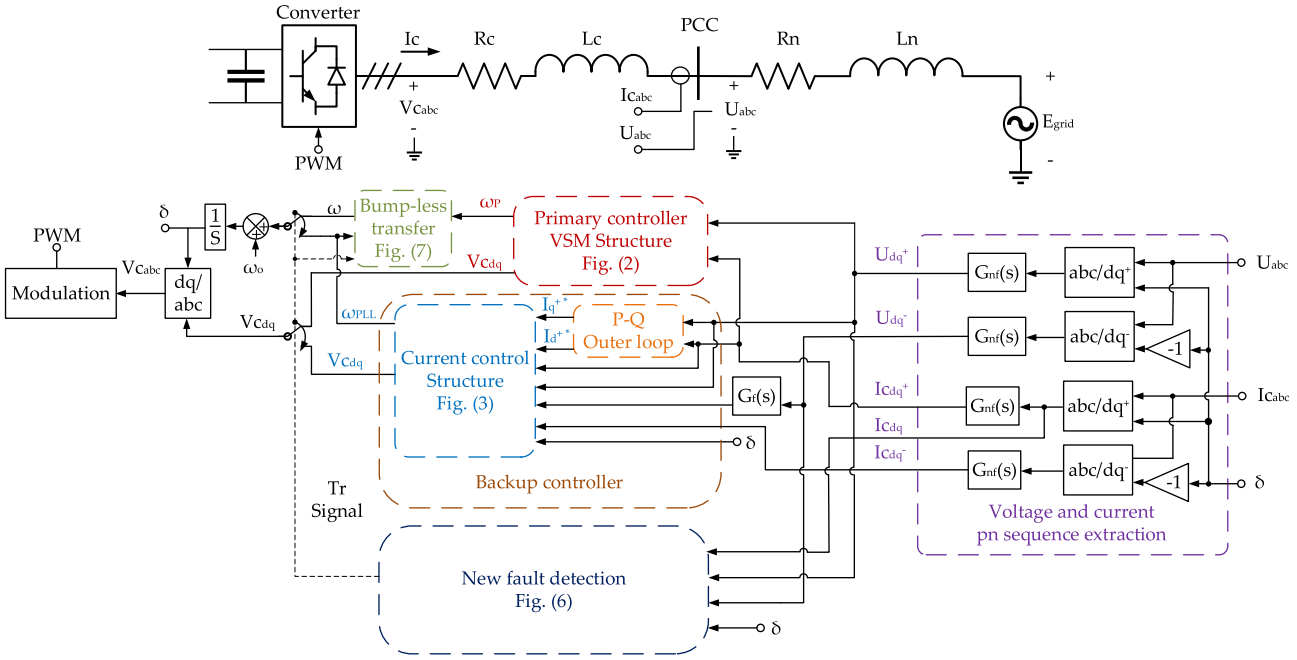

FIGURE 5. A full schematic of the improved dual VSM structure. outer loop (orange), bump-less transfer (green), new FDA (dark blue).

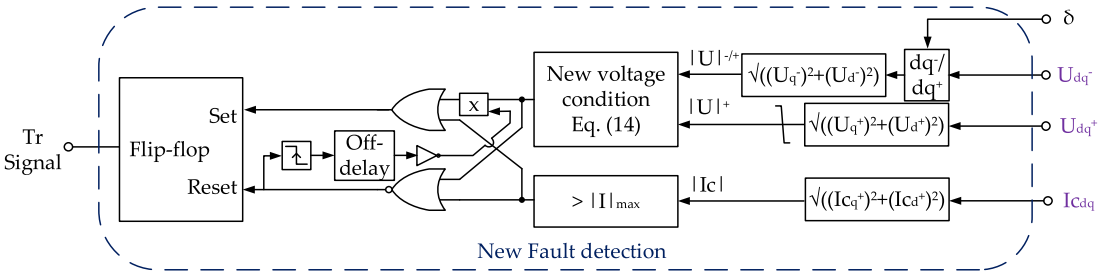

FIGURE 6. Schematic of the new FDA.

where $0 < |U|^{+} < |U|_{\text{rated}}$, $|U|^{-/+}$ is the negative sequence voltage aligned to the positive sequence frame, and $G_{fv}(s)$ is a first-order filter applied to voltage signal before the condition represented by

$$G_{fv}(s) = \frac{1}{\tau_{fv}s + 1} \tag{15}$$

where, τ_{fv} is the time constant for the first-order filter $G_{fv}(s)$.

The new voltage condition guarantees the detection of the unbalanced faults in weak grid condition, as the negative sequence voltage is used to decrease the high voltage created by the healthy phases. The current condition is the same as described in Eq. (13), but the condition input is the current measurement after the Park transformation so the negative sequence is considered as well.

During the fault recovery, the new FDA clears the Tr signal when both conditions are false. However, the voltage condition may experience a false voltage drop, caused by the transients created by the transition to the primary controller. As a result, the voltage condition is disabled for a short period using a Set/Reset flip-flop, an edge trigger and an off-delay time. This method prevents false re-engaging for a short time during the fault recovery while maintaining the converter protection as the current is continuously monitored, according to Eq. (13). The new improved FDA schematic is depicted in Fig. 6.

An outer loop is added to limit high voltages in the healthy phases during unbalanced faults in weak grids as observed in the simulations described in section III. The active power loop controller $G_{OP}(s)$ is expressed by

$$G_{OP}(s) = k_{p-OP} + \frac{k_{i-OP}}{s} \tag{16}$$

where, k_{p-OP} and k_{i-OP} are the proportional and the integral gain for the PI controller respectively.

And, the reactive power loop controller $G_{OQ}(s)$ is expressed by

$$G_{OQ}(s) = k_{p-OQ} + \frac{k_{i-OQ}}{s} \tag{17}$$

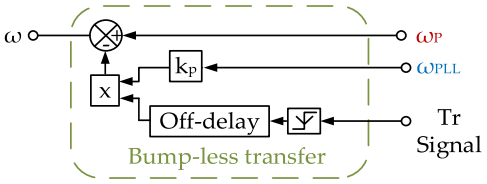

FIGURE 7. Bump-less transfer activated during fault recovery.

where, k_{p-OQ} and k_{i-OQ} are the proportional and the integral gain for the PI controller respectively. The outer loop current outputs are saturated to avoid overcurrent in high SCR conditions. The active power loop is set to zero to prioritize reactive power injection, and a current reference saturation is used to limit the output of the reactive power loop only. The active power controller can be used to provide flexible active power control for future developments.

The bump-less transfer depicted in Fig. 7 is added to smooth the transition between controllers during recovery. The method uses the PLL output for one cycle to support the active power loop resynchronization. The method multiplies the PLL output by a gain k_p, which is subtracted from the active power loop output.

This method is activated for one cycle after a reset signal is received from the new FDA, which is implemented using an edge detector and off delay timer. The active power loop reference is increased gradually to the rated value after the fault clearance, which introduces further damping in the transitional transients.

B. COMPARISON BETWEEN IMPROVED DUAL VSM STRUCTURE AND CONVENTIONAL DUAL VSM STRUCTURE

This section shows a comparison between the conventional Dual VSM structure and the Improved Dual VSM structure. In this comparison the same test conditions applied in section III are reapplied on the Improved Dual VSM structure to produce a fair comparison for both control structures.

Fig. 8 shows a comparison between the two control structures with a high SCR, where at Fig. 8(a-c) are the positive sequence voltage, the positive sequence current, and the Tr Signal respectively. The improved Dual VSM structure has lower current transients compared to the conventional structure. Moreover, Fig. 9(a-c) show a stable operation for the improved Dual VSM structure, while the conventional Dual VSM structure presents some issues with the fault detection in low SCR as discussed in Section III.

V. VERIFICATION OF THE IMPROVED DUAL VSM STRUCTURE THROUGH SEVERAL TEST CONDITIONS

The Improved Dual VSM structure is tested for balanced and unbalanced faults in low and high SCR grid conditions for the same parameters presented in Table 1. The test cases involve four different fault locations as shown in Fig. 10, where Z_C is the equivalent impedance of the filter and the transformer and Zn is the grid Thevenin impedance. The fault location is moved further away from the PCC from FL1 to FL4. The faults are all applied at 5 s and cleared at 5.5 s, as in Section III.

A. FAULT DISTANCE SENSITIVITY ANALYSIS IN LOW SCR

The Improved Dual VSM structure with the new FDA is tested in low SCR (1.4), to investigate the performance of the Improved Dual VSM structure response to the faults applied at the specified fault locations, as discussed before.

Fig. 11 shows the controller voltage and current waveform responses to a single-phase to ground fault. The new FDA shows good accuracy in detecting the single-phase to ground fault and its clearance at all locations. Fig. 11(a,b) are responses to the single-phase to ground faults applied at FL_4 and FL_3 where the controller responds to the fault applied at almost 5 s, and the new FDA detects the fault clearance at 5.5 s and switches back to primary controller at 5.52 s. Fig. 11(c,d) show the controller response to a single-phase to ground fault at FL_2 and FL_1 where the fault is detected at almost 5 s and the controller starts to inject the maximum reactive current (was tuned to be 150 A peak). The controller is switched back to VSM before 5.52 s. The zoomed area on the right of each figure shows that the proposed structure can inject a balanced current under all the test cases.

Fig. 12 shows the controller response to a three-phase to ground fault at the same fault locations discussed before. The new FDA also shows good accuracy in detecting all the three-phase to ground faults and clearances. Fig. 12(a-d) show the voltage and current waveforms for a fault applied at FL_4 to FL_1, the new FDA detects the fault at almost 5 s and detects the clearance before 5.52 s. The current during the fault is kept at 150 A peak, and a short time high current transient can be observed during the first instance of the fault, but it remains within the converter capability limit of 200 A.

B. FAULT DISTANCE SENSITIVITY ANALYSIS IN HIGH SCR

The same test case scenarios are applied at high SCR to investigate the controller behaviour. Fig. 13 shows the controller response to a single-phase to ground fault, where Fig. 13(a) is the voltage and current waveforms for the unbalanced faults applied at location FL_4. The waveforms show stable operation and the current is quickly limited. Fig. 13(b,c,d) show the voltage and current waveforms response to the unbalanced faults applied at locations FL_3, FL_2, and FL_1. Considering the four locations, the new FDA successfully identifies the fault at almost the same time as it is applied, and resets the fault signal to switch back to the VSM structure at almost 5.52 s.

Fig. 14 shows the controller response to the three-phase to ground fault at the same fault locations applied before. Fig. 14(a-d) show the voltage and current waveforms when a balanced fault is applied at FL_4, FL_3, FL_2, and FL_1. The four responses show that the controller detects the fault at almost 5 s with high peak current transient observed in the waveforms at the beginningof each fault. While the current is maintained at 150 A peak in the steady-state of the fault. Finally, the new FDA successfully resets the fault signal at about 5.52 s, and the structure switches from the current

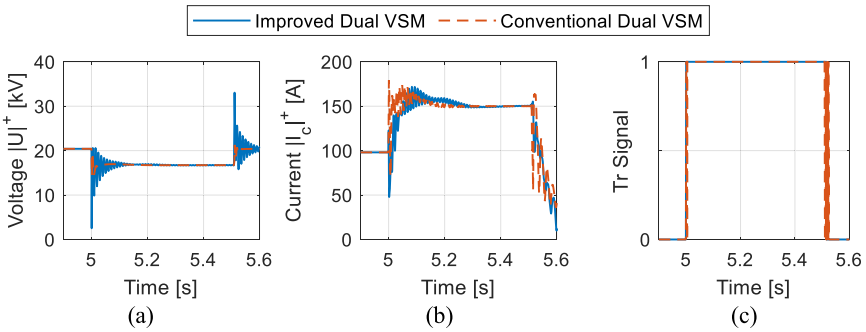

FIGURE 8. Comparison between improved dual VSM and conventional dual VSM in the high SCR case.

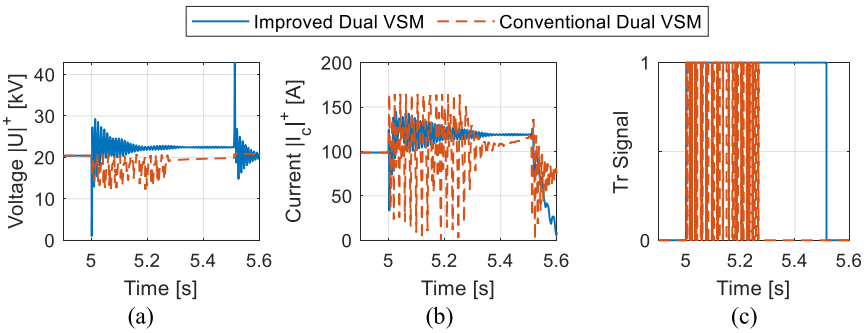

FIGURE 9. Comparison between improved dual VSM and conventional dual VSM in the low SCR case.

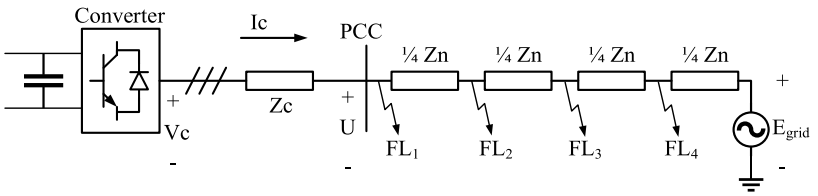

FIGURE 10. Fault locations used in the first analysis.

control to the VSM structure. The zoomed area in all the test cases has the same purpose as in low SCR, which shows the balanced current injection in all the test cases.

C. CONSECUTIVE FAULTS ANALYSIS

This analysis investigates the Improved Dual VSM structure response in two consecutive faults scenarios. This simulation aims to show that even though the voltage condition is disabled during the recovery, the improved FDA can operate safely if two consecutive faults occur.

The analysis involves subjecting the VSC to a single-phase to ground fault applied from 5s to 5.5s, then a three-phase to ground fault from 5.55s to 6.05s. These two faults are applied in strong and weak grid conditions, with the PCC voltage and current observed.

Fig. 15 shows the voltage and current waveforms after applying the two consecutive faults in high SCR. The current waveform shows the control structure is switched from the primary to the backup controller, which limits the current to be within the safe operational range. The Controller switches back to the primary controller at 6.07s.

The voltage and current waveforms in low SCR are depicted in Fig. 16. The current waveform shows that the current is limited successfully, and the controller switches back to the VSM 20 ms after both faults are cleared.

The current peak during the unbalanced fault is lower than the peak during the balanced fault. This is caused by the outer loop action, as the voltage created by the healthy phases during unbalanced faults is increased by decreasing the SCR.

This analysis shows that the Improved Dual VSM structure can survive two or more consecutive faults, and the blocked voltage condition during the recovery does not impact the reliability of the new FDA. In addition, the mitigation of the current peak during the single-phase to ground fault is clearly observed, which is used to damp the healthy phases voltage.

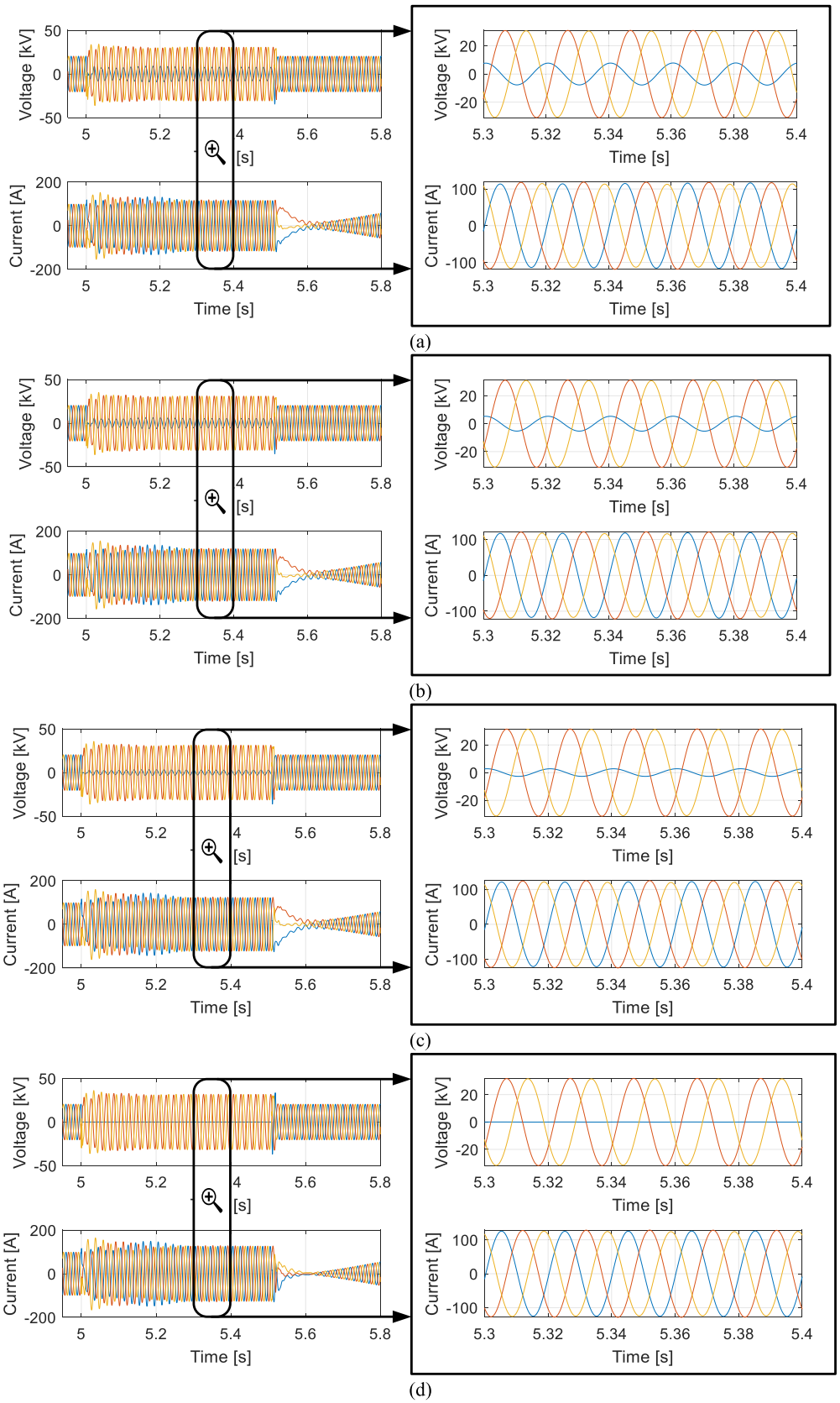

FIGURE 11. A single-phase to ground fault results at different locations in low SCR, (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1.

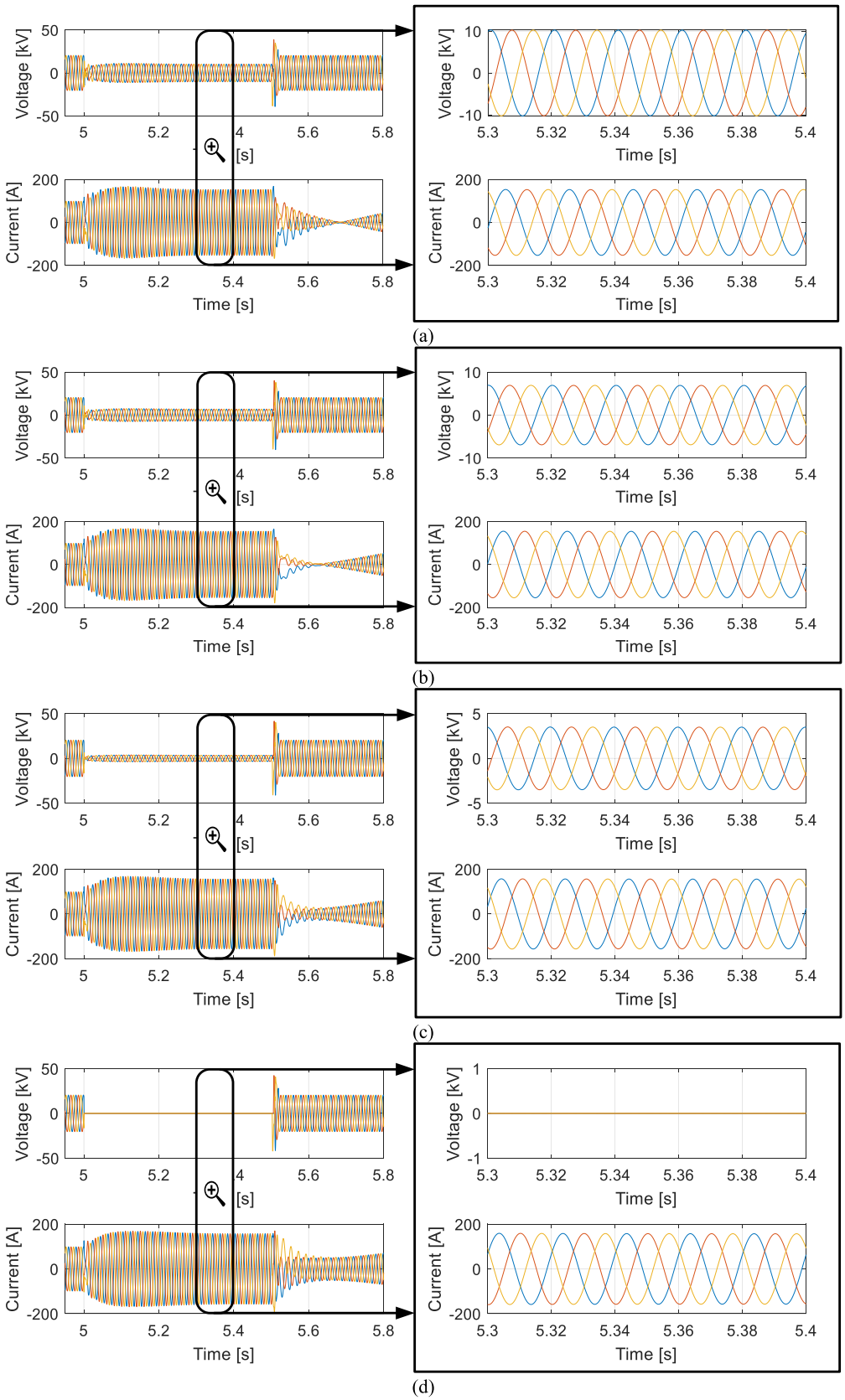

FIGURE 12. A three-phase to ground fault was applied at different locations in low SCR, (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1.

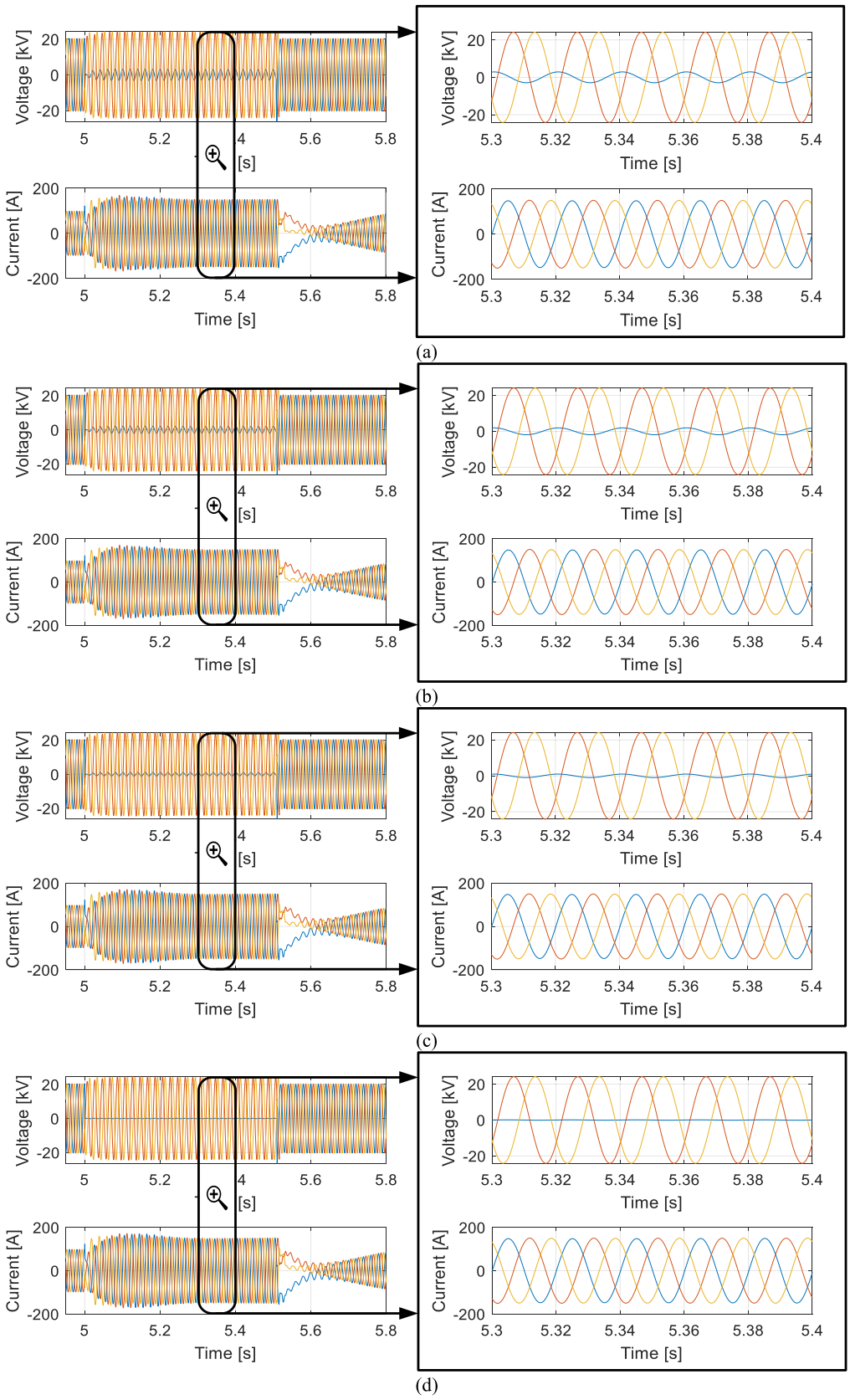

FIGURE 13. A single-phase to ground fault results at different locations with high SCR, (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1.

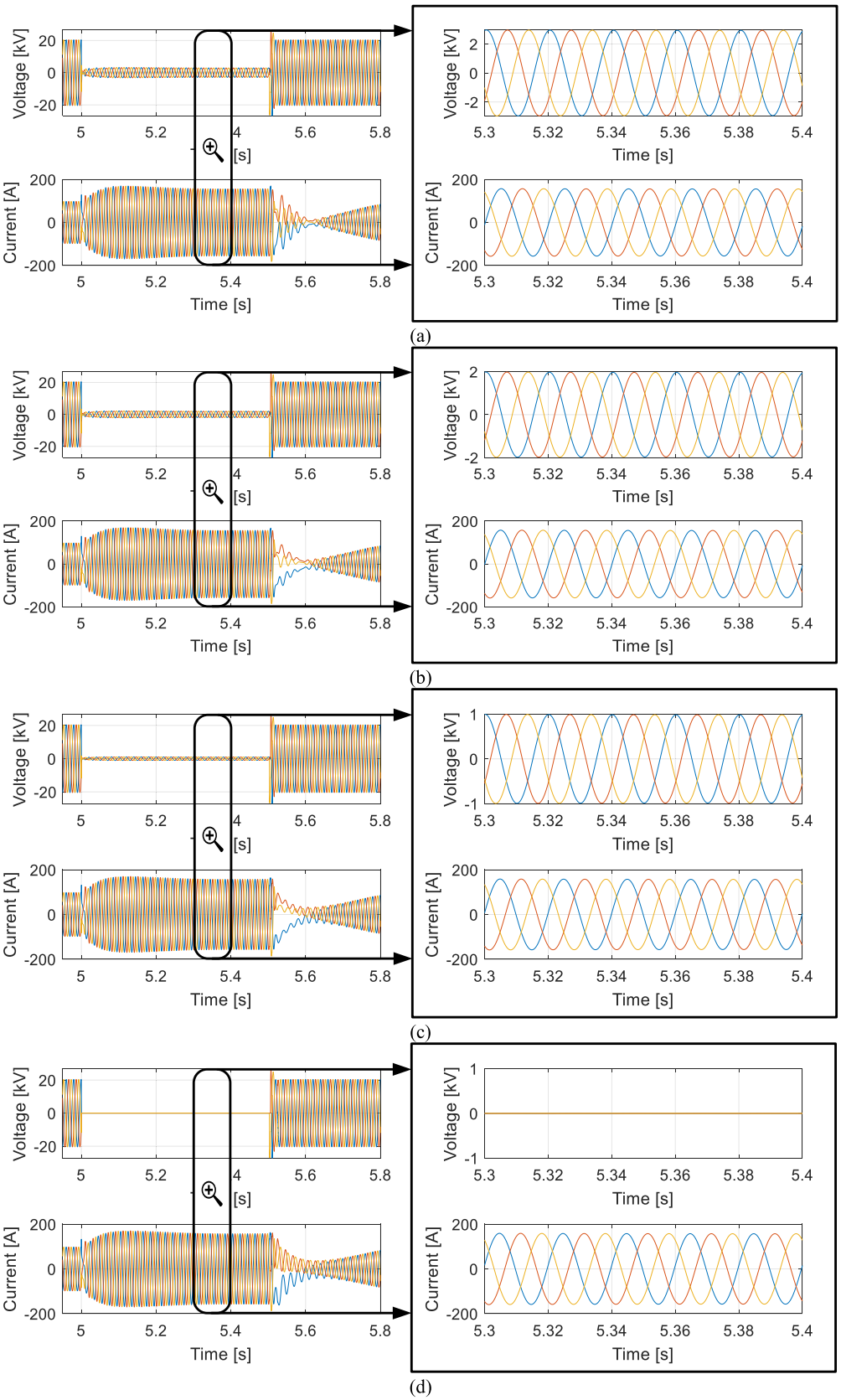

FIGURE 14. A three-phase to ground fault was applied at different locations in high SCR, (a) FL_4, (b) FL_3, (c) FL_2, and (d) FL_1.

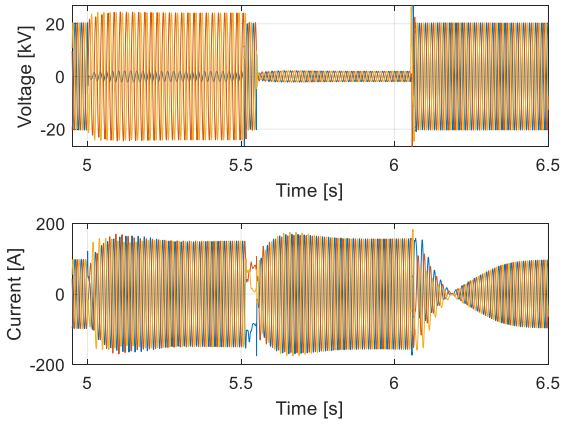

FIGURE 15. Unbalanced fault followed by a balanced fault in high SCR.

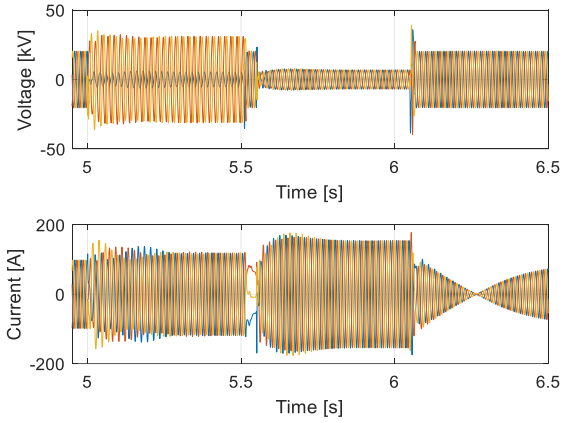

FIGURE 16. Unbalanced fault followed by a balanced fault in low SCR.

VI. CONTROL PARAMETERS SENSITIVITY ANALYSIS FOR THE IMPROVED DUAL VSM STRUCTURE

A parametric sensitivity study of the proposed controller is introduced in this section to determine the best tunning of the Improved Dual VSM structure. The parameters discussed are the voltage first-order filter time constant, τ_{fv}, of the new FDA, the current first-order filter time constant, τ_{fi}, of the new FDA, the current control loop time constant, τ_{cc}, the bandwidth of the PLL k_{i-PLL}/k_{p-PLL}, and the tuning of the active power loop k_{i-P}/k_{p-P}. Each different parameter configuration is subject to a single-phase to ground fault to observe the effect on the control response at the beginning, during the fault and during the recovery. The controller response is assessed by the current magnitude and the New FDA output for high and low SCR.

A. HIGH SCR STUDY

The parameter sensitivity analysis is used to study the change in the control response for high SCR. The first assessed parameter is the time constant of the voltage first order filter in the new FDA.

Fig. 17(a) shows that increasing the filter time constant increases the transient peak in the first instances after the fault. The transient peak is driven by the delay introduced by the first-order filter time constant to the new FDA action. However, the filters are necessary for smoothing the new FDA inputs. The steady-state fault current (Fig. 17(b)) and the recovery period after fault clearance (Fig. 17(c)) are not significantly affected by the voltage filter time constant. Fig. 17(d) shows the new FDA output, as the change in the filter time constant has no effect on the new FDA output.

The second parameter is the current control time constant τ_{cc}. Fig. 17(e-g) show that as the controller time constant increases, the oscillations in the fault current escalate and degrade the controller performance. Fig. 17(h) shows that the increase in τ_{cc} has no change on the new FDA output.

The third parameter is the PLL tuning k_{i-PLL}/k_{p-PLL}, defined as the ratio of the PLL proportional and integral control parameters. Fig. 17(i) shows that increasing the proportional gain increases the oscillations during the fault beginning period. Decreasing the proportional gain also introduces delays to the transient current in the fault recovery, as shown in Fig. 17(k). Fig. 17(l) shows that the new FDA output clearance is delayed by the highest tuning parameters ratio.

The fourth parameter is the active power loop tuning k_{i-P}/k_{p-P}, defined as the ratio of the active power loop proportional and integral gains. Fig. 17(m-p) shows that the active power loop tuning does not affect the response of the new FDA responses.

B. LOW SCR STUDY

The same parameters are studied for low SCR, which is more challenging due to the voltage instability in weak grid conditions. The first parameter is the voltage time constant τ_{fv} in the new FDA. Fig. 18(a) show that a low filter time constant has the lowest transient peak. While, Fig. 18(c) shows that the lowest time constant has the highest peak during recovery. Fig. 18(d) shows the new FDA output, at which the lowest time constant has the fastest recovery.

The second parameter is the current controller loop time constant τ_{cc}. Increasing τ_{cc} increases the oscillations in the fault current during the fault beginning, steady-state, and clearance (Fig. 18(e-g)). Fig. 18(h) shows no change on the new FDA output.

The third parameter is the PLL tuning k_{i-PLL}/k_{p-PLL}. The medium proportional gain value of the PLL has the best response at the beginning, and the recovery periods of the fault, as shown in Fig. 18(i-l).

The fourth parameter is the active power loop control gains ratio k_{i-P}/k_{p-P}. The sensitivity of the control response to the active power loop tuning is the same in low SCR as in high SCR, and no change is observed while changing the active power loop tuning, as shown in Fig. 18(m-p).

C. COMPARISON BETWEEN LOW SCR AND HIGH SCR

The parameter sensitivity analysis can be used as a reference for tuning such a control structure. Table 2 summarizes the best value for each case.

TABLE 2. Summary of the optimal control parameters with respect to fault beginning, steady-state and recovery.

Factors	SCR	Fault response performance		
		Fault beginning	Fault steady state	Fault recovery
τ_{fv} for the filter voltage signal	1.4	Low	No change	No change
	5	Low	No change	No change
PLL parameters ratio $k_{i\text{-}PLL}/k_{p\text{-}PLL}$	1.4	Medium	Medium	Medium
	5	Medium	Medium	Medium
CC time constant τ_{cc}	1.4	Low	Low	Low
	5	Low	Low	Low
Active power loop parameters ratio $k_{i\text{-}P}/k_{p\text{-}P}$	1.4	No change	No change	No change
	5	No change	No change	No change

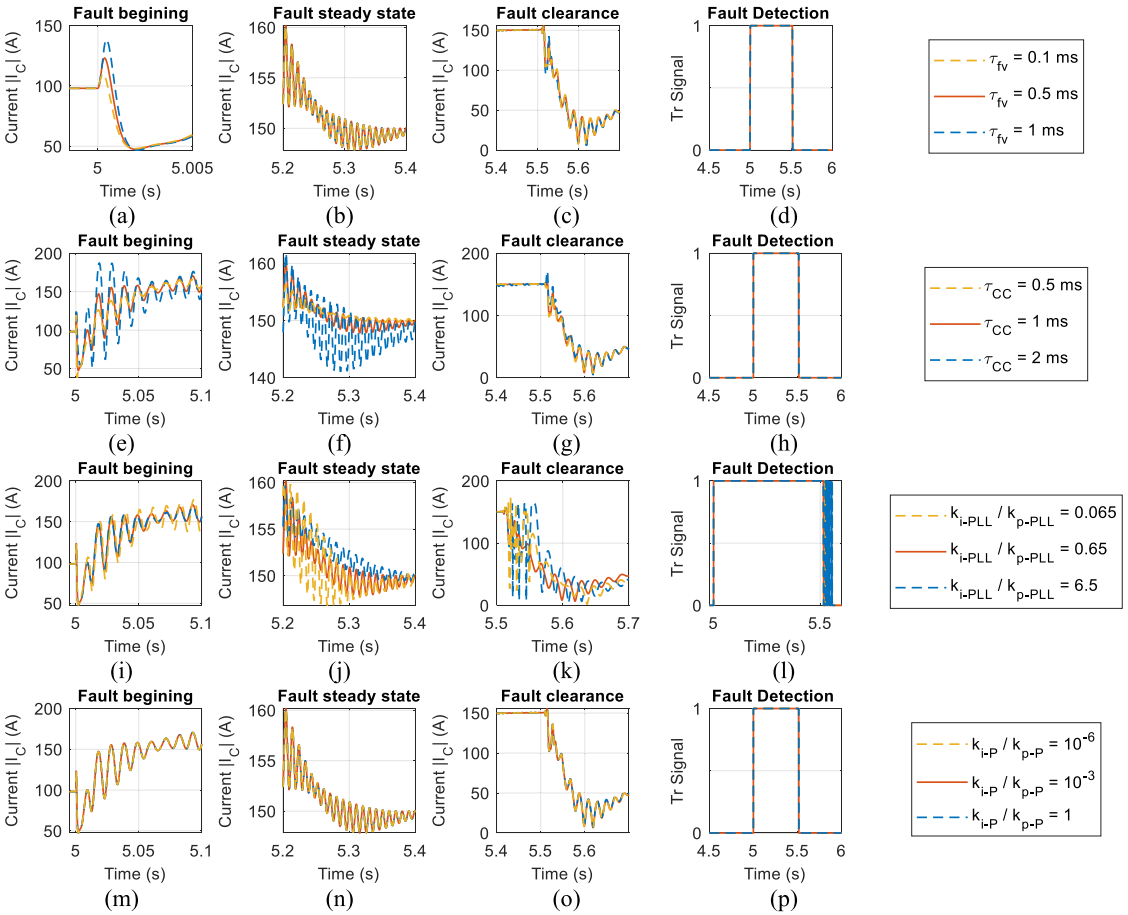

FIGURE 17. Parameter sensitivity analysis in the high SCR case: the coloumn (a,e,i,m) shows the currents during the fault beginning, the coloumn (b,f,j,n) shows the currents during the fault steady state, the coloumn (c,g,k,o) shows the currents during the fault recovery, and the coloumn (d,h,l,p) shows the new FDA outputs. While the row (a,b,c,d) shows the response for changing the new FDA voltage filter time constant τ_{fv}, the row (e,f,g,h) shows the response for changing the current controller time constant τ_{cc}, the row (m,n,o,p) shows the response for changing the PLL bandwidth k_{i-PLL}/k_{p-PLL}, and the row (q,r,s,t) show the response for changing the active power loop bandwidth k_{i-P}/k_{p-P}.

The lowest voltage filter time constant (τ_{fv}) was best for the two fault periods (beginning and recovery) in both SCR cases. The same effect is observed for the current controller time constant (τ_{cc}), where the lowest value shows the best current response in both SCR cases, which indicates that the faster current controller is recommended. The PLL control gains ratio k_{i-PLL}/k_{p-PLL} had a better performance for the medium value in both SCR cases, because the PLL behaviour is highly affected by the faults and inappropriate tuning may cause unsuccessful controller switching during the fault recovery. The change in the active power loop parameters k_{i-P}/k_{p-P} has no effect on control response.

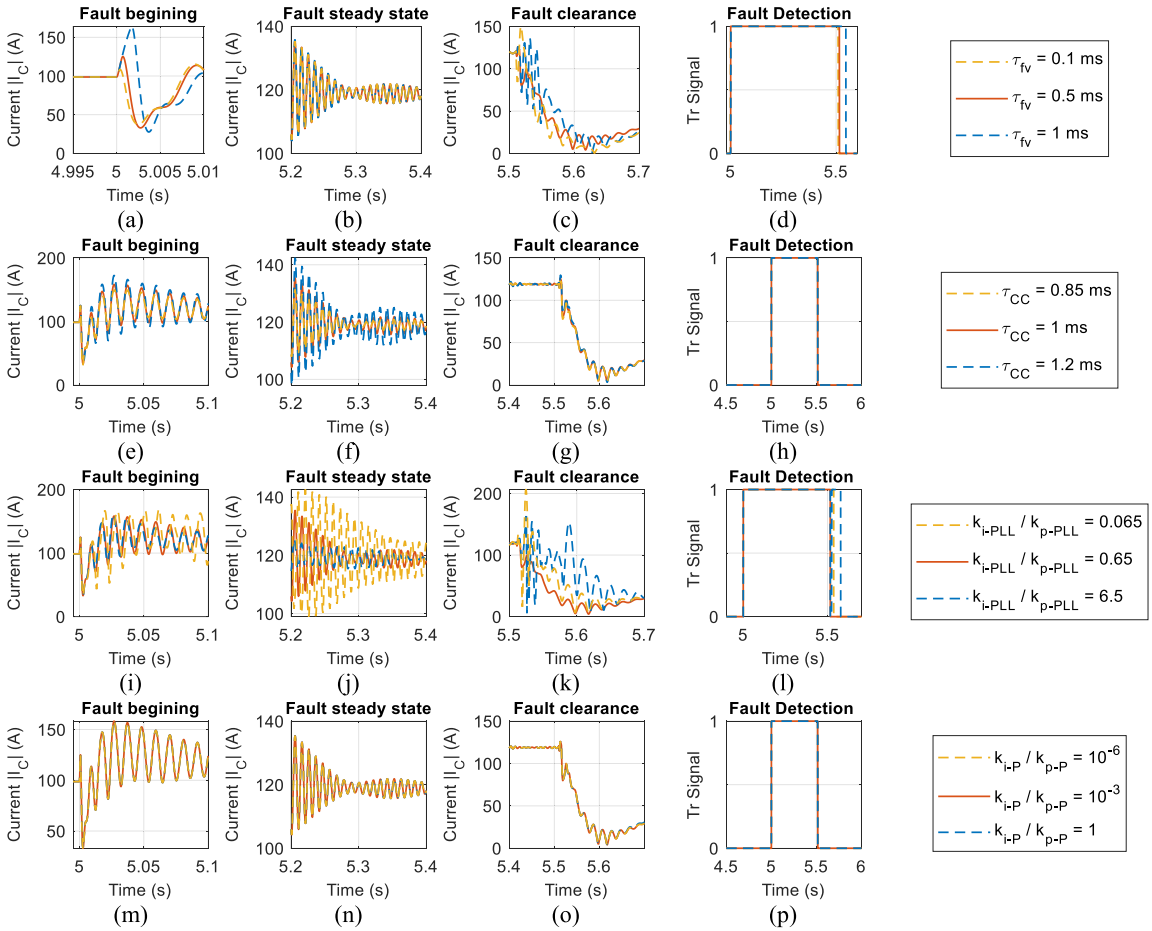

FIGURE 18. Parameter sensitivity analysis in the low SCR case: the coloumn (a,e,i,m) shows the currents during the fault beginning, the coloumn (b,f,j,n) shows the currents during the fault steady state, the coloumn (c,g,k,o) shows the currents during the fault recovery, and the coloumn (d,h,l,p) shows the new FDA outputs. While the row (a,b,c,d) shows the response for changing the new FDA voltage filter time constant τ_{fv}, the row (e,f,g,h) shows the response for changing the current controller time constant τ_{cc}, the row (m,n,o,p) shows the response for changing the PLL bandwidth k_{i-PLL}/k_{p-PLL}, and the row (q,r,s,t) show the response for changing the active power loop bandwidth k_{i-P}/k_{p-P}.

VII. CONCLUSION

This article discussed the limitations of the conventional Dual VSM structure. The structure was tested in Section III to show the challenges introduced by weak grid conditions. Under weak grid conditions, an increase in the voltage applied by the converter, as a result of the grid impedance increase, caused the voltage signal of the conventional FDA to fail. Therefore, a new FDA was proposed in Section IV, which had a better performance in strong and weak grids. Moreover, an outer loop was added to the current controller. This used a current reference saturation method to limit the current in strong grids.

A sensitivity analysis of the Improved Dual VSM structure at different fault locations was conducted under strong and weak grid conditions. The analysis showed that the new FDA overcomes the high voltage issue seen in weak grids. The balanced and unbalanced faults were handled by the Improved Dual VSM structure at each fault location.

The outer loop provides adequate maximum reactive current injection for the fault locations in low and high SCR. The current reference saturation method was able to limit the current in all the test cases in the strong grid condition it was designed for.

The consecutive faults test showed that the controller can limit the current even under tough conditions such as two consecutive close faults. A control parameters sensitivity analysis was introduced to show the effect of changing the controller parameters on the control response. The control response is stable for all the test cases using the medium tuning values. Then, each control parameter is changed to two different values to observe the change in the control response. The result showed the effect of changing each control parameter on the controller response during unbalanced faults in low and high SCR.

A set of observations are obtained from the control parameter sensitivity analysis:

- The lower the new FDA voltage time constant the better the fault detection response.
- Reducing the PLL bandwidth significantly, as suggested by the literature, is less effective at stabilizing the response during low SCR during faults.
- The faster the CC time constant the is recommended for lower current transients.
- The tuning of the active power loop is not effective on the controller response

Finally, the control parameters sensitivity analysis can be used as a reference for the tuning of a control structure resembling the improved Dual VSM.

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AHMED ABDELRAHIM was born in Alexandria, Egypt, in 1990. He received the B.S. and M.S. degrees in electrical and control engineering from the Arab Academy for Science, Technology and Maritime Transport, Alexandria, in 2017. He is currently pursuing the Ph.D. degree in electronics and electrical engineering with the University of Strathclyde, Glasgow, U.K.

From 2013 to 2018, he was a Teaching Assistant with the Arab Academy for Science, Technology and Maritime Transport. His research interests include control of grid forming converters, fault tolerant grid forming converters, and VSC operation in weak grids.

MICHAEL SMAILES received the M.Eng. degree (Hons.) in electrical and mechanical engineering from The University of Edinburgh, in 2011, and the D.Eng. degree from The Universities of Edinburgh, Stathclyde, and Exeter through the IDCORE Program on Hybrid HVDC Transformers in Multiterminal HVDC networks, in 2018. Since 2016, he has been working with the Applied Research Team, ORE Catapult, where he became a Senior Research Engineer in grid integration, in 2020. He has published numerous conference and journal articles and has an international patent on MMC converter control. His research interests include new ancillary services for offshore renewables, including, inertial, frequency and blackstart as well as novel grid compliance testing strategies.

KHALED H. AHMED (Senior Member, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees from Alexandria University, Egypt, in 2002 and 2004, respectively, and the Ph.D. degree in power electronics applications from the University of Strathclyde, U.K., in 2008. Since 2019, he has been a Professor with Alexandria University. He is currently a Reader in power electronics with the University of Strathclyde. He has published more than 110 technical articles in refereed journals and conferences as well as a published textbook entitled *High Voltage Direct Current Transmission: Converters, Systems and DC Grids*, a book chapter contribution, and a PCT patent PCT/GB2017/051364. His research interests include renewable energy integration, high-power converters, offshore wind energy, dc–dc converters, HVDC, and smart grids. He is a Senior Member of the IEEE Power Electronics and Industrial Electronics societies.

PAUL MCKEEVER received the B.Eng. and M.Eng. (Hons.) degrees in electrical and electronic engineering from the University of Bradford, Bradford, U.K.

He is currently the Head of Electrical Research with the Offshore Renewable Energy Catapult, U.K. Previously, he occupied the role of Head of Strategic Research and prior to that, he was the Project Coordinator for the OPTIMUS FP7 Project (prognostic condition monitoring), the Snapper FP7 Project, and Aqua-marine Power's Oyster Project (both wave energy converter projects). He is a member of the Durham Energy Institute's Industrial Advisory Board. He is also a member of the Institution of Engineering and Technology. He is also a Board Member of the European Association of Renewable Energy Research Centres, a Management Board Member of the European Energy Research Alliance Joint Program for Wind, and part of the Executive Committee for the European Technology and Innovation Platform for Wind. He also chairs the Industrial Advisory Board for the SuperGen ORE Hub. He is also a Chartered Engineer.

AGUSTÍ EGEA-ÀLVAREZ (Member, IEEE) received the B.Sc., M.Sc., and Ph.D. degrees from the Technical University of Catalonia, Barcelona, in 2008, 2010, and 2014, respectively. He was a Marie Curie Fellow with China Electric Power Research Institute (CEPRI), in 2015. He joined Siemens Gamesa, as Converter Control Engineer, working on grid forming controllers and alternative HVDC schemes for offshore wind farms, in 2016. He has been involved in several CIGRE and ENTSO-E working groups. Since 2018, he has been a Strathclyde Chancellor's Fellow (Lecturer) with the Electronic and Electrical Engineering Department. His current research interests include control and operation of high-voltage direct current systems, renewable generation systems, electrical machines, and power converter control. He is a member of IET. He is also a member of the Power Electronics, Drives and Energy Conversion (PEDEC) Group.