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Standardized Assessment Framework for Design and Operation of Weak AC Grid-Connected VSC Controllers

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ABSTRACT Significant research attention is focused on the stability and control of voltage-source converters (VSCs) in weak ac grids. However, the assessment of VSC control strategies has never been standardized, such that novel solutions proposed in the literature are not objectively evaluated against current best-practice. This paper establishes a comprehensive, standardized assessment framework for grid-connected VSC controllers, which allows objective comparison of novel controllers under development and established methods already in operation. The assessment consists of a tuning stage, time-domain analysis and frequency-domain analysis to form a complete evaluation that can be applied in its full aggregated form or as individual assessment steps. Three VSC controllers, namely vector current control, power-synchronization control and a virtual synchronous machine, are compared in this paper using small-signal models, time-domain simulations and control hardware-in-the-loop Real-Time Digital Simulation (RTDS) experiments to demonstrate the versatility and robustness of the proposed framework for controllers with very different structures.

INDEX TERMS Voltage-source converters, weak ac grids, vector current control, virtual synchronous machine, power-synchronization control.

I. INTRODUCTION

The increasing penetration of renewable energy generation, distributed generation and energy storage in power networks across the world has led to much stricter requirements for the stability and performance of grid-connected power electronic converters. Voltage-source converters (VSCs) are becoming the most dominant technology choice for this task due to their robust performance in weak grids and adaptable control techniques. However, in very weak grids (that is, AC grids with short circuit ratio (SCR) < 2), the control of VSCs for high active power transfer is challenging and ongoing research has not satisfactorily solved the problem. No VSC control strategy has yet prevailed as the ultimate solution to the weak grid issue, and so novel controllers are regularly proposed in the literature in an attempt to move closer to an optimum strategy, e.g., [1]–[7]. In strong grids, grid-following strategies based on vector current control (VCC) are the favored approach due to the decoupled active and reactive power control and intrinsic current-limitation capability in fault conditions. However, as the grid strength weakens, instabilities caused by PLL dynamics and outer loop interactions can occur [7]–[9]. Proposed enhancements to VCC to improve the weak grid performance have included re-tuning [1], [10], virtual impedance [2], [3] and feedforward methods [4], [5]. These controller modifications appear to show improvements for maximum power transfer and reactive power support in weak grids. However, re-tuning approaches inevitably involve slowing down the PLL or outer loops, which degrades the dynamic performance. A virtual impedance approach assumes that the grid conditions have been accurately quantified and are unchanging. A fundamental issue remains for grid-following control, namely that synchronization is aligned to the voltage at the point of common coupling (PCC), which is not constant in a very weak grid. This problem of synchronization and voltage support has led to an increase in research attention on grid-forming controllers for weak AC grid-connected VSCs.

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The principle of grid-forming control is for the converter to appear as a stiff voltage source to the grid and thus provide frequency and voltage support in conditions where the PCC voltage is very sensitive [11], [12]. Grid-forming controllers do not use a PLL for synchronization but instead use a form of modified droop-control on the active power error to produce the controller reference angle. One such strategy is power-synchronization control (PSC), first proposed in [7]. This control uses first order droop-control for power control/synchronization, a PI controller for ac voltage control and a high-pass current filter to damp out grid-frequency resonances. Studies in [13]–[15] have suggested that PSC performs well at high power transfer for connecting two very weak grids and for connecting wind farms to weak systems. However, PSC does not have inherent current-limitation in the event of faults and so a back-up current controller and PLL will always be required. The effects of this protection on effective inertia emulation can be unpredictable [6].

More robust inertia support is provided by a class of controllers called virtual synchronous machine (VSM) control. The idea of VSM control was first proposed in [16] but the title now encompasses a broad range of controller structures which emulate the behavior of synchronous generators to a greater or lesser degree. Some VSM control methods imitate all the characteristics of a synchronous machine, including virtual fluxes and torques [17]. Simpler implementations use a form of the swing equation for synchronous machines combined with PI control of the ac voltage or reactive power [12], [18]. Other modifications to VSM include the addition of fast frequency response (FFR) branches, zero inertia implementations and maximum power point tracking [19]–[21]. VSM controllers, within the wider category of grid-forming controllers, are already in operation in microgrids and are being proposed for mass-market applications requiring voltage support and black-start capability [22]. However, there remains no consensus on the optimum approach within the VSM class of controllers and each specific form of VSM is assessed according to a diverse and inconsistent range of tests at only a single controller operating point.

As demonstrated in literature, the wide range of grid-following and grid-forming controllers proposed for weak AC grid-connected VSCs can have very different configurations, including different synchronization methods, cascaded structures and choice of high-level control variables (e.g. reactive power versus AC voltage control). Because of this variety, assessment of VSC control strategies has never been standardized or formalized. Each controller designer has generally chosen their own evaluation methods and metrics, performing a varying set of reference step changes or fault conditions to the proposed controller at only a single operating point. This inconsistent approach has meant that a fair, objective comparison between VSC control strategies has so far been impractical. Power network operators do not have the tools to make an informed choice to select the best control strategy for their system parameters and performance requirements. In addition, power grid-connected converter designers cannot fairly evaluate their work against the current industry standard or quantify the full strengths and weaknesses of a given strategy.

This paper proposes a novel standardized assessment framework for all VSC controllers. The evaluation procedure can be applied to analytical converter-controller models at the design stage or to real grid-connected converters already implemented in operation. Three stages of assessment are used to evaluate: 1) the effect of controller tunings and bandwidths across a broad range of operating points, 2) the controller performance in the time-domain and 3) the controller stability in the frequency-domain. Multiple paths through the framework are provided to accommodate designers (with a full knowledge of the analytical equations behind the system) and operators (with unmodifiable, 'black box' systems), alike. In this work, small-signal modelling, time-domain MATLAB/Simulink simulations and control hardware-in-the-loop (CHIL) Real Time Digital Simulation (RTDS) experiments are all used in order to demonstrate that converter-controller systems at any level of implementation can be assessed using this framework. This framework thus provides a standardized objective method for assessing any new or existing VSC control strategy. The metrics produced at each stage are easily comparable and the modular design of the framework means that each stage can be used as a standalone evaluation criterion if required. This comprehensive approach unifies the numerous tests that are used to assess VSC control strategies and thus provides a consistent benchmark to which all new control strategies can be easily compared.

II. VSC STANDARDIZED ASSESSMENT FRAMEWORK

The flowchart of the proposed assessment framework is shown in Figure 1. There are 3 possible paths through the framework, which depend on the objectives of the user. In the case of controller designer, the full analytical model of the controller-under-test is known, and therefore assessment should include a tuning and bandwidth assessment and any frequency-domain analysis can make use of the analytical model. The objective in the designer case is to compare the performance of a novel controller to existing methods or to compare multiple strategies in order to select the most appropriate controller for a given system. However, in the case of a system operator, the controller-under-test is much closer to a 'black box', with the exact structure unknown. The operator may be provided with some controller parameters to modify and tune, but in other instances the converter-controller may be completely hidden such that no tuning changes can be made. The objective in the operator case is to assess the performance of the controller in the grid system for which it is intended, either in the fixed, pre-tuned state or with a tuning and bandwidth assessment included. Whether or not tuning can be performed, any frequency domain analysis in the operator case will require frequency scanning as the full analytical model remains unknown. In the following sections,

the operator case with fixed tuning will be known as case (a), the operator case with modifiable tuning is case (b) and finally the designer case will be known as case (c).

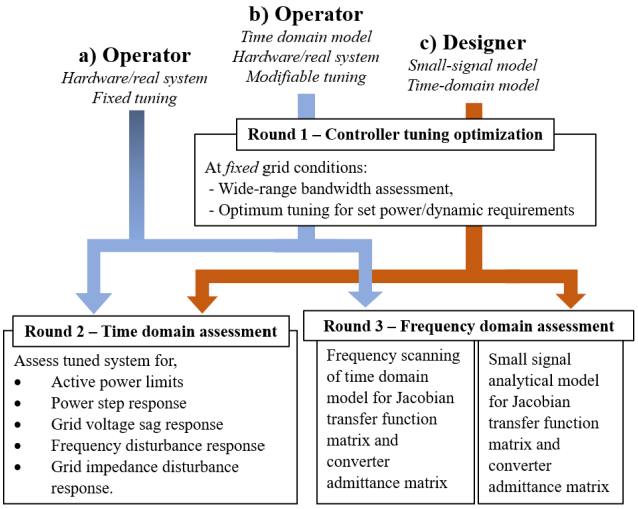

FIGURE 1. Flowchart of assessment steps in the proposed VSC control standardized assessment framework.

A. ROUND 1–CONTROLLER TUNING OPTIMIZATION

The first stage of the assessment procedure is applied in cases (b) and (c) only, i.e. for operators with an unknown but tunable controller, and for designers. The goal of this stage is to perform an assessment of controller performance across a wide range of controller bandwidths in order to find the optimum tunings as defined by a given set of active power transfer and dynamic performance requirements. This provides the feasible tuning and bandwidth ranges of the controller-under-test that can be implemented to meet the operational requirements. The tuning step is performed by examining stability and dynamic performance at a wide range of controller parameters. This process does not require knowledge of the converter-controller analytical model as the stability and step response data can be gathered from either a 'black box' time-domain model or a small-signal analytical model.

B. ROUND 2–TIME-DOMAIN PERFORMANCE ASSESSMENT

This stage of the framework is applied by operators and designers in all cases. A set of 5 standardized tests are performed in the time-domain on the AC grid-connected converter-controller system. These tests inform the power limits, dynamic performance, robustness and frequency response of the tuned controller, and are detailed in Table 1. Grid parameters are held constant in all cases except during test 4, which requires a step change in grid impedance.

C. ROUND 3–FREQUENCY-DOMAIN ASSESSMENT

This stage of the framework can also be applied by operators and designers in all cases, but the process of extracting the frequency domain data is case-dependent. In case (a) and (b) where the controller structure is unknown, frequency scanning must be performed to extract the Jacobian transfer function matrix and the converter admittance matrix. In case (c), the analytical model of the converter-controller is known and so these matrices can be derived directly from the state space or impedance small-signal models.

TABLE 1. Time-domain assessment test descriptions.

Test	Description	Result(s)/metric(s)
1	Active power reference ramp (-1 p.u. to 1.0 p.u.)	Bidirectional active power limits, tracking errors
2	0.1 p.u. step change in active power reference at P = -0.9 p.u., U = 1.0 p.u.	Settling times, overshoots
3	25% voltage sag at the AC grid (U_g) for 500 ms	Settling times, overshoots
4	1.0 p.u. step changes in SCR of AC grid at P = -0.9 p.u. (SCR 1 → SCR 2 → SCR 3)	Stability, overvoltage
5	1 Hz step change in grid frequency at P = -0.9 p.u.	Stability, inertia provided, overvoltage

III. CONTROLLERS UNDER TEST

The proposed framework can be used to assess any VSC controller. In this section, its flexibility will be demonstrated by evaluating the performance of three common VSC controllers with distinct structures, namely:

1. Standard vector current control (VCC)
2. Power-synchronization control (PSC)
3. Virtual synchronous machine (VSM)

Each controller is modelled in the time-domain (using MATLAB/Simulink) with small-signal analytical models and control hardware-in-loop RTDS experiments. This allows each controller to be treated as if it belongs to any of the three operator/designer cases in the proposed framework. A brief description of each controller is presented in this section, with further details and derivations of the linearized models available in [4], [23], [24]. The same AC grid system is used for all controllers under test and is shown in Figure 2. The Thevenin-equivalent AC grid resistance and impedance are R_g and L_g, the ac filter resistance and impedance are R_c and L_c, the converter voltage and current are U_c and I_c, the ac filter bus voltage is U_f, and the grid voltage and current are U_g and I_g. The ac system parameters are given in the Appendix.

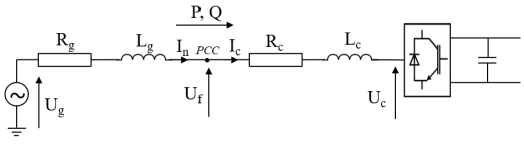

FIGURE 2. AC Grid-connected converter system under test.

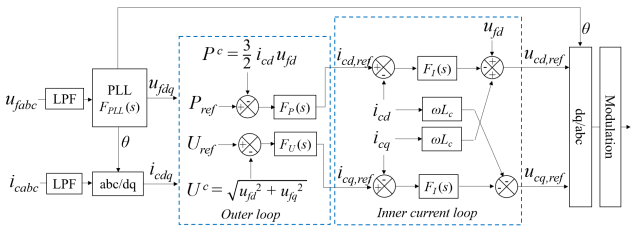

FIGURE 3. VCC control structure.

A. VECTOR CURRENT CONTROL

The VCC strategy is implemented in the dq-frame with outer loop active power, ac voltage control and inner loop current control. This control structure is shown in Figure 3.

PI controllers are used for the PLL, active power control, ac voltage control and current control. Their transfer functions are $F_{PLL}(s)$, $F_P(s)$, $F_U(s)$ and $F_I(s)$, respectively, in Fig. 3. A fast current loop is generally considered essential for stable VCC and so these gains are held fixed throughout the study. During the tuning assessment in Round 1, the proportional gains of the active power and ac voltage controllers (k_{p-P} and k_{p-U} respectively) are held constant whilst the integral gains (k_{i-P} and k_{i-U} respectively) are varied so as to vary the bandwidth of each loop. The PLL bandwidth is set directly using the proportional and integral gains according to (1).

$$\tau_{pll} = \frac{2\xi}{\omega_{pll}}, \quad k_{p-pll} = \frac{2\xi\omega_{pll}}{u_{fd0}}, \quad k_{i-pll} = \frac{k_{p-pll}}{\tau_{pll}} \tag{1}$$

Remaining gain values that are held fixed are detailed in Table 5 in the Appendix. The small-signal model for VCC is fully derived in [4] and the validation of the small-signal model used in the analysis is shown in Fig. 6(a) by comparison with the time-domain MATLAB/Simulink model.

B. POWER-SYNCHRONIZATION CONTROL

The PSC strategy uses first order control of the active power error for synchronization and control of active power. This control structure is shown in Figure 4 and developed in full in [23], where the detailed small-signal model is also given. In fault conditions, a back-up PLL and current controller are employed to limit the converter current. Fault conditions are outside the scope of this paper and so, for clarity, these elements are not shown. For the Round 1 tuning optimization, the integral gains k_p and k_u of the power-synchronization and voltage control loops are varied to change the bandwidth of the respective loops. The high-pass filter gain, k_v, is also varied to investigate the effect on stability. The remaining gain values are fixed at the values given in Table 5 in the Appendix. Validation of the PSC small-signal model is shown in Fig. 6(b) by comparison with the time domain MATLAB/Simulink model.

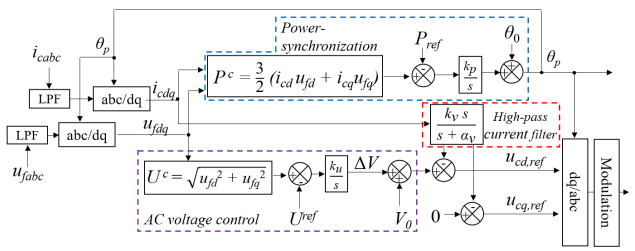

FIGURE 4. PSC control structure.

C. VIRTUAL SYNCHRONOUS MACHINE

A simple VSM controller is employed, implementing the second order swing equation for the active power control and synchronization, and a PI controller for the ac voltage control. This control structure is shown in Figure 5.

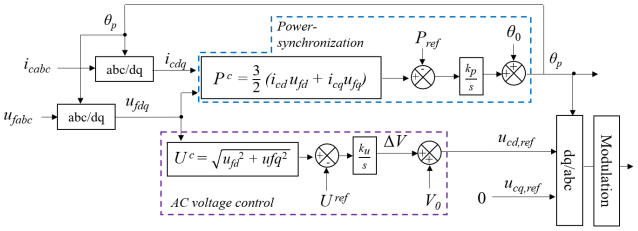

FIGURE 5. VSM control structure.

As with the VCC strategy, the proportional gain (k_{p-Uv}) of the ac voltage gain is held fixed so that variation of the integral gain (k_{i-Uv}) can be used to control the bandwidth of this loop. Tuning of the PI controller for synchronization and active power control is much more sensitive than the ac voltage control, and so both the proportional and integral gains of the active power control (k_{p-Pv} and k_{i-Pv} respectively) are varied in Round 1 tuning stage. All fixed gain values are given in Table 5 in the Appendix. The small-signal model for VSM is adapted from the PSC model in [23] but with slightly modified power synchronization and voltage control blocks. The power control and reference angle generation is described in (2)-(6).

$$\Delta\dot{x}_P = B_P\Delta u_P \tag{2}$$

$$\Delta y_P = C_P\Delta x_P + D_P\Delta u_P \tag{3}$$

where the input and output vectors are $\Delta u_P = [\Delta P^c_{ref}\ \Delta P^{cf}\ \Delta f_{P,ref}]^{\mathrm{T}}$ and $\Delta y_P = \Delta f_P$ respectively. The corresponding state-space matrices are,

$$B_P = \begin{bmatrix} -1 & 1 & 0 \end{bmatrix} \tag{4}$$

$$C_P = \frac{k_{i-Pv}}{S_{base}} \tag{5}$$

$$D_P = \frac{1}{S_{base}}\begin{bmatrix} -k_{p-Pv} & k_{p-Pv} & 1 \end{bmatrix} \tag{6}$$

The small-signal voltage reference control is given in (7)-(11).

$$\Delta\dot{x}_U = B_U\Delta u_U \tag{7}$$

$$\Delta y_U = C_U\Delta x_U + D_U\Delta u_U \tag{8}$$

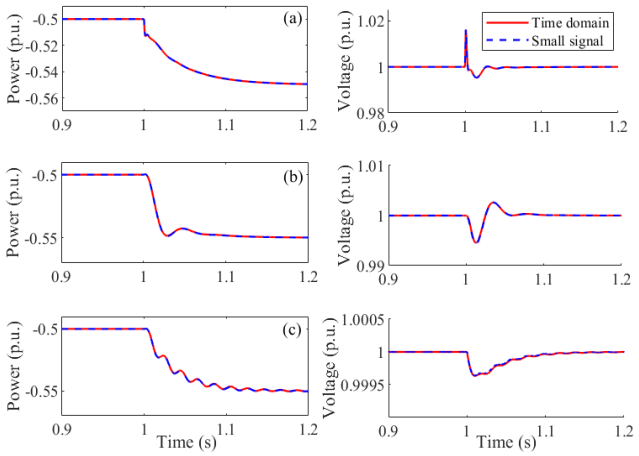

FIGURE 6. Validation of (a) VCC, (b) PSC and (c) VSM control small-signal models for a 0.05 p.u. step change in active power demand.

where the input and output vectors are $\Delta u_U = [\Delta U^c_{ref} \Delta U^{cf}]^{\mathrm{T}}$ and $\Delta y_U = [\Delta u^c_{cd} \quad \Delta u^c_{cq}]^{\mathrm{T}}$ respectively. The corresponding state-space matrices are,

$$B_U = \begin{bmatrix} 1 & -1 \end{bmatrix} \tag{9}$$

$$C_U = \begin{bmatrix} k_{i-Uv} & 0 \end{bmatrix}^{\mathrm{T}} \tag{10}$$

$$D_U = \begin{bmatrix} k_{p-Uv} & -k_{p-Uv} \\ 0 & 0 \end{bmatrix} \tag{11}$$

Validation of the VSM small-signal model by comparison with the time-domain Simulink model is shown in Fig. 6(c).

IV. ASSESSMENT RESULTS

A. ROUND 1–CONTROLLER TUNING OPTIMIZATION

For the demonstration in this paper, the small-signal models were used to gather Round 1 tuning results for expediency. The goal is to assess the effect of the bandwidth (i.e. the ±3 dB bandwidth) of each controller element on stability. However, there is significant cross-coupling between the d- and q-axes in weak AC grid-connected VSC systems, and so the tuning parameters of individual loops cannot usually directly determine the loop bandwidth. Therefore, a set of controller gains are used as proxies for the bandwidth of each control loop. The parameters varied and the ranges covered in this assessment are given in Table 2, with an approximate indication of the relevant bandwidth range covered. For each controller, the three associated parameters listed in Table 2 are varied simultaneously across the whole range. The small-signal stability and dynamic response to a step change in active power demand at $P = -1.0$ p.u. and $P = 0.89$ p.u. (i.e. just below the theoretical limit of an SCR = 1 grid, as calculated in [10]) are measured at each distinct operating point. This produces a 3D volume which represents all the controller tunings that provide stability and a specified level of dynamic performance within these power limits. For this example, stable operating regions are presented which show the controller tuning parameter space that ensures stability and the following minimum requirements of dynamic performance:

1) 2% settling time (ST) < 5 s, overshoot (OS) < 50%
2) 2% settling time (ST) < 1 s, overshoot (OS) < 20%
3) 2% settling time (ST) < 0.5s, overshoot (OS) < 15%

The stability regions representing these points for the VCC, PSC and VSM controllers are shown in Figure 7, Figure 8 and

TABLE 2. Parameter and bandwidth ranges for round 1 assessment.

	Parameter	Range	Equivalent bandwidth range
VCC	τ_{pll} (s/rad)	0.0045 – 0.45	ω_{pll} = 0.5 – 50 Hz
	$k_{i\text{-}P}$	10^{-4} – 10^{-2}	$\omega_P \approx$ 2.5 – 480 Hz
	$k_{i\text{-}U}$	0.03 – 30	$\omega_U \approx$ 0.5 – 230 Hz
PSC	k_p	0.5 x 10^{-7} – 15 x 10^{-7}	$\omega_P \approx$ 0.5 – 100 Hz
	k_u	0.1 – 1000	$\omega_U \approx$ 0.02 – 50 Hz
	k_v	0 – 500	-
VSM	$k_{p\text{-}Pv}$	0.1 – 20	$\omega_P \approx$ 0.1 – 60 Hz
	$k_{i\text{-}Pv}$	0.1 – 4000	
	$k_{i\text{-}Uv}$	0.01 – 1000	$\omega_U \approx$ 0.02 –100 Hz

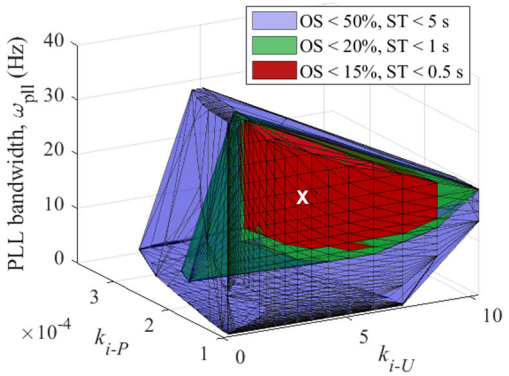

FIGURE 7. Stability bubbles for VCC with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

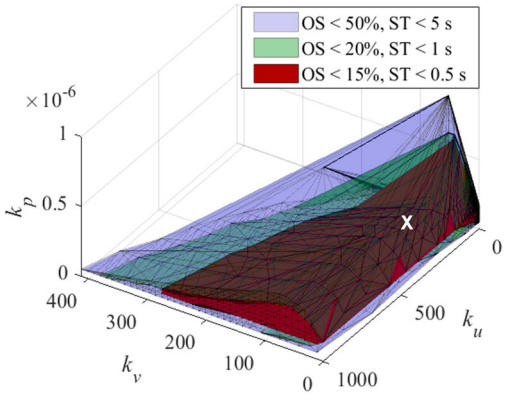

FIGURE 8. Stability bubbles for PSC with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

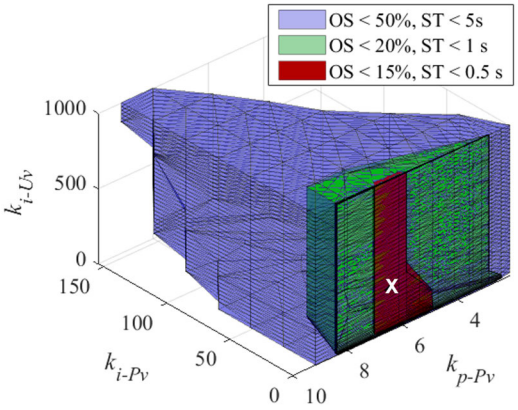

FIGURE 9. Stability bubbles for VSM with poor dynamic performance (blue), moderate dynamic performance (green) and good dynamic performance (red).

TABLE 3. Round 1 results–optimum controller tunings.

Control	Optimum tuning
VCC	$\omega_{pll} = 22.8$ Hz, $k_{i\text{-}P} = 1.1 \times 10^{-4}$, $k_{i\text{-}U} = 3.88$
PSC	$k_p = 1.69 \times 10^{-7}$, $k_u = 394.78 \cdot k_v = 91.2$
VSM	$k_{i\text{-}Uv} = 321.6$, $k_{p\text{-}Pv} = 5.880$, $k_{i\text{-}Pv} = 0.4826$

Figure 9, respectively. The optimum tuning for each controller is then calculated as the 'center of gravity' of the innermost stability bubble (i.e. the center point of the bubble with the best dynamic performance). These tuning points meet all the stability and dynamic performance requirements and have the greatest stable operating space around them, which provides maximum robustness against tuning errors. These points are also marked on Figure 7, Figure 8 and Figure 9 and detailed in Table 3. The optimum tunings constitute the results from Round 1 of the assessment and the controller parameters will be fixed at these values in Rounds 2 and 3. If an alternative tuning procedure is required for a specific application, this can be used in place of Round 1 without affecting the rest of the framework steps.

B. ROUND 2–TIME-DOMAIN ASSESSMENT

The performance of each controller in the time-domain can be analyzed using the tests described in Table 1. For this demonstration, the results from Round 1 are used to tune each controller and the five time-domain tests are executed using control hardware-in-the-loop (CHiL) RTDS experiments. The test set-up of the RTDS and microcontroller for this stage are shown in Figure 10. A Texas Instruments C2000 microcontroller is connected to the RTDS with an identical interface as would be used to connect to the grid, and the system is controlled in RSCAD and Simulink/C++. This stage of assessment can also easily be performed with a simple time-domain simulation, a small-signal model, or the

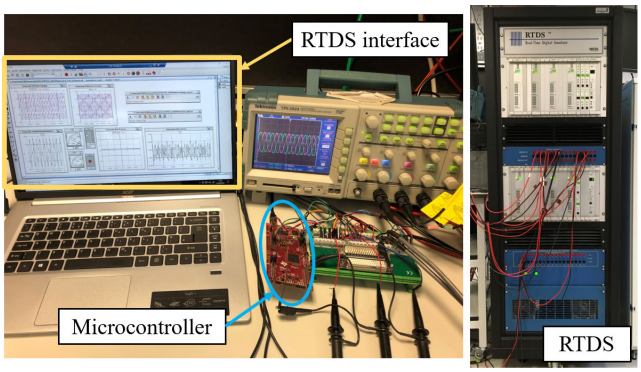

FIGURE 10. Experimental set-up for RTDS and control hardware-in-the-loop testing.

experimental set-up demonstrated here. Pre-tuned controllers can also be tested at this stage without performing the Round 1 tuning assessment.

1) TEST 1–ACTIVE POWER RAMP

Active power demand ramps at 0.5 p.u./s are applied in both inverting and rectifying mode to determine the power transfer limits of each controller with SCR = 1 and the voltage deviation during the ramp. In inverting mode, the power demand reaches 1.0 p.u. but in rectifying mode the active power ramp stops at 0.80 p.u. so as to stay within the converter rating limits. The CHiL experimental results for this test on each controller are shown in Figure 11 and Figure 12. All three controllers can achieve the theoretical active power transfer limits in both inverting and rectifying modes. The VSM is the slowest controller, but all three controllers have a similar power tracking error throughout the ramp and show good voltage support.

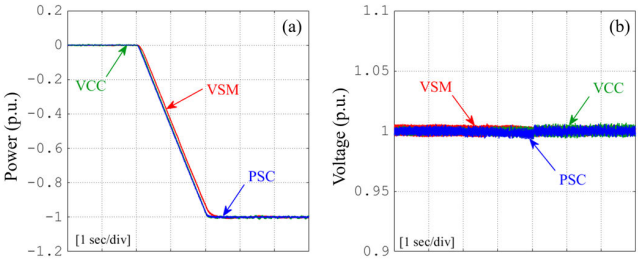

FIGURE 11. CHiL experimental results with an inverting ramp: (a) active power and (b) PCC voltage magnitude, VCC (green), PSC (blue) and VSM control (red).

2) TEST 2–ACTIVE POWER DEMAND STEP

A step of 0.1 p.u. is applied to the active power reference at $P = -0.9$ p.u. to reach rated active power injection. The CHiL experimental results for this test are shown in Figure 11 and Figure 12. All three controllers show a good dynamic power response, but the VCC and PSC have an obvious voltage undershoot due to stronger coupling between the power reference and the PCC voltage (discussed further

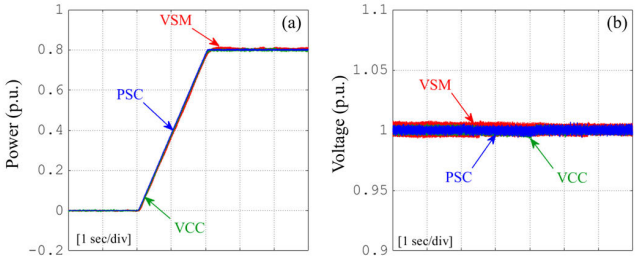

FIGURE 12. CHiL experimental results with a rectifying ramp: (a) active power and (b) PCC voltage magnitude, VCC (green), PSC (blue) and VSM control (red).

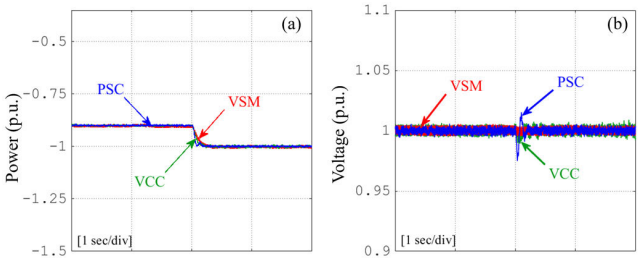

FIGURE 13. CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a step change of 0.1 p.u. in active power demand at $P = -0.9$ p.u., $U = 1.0$ p.u. with VCC (green), PSC (blue) and VSM control (red).

in Section IV.C). The VSM has a slower response than PSC or VCC, but the voltage support during the power step is excellent. Both VSM and PSC exhibit slight non-minimum phase behavior in the power response.

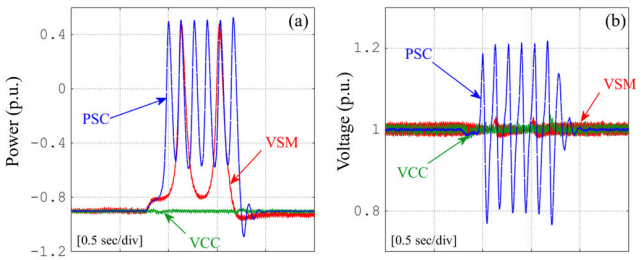

FIGURE 14. CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a 25% voltage sag in AC grid voltage (U_g) with 500 ms at $P = -0.9$ p.u. for VCC (green), PSC (blue) and VSM control (red).

3) TEST 3–AC GRID VOLTAGE SAG

For this test, a 25% voltage sag, lasting 500 ms, is applied to the grid voltage (U_g). Before the event, the system in inverting 0.9 p.u. active power. The control performance is measured according to the system stability both during the sag event and after it is cleared, and the overall voltage deviation at the PCC. The CHiL experimental results for this test are shown in Figure 14. As expected, the VCC performs best under such sag conditions due to the inherent current limiting capability of the controller. Although the VSM and PSC-controlled systems are able to recover stability and reference power transfer once the sag is cleared, there is an unacceptable power oscillations during the sag event. Under PSC, the PCC voltage is also highly oscillatory during the sag, but the VSM provides much better voltage support. This difference in voltage stability between the two grid-forming controllers is largely influenced by the coupling between power and voltage under PSC. Figure 15 shows the system frequency response from P to U_f with PSC and VSM controllers. The gain margin of PSC is much smaller than that of VSM, indicating stronger coupling between P and U_f and reduced voltage stability when the power is perturbed.

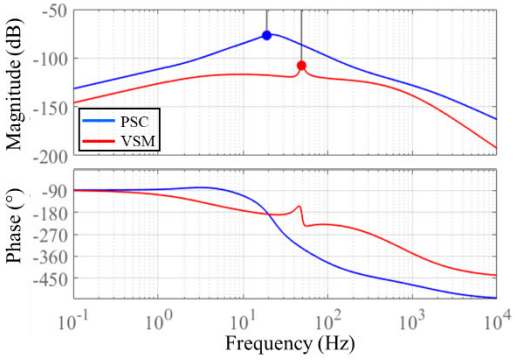

FIGURE 15. Frequency response from active power, P, to PCC voltage magnitude, U_f, for PSC (blue) and VSM control (red).

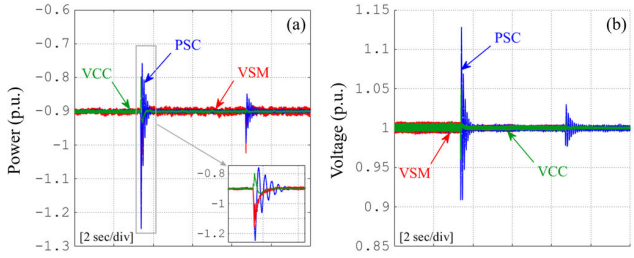

FIGURE 16. CHiL experimental results: (a) active power and (b) PCC voltage magnitude to step changes in grid SCR from SCR = 1 to SCR = 2 and from SCR = 2 to SCR = 3 with VCC (green), PSC (blue) and VSM control (red).

4) TEST 4–GRID IMPEDANCE STEP

A step change in grid impedance is performed such that the AC grid changes from SCR = 1 to SCR = 2, is allowed to settle for 5 s, and then changes from SCR = 2 to SCR = 3. The CHiL experimental results for this test are shown in Figure 16. All three control strategies maintain stability and power tracking at the impedance step changes. However, the PSC and VSM show large transitory power oscillations, with a similar maximum power overshoot (the inset of Figure 16(a) shows a close-up view of this power transient with the VSM trace brought to the front of the scope). These temporary power fluctuations could cause instability if there are any errors at all in the parameters used to tune the system. PSC also shows a significant voltage oscillation at each impedance change, which could lead to voltage collapse if any system parameters

have not been accurately quantified. After the initial transients, the steady- state performance of VCC and PSC appears unchanged as the grid is strengthened, but the power quality of the VSM deteriorates as the SCR is increased, i.e. the VSM appears to become less stable as the grid strength increases.

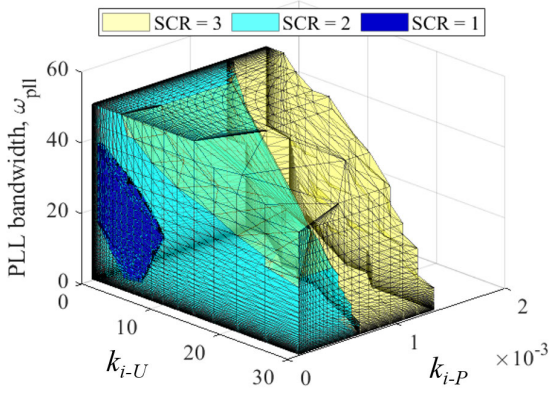

FIGURE 17. Stable operating region for moderate dynamic performance with VCC at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

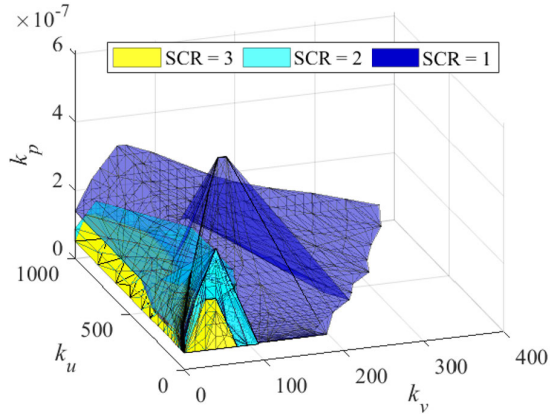

FIGURE 18. Stable operating region for moderate dynamic performance with PSC at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

The decreased stability of VSM at higher grid SCR may be addressed by retuning the controller, but effective control is therefore dependent on regular, accurate impedance estimation. Conversely, for the VCC system, the weakest grid is the limiting condition for tuning the controller, so stability in a SCR = 1 (or weaker) grid is sufficient to ensure stability at higher SCRs. This is demonstrated by the stable tuning regions for moderate dynamic performance (OS < 20%, ST < 1s, as in Section IV.A) at different grid SCRs, shown in Figure 17, Figure 18 and Figure 19. With VCC control, Figure 17 shows that increasing the grid SCR increases the size of the stability region in all directions. The same comparison is made for PSC in Figure 18, which shows that there is a large region of overlap between the stable operating regions at different grid strengths, but none of the regions are perfectly coincident. The overlap region is even smaller for VSM control, as shown in Figure 19. This means that

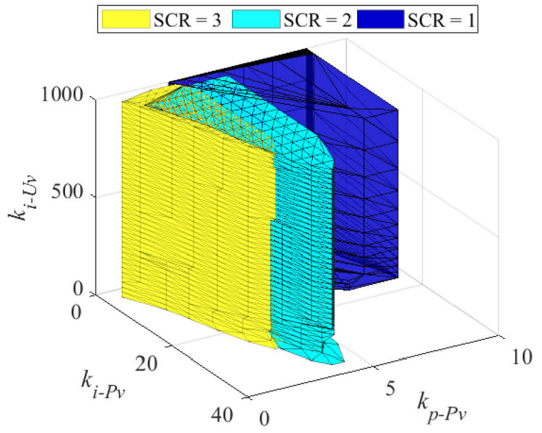

FIGURE 19. Stable operating region for moderate dynamic performance with VSM control at SCR = 3 (yellow), SCR = 2 (cyan) and SCR = 1 (blue).

stability must be verified under every possible grid condition if employing PSC or VSM control in a variable grid; no single set of grid parameters can be guaranteed to be the limiting condition. If VCC is employed, tuning only needs to be performed at the weakest possible grid setting.

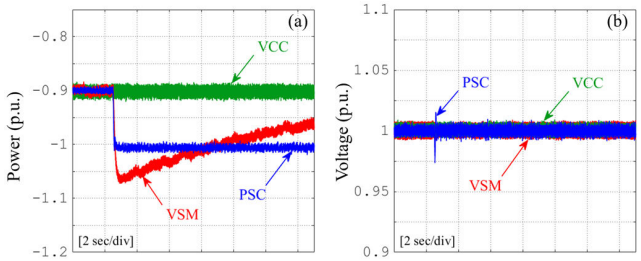

FIGURE 20. CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a 1 Hz drop in AC grid frequency and 0.25 Hz/s recovery with VCC (green), PSC (blue) and VSM control (red).

5) TEST 5–GRID FREQUENCY DROP

To test the inertial response of the three controllers, a frequency drop of 1 Hz is applied to the AC grid. Before the frequency event, the converter is injecting 0.9 p.u. active power into the grid. The CHiL results for this test are shown in Figure 20. It can be seen that the VCC grid-following control successfully maintains the active power demand during the frequency event but does not provide any additional power injection into the grid to respond to the frequency drop. However, good voltage and power support is provided throughout. The VSM provides an inertia-emulating response by injecting an extra 0.075 p.u. active power into the grid at the frequency event and then returning eventually to the original, pre-event power level. The PSC also injects additional active power, but at a constant value throughout the period of the frequency event due to the inherent droop behavior. The PSC also shows a small voltage oscillation (related to the coupling discussed in Figure 15) that is not seen with VSM or VCC.

C. ROUND 3–FREQUENCY-DOMAIN ASSESSMENT

1) IMPEDANCE TRANSFER FUNCTION MATRIX

The most common and established form of frequency-domain assessment for AC grid-connected VSCs is the admittance-impedance model. As discussed in Section II.C, the impedance of the converter-controller can be generated via frequency scanning (in cases (a) and (b)) or using the full analytical model (in case (c)). For this comparison, the converter impedances are extracted from the small-signal models introduced in Section III and further details of impedance modelling for the respective controllers can be found in [25]–[27]. The converter and grid are represented as a current source in parallel with a Norton-equivalent impedance, $\mathbf{Z_c}(s)$, and a voltage source in series with a Thevenin-equivalent impedance, $\mathbf{Z_g}(\omega_g, 's)$, respectively, as shown in Figure 21, where ω_g is the nominal grid frequency [25].

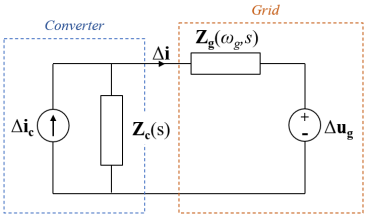

FIGURE 21. Equivalent circuit diagram of the system impedance model.

The bode plots of the $\mathbf{Z_c}(s)$ impedance matrix in the dq-frame for each controller at SCR $= 1$, $P = -1.0$ p.u. are shown in Figure 22, along with the grid impedance frequency response. Stability of the system is governed by the ratio of $\mathbf{Z_g}(s)/\mathbf{Z_c}(s)$, which can be interpreted graphically to a certain extent by the phase margin where the magnitudes of $\mathbf{Z_c}(s)$ and $\mathbf{Z_g}(s)$ intersect [25]. It can be seen that this intersection occurs at a higher frequency for VCC than for the other two controllers, where greater phase loss has occurred and so the phase margin is correspondingly smaller. Figure 22(b) and (c) also show that the off-diagonal impedances of VCC are higher than either PSC or VSM at high frequencies, implying stronger cross-coupling between the converter voltages and currents at high frequencies. The assumptions made for VCC in strong grids of independent power and voltage control therefore cannot be applied in these operating conditions. The VSM shows a resonance at the grid frequency (50 Hz), which is far less prominent in either PSC or VCC control. This resonance may cause oscillations if additional damping is not employed.

2) JACOBIAN TRANSFER FUNCTION MATRIX

The Jacobian transfer function matrix, $\mathbf{J}(s)$, of the controlled, AC grid-connected converter system is defined as:

$$\begin{bmatrix} \Delta P \\ \Delta U \end{bmatrix} = \underbrace{\begin{bmatrix} J_{P_{ref}P}(s) & J_{U_{ref}P}(s) \\ J_{UP_{ref}}(s) & J_{UU_{ref}P}(s) \end{bmatrix}}_{\mathbf{J}} \begin{bmatrix} \Delta P_{ref} \\ \Delta U_{ref} \end{bmatrix} \quad (12)$$

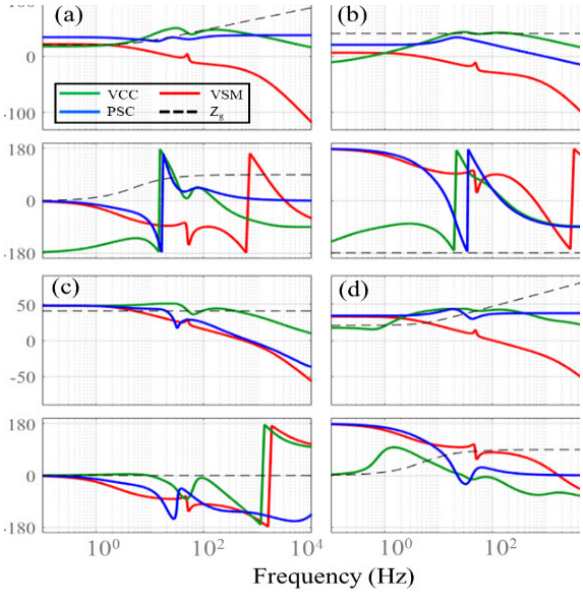

FIGURE 22. Bode plots of the converter impedances, $\mathbf{Z_c}$ (s), for VCC (green), PSC (blue) and VSM control (red) in a SCR = 1 grid with impedance $\mathbf{Z_g}$ (s): (a) from i_{cd} to u_{fd} (b) from i_{cq} to u_{fd} (c) from i_{cd} to u_{fq} and (d) from i_{cq} to u_{fq}.

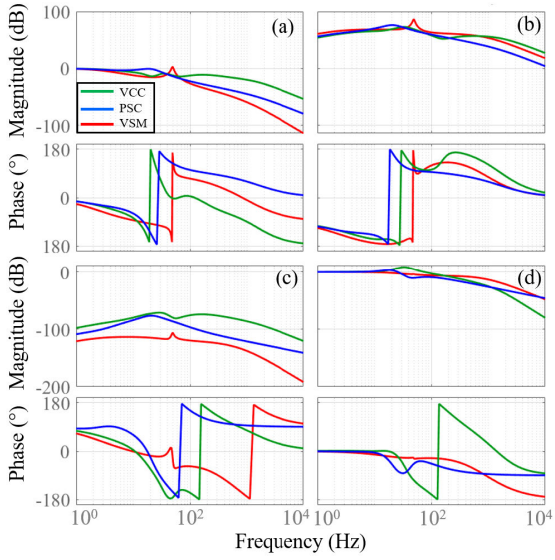

FIGURE 23. Bode plots of the Jacobian transfer function matrix for VCC (red), PSC (green) and VSM control (blue) in a SCR = 1 grid: (a) from P_{ref} to P, (b) from U_{ref} to P, (c) from P_{ref} to U and (d) from U_{ref} to U.

The Jacobian form is used in particular in [7], [23] for modelling PSC, but it can also be applied to any other VSC control strategy that employs active power and AC voltage control (the AC voltage control can also be substituted for reactive power control). This form of the system allows analysis of the upper level system coupling and the condition of the controlled process. Figure 23 shows the bode plots of the Jacobian transfer function matrix of each of the controllers under test. If the off-diagonal magnitudes exceed the diagonal

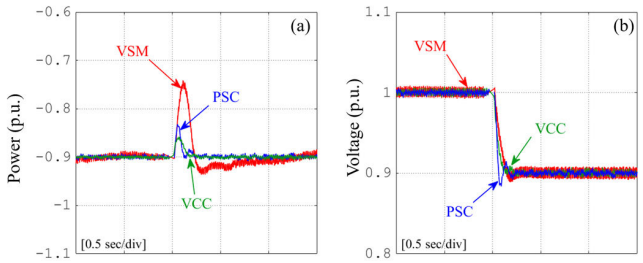

FIGURE 24. CHiL experimental results: (a) active power and (b) PCC voltage magnitude to a step change of 0.1 p.u. in voltage reference at $P = -0.9$ p.u., $U = 1.0$ p.u. with VCC (green), PSC (blue) and VSM control (red).

TABLE 4. Summary of inverter controller performance, SCR = 1.

	VCC	PSC	VSM
-1.0 < P < 0.89 p.u.	Yes	Yes	Yes
U_f support in power step	Good	Moderate	Good
U_f support in voltage sag	Good	Poor	Poor
Grid strength robustness	Good	Re-tune	Re-tune
Inertia emulation	No	Yes	Yes
PQ cross-coupling	Strong	Strong	Strong

magnitudes, the process is ill-conditioned [28] and this has a corresponding impact on the time-domain performance. For instance, it can be seen that the magnitude of $J_{U_{ref}P}(s)$ in Figure 23(b) is greater than the diagonal transfer functions for all three controllers, suggesting that the active power is strongly coupled to the AC voltage reference. This effect can be seen in the time-domain by performing a step change in AC voltage reference using the CHIL RTDS experimental set-up, as shown in Figure 24. Applying a 0.1 p.u. step change in U_{ref} produces a large deviation in P with all three control strategies. In contrast, the magnitudes of $J_{P_{ref}U}(s)$ in Figure 23(c) are smaller than the diagonal transfer functions and so the effect of a power reference change on the PCC voltage is much smaller, as was demonstrated by the power reference step in Figure 23. Again, the VSM shows a resonance at 50 Hz grid frequency.

D. COMPARISON BETWEEN THE THREE CONTROLLERS

The results of the standardized assessment framework for VCC, PSC and VSM in a very weak AC grid have revealed significant advantages and disadvantages of each strategy. Round 1 results show that all three controllers have a sufficient parameter space that can achieve stable operation with good dynamic performance between the theoretical limits of -1.0 p.u. and 0.89 p.u. active power transfer in a SCR $= 1$ AC grid. All three control strategies provide good voltage support and the same active power limits during a reference ramp. However, VSM control is slower than the other two control strategies. The VCC is the most robust to increases in grid strength (i.e. increase in SCR) without re-tuning. Though stable, the PSC exhibits large voltage and power oscillations during a grid parameter change and the VSM shows increasing oscillations in active power as the grid is strengthened. The PSC and VSM can inject additional active power to support the grid during frequency disturbances. Although the VCC does not offer inertia support, it shows good voltage support during frequency event and the active power is maintained at the reference level throughout. This comprehensive assessment suggests that VCC is the most robust choice for variable (or unknown) AC grid impedance systems, but independent active power and voltage control cannot be assumed in a very weak grid. For frequency support applications, the VSM or PSC strategies are preferable and, of these strategies, the VSM control provides better voltage support in a very weak grid. However, additional damping should be considered for VSM control. A summary of the performance of the VCC, PSC and VSM under this framework is given in Table 4.

VSC controllers with non-classical structures or additional complexity – such as model predictive control (MPC), passivity-based control and additional droop controls – can also be assessed using this framework. For these alternative controllers, the Round 2 (time-domain) and Round 3 (frequency-domain) assessments can be applied directly as described in Sections IV.B and IV.C, using either models or full hardware implementation. The optional Round 1 tuning stage should be adapted to include the most relevant additional controller parameters. For example, for MPC, the effect of the prediction horizon and choice of cost function on the stable controller operating space should be considered. In this case, multiple stable operating regions would be constructed during Round 1 with different baseline prediction algorithms. For droop-controlled VCC, the droop gain would be considered as an extra tuning variable in this step. The extension of this framework to controllers such as these will be investigated further in future work.

V. CONCLUSION

This paper has proposed a standardized assessment framework for performance analysis of any VSC controller at the design or implementation stage. The modular assessment format accommodates all controllers from analytical models at the design stage to pre-tuned 'black box' controllers installed in a real ac grid system. Three stages of assessment are proposed to perform tuning, time-domain and frequency-domain analyses. The first stage incorporates a tuning assessment across a much broader range of controller operating points and bandwidths than are usually considered and varies three controller parameters simultaneously to establish the safe operating region for that controller. Imposing dynamic performance constraints on this area of stable

operating points narrows down the stable region so that an optimum tuning point can be extracted. These tunings are carried forward to the second stage where control hardware-in-the-loop RTDS experiments have been performed to compare the active power limits, dynamic response to power and voltage changes, robustness to grid impedance and the frequency disturbance response. In the third stage, the Jacobian transfer function matrices and impedance matrices were extracted to compare cross-coupling, condition of the process and resonances. An example analysis of VCC, PSC and VSM control strategies using the proposed framework has shown that these control strategies offer comparable performance in steady-state, non-fault conditions, but the grid-forming controllers give a slower response. VCC is the most robust strategy for sag conditions or changes in grid impedance but demonstrates strong cross-coupling in the frequency domain.

APPENDIX

Rated AC grid voltage (RMS l-l) = 195 kV, rated AC grid power = 350 MW, AC grid frequency = 50 Hz, SCR = 1, X/R ratio = 10, ac grid inductance, Lg = 344 mH, ac grid resistance, Rg = 10.86 Ω, filter inductance, Lc = 69.2 mH, filter resistance, Rc = 1.09 Ω.

TABLE 5. Fixed controller gain values.

Controller	Parameter	Fixed
VCC	α_c (s)	0.0015
	$k_{p\text{-}P}$	1 x 10^{-6}
	$k_{p\text{-}U}$	2 x 10^{-2}
PSC	α_v (rad/s)	40
VSM	$k_{p\text{-}Uv}$	1

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