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Low-Frequency Converter-Driven Oscillations in Weak Grids: Explanation and Damping Improvement

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***Abstract*—Low-frequency oscillations have been reported in several weak-grids-connected voltage-source-converter(VSC) systems. Although efforts have been devoted to understand the parametric and sensitivity impact of the VSC controller gains, a general formulation of the oscillation mechanism is still missing. Using transfer function dynamic modelling approach, we find that the outer loop active power control's bandwidth mainly determines the oscillation frequency. The PLL introduces a large phase lag around the frequency of the PLL bandwidth in weak grids which decreases the oscillation damping. A simple but effective PI+Clegg integrator (CI) compensator is proposed to replace the standard outer loop active power controller compensating the PLL's phase delay and increase the oscillation damping. The results are verified in a real time digital simulator.**

***Index Terms*—Weak grids, low-frequency oscillations, oscillation damping.**

I. Introduction

WHEN voltage-source-converters (VSCs) are connected to weak grids, low-frequency oscillations have been reported, like 4 Hz oscillations in Texas [1] or 6 Hz oscillations in Type-4 wind turbines [2]. Fan *et al.* and Hu *et al.* investigated this phenomenon using eigenvalue and complex torque analysis [3]–[5] and revealed that the phase-locked loop (PLL)'s parameters are the critical factors that influence the oscillation damping. However, the exact determinant for the low-frequency oscillation mode and in-depth mechanism how the PLL affects the damping have not been clearly revealed.

According to the the authors' prior work [6], the transfer function model is simple as well as accurate to analyze the low-frequency oscillations of the weak-grids-connected VSC. Based on [6], we perform the oscillation frequency and damping analysis. It is found that the outer loop control bandwidth determines the oscillation frequency. The PLL parameters affect the oscillation damping by introducing a large phase lag around the frequency of PLL bandwidth in weak grids. To compensate the PLL's phase delay and increase the oscillation damping, a simple but effective outer loop PI+Clegg integrator (CI) reset compensator is proposed by resetting part of the integrator when the active power error signal is zero.

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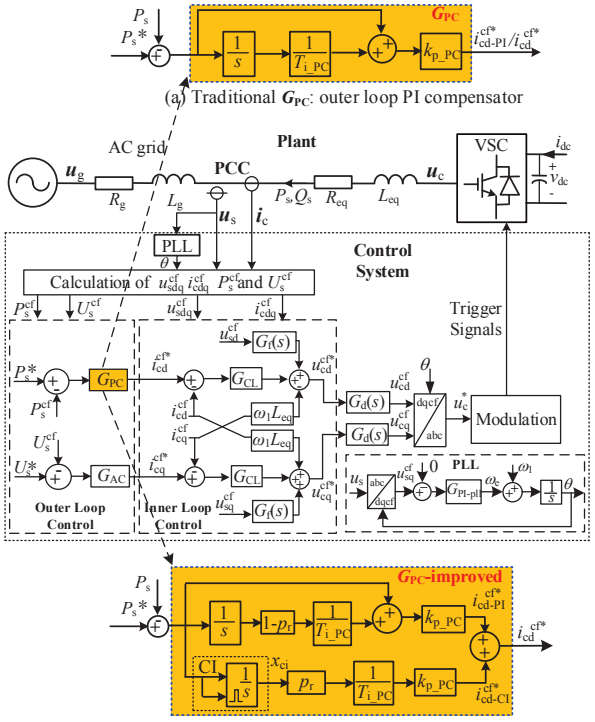

Fig. 1. A diagram of the weak-grids-connected VSC.

The proposed method is a generalized one to improve the low-frequency oscillation damping in the weak grids and can be easily implemented by adding a Clegg integrator to the standard PI without changing the converter control structure.

II. Dynamic Models

Fig. 1 presents the study system of the weak-grids-connected VSC where the system parameters are presented in Table I. The grid connected VSC can adopt active power control (for VSC-HVDC) or DC voltage control (for Type-4 wind). The active power control is adopted in this letter. Two dynamic models are built, one is the detailed time-domain simulation model built in the Matlab/simulink according to Fig. 1. The other is the single-input-single-output (SISO) model presented as follows,

$$G_{PC0}=\underbrace{\omega_{OL_PC}\frac{(sT_{i_PC}+1)}{s}}_{G_{PC0_1}}\underbrace{\frac{\frac{m}{1.5u_{sd0}}\left[s^2+\left(2\zeta\omega_{pll}s+\omega_{pll}^2\right)\frac{1+s(T_{eq_AC}+k_2)}{1+sT_{eq_AC}}\right]}{\left[s^2+\left(2\zeta\omega_{pll}s+\omega_{pll}^2\right)(k_1+1)\right]}}_{G_{PC0_2}},\tag{1}$$

where,

$$\begin{cases} T_{eq_AC}=T_{i_AC}+1/\omega_{OL_AC} \\ k_1=\frac{X_g i_{cq0}}{u_{sd0}}, k_1\in(-1,1) \\ k_2=\frac{1}{\omega_{OL_AC}}\frac{-1.5(i_{cd0}X_g)^2}{u_{sd0}m}<0 \end{cases}.\tag{2}$$

TABLE I
PARAMETERS OF THE VSC SYSTEM

Parameters	Unit	Value
Rated power/voltage	MW/kV	12/35
SCR,R_g,L_g,frequency	p.u.,Ω,mH,Hz	1.1, 0.928, 295.4,50
R_{eq},L_{eq}	Ω, mH	1.021, 65
ω_{pll},k_{p_pll},k_{i_pll}	rad/s, rad/(V · s), rad/(V · s^2)	$2\pi11$, 3.4×10^{-3}, 0.1672
ω_{OL_PC},k_{p_PC},k_{i_PC}	rad/s, A/W, A/(W · s)	$2\pi6$,1.12×10^{-6},8.79×10^{-4}
ω_{OL_AC},k_{p_AC},k_{i_AC}	rad/s, A/V, A/(V · s)	$2\pi6$, 5.17×10^{-4}, 0.41
ω_{CL}, k_{p_cl}, k_{i_cl}	rad/s, Ω, V/(A · s)	$2\pi125$, 51.04, 801.76
P_s,U_s	p.u., p.u.	1.0, 1.0
ζ	1	0.707

In (1) and (2), G_{PC0_1} corresponds to the outer loop active power control, G_{PC0_2} corresponds to the PLL, the AC voltage control, the AC system strength, and the active power, ω_{OL_PC} and T_{i_PC} are the active power control bandwidth and time constant, ω_{pll} and ζ are the PLL bandwidth and damping ratio, ω_{OL_AC} and T_{i_AC} are the AC voltage control bandwidth and time constant, T_{i_AC}=1/ω_{CL} and ω_{CL} is the bandwidth of the inner loop control. X_g is the grid impedance, i_{cd0} and u_{sd0} are the d-axis steady state current and voltage, $m \approx 1.5u_{sd0}$. More details regarding this model can be found in the authors' prior work [6].

III. Oscillation Frequency and Damping Analysis

The oscillation frequency of the closed loop system is analyzed in the ideal grid condition and weak grids condition by examining the gain-crossover frequency of the open-loop transfer function G_{PC0}, as they are close to each other when the oscillation is significant in practice. The PLL's phase delay in the weak-grids-connected VSC is revealed and its impact on the system damping is examined.

A. Oscillation Frequency and Damping in an Ideal-grid

In an ideal grid condition, the term G_{PC0_2}=1 due to X_g≈0, k_1≈0 and k_2≈0. Thus, $G_{PC0} = G_{PC0_1}$ satisfies. In the low-frequency range of $\omega < 1/T_{i_PC}$, the magnitude of G_{PC0} is

$$\mathrm{Lm}G_{PC0}(\omega)|_{\omega<\frac{1}{T_{i_PC}}} \approx 20\log_{10}\left(\frac{\omega_{OL_PC}}{\omega}\right). \quad (3)$$

By solving LmG_{PC0}=0, we have $\omega = \omega_{OL_PC}$, indicating that G_{PC0}'s gain-crossover frequency ω_c=ω_{OL_PC}. According to G_{PC0_1} in (1), its phase at ω_c=ω_{OL_PC} is about −90°. Thus, the gain-crossover frequency and phase margin of G_{PC0} are

$$\omega_c = \omega_{OL_PC}, \gamma_c \approx -90° - (-180°) = 90°, \quad (4)$$

where γ_c is the phase margin. Fig. 2(a) presents the Bode plots of G_{PC0_1} for different active power control bandwidths.

B. PLL's Phase Delay Effect in Weak grids

As the grid becomes getting weaker, G_{PC0_2} doesn't equal to 1 and has the representation of a notch filter. In the following, G_{PC0_2} magnitude-frequency and phase-frequency characteristics will be examined to evaluate how it will affect the gain-crossover frequency and the phase margin of G_{PC0} in weak grids. Fig. 2(b) presents the Bode plots of G_{PC0_2} with with PLL's bandwidth equalling to 10, 12, 14 and 16 Hz.

1) Magnitude-frequency characteristic: In the low frequency range of $\omega < \omega_{pll}$, the magnitude of G_{PC0_2} satisfies LmG_{PC0_2} ≈ 0dB.

2) Phase-frequency characteristic: Fig. 2(b) shows that G_{PC0_2} has a large phase delay and the corner frequency equals to PLL's bandwidth (denotes by ω_{pll}). Increasing the AC voltage control bandwidth can slow down the phase delay but will not change the trend. In Fig. 2(b), the phase starts from 0° and ends with −360° as it's a non-minimum-phase system in weak grids [6].

C. Impact of PLL's Phase Delay on the Oscillation

In weak grids, according to (1), we have

$$\begin{cases} \mathrm{Lm}G_{PC0} = \mathrm{Lm}G_{PC0_1} + \mathrm{Lm}G_{PC0_2} \\ \angle G_{PC0} = \angle G_{PC0_1} + \angle G_{PC0_2} \end{cases}. \quad (5)$$

Since LmG_{PC0_2} ≈ 0dB satisfies, the gain-crossover frequency of G_{PC0} is not affected by G_{PC0_2} and it still satisfies $\omega_c \approx \omega_{OL_PC}$. However, its phase margin will be affected by the phase delay effect of PLL. The phase delay at $\omega = \omega_{OL_PC}$ will decrease G_{PC0}'s phase margin and weaken the oscillation damping in weak grids especially if the active power control and the PLL bandwidths are not properly set.

Fig. 2(b) shows that a larger PLL bandwidth results in a smaller phase delay at $\omega = \omega_{OL_PC}$. Thus, a larger PLL bandwidth can help to improve the oscillation damping. However, the PLL bandwidth is usually set comparatively small to avoid interaction with the inner current loop [7].

Fig. 2(c) and Fig. 3 present the Bode plots and simulation results of G_{PC0} and with different PLL bandwidths at an active power control bandwidth of 6 Hz. We can see that at the gain-crossover frequency of $\omega = \omega_{OL_PC}$, a larger PLL bandwidth results in a smaller phase delay and a larger phase margin, which indicates effective oscillation damping in Fig. 3.

IV. Compensating the PLL's Phase Delay Effect to Improve the Oscillation Damping

The PLL's phase delay is mainly brought by right half-plane zeros [6] which is difficult to compensate with standard linear

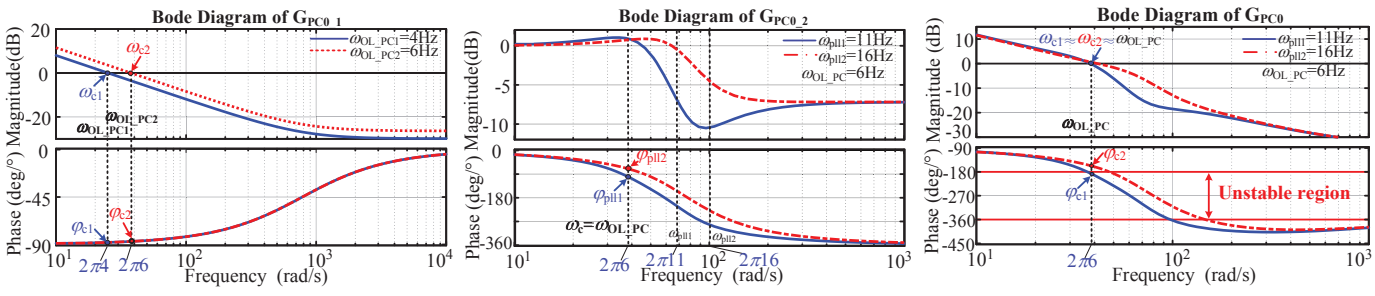

Fig. 2. Gain-crossover frequencies and phase margins on the bode plots of G_{PC0_1}, G_{PC0_2} and G_{PC0}: (a) G_{PC0_1} with active power control bandwidths being 4 and 6 Hz, (b) PLL's phase delay effect: G_{PC0_2} with PLL bandwidths being 11 and 16 Hz, (c) G_{PC0} with PLL bandwidths being 11 and 16 Hz.

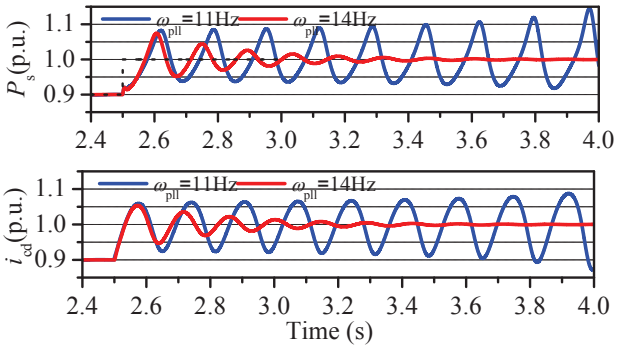

Fig. 3. Simulation results with PLL bandwidth being 11 and 14 Hz.

lead-lag or PI. We can use a PI+CI active power controller to compensate the PLL's phase delay and increase the oscillation damping in weak grids. Moreover, the modification required to the control structure is minimum with PI+CI controller.

A. Design of PI+Clegg Integrator Reset Compensator

The reset control was proposed by J. Clegg to improve the performance of the integrator [8]. It is a strategy that resets the controller state (or part of it) to zero when some condition holds, which can reduce the phase lag. Hence, we propose to use the PI+Clegg Integrator reset compensator in replace of the standard PI in the outer loop active power control to compensate PLL's phase delay, as shown in Fig. 1. The CI reset compensator can be described by

$$\begin{cases} \dot{x}_{ci}(t) = \Delta P_s(t), \text{if} \Delta P_s(t) \neq 0 \\ x_{ci}(t^+) = 0, \text{if} \Delta P_s(t) = 0 \end{cases}. \tag{6}$$

The transfer functions of the PI and PI+CI can be derived as

$$\begin{cases} G_{PC-PI} = k_{p_PC}\left(1 + \frac{1}{sT_{i_PC}}\right) \\ G_{PC-PI+CI} = k_{p_PC}\left(1 + \frac{1}{sT_{i_PC}} + \frac{j4p_r/\pi}{sT_{i_PC}}\right) \end{cases}, \tag{7}$$

where p_r is a parameter to tune the reset rate, and $0 \le p_r \le 1$ [8]. The reset control devolves into a PI controller when p_r = 0, and devolves into a Clegg integrator when p_r = 1. Using the outer loop PI+CI reset compensator, the G_{PC0_1} in (1) can be modified to

$$G_{PC0_1} = \frac{\omega_{OL_PC}(sT_{i_PC}+1+j4p_r/\pi)}{s}. \tag{8}$$

B. Bode Plots Based Parameter Tuning and Verification

In the design the PI parameters for the proposed PI+CI controller, the CI controller parameter p_r will firstly be set to 0 to disable the CI controller. Then, the traditional outer loop PI tuning methods can be used to design the PI parameters. Using the analysis in Sec.III, the PI adopts a 6 Hz bandwidth. When the PI controller parameters are selected, the CI controller parameter p_r can be tuned according to the Bode plots analysis and the sensitivity analysis as shown in Fig. 4.

Fig. 4 presents the the Bode plots of G_{PC0_1} and G_{PC0} when outer loop adopts the PI+CI compensator with $p_r = 0, 0.5$. It shows that the proposed compensator increases the phase delay of G_{PC0_1} significantly while slightly influences the gain-crossover frequency. The phase delay of G_{PC0_1} is decreased approximately from −90° to −50° when p_r = 0.5. Fig. 4 shows that G_{PC0}'s phase margin is increased from negative values to positive values when p_r = 0.3 and 0.5, which verifies the effectiveness of the PI+CI reset compensator in improving the phase margin of the weak-grids-connected VSC.

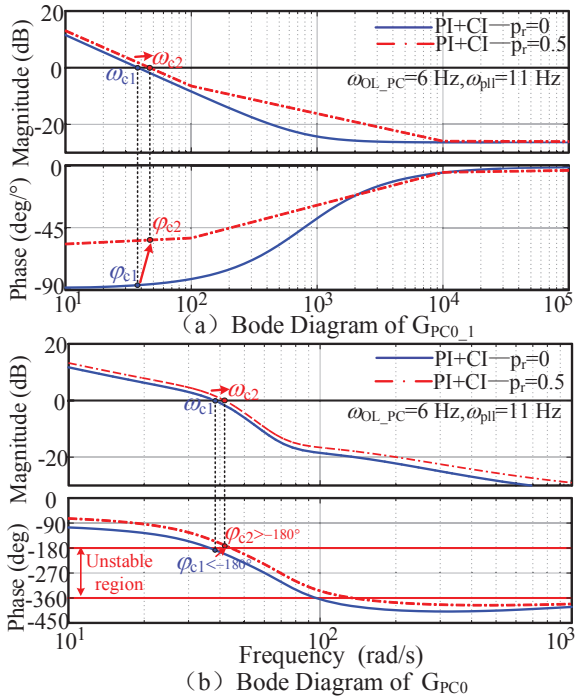

Fig. 4. Bode plots of G_{PC0_1} and G_{PC0} with PI+CI when p_r = 0, 0.5.

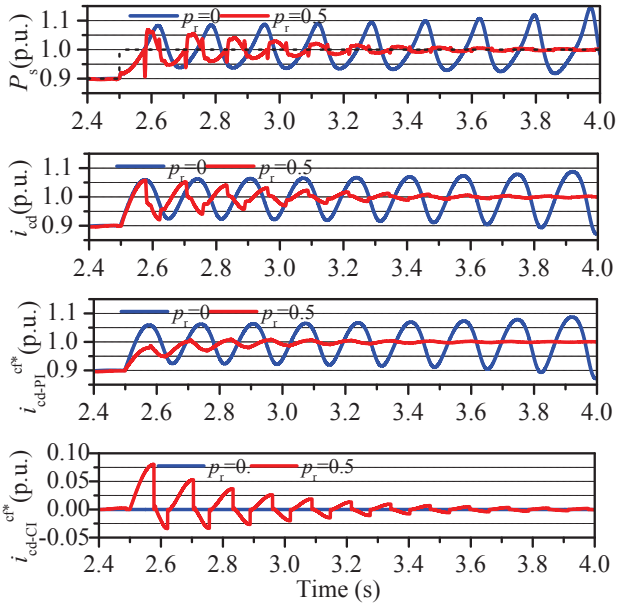

Fig. 5. Matlab/simulink based power and current responses with PI+CI when p_r = 0, 0.5 (ω_{OL_PC} =6 Hz, ω_{pll} =11 Hz).

Fig. 5 presents the simulation results when outer loop adopts the PI+CI with p_r = 0, 0.5, ω_{OL_PC}=6 Hz and ω_{pll}=11 Hz. The reference P_s^* steps from 0.9 p.u. to 1.0 p.u. at t=2.5 s. The power response has increasing oscillations with p_r = 0 as it has negative phase margin according to Fig. 4. However, the oscillations are damped when p_r = 0.5. The d-axis current i_{cd} and the output of the CI compensator i_{cd-CI}^{cf*} in Fig. 5 show the principle of how the CI compensator can help to suppress the oscillations through resetting part of the integrator. The effectiveness of the proposed method is demonstrated by a RTDS simulation (shown in Fig. 6) [6]. The experiment presented in Fig. 7 proves that the PI+CI with a gain of p_r = 0.5 can damp the weak grids oscillations as predicted

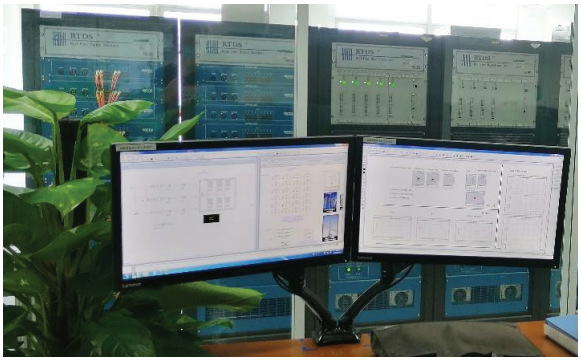

Fig. 6. The RTDS used in the experiment.

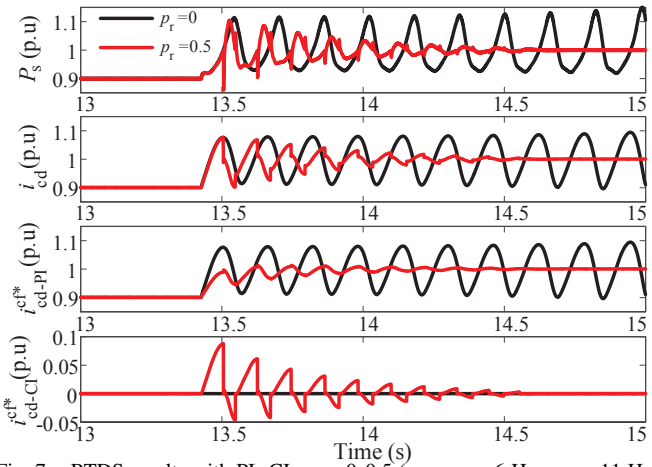

Fig. 7. RTDS results with PI+CI, $p_r = 0, 0.5$ (ω_{OL_PC} =6 Hz, ω_{pll} =11 Hz).

using the Bode plots and simulations in Sec.IV-B.

V. Conclusion

In this letter, we demonstrate that the outer loop active power control bandwidth determines the low-frequency oscillation frequency, and the PLL introduces a large phase delay in weak grids which decreases the phase margin and system damping. A modification of the outer loop active power PI controller based on PI+CI is suggested to improve the performance of the weak-grids-connected VSC. A real time digital simulator has shown the effective compensation of the PLL's phase delay in weak grids and the improvement of the damping.

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