A Switched-Capacitor Based Multilevel Inverter with Reduced Circuit Components and Voltage Boosting Capability

Yi Hu [1], Roya Naderi [2], Yahya Naderi [3,*]

[1] Fujian College of Water Conservancy and Electric Power, Yong'an 366000, China

[2] Department of Electrical Engineering, Islamic Azad university, Heris branch, Heris, Iran

[3] School of Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, United Kingdom

* Corresponding Author Email: Yahya.Naderi@strath.ac.uk

Abstract

In this paper a novel topology of switched capacitor based multilevel inverters is proposed. In this topology, to increase the output voltage levels and to add the voltage boosting capability, several switched capacitor units are cascaded in series. Having voltage boosting capability and generating maximum number of output voltage levels using minimum number of circuit components, is a merit for this topology. To highlight the attributes of the proposed topology, it is compared with other recently proposed multilevel inverters on number of circuit components such as power electronic switches, diodes and capacitors, voltage boosting capability, total standing voltage (TSV), cost and efficiency. The comparison results verify the superiority of the proposed topology over other proposed topologies on number of circuit components, and number of output voltage levels. It is also clear that, this topology has lower voltage stress on power electronic switches, which makes it an appropriate solution for industrial applications. Finally, to show the capabilities of the proposed topology, and to verify the accurate operation of the topology, circuit analysis as well as the experimental results are provided.

Keywords: *Multilevel Inverter, Switched Capacitor Inverter, Cascade H-bridge (CHB), Renewable Energies Applications*

I. Introduction

In the recent years multilevel inverters have become popular in photovoltaic power systems, wind turbine conversion systems, electrical vehicle charging infrastructure and other medium and high-power applications [1-8]. Using multilevel inverters can generate different output voltage waveforms combining different input dc voltage sources. In these inverters, increasing the number of output voltage levels, will improve the output voltage quality and will decrease the total harmonic distortion (THD) of the output voltage waveform, hence the output voltage will look like a sinusoidal waveform. A merit that multilevel inverters have to other conventional inverters is its capability in generating high voltage rating waveforms using lower rate power electronic components [9-12]. Basically, multilevel inverters can be divided into three main categories, diode clamped inverters, cascaded H-Bridges and flying capacitor multilevel inverters. However, to increase the number of output voltage levels, in multilevel inverters, number of utilized power electronic components and dc sources have been increased which is not always cost effective and can be counted as a disadvantage for these inverters. Also, in flying capacitor multilevel inverters,

balancing the dc link capacitor voltage requires a complicated control system which is another disadvantage for multilevel inverters [13-16]. To solve this issue of conventional multilevel inverters, several control methods have been introduced in [17-22]. Topologies proposed in [17-19], can balance the dc link capacitor voltage, using alternative switching patterns, operation accuracy of which is highly dependent on the closed loop controller design.

To overcome the discharge issue of main unit and flying capacitor of single dc source multilevel inverters, a phase shift modulation method is developed in [20], in which the gate pulses of auxiliary and main switches are generated in high frequency and fundamental frequency respectively.

Because of the importance of output power quality in grid connected converters, third harmonic compensation method based on fundamental frequency is reported in [21, 23], in which the goal is to extend the modulation index for three phase applications. In multilevel inverters proposed in [24-29], sum of input dc voltage magnitude and output peak voltage magnitude are the same. Not being able to increase the output voltage magnitude compared to input voltage values, is another drawback for conventional multilevel inverters, to overcome which, several improved multilevel topologies have been proposed in the literature [9, 11, 28-38].

To overcome the mentioned issues of multilevel inverters, switched capacitor multilevel inverters have been introduced in [5, 36-42]. These inverters can generate a large amount of output voltage levels using minimum number of input dc voltage sources. Moreover, these inverter topologies, can increase the maximum output voltage without requiring a boosting stage. In switched capacitor base multilevel inverters, to increase the output voltage levels, number of power electronic elements must increase, which consequently will increase the cost and volume of the inverter. Also, switched capacitor-based inverters, require high voltage rating switches, which limits their application for medium voltage applications. Switched capacitor inverters are composed of several switched capacitor units, voltage sources and semiconductors. In these topologies, voltages of capacitors are balanced using series, parallel charging technique and there is no need for auxiliary control circuits. New switched capacitor based multilevel inverters based on series-parallel connection of basic units are introduced in [43] and [44]. These topologies increase the flexibility of the system, using the series-parallel connection of capacitors, and are increasing the total efficiency of the converter, by transferring a larger portion of input energy to the output.

In this research, a novel topology of switched capacitor multilevel inverters with decreased power electronic elements count is introduced, which has the voltage boosting capability using switched capacitor units and applying an appropriate control system. This topology also has the merit of a decreased voltage stress on power electronic switches. Another advantage for this topology is the fact that it uses lower number of input dc voltages to generate larger numbers of output voltage levels. In this topology, by increasing the number of switched capacitor units, number of output voltage levels increases, which leads to a lower output voltage THD and higher output power quality. This will also increase the maximum output voltage magnitude, however if this task was performed using a boost conversion stage, output voltage quality would have remained the same.

II. BASIC UNIT OF SUGGESTED MULTILEVEL INVERTER

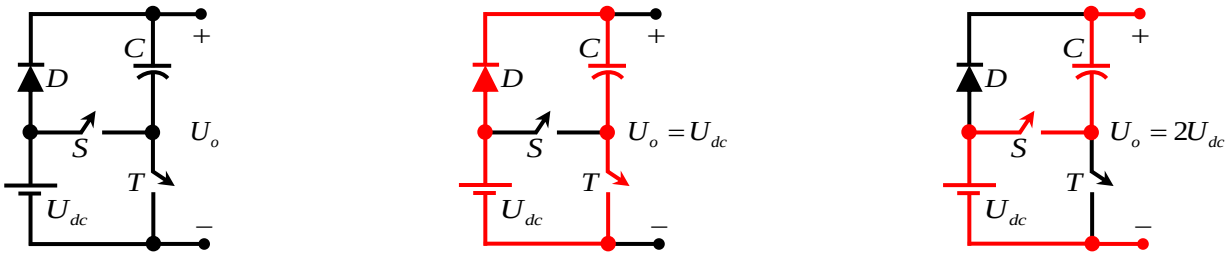
A) Operation of proposed switched capacitor multilevel inverter

The basic unit of the proposed topology is shown in Fig. 1 (a). This unit consists of one single dc source, two power electronic switches (IGBT), one capacitor, and one power diode. The operation of this basic unit consists of two modes: charging mode and discharging mode. The charging operation mode of basic topology is indicated in Fig. 1 (b). regarding this figure when the switch K is on the ON state, the capacitor and input dc voltage source are in parallel in this case the capacitor C is charged, and its voltage (U_C) will be equal to V_{dc} ($U_C=U_{dc}$). The discharging operation mode is presented in Fig. 1 (c). Considering this figure, when the switch S will be turned on, the capacitor C is discharged to the output and the voltage of the output is equal to sum of dc source voltage and capacitor voltage ($U_{out}=2U_{dc}$). Therefore, the basic unit of the proposed inverter can generate two levels of output voltage waveform. It should be noted that, in the charging operation mode of capacitor, the input dc voltage source is in series connection with the resistance of power diode and capacitor. Therefore, during charging operation mode the inrush current will be damped, which is a benefit for the circuit.

The extended circuit of proposed topology is shown in Fig. 2, to increase the positive output voltage level generation and applying the voltage boosting capability, the basic unit of switched capacitor topology can be extended. With respect to Fig. 2, in the extended topology n capacitors, n power diodes, and 2n power switches (unidirectional IGBT) are utilized. The number of generated output voltage levels can be obtained as; $N_{Level}=n+1$. Table I indicates charging capacitors, ON-state power electronic switches, and ON-state diodes for generation of desired output levels in the extended topology. It is worth mentioning that in this table all the components are assumed ideal. Regarding Table I, all of the utilized capacitors are in parallel connection with dc source when the switches T_1, T_2… T_n are in ON-state. Under this condition, the capacitors C_1, C_2, ..., C_n will be charged, and the voltage magnitude of the capacitors will be equal to $+U_{dc}$. In this structure, the positive voltage levels such $+U_{dc}$, $+2U_{dc}$, $+3U_{dc}$, …, $+nU_{dc}$, $+(n+1)U_{dc}$ can be generated, however, this structure cannot produce zero level and negative half cycle of output voltage waveform. To validate the performance of suggested expanded switched capacitor multilevel inverter, three-level topology with two capacitors is considered. This structure is shown in Fig. 3, in which the current path for producing the level $+U_{dc}$ is indicated in Fig. 3 (a). In this operation mode, all utilized capacitors are in parallel with the input dc source. In this mode, capacitors will be in charging mode and the current path of generation $2U_{dc}$ output level is shown in Fig. 3 (b), as it can be seen in this figure, the capacitor C_1 is in current path. Considering Fig. 3 (C), to generate third level of output voltage waveform ($3U_{dc}$), both C_1 and C_2 capacitors will be in the current path.

It should be noted that, the proposed structure cannot produce the zero level and negative half cycle of output voltage. To balance the capacitors voltage in the proposed topology, there is no need for any auxiliary and complex control system, and it is the main advantage of the proposed switched capacitor multilevel inverter. It should be noted that, the voltage difference between input dc source and utilized capacitor is damped by the internal resistance of diodes, capacitors,

and the power electronic switches during the charging mode, meanwhile the created eddy current will be reduced.



(a) (b) (C)

Fig.1. (a): basic switched capacitor structure, (b): charging operation mode, (C): discharging operation mode

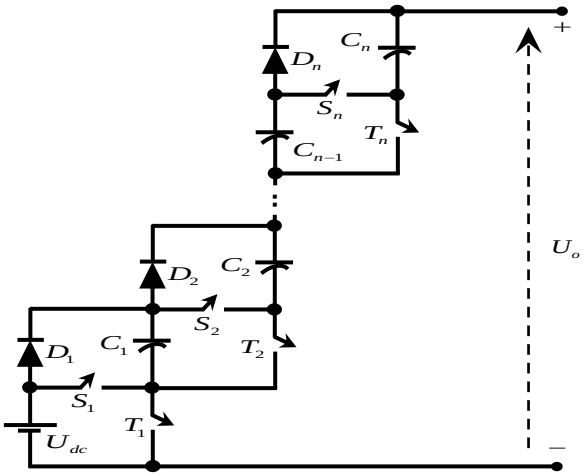
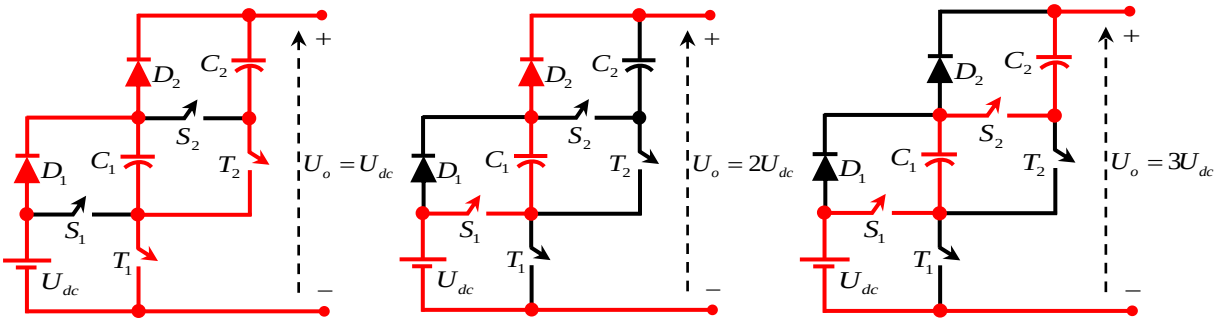


Fig. 2. Extended switched capacitor topology



(a) (b) (c)

Fig. 3. The current path of switched capacitor; (a) the current path for producing output level $U_{out}=U_{dc}$, (b) the current path for producing output level $U_{out}=3U_{dc}$

A) Operation of suggested switched capacitor sub-multilevel converter

To generate zero-voltage level and the negative half cycle of the output voltage waveform, a new topology which is named sub-multilevel, is recommended. This proposed sub-multilevel inverter

is presented in Fig. 4 as it can be seen, the proposed sub-multilevel inverter uses two similar expanded switched capacitor units with two bidirectional switches (K_1 and K_2) and six unidirectional power switches (M_1,...,M_6). Each utilized unidirectional power switch includes an insulated gate bipolar transistor (IGBT) and an antiparallel power diode. The bidirectional power switches can conduct current in both directions. The ON-state switches and power diodes and the charging mode of capacitors to produce all levels of output voltage waveforms are presented in Table II. Here, the $U_{out,U}$ and $U_{o,D}$ are of the up and down extended switched capacitor voltages, respectively. By controlling the power switches of the upper side of the extended switched capacitor, the voltage levels could be obtained as $U_{dc,U}$, $2U_{dc,U}$, $3U_{dc,U}$,..,$nU_{dc,U}$, $(n+1)U_{dc,U}$.

Table I. ON-state diodes, ON-state power switches, and charging capacitors of expanded switched capacitor inverter

states	ON-State Diodes	ON-State Switches	Capacitors charging	U_O
1	$D_1,...,D_n$	$T_1,T_2,...T_n$	$C_1,C_2,...C_n$	$+U_{dc}$
2	$D_2,...D_n$	S_1	-	$+2U_{dc}$
3	$D_3,...D_n$	S_1,S_2	-	$+3U_{dc}$
.	.	.		.
N	D_n	$S_1,S_2,...S_{n-1}$	-	$+nU_{dc}$
n+1	.	$S_1,S_2,...S_n$	-	$+(n+1)U_{dc}$

Table II. ON state switches, and output voltage of recommended sub multilevel inverter

states	ON-State Switches	U_O
1	S_{M4},S_{M5},S_{M6}	0
2	S_{M2},S_{M3},S_{M4}	$+U_{O,U}$
3	S_{M1},S_{M5},S_{M6}	$-U_{O,U}$
4	S_{M1},S_{M2},S_{M6}	$+U_{O,D}$
5	S_{M3},S_{M4},S_{M5}	$-U_{O,D}$
6	S_{M2},S_{M4},S_{M6}	$+(U_{O,U}+U_{O,D})$
7	S_{M1},S_{M3},S_{M5}	$-(U_{O,U}+U_{O,D})$
8	S_{K2},S_{M3},S_{M4}	$-(U_{O,D}+U_{O,U})$
9	S_{K1},S_{M1},S_{M6}	$+(U_{O,D}-U_{O,U})$

The possible generated levels at output of the inverter are $U_{dc,D}$, $2U_{dc,D}$, $3U_{dc,D}$… $nU_{dc,D}$, $(n+1)V_{dc,D}$. To generate the zero, positive, and negative levels in the proposed switched capacitor multilevel inverter, which is shown in Fig. 4, the up and down sides should be combined. With respect to Table II, to avoid the short circuit problems of the proposed structure, (S_{M3}, S_{M6}) and (S_{M1}, S_{M4}) should not be turned on simultaneously. Since the up and down extended switched capacitor topology could have different output voltages, the switches S_{K1} and S_{K2} should not be turned on simultaneously as well. The number of utilized capacitors ($N_{cap,sub}$), power switches ($N_{sw,sub}$), and diodes ($N_{diode,sub}$) in the switched capacitor multilevel inverter can be calculated as;

$$\begin{cases} N_{cap,sub} = N_{diode,sub} = 2n \\ N_{sw,sub} = 4n+8 \\ C_x = 6U_{ref} \\ \Delta U_{Cx} = \dfrac{1}{\left(2\pi f_{ref}\right)\times C_x} \end{cases} \quad (1)$$

$$N_{sw,sub} = 4n+8 \quad (2)$$

Where, n is number of capacitors in each extended switched capacitor. In order to generate the maximum number of output levels, the up and down dc sources should be calculated as follows;

$$U_{dc,D} = (2n+3)U_{dc,U} \quad (3)$$

Therefore, the number of produced output voltage levels of the proposed switched capacitor multilevel inverter can be obtained as;

$$N_{level,sub} = (2n+3)^2 \quad (4)$$

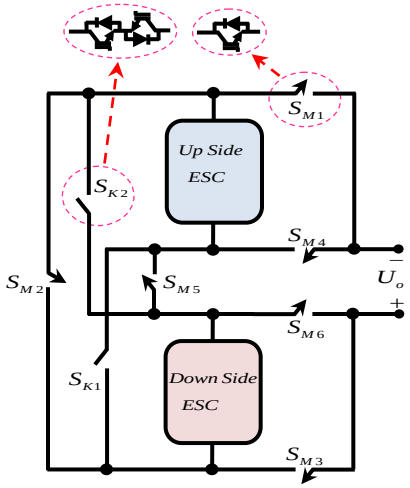


Fig. 4. Recommended sub multilevel inverter

The technique of determining the magnitude of the dc voltage sources (equation (3)), the voltage gain of suggested switched capacitor multilevel inverter assuming the values of dc voltage sources for different number of utilized capacitors (n), and the number of generated voltage levels (equation (4)) are shown in Table III.

Table III. The number of produced output levels, amplitudes of dc voltage sources, and voltage gain of suggested sub multilevel inverter

Number of capacitors	N_{level}	$U_{dc,up}$	$U_{dc,down}$	Voltage Gain
1	25	U_{dc}	$5U_{dc}$	$2\left(U_{dc,U}+U_{dc,D}\right)$
2	49	U_{dc}	$7U_{dc}$	$3\left(U_{dc,U}+U_{dc,D}\right)$
…	…	…	…	…
N	$(2n+3)^2$	U_{dc}	$(2n+3)U_{dc,U}$	$\left(U_{dc,U}+U_{dc,D}\right)(n+1)$

To verify the performance of the proposed inverter, a conventional 25-level inverter would be discussed which is shown in Fig. 5. Considering equation (3), values of the utilized dc sources for 25-level inverter can be obtained as; $U_{dc,U} = U_{dc}$ and $U_{dc,D} = 5U_{dc}$. Table IV presents the conducting condition of diodes, power switches, and capacitors for n=1. This table also shows that the capacitor C_U and C_D are charged in the different ON periods which will balances the capacitors voltage. The sum of input dc voltage sources values is equal to $6U_{dc}$. Nevertheless, regarding Table IV, the peak value of the output voltage level is equal to $12U_{dc}$. This demonstrates that, the proposed 25-level inverter has voltage boosting capability. Fig. 6 shows the current path for generating other output levels.

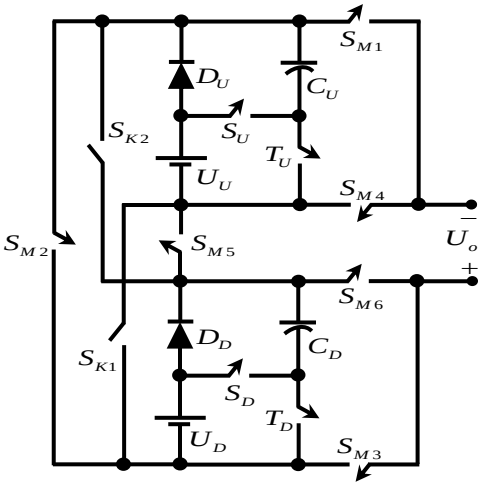
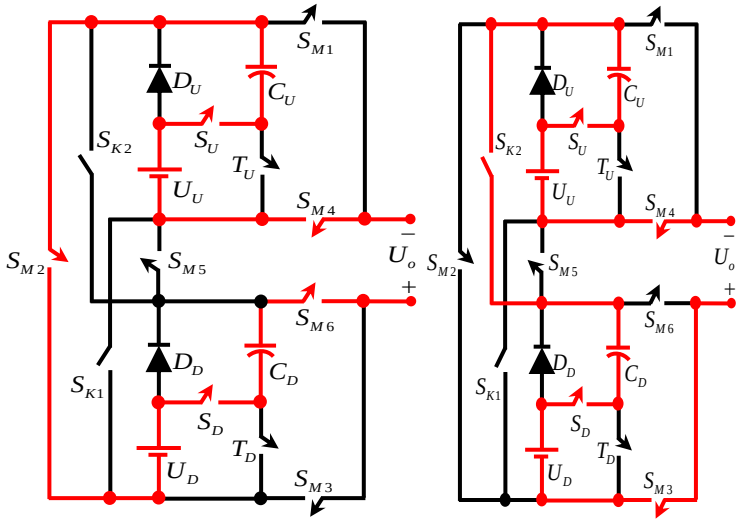


Fig. 5. 25-level switched capacitor topology



(a) (b)

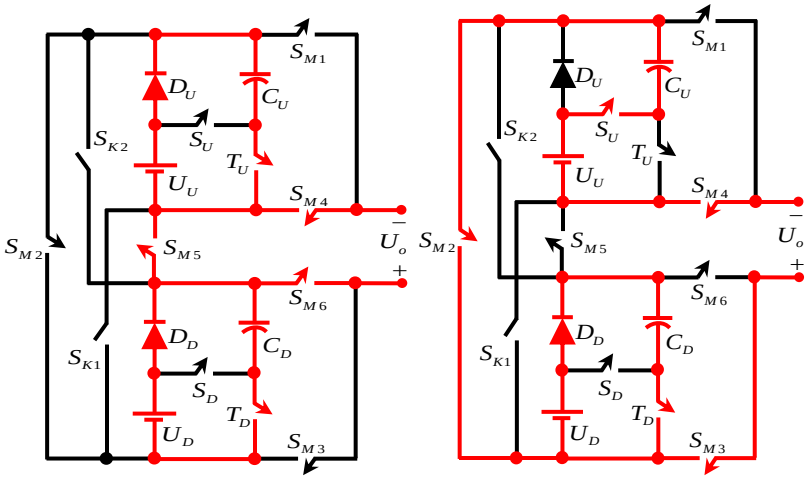


Fig. 6. Some operation modes of proposed 25-level inverter: (a) $U_O=(2U_U+2U_D)$, (b) $U_O=-2U_U$, (C) $U_O=0$, (d) $U_O=2U_D-2U_U$

Table IV. ON-state diodes, power switches, and charging capacitors of recommended 25-level inverter

states	ON-State Diodes	ON-State Switches	Capacitors charging	U_O
1	D_U	$S_{M_4}, S_{M_5}, S_{M_6}, T_U, T_D$	C_U, C_D	0
2	D_D	$S_{M_2}, S_{M_3}, S_{M_4}, T_U, T_D$	C_U, C_D	$+U_{dc}$
3	D_U	$S_{M_2}, S_{M_3}, S_{M_4}, S_U, T_D$	C_D	$+2U_{dc}$
4	D_D	$S_{M_1}, S_{K_1}, S_{M_6}, S_U, T_D$	C_D	$.+3U_{dc}$
5	D_D , D_U	$S_{M_1}, S_{K_1}, S_{M_6}, T_U, T_D$	C_U, C_D	$+4U_{dc}$
6	D_D, D_U	$S_{M_1}, S_{M_2}, S_{M_6}, T_U, T_D$	C_U, C_D	$+5U_{dc}$
7	D_D, D_U	$S_{M_2}, S_{M_4}, S_{M_6}, S_U, T_D$	C_U, C_D	$+6U_{dc}$
8	D_D	$S_{M_2}, S_{M_4}, S_{M_6}, S_U, T_D$	C_D	$+7U_{dc}$
9	…	$S_{M_1}, S_{K_1}, S_{M_6}, S_U, S_D$	…	$+8U_{dc}$
10	D_U	$S_{M_1}, S_{K_1}, S_{M_6}, T_U, S_D$	C_U	$+9U_{dc}$
11	D_U	$S_{M_1}, S_{M_2}, S_{M_6}, T_U, S_D$	C_U	$+10U_{dc}$
12	D_U	$S_{M_2}, S_{M_4}, S_{M_6}, T_U, S_D$	C_U	$+11U_{dc}$
13	…	$S_{M_2}, S_{M_4}, S_{M_6}, S_U, S_D$	…	$+12U_{dc}$
14	…	$S_{M_1}, S_{M_3}, S_{M_5}, S_U, S_D$	…	$-12U_{dc}$
15	D_U	$S_{M_1}, S_{M_3}, S_{M_5}, T_U, S_D$	C_U	$-11U_{dc}$
16	D_U	$S_{M_3}, S_{M_4}, S_{M_5}, T_U, S_D$	C_U	$-10U_{dc}$
17	D_U	$S_{M_3}, S_{M_4}, S_{K_2}, T_U, S_D$	C_U	$-9U_{dc}$
18	…	$S_{M_3}, S_{M_4}, S_{K_2}, S_U, S_D$	…	$-8U_{dc}$

19	D_D	$S_{M_1}, S_{M_3}, S_{M_5}, S_U, T_D$	C_D	$-7U_{dc}$
20	D_U , D_D	$S_{M_1}, S_{M_3}, S_{M_5}, T_U, T_D$	C_U, C_D	$-6V_{dc}$
21	D_U , D_D	$S_{M_3}, S_{M_4}, S_{M_5}, T_U, T_D$	C_U, C_D	$-5U_{dc}$
22	D_U , D_D	$S_{M_3}, S_{K_2}, S_{M_4}, T_U, T_D$	C_U, C_D	$-4U_{dc}$
23	D_D	$S_{M_3}, S_{K_2}, S_{M_4}, S_U, T_D$	C_D	$-3U_{dc}$
24	D_D	$S_{M_6}, S_{M_5}, S_{M_1}, S_U, T_D$	C_D	$-2U_{dc}$
25	…	$S_{M_6}, S_{M_5}, S_{M_1}, T_U, T_D$	C_U, C_D	$-U_{dc}$

B) Determination of capacitance value for utilized capacitors

Several switching methods have been presented for multilevel inverters in the literature [45, 46], however in this paper, the nearest level control (NLC) method presented in [21], is used to control the proposed multilevel topology where, $\alpha_{1,2,\ldots}$ refer to switching angles. To design the value of utilized capacitors (C_X), the voltage ripple should be calculated which is calculated as;

$$\Delta U_{C_x} = \frac{1}{(2\pi f_{ref}) \times C_x} \int_{\alpha_n}^{\alpha_m} i_{C_x} d(\omega t) \tag{5}$$

In which α_n and α_m are the switching angels. Therefore, in the ($\alpha_n - \alpha_m$) interval, C_x is the longest discharging period based on which, the voltage ripple of the capacitor is equal to $\Delta U_{C_X} = K.U_{C_X}$. Under this condition, the capacitance of capacitors can be calculated as:

$$C_x = \frac{1}{2\pi (K U_{C_x}).f_{ref}} \int_{\alpha_n}^{\alpha_m} i_{C_x} d(\omega t) \tag{6}$$

However, the switching angles can be calculated as follows.

$$\alpha_j = \arcsin\left(\frac{2j-1}{2N_{level}}\right) \quad j = 1, 2, \ldots, \left(\frac{N_{level}-1}{2}\right) \tag{7}$$

Table V. Standing voltage on the utilized switches in the suggested sub multilevel inverter

Power Switches	Voltage on Switches in the switched capacitor inverter
S_{M_3}, S_{M_6}	$U_{S_{M3}} = U_{S_{M6}} = 2U_{dc,D}$
S_{M_1}, S_{M_4}	$U_{S_{M1}} = U_{S_{M4}} = 2U_{dc,U}$
S_{M_2}, S_{M_5}	$U_{S_{M2}} = U_{S_{M5}} = 2\left(U_{dc,D} + U_{dc,U}\right)$
S_{K_1}, S_{K_2}	$. U_{S_{K1}} = U_{S_{K2}} = 2U_{dc,D}$
$S_{1,D}, T_{1,D}, \ldots, S_{n,D}, T_{n,D}$	$U_{S_{1,D}} = U_{T1,D} = \ldots U_{Sn,D} = U_{Tn,D} = U_{dc}$
$S_{1,U}, T_{1,U} \ldots, S_{n,U}, T_{n,U}$	$U_{S_{1,U}} = U_{T1,U} = \ldots U_{Sn,U} = U_{Tn,U} = U_{dc}$

C) Voltage on switches

In the upper side of the extended switched capacitor inverter, standing voltage on the switches is equal to $U_{dc,up}$ whereas in the lower half of this converter the voltage on the switches is equal to $U_{dc,down}$, the voltage on the other utilized switches are different where the standing voltage of the switches M_2 and M_5 are higher than other switches. The standing voltages of the switches are presented in Table V.

III. Suggested cascaded multilevel inverter

The recommended switched capacitor multilevel inverter consists of large amount of circuit components and is suitable for low voltage applications. To increase the number of output voltage levels for high voltage applications, the cascaded topology based on the series connection of switched capacitor multilevel inverters is presented in Fig. 7. The presented cascaded multilevel inverter composed of Z sub-multilevel inverters which are in series connection. The peak value of the output voltage can be calculated as;

$$U_{o,peak} = \sum_{i=1}^{P} V_{(o,peak)i} \tag{8}$$

In which, $V_{(o,peak)1}$, $V_{(o,peak)2}$, …, $V_{(o,peak)P}$ are the peak values produced by each sub-multilevel inverter. In the recommended cascaded multilevel inverter, the number of utilized capacitors in the P^{th} sub-multilevel inverter is equal to $2n_z$.

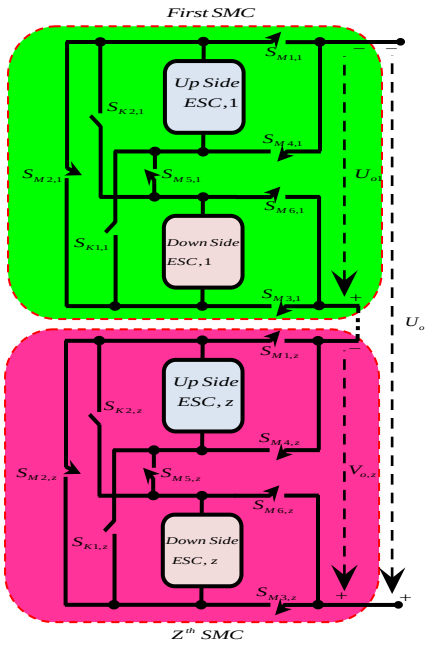


Fig. 7. Recommended cascaded multilevel inverter

In the recommended cascaded structure, the values of utilized dc sources can be obtained as:

$$2_{n1} = 2_{n2} = \ldots 2_{nz} = 2_n \tag{9}$$

In the recommended cascaded structure, the value of dc sources can be given as:

First switched capacitor multilevel inverter;

$$U_{dc,U1} = U_{dc} \tag{10}$$

$$U_{dc,D1} = (2n+3)U_{dc} \tag{11}$$

In the first switched capacitor multilevel inverter, the peak value of output voltage will be calculated as;

$$\begin{aligned} U_{o1,peak} &= \left(V_{dc,U1} + V_{dc,D1}\right)(n+1) \\ &= \left(2n^2 + 6n + 4\right) \end{aligned} \tag{12}$$

Second switched capacitor multilevel inverter:

$$U_{dc,U2} = 2U_{o1,peak} + U_{dc} = \left(4n^2 + 12n + 9\right)U_{dc} \tag{13}$$

$$U_{dc,D2} = \left(4n^2 + 12n + 9\right)(2n+3)U_{dc} \tag{14}$$

So, the peak value of output voltage waveform in the second switched capacitor multilevel can be obtained as;

$$U_{o2,peak} = \left(U_{dc,U2} + U_{dc,D2}\right)(n+1) \tag{15}$$

P^{th} Switched capacitor multilevel inverter:

$$\begin{aligned} U_{dc,Uz} &= 2\left(U_{o1,peak} + U_{o,peak}\right) + U_{dc} \\ &= \left(4n^2 + 12n + 9\right)^{p-1} U_{dc} \end{aligned} \tag{16}$$

$$U_{dc,Dz} = \left(4n^2 + 12n + 9\right)^{p-1}(2n+3)U_{dc} \tag{17}$$

The number of output levels in the cascaded structure is;

$$N_{level,cascade} = \left(4n^2 + 12n + 9\right)^{p} \tag{18}$$

Also, the number of dc sources ($N_{source,cascade}$), ($N_{cap,cascade}$), ($N_{switch,cascade}$) can be calculated as;

$$N_{source,cascade} = 2p \tag{19}$$

$$N_{cap,cascade} = 2nz \tag{20}$$

$$N_{switch,cascade} = (4n+8) \tag{21}$$

IV. Calculation of voltage on switching in the recommended cascaded structure

To calculate the standing voltage of the utilized power switches in the proposed cascaded inverter, the following equations should be used.

$$\begin{aligned} T_{switch,cascade} = &\sum_{j=1}^{z}\sum_{i=1}^{n}\left(U_{Si,U\_j} + U_{Ti,U\_j} + U_{Si,D\_j} + U_{Si,U\_j}\right) + \sum_{i=1}^{z}\left(U_{S_{K1i}} + U_{S_{K2i}}\right) \\ &+ \sum_{i=1}^{z}\left(U_{S_{M1i}} + U_{S_{M2i}} + U_{S_{M3j}} + U_{S_{M4i}} + U_{S_{M5i}} + U_{S_{M6i}}\right) \end{aligned} \tag{22}$$

Where, the $U_{S_{M1i}}, U_{S_{M2i}}, U_{S_{M3j}}, U_{S_{M4i}}, U_{S_{M5i}}$ and U_{M6i} are the standing voltages of the switches $S_{M_{1i}}, S_{M_{2i}}, S_{M_{3i}}, S_{M_{4i}}, S_{M_{5i}}$ and M_{6i} in the i^{th} switched capacitor inverter, respectively. Also, the standing voltage of the switches K_{1i} and K_{2i} in the i^{th} switched capacitor are indicated as $U_{S_{K1i}}$ and $U_{S_{K2i}}$ respectively.

The values of $U_{S_{M1i}}, U_{S_{M2i}}, U_{S_{M3j}}, U_{S_{M4i}}, U_{S_{M5i}}$ and U_{M6i} can be calculated as;

$$U_{S_{M1i}} = U_{S_{M4i}} = U_{dc,U\_i}(n=1) \tag{23}$$

$$U_{S_{M2i}} = U_{S_{M5i}} = (U_{dc,U\_i} + U_{dc,D\_i})(n+1) \tag{24}$$

$$U_{S_{M3i}} = U_{dc,U\_i}(n+1) \tag{25}$$

U_{K1i} and U_{K2i} can be calculated as:

$$U_{S_{K1i}} = U_{S_{K2i}} = 2nU_{dc,U\_i} \tag{26}$$

However, the voltage of power switches $S_{i,U\_j}, T_{i,U\_j}, S_{i,U\_j}$ and T_{i,U_j} can be obtained as:

$$U_{Si,L\_j} = U_{Ti,L\_j} = U_{dc,L\_j} \tag{27}$$

$$U_{Si,U\_j} = U_{Ti,U\_j} = U_{dc,U\_j} \tag{28}$$

With respect to equations (22) and (27), the total standing voltage on the switches of the suggested switched capacitor inverter can be written as;

$$T_{switch,cascade} = [\sum_{j=1}^{z}(U_{dc,U\_j} + U_{dc,D\_j})](6n+4) + [\sum_{j=1}^{z}(U_{dc,L\_j}](4n) \tag{29}$$

The peak output voltage of the recommended cascaded topology can be obtained as follows;

$$U_{o,peak} = (\frac{N_{level}-1}{2})U_{dc} \tag{30}$$

So that, the equation (29) can be rewritten as follow:

$$T_{switch,cascade} = \left[4n(2n+3) + \frac{4+6n}{2+2n}(N_{level}-1)\right] \tag{31}$$

V. Power losses analysis in the recommended structure

The total power loss of the inverter (P_{Total}) is equal to sum of switching losses ($P_{switching}$), conduction losses (P_{Con}), and ripple losses of utilized capacitors ($P_{C,ripple}$).

$$P_{Total} = P_{switching} + P_{Con} + P_{C,ripple} \tag{32}$$

a) Conduction losses

In the proposed switched capacitor inverter, the conduction losses are consumed by utilized power switches ($P_{Con,switch}$), power diodes ($P_{Con,diode}$), and capacitors ($P_{Con,cap}$) which are in the current path.

$$P_{Con,total} = P_{Con,diode} + P_{Con,cap} + P_{Con,switch} \tag{33}$$

The average value of the conduction losses can be calculated as:

$$P_{Con,total} = \left[\frac{a(t)}{\pi}\int_0^{\pi}\left(V_{on,diode}.i(t) + R_{diode}.i^2(t)\right)d(\omega t)\right] + \left[\frac{b(t)}{\pi}\int_0^{\pi}\left(R_{cap}.i(t)^2\right)d(\omega t)\right] + \left[\frac{c(t)}{\pi}\int_0^{\pi}\left(R_{switch}.i^{\gamma+1}(t) + V_{on,switch}.i(t)\right)d(\omega t)\right] \quad (34)$$

Where, γ is a constant factor that depends on the characteristic of power switch. $V_{on,diode}$ and $V_{on,switch}$ are the ON-state voltage drop of the diode and the power switch, respectively. R_{diode} , R_{switch} , and R_{cap} are the resistances of the diode, switch and utilized capacitor, respectively. In the above-mentioned equation (34), $a(t), b(t), c(t)$ refer to number of diodes, capacitors, and switches in the current path, respectively.

(b) Switching losses

The switching losses of the power switches during the turn-on transition ($P_{switch,on}$) and turn-off transition ($P_{switch,off}$) can be determined as;

$$P_{switch,on} = f\left(\frac{N_{on}.U_{switch}.i}{6}\right)t_{off} \quad (35)$$

$$P_{switch,off} = f\left(\frac{N_{on}.U_{switch}.i}{6}\right)t_{on} \quad (36)$$

In which, f is equal to switching frequency of the proposed inverter. The total switching losses can be written as:

$$P_{switch,total} = P_{switch,on} + P_{switch,off} \quad (37)$$

C) Ripples losses

The power losses of the capacitor voltage ripples can be calculated as:

$$P_{C,ripple} = \frac{1}{2T_{ref}}\left[\sum_{j=1}^{z}\sum_{i=1}^{n}\left(C_{i,U\_j}\Delta U_{Ci,U\_j} + C_{i,D\_j}\Delta U_{Ci,D\_j}\right)\right] \quad (38)$$

VI. Optimization of proposed cascaded structure

In this part, to achieve the maximum number of output levels based on reduced components, the cascaded structure will be optimized. The optimized number of capacitors in each side of switched capacitor multilevel inverters for different aims (n) should be obtained.

a) Optimal structure for n with reduction number of power switches

The aim of this section is to find the value of (n) to generate the maximum number of output voltage levels using minimum number of power switches. With respect to (18) and (21), it can be written as:

$$N_{switch,cascade} = \frac{(4n+8)}{\ln\left(4n^2+12n+9\right)}\ln\left(N_{level,cascade}\right) \quad (39)$$

In the above equation, the parameter $N_{level,cascade}$ is a constant value and is minimized when $\frac{(4n+8)}{\ln\left(4n^2+12n+9\right)}$ has the minimum value. By solving this equation, n=1 provides the optimized structure to produce maximum output levels with minimum utilized capacitors.

b) Optimal structure to minimize the number of utilized capacitors

To generate the maximum output levels with minimum number of used capacitors, the parameter n, should be calculated. Considering (18) and (20), it can be written as:

$$N_{cap,cascade}=\frac{2n}{\ln\left(4n^2+12n+9\right)}\ln\left(N_{level,cascade}\right) \tag{40}$$

Considering (40), $N_{level,cascade}$ is a constant parameter, so when $\frac{2n}{\ln\left(4n^2+12n+9\right)}$ becomes minimum, $N_{cap,cascade}$ is minimized. By solving the above equation, n=1 provides the optimized structure for producing output levels with minimum number of utilized capacitors.

VII. Comparison of the proposed inverter with other conventional topologies

To highlight the benefits of optimized structure, comparison results are presented by considering the number of utilized capacitors, independent input dc-sources, power electronic switches, and maximum voltage on switches. The optimized multilevel inverter is compared with presented structures in [5, 24-27, 36-39, 44] and trinary CHB multilevel inverter structures presented in [24-26]. However, the structures which are presented in [37, 44] are called switched ladder multilevel inverter, switched capacitor inverter, hybrid multilevel inverters, and step-up switched capacitor multilevel inverters, respectively. The structures in [40] and [41] have been named high step up multilevel inverters, hybrid multilevel inverters, boost switched capacitor multilevel inverters, and hybrid switched capacitor multilevel inverters, respectively. Compared with other topologies, the proposed topology uses the lowest number of capacitors. Magnitude of the voltage generated by PV panels is usually low to be used in the inverter, so if the dc power supplies are to be replaced with PV panels, adding of a dc-dc converter should be considered. Generally, single-input multi-output dc-dc converters are more suitable option to produce multiple dc voltage sources.

In the recommended cascaded multilevel inverter, the switches $S_{M_{2z}}$ and $S_{M_{5z}}$ stand a higher voltage which is equal to $\left(U_{dc,Uz}+U_{dc,Dz}\right)\left(n+1\right)$. Meanwhile, the presented topologies in [24-26] and [36, 37, 39] use four high voltage rating power switches which tolerate peak amplitude of output voltage. Table VI presents a comparison on the proposed 25-level structure with trinary CHB and other conventional topologies. With respect to this Table, in the proposed 25-level inverter the ratio of number of independent power dc-sources, power electronic switches, and number of capacitors to the number of output voltage levels are less than other structures. In the recommended structure the number of high voltage power switches is the same with the suggested structures in [38, 40], and is lower than other proposed structures. The proposed 25-level cascaded inverter has the voltage boosting capability, but the proposed structures in [29-31] and [38-39] do not have voltage boosting feature. The recommended structures and topologies in [29-31], [38-39], [20], [37], [40] and [18]-[20] can operate in bidirectional power flow applications, however the

recommended structure in [17] is a unidirectional power flow inverter. The values of input power, output power, efficiency, N_{level} and ratio of the output voltage THD to N_{level} in the recommended structure and other structures are indicated in Table VII. Regarding this Table, compared with other structures the efficiency of experimented proposed 25-level inverter is lower. However, compared to present topologies in [29-30], in the proposed inverter the output voltage THD is lower. Moreover, the proposed topology has been compared with other topologies on total standing voltage (TSV), cost, total harmonic distortion (THD) and efficiency and the results are summarized in Table VI. Based on these results, the TSV for this topology is lower than all the other proposed topologies in the literature, which is an industrial design merit for this topology. The design cost for the proposed topology is lower than all the topologies except the topology in [47], which has a higher THD and consequently lower output voltage quality in comparison to the proposed technology. Considering the data summarized in Table VI, the efficiency of the proposed converter is in an acceptable range in comparison to other topologies. Although the efficiency of the proposed topology is lower than topologies proposed in [47], [48] and [49] but the proposed topology is in a better situation regarding the cost and the output voltage THD. In general, it can be concluded that the proposed topology has merit over other relevant topologies in the literature on TSV, cost and THD aspects, as well as being in an acceptable range of efficiency.

Table VI. Comparison results of proposed 25-level inverter with other conventional topologies

Ref *	Voltage boosting capability	Bidirectional power flow capability	N_{level}	$\frac{N_{capcitor}}{N_{level}}$	$\frac{N_{dc}}{N_{level}}$	$\frac{N_{switch}}{N_{level}}$	$\frac{N_{diode}}{N_{level}}$	Number of high voltage switches	TSV	Cost ($)	THD (%)	E_{ff} (%)
Proposed	Yes	Yes	25	0.08	0.08	0.48	0.08	2	14.6	49.04	2.9	96.54
[24]	No	Yes	17	-	0.2352	0.95	-	4	21	64	3.17	N.R
[25]	No	Yes	17	-	0.2352	1.18	-	4	52	80	1.44	N.R
[26]	No	Yes	27	-	0.25	0.6	-	4	105	64	5.9	N.R
[27]	No	Yes	25	-	0.15	0.64	-	4	128	64	1.92	92.23
[36]	Yes	No	25	0.44	0.15	0.64	0.88	44	72	160	N.R	83
[33]	No	Yes	49	-	0.082	0.49	-	4	120	96	2.8	92
[37]	Yes	Yes	25	0.44	0.15	1.36	-	4	36	168.5	3.25	N.R
[5]	Yes	Yes	19	0.3157	0.1578	1.105	0.473	4	140	410.04	4.5	90
[50]	No	Yes	17	-	0.2353	0.705	-	2	36	N.R	N.R	N.R
[39]	Yes	Yes	17	0.1176	0.1176	0.705	0.47	4	48	-	N.R	89.2
[40]	No	Yes	19	-	0.42	0.95	-	2	20		N.R	N.R
[41]	Yes	Yes	17	0.12	0.12	0.6	0.12	2	48	-	N.R	95
[42]	Yes	Yes	19	0.105	0.20	0.632	0.105	4	36	56.384	4.26	93.5
Trinary CHB	Yes	Yes	27	-	0.1111	0.4444	-	4	26	138.84	N.R	N.R
[51]	Yes	Yes	25	0.08	0.08	0.58	-	4	70	77.56	3.25	N.R
[48]	Yes	Yes	25	0.24	0.04	1.63	-	6	82	108	N.R	97.25
[49]	Yes	Yes	9	-	0.44	0.66	-	2	20	72	13.01	96.75
[47]	No	No	17	-	0.24	0.58	-	4	32	32.66	5.17	98.8
[52]	Yes	Yes	7	0.15	0.28	1.28	0.28	2	16	113.87	N.R	97.21

[53]	Yes	Yes	17	0.12	0.12	0.58	0.12	6	25	132.16	N.R	N.R
[54]	No	Yes	15	-	0.2	0.6	0.26	4	30.9	121.16	1	94.1
[55]	No	Yes	31	-	0.12	0.97	-	4	67	129.9	1.13	N.R
[56]	Yes	Yes	11	0.82	0.09	1.81	1.81	-	28	366.5	1.45	N.R
[57]	No	Yes	31	-	0.13	0.39	0.39	6	45	282.6	3.35	

***** The circuit topology for all the compared references are presented at the Appendix section

Table VII. The values of input power, output power, efficiency, N_{level}, and the ratio of output voltage THD to N_{level} in the recommended structure and other topologies

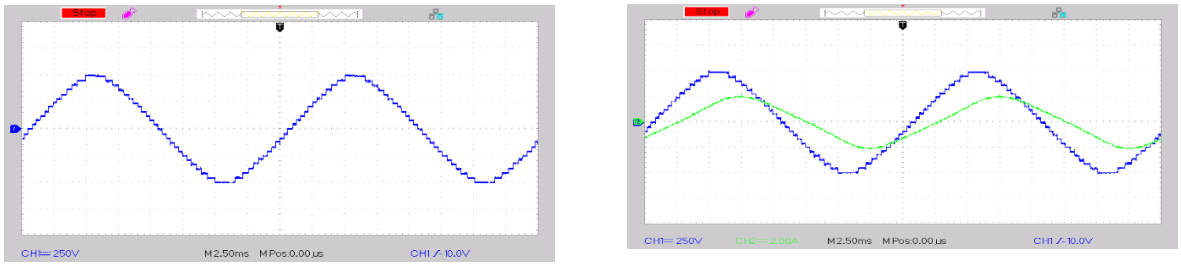
Inverter type	Input power	Output power	efficiency	N_{level}	THD of output voltage/ N_{level}	Adjustable DC-link voltage
proposed	120 2830	124.9 2732	96.07 96.54	25	Yes	Yes
[24]	-	-	-	15	NO	NO
[38]	62.6W	67.8W	92.33	49	Yes	No
[25]	205W	217W	94.7	31	NO	NO
[27]	-	-	-	13	NO	NO
[50]	1345W	1270W	94.42	49	NO	NO

VIII. Experimental results

To indicate the performance and verify the mathematical analysis of the proposed structure, experimental results are presented for 25-level inverter. The 25-level inverter is shown in Fig. 4, which consists of two capacitors, two dc power supplies, and twelve power switches. The main objectives of this section are to analyze the experimental results of topology in term of current and voltage of power switches, output voltage waveform, output current waveform, current waveform of utilized capacitors (I_{CU} and I_{CD}) and balanced voltage of capacitors (V_{CU} and V_{CD}) with their ripple waveform. To validate the feasibility of the proposed multilevel inverter, the experimental results for a 25-level inverter are presented. Details of the utilized elements and description thereof have also been presented in Table VIII. The experimental results are indicated in this section, the amplitude of utilized dc sources are chosen as $U_{dc,U}$ = 42V and $U_{dc,D}$ =210V. The proposed topology feeds the inductive load with R_L=120 and L=60mH and the output voltage and current waveforms are shown in Fig. 8 (a) and (b).

Table VIII. List of utilized elements and needed descriptions experimental prototype

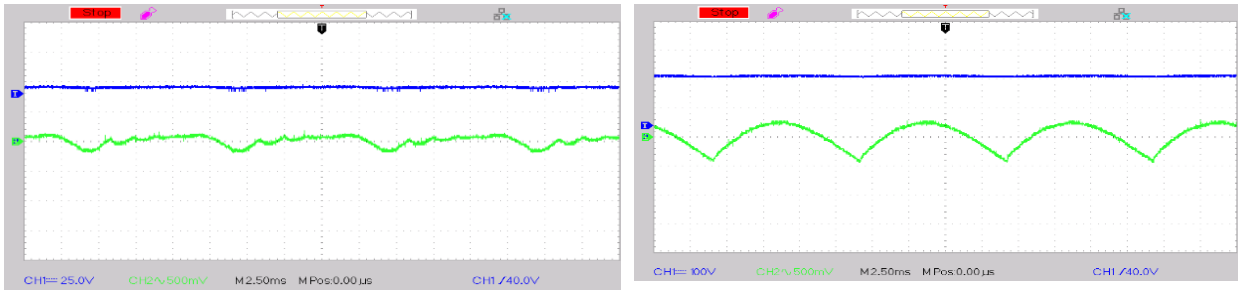
Component	Type	Description
Power switches	12N60A4	600V/54A
Gate driver	TLP250	IC
Power didoes	RURP36D	600V/30A
Capacitor C_U	Electrolytic capacitor	1000uF/50V
Capacitor C_D	Electrolytic capacitor	1000uF/250V



(a) (b)

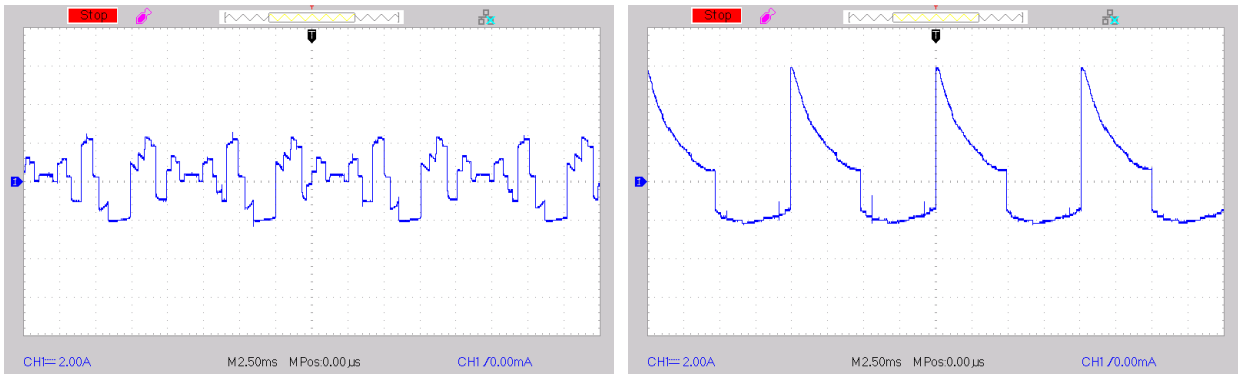
Fig. 8 (a) output voltage waveform, (b) output voltage and current waveform

With respect to Fig.8, the peak values of voltage and current ($V_{O,peak}$ and $I_{O,peak}$) are equal to 42V and 210V respectively. The sum value of input dc sources is equal to 252V; however, the peak value of output voltage is 500V and this verifies the voltage boosting capability of the proposed 25-level inverter. The voltage waveform and voltage ripple of used capacitors are presented in Fig. 9 (a) and (b) respectively. These figures indicate that the voltage of capacitors CU and CD are 42V and 210V, respectively. The currents passing capacitors C_U and C_D are shown in Fig. 10 (a) and (b). From Fig 10. (a) the peak current of C_U is 2.4 amps, and since the peak load current is 2 amps, then the charging current of C_U is 20% bigger than the peak load current. From Fig 10. (b), the peak current of C_D is 6 amps, and since the peak load current is 2 amps, then the charging current of C_D is 3 times the peak load current.



(a) (b)

Fig. 9. (a) Voltage capacitor waveform and voltage ripple of capacitor C_U, (b) voltage capacitor waveform and voltage ripple of capacitor C_D



(a) (b)

Fig. 9. (a) Current waveforms passing through capacitor C_U (b). Current waveforms passing through capacitor C_D

The standing voltage for different power switches in the proposed 25-level inverter are shown in Fig. 11.

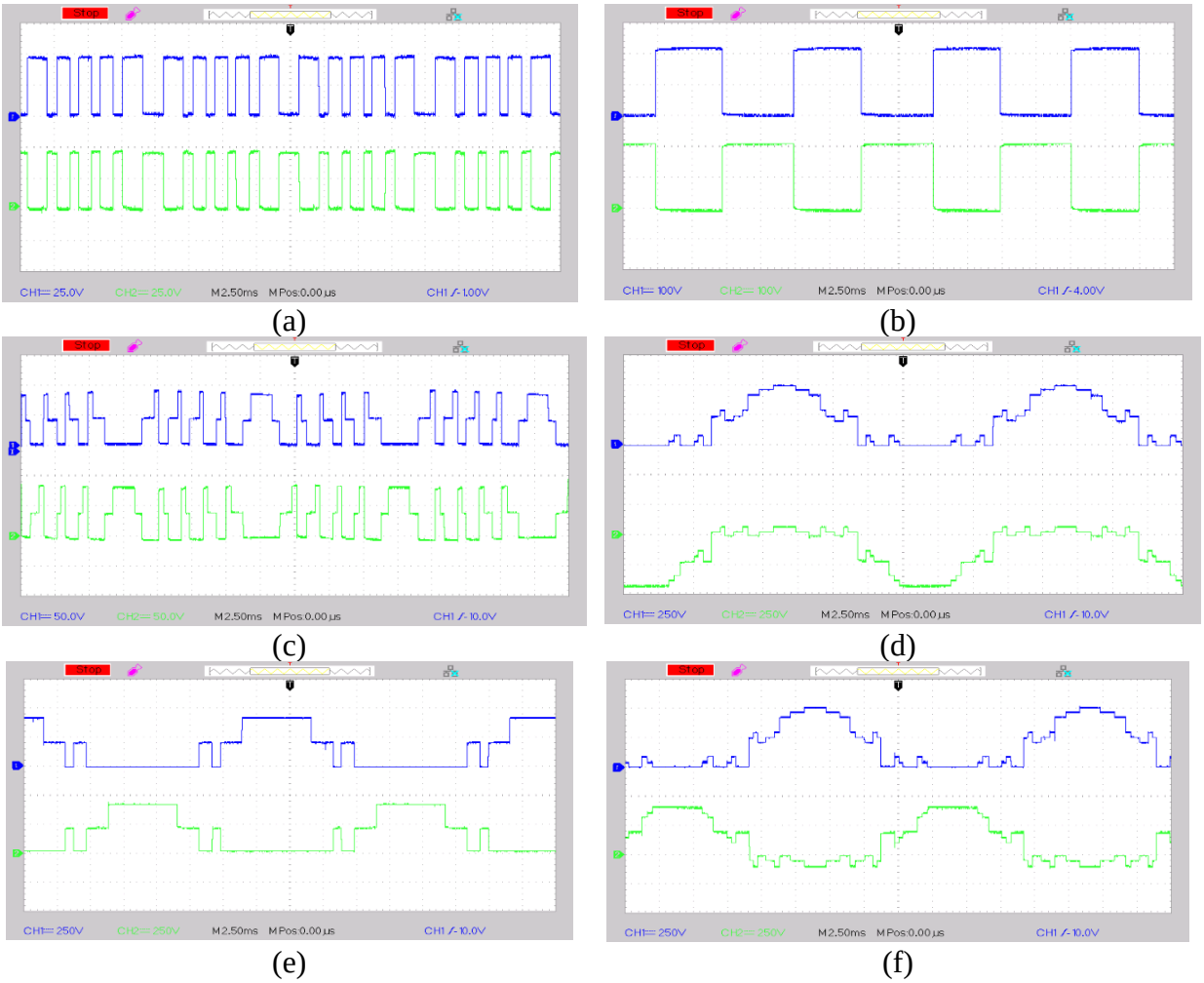
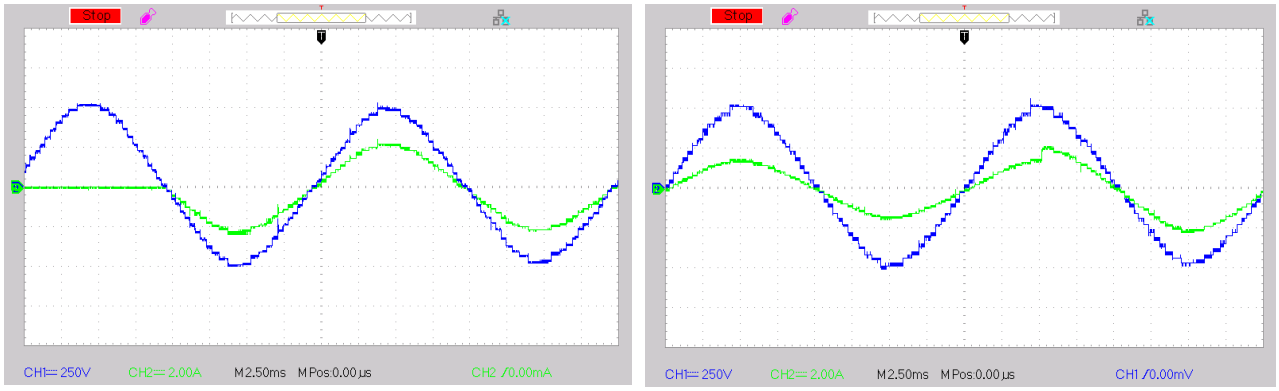


Fig. 11. Blocked voltage of power switches: (a) S_D, T_D, (b) S_U, T_U, (c) S_{M1}, S_{M4},(d) S_{M2}, S_{K2} , (e) S_{M3}, S_{M6} , (f) S_{M5}, S_{K1}

The blocked voltage of power switches S_D, T_D and S_U, T_U are shown in Fig. 11 (a) and (b), respectively. Regarding this figure, the peak value of blocked voltage of S_D, T_D and S_U, T_U are equal to $200V$ and $45V$, respectively. Fig. 11 (c) and (d) present the blocked voltage of the switches S_{M1}, S_{M4} and S_{M2}, S_{K2}, respectively. The peak value of blocked voltage of switches S_{M1}, S_{M4} and S_{M2}, S_{K2} are equal to 80V and 500V, respectively. Also, the blocked voltage of switches S_{M3}, S_{M6} and S_{M5}, S_{K1} are indicated in Fig. 11 (e) and (d) respectively. Considering these figures, the peak values of blocked voltage of power switches S_{M3}, S_{M6} and S_{M5}, S_{K1} are equal to $480V$ and $500V$, respectively. According to the provided experimental results, the total voltage of utilized power switches of proposed 25-level inverter is 3610V. Regarding Table IV, the number of ON power

switches in current path is five. Considering experimental results, the value of input and output powers are 517W and 500W, respectively. The calculated efficiency of the proposed 25-level inverter is 96.54%.

To evaluate the transient behavior of the inverter topology, in this section, the output load current has suddenly changed from 0 to 70% of the nominal power and the results are shown in Fig (12). Fig 12 (a) shows the dynamic behavior of the converter when this sudden change has been applied, and the system is working seamless after applying a 70% sudden change. In the second scenario, a sudden change has been applied and the output power has been changed from 70% of nominal load to 100% nominal load. Fig 12 (b) shows the dynamic behavior of the converter when this sudden change has been applied, and the inverter is still generating 25 levels of voltage after applying a 30% sudden change when the inverter was working on its peak power.



(a) (b)

Fig. 12. Experimental result of the transient analysis of output voltage and current for load change (a) from 0 to 70 % of nominal load, (b) from 70% of nominal load to 100% nominal load

A. Capacitor Charging Inrush Current

Switched-capacitor circuits or similar circuits which utilize capacitors in their topology, have start-up issues and pre-charging of the capacitors. If the start-up inrush current is not limited/controlled, it will damage the power electronic elements on the capacitor charging path. There are two main solutions for this issue, first one is to use Negative Temperature Coefficient (NTC) thermistor, which is a passive solution and can be used in lower power applications. NTC Thermistor shows a large amount of resistance when starting the charging of capacitors, which limits the capacitor inrush current. The second solution for this issue is to use a power relay in parallel to a resistor, which is also called the active damping method. In this method, when starting the capacitor charging, the resistance is in the current path and the relay is turned off, when the capacitors are charged by their nominal voltage, the relay is triggered and bypasses the resistance to decrease the power loss. Both these methods are shown in the Figure 13.

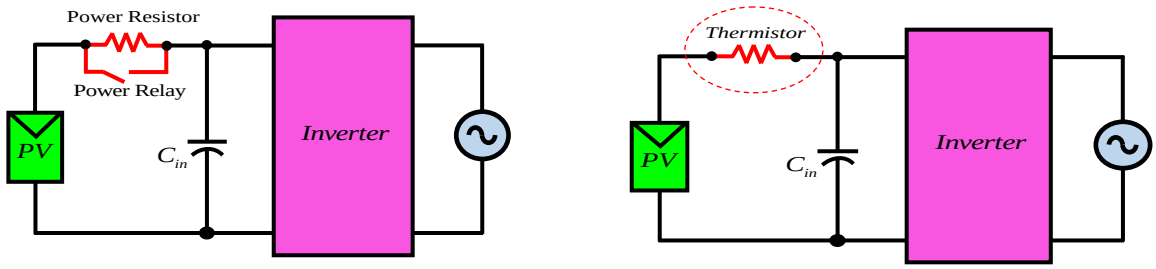


Fig. 13. Active and Passive methods to control the capacitor charging inrush current. A) Active damping circuit using a relay b) Passive NTC thermistor damping method

IX. Conclusion

A new structure of generalized cascaded switched capacitor multilevel inverter based on the cascaded connection of several switched capacitor units is presented in this paper. This structure is recommended for high voltage applications since all utilized switches stand a voltage lower than the peak output voltage. A merit for this proposed structure is the fact that, using switched capacitor units, it can boost the magnitude of the input power sources. To improve the output power quality while generating maximum number of voltage levels at the output based on minimum number of elements, an optimization technique has been utilized. Other advantages of the suggested structure are highlighted through various comparison with the structures suggested in the recent literate. The results have indicated the improved performance of the suggested structure based on reduced components count and maximum voltage on the utilized power switches. Several experimental results for the 25-level inverter are obtained to validate the performance of the proposed inverter. Last but not the least, is the fact that recommended 25-level inverter would be a preferable solution for applications in photovoltaic systems.

Appendix

The topologies for different multilevel topologies presented in the comparison tables are provided in the appendix for the ease of access.

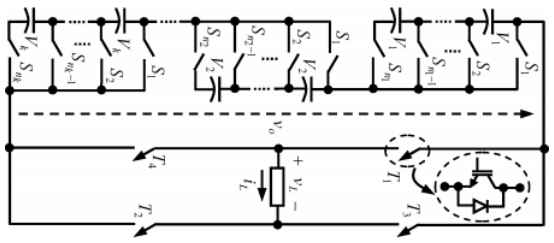


Fig. 14. Topology Presented in Reference [24]

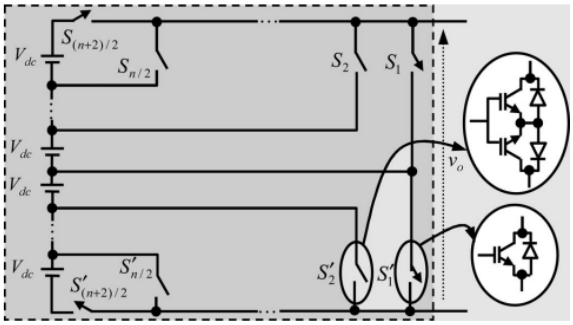


Fig. 15. Topology Presented in Reference [25]

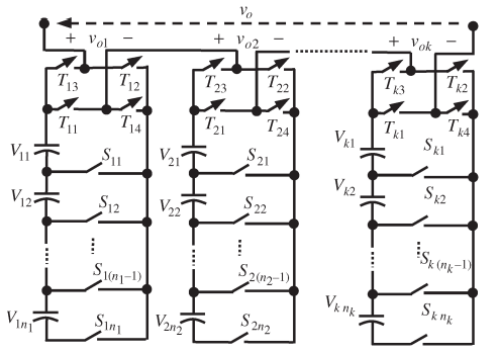


Fig. 16. Topology Presented in Reference [26]

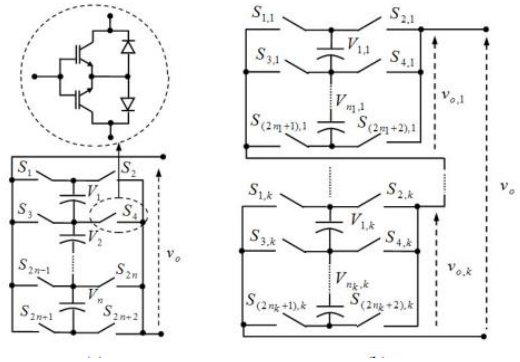


Fig. 17. Topology Presented in Reference [27]

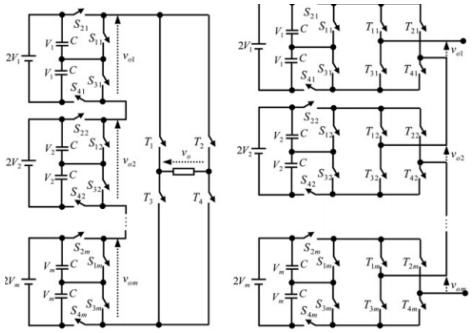


Fig. 18. Topology Presented in Reference [33]

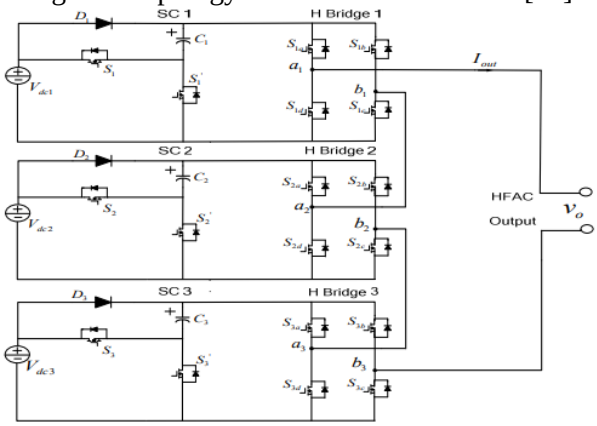


Fig. 19. Topology Presented in Reference [36]

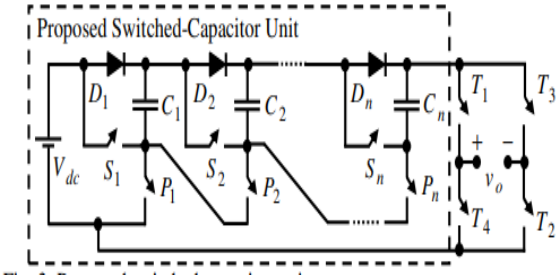
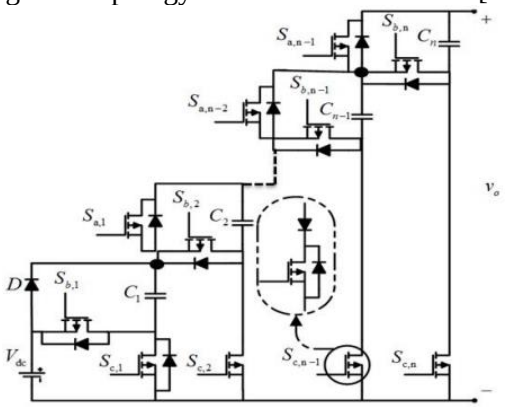


Fig. 20. Topology Presented in Reference [37]



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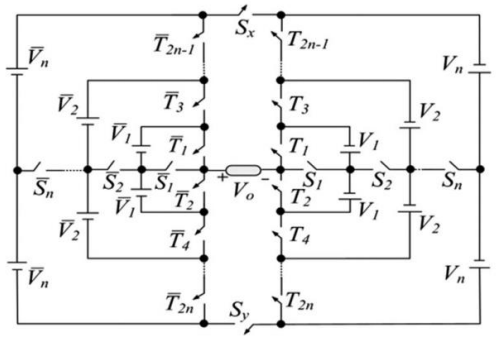

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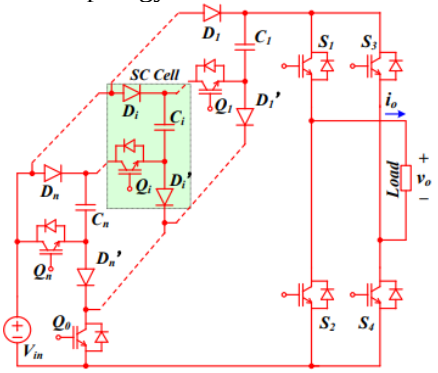

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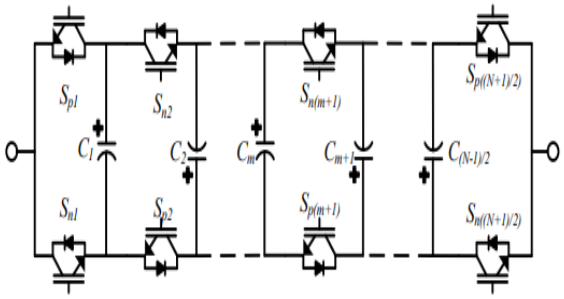

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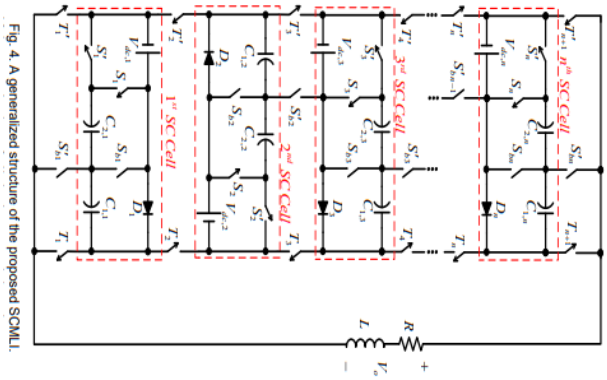

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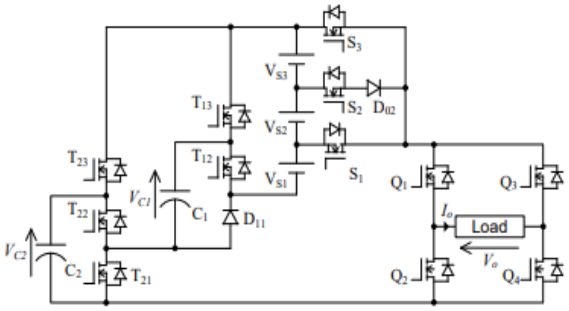

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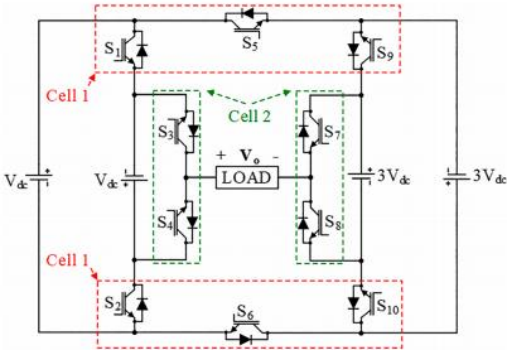

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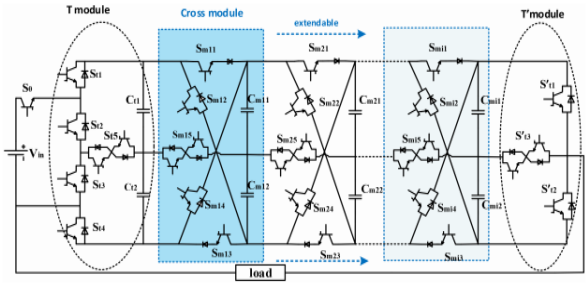

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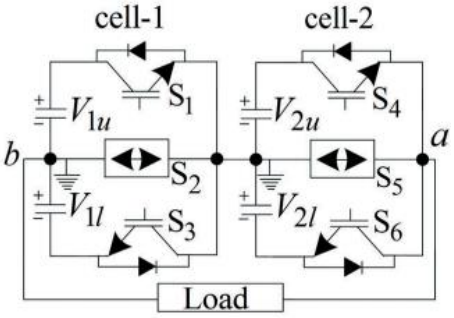

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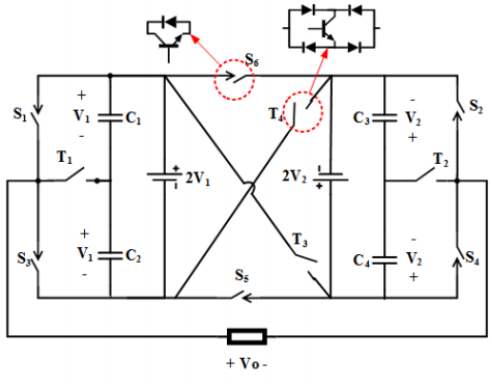

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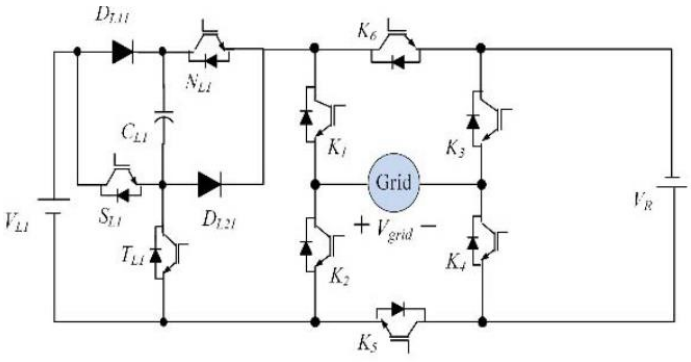

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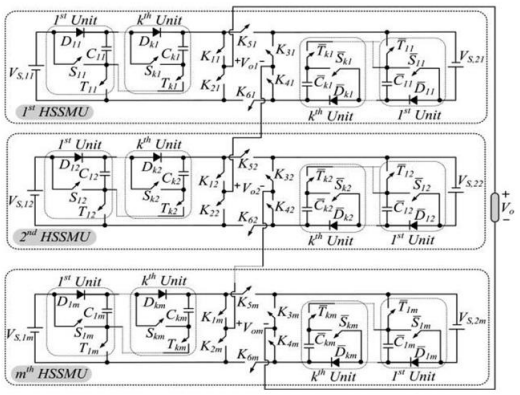

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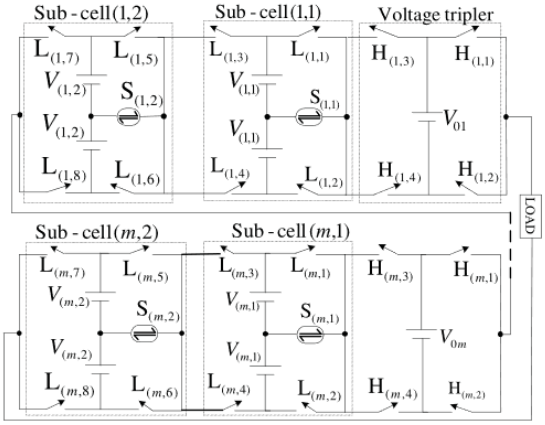

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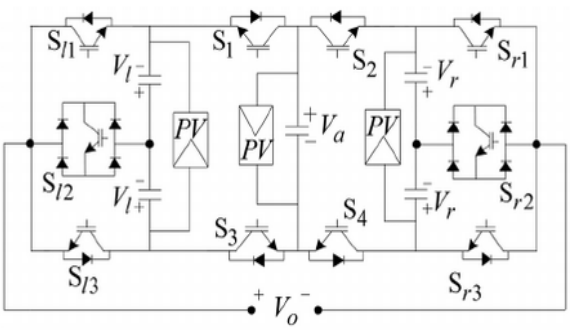

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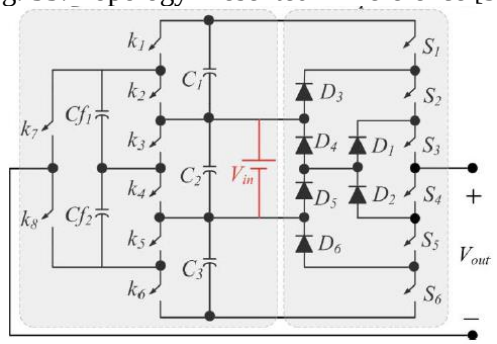

Fig. 35. Topology Presented in Reference [56]

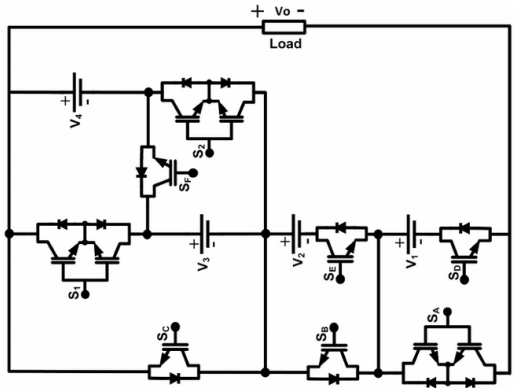

Fig. 36. Topology Presented in Reference [57]

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