Customized Converter for Cost-Effective and DC-Fault Resilient HVDC Grids

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Abstract

This paper presents a comprehensive study that aims to establish the meaningful range for the ratios of full-bridge cells to the total number of cells per arm, in which the performance of the mixed cells modular multilevel converter (MC-MMC) can be customized by trading the number of FB cells for high value features such as: resiliency to DC faults, reduced capital costs of DC circuit breakers (DCCBs) and running costs of the semiconductor, and continued operation. The MC-MMC design for particular ratio of FB cells to total number of cells per arm to achieve tailored features at system level is termed as an customized modular multilevel converter (CMMC). The primary motivation for the CMMC is to facilitate the use of low-cost and relative slow mechanical DC circuit breakers, with fault isolation times in the order of 8 ms to 12.5 ms. With these objectives to be achieved, interruption of power flows across the DC grid and surrounding AC grids must be minimized. It has been found that after certain ratios of FB cells to total cells per arm, the CMMC starts to exhibit current limiting mode, which helps to reduce DCCBs current breaking capacities and extend critical fault clearance times for remote converters from the fault point. Results of the pole-to-ground and pole-to-pole DC faults, semiconductor loss studies, and extended control range indicate that the presented CMMC is promising for future realization of DC grids.

Keywords: HVDC, Hybrid converter, DC faults, PQ envelope

1. Introduction

High-voltage direct current (HVDC) grid represents an important step towards efficient utilization of electricity generated from massive and diverse renewable energy resources, which are spread over wide geographical areas[1, 2]. With HVDC grids, the variation of the peaks of power generation from diverse

Nomenclature

α_{DC}	DC modulation index	N_{hb}	Total number of HB cells in an arm
γ	FB over HB cell ratio	s_{cell}	Cell switching function
$\overline{V}_c$	Average total arm capacitor voltage	V_{diff}^{Δ}	Differential arm voltage
C_{cell}	Cell capacitor	$V_{arm}^{\sum}$	Total phase voltage
E_{fb}	FB chainlink energy	$V_{fb}^{\sum}$	Total FB voltage
E_{hb}	HB chainlink energy	$V_{hb}^{\sum}$	Total HB voltage
i_{arm}	Arm current	V_{AC}	AC voltage
i_{cell}	Cell switching current	v_{arm}	Arm voltage
M	Modulation index	v_{cell}	Cell voltage
m	Modulation function	V_{DC}	DC voltage
N	Total number of cells in an arm	$V_{fb,CL}$	FB chainlink voltage
N_{fb}	Total number of FB cells in an arm	$V_{hb,CL}$	HB chainlink voltage

renewable energy resources in different geographical areas in seasonal manner may lead to substantial reduction in the need for expensive energy storage systems (ESSs), detrimental impacts on stability of connected AC grids during major transient events[3].

In recent years, a wider consensus has emerged both in the industry and academic literature with regard to the construction of HVDC grids, particularly around the voltage source converter (VSC) technologies[4, 5, 6, 7]. This consensus is supported by the following:

- Active or DC power reversal at one or multiple converter terminals is achieved with change of DC current polarity, thus no interruption is caused to the power flows across the DC grid as expected in current source converter (CSC) based DC grids.

- Resiliency to AC faults and improved controllability over active and reactive powers enhance stability of surrounding AC grids.

- Ease of scalability and high-reliability and efficiency of the recently developed modular type VSCs support the global ambitions of multi-gigawatt-scale offshore and transnational HVDC grids with

high availability.

It is worth highlighting that the majority of VSCs developed in the last two decades offer several attractive features well-suited for HVDC grids, and different levels of resiliency against DC faults[8]. However, the VSC resiliency against DC faults comes at the expense of increased running cost of semiconductor losses over the project lifetime[9, 10]. Therefore, a significant research effort has been invested in the development of a range of DC fault-proof converters and dedicated DC fault ride-though and protection strategies for HVDC grids.

Most DC fault-proof VSCs populate their arms with symmetrical and asymmetrical bipolar cells, with FB-MMC and MC-MMC being representative of the former and the latter, respectively [8, 11]. As the DC short-circuit-resilient VSCs were merely motivated by protecting the converter station equipment, the global view on modern power systems considers that converter protection and overall system stability go hand by hand, to achieve uninterruptible power-flow and blackout avoidance[12]. Therefore, to complement the actions of the converters, several hybrid and mechanical DC circuit breakers (DCCBs) have been developed, targeting fault critical times ranging from 2 ms to 12.5 ms. These DCCBs have necessitated developments of highly and partially selective DC fault protection and ride-through control methods[13, 14]. Many solutions have been proposed, which put forward the use of reduced number of DCCBs in combination with AC circuit breakers (ACCBs) in an effort to prioritize the reduction of DC grid protection cost over continued operation[15].

Generally, there are three competing approaches widely discussed in the open literature for handling DC faults in multi-terminal DC grids:

Incorporation of fast acting DCCBs into each DC line of the DC grid to isolate the faulty section. However, this approach increases the capital cost of DC grids[2]. As the ACCBs are essential for fault isolation in conventional AC grids, similarly, DCCB is a key component of future HVDC grids.

The use of limited number of DC/DC converters to split a HVDC grid into several strategic protection zones that operate at the same or different DC voltage. In this way, the DC fault impact will be contained within a well-defined protection zone, and the healthy zones will continue to operate with the same or adjusted level of power transfer compared to pre-fault condition. However, the use of DC/DC converters increases the capital and operational costs due to losses, as most of these topologies use multiple conversion stages[16].

Several DC fault blocking converters have been put forward as viable means of minimizing or eliminating the impact of DC faults on the connected AC grids, however, despite the elevated level of operational

losses, they compromise DC grid continued operation[8, 17]. Therefore, such an approach could be justified only for use in less critical power corridors, and certain scenarios, in which the costs of losses could be overlooked or traded for citizens welfare[9]. This approach prioritizes converter protection over wider stability of the connected AC grids, which will be affected by extended period of active power mismatch should the entire power exchange across the DC grid drop to zero[18].

Based on the above discussion, it can be concluded that DC fault isolation using DCCBs is the most practically attractive and in line with business as usual practices in protection of interconnectors, and it is therefore expected to be applied to meshed multi-terminal HVDC grids[19]. Moreover, it is worth stressing that the existing fast acting DCCB technologies with operating times in the order of 2 ms to 3 ms, do not allow for cost-effective designs (comparable to that of equivalent ACCBs)[20, 21]. Additionally, a DCCB must be upgradable to account for possible DC grid future expansion to cope with the elevated levels of DC fault currents. Although it is possible to restrict the rise of DC fault current with the aid of DC inductors, their size should be very large to restrict the fault level and breaking capacities of DCCBs[22, 23]. However, large current limiting DC inductors are less attractive as they increase control interactions between high-level system controllers[23].

This paper presents an customized modular multilevel converter (CMMC), in which the number of FB cells to be incorporated into the arms of the half-bridge modular multilevel converter (HB-MMC) are traded for bespoke and invaluable features from a wider system point of view. Structurally, the proposed CMMC could be similar or distinctly different from the conventional mixed-cells modular multilevel converter (MC-MMC)[24, 25]. Hence, the CMMC is put forward in an attempt to reduce the design requirements for the DC circuit breakers, by extending fault clearance times, suitable for mechanical DC circuit breakers[26], and achieving substantial reduction in the magnitude of the DC fault currents to be interrupted. Comprehensive studies show that after a certain proportion of FB cells, the CMMC exhibits current limiting capability, which can help to reduce the current breaking capacity of potential DCCBs. In addition, the CMMC facilitates asymmetrical monopole operation during pole-to-ground (P2G) DC faults, without exposing healthy DC cables and interfacing transformers to excessive DC voltage stresses. Moreover, simulation results show that the expanded P-Q envelope of the proposed CMMC can support operation in weak AC grids[27]. Therefore, this paper demonstrates the technical viability of the CMMC, with particular emphasis on extension of fault clearance times during pole-to-pole (P2P) DC short circuit to levels compatible with the speed of mechanical DCCBs, and facilitation of controlled asymmetric monopole operation during P2G DC faults. The main findings and observations drawn from these comprehensive studies are presented and

contextualized.

The rest of the paper is organized as follows: Section 2 presents the fundamentals and a basic analysis of the CMMC. Section 3 presents an analysis of the CMMC behavior during pole-to-ground and pole-to-pole faults. Section 4 presents a series of quantitative studies which aim to establish the minimum number of FB cells per arm beyond which the CMMC starts to become practically meaningful. Section 5 presents studies that assess the semiconductor losses and associated costs for various ratios of FB cells per converter. Section 6 provides a relative comparison for various FB cell ratios and discussions and finally, section 7 presents the conclusions.

2. customized Modular Multilevel Converter

2.1. Fundamental operation

Fig. 1 shows a generic one phase-leg of the CMMC, in which each of the arms consists of FB and HB chainlinks, which are formed by series connection of FB and HB cells respectively. For an CMMC with an arbitrary ratio $\gamma = \frac{N_{fb}}{N}$, the FB and HB chainlinks in each arm can sustain DC voltages of γV_{DC} and $(1-\gamma)V_{DC}$, respectively, where N_{fb} is the number of FB cells and N is the total number of cells per arm. Therefore, the CMMC requires new dedicated controllers to ensure that the voltages across the FB and HB chainlinks are tightly controlled at γV_{DC} and $(1-\gamma)V_{DC}$, in order to avoid excessive voltage stresses on the semiconductors and capacitors of the FB and HB cells. As in other MMCs, the CMMC uses per arm sorting based capacitor voltage balancing to ensure that the total DC voltage across the arm is evenly distributed between the cell capacitors of the HB and FB cells, i.e., $\frac{\overline{V_c}}{N}$; where V_c denotes the sum of FB and HB capacitor voltages per arm. In this paper, a capacitor voltage balancing is employed for the CMMC, which is not significantly different from that of the conventional HB-MMC, except it distinguishes the FB cells from the HB cells, for the sole purpose of prioritizing the use of FB cells during controlled operation with reduced DC voltage, in which a particular number of selected FB cells (based on their capacitor voltage magnitudes and arm current polarity) are inserted with negative polarity. The negative part of modulating function that is displayed in Figure 2 defines the numbers of FB cells to be inserted with negative polarity during reduced DC voltage operation. High-frequency pulse width modulation or a version of amplitude modulation (nearest voltage level modulation or tolerant band) can be used with the CMMC to define the total number of cells to be inserted and bypassed from each arm during each modulation or sampling period. However, the nearest voltage level modulation is adopted in this paper for simplicity of implementation and scalability. Also, the upper and lower arms of each phase-leg of the CMMC conduct simultaneously, in

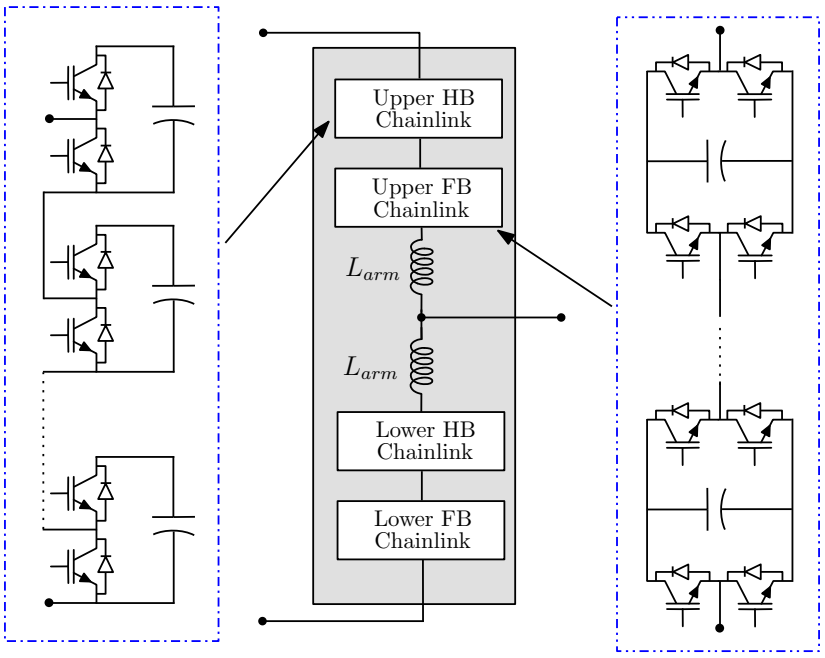


Figure 1: Multilevel HVDC converter topologies.

which the cell insertion and bypass patterns in the upper arm complement those of the cells in the lower arm. In this way, the upper and lower arms of the same phase-leg synthesize a common-mode voltage that is slightly higher or lower than the imposed pole-to-pole DC voltage to allow a DC current flow from/to the converter, and a differential-mode voltage that is equal to the fundamental phase voltage, as in the conventional MMC.Compared to the conventional MC-MMC, the CMMC offers tailored converter design, in which the ratio of the FB cells to the HB cells is used to achieve trade-offs between losses and specific control objectives at system level. A generic arm voltage of modular type converters can be approximated by:

$$v_{arm}(t) = \frac{1}{2}\overline{V}_c(M \cdot \cos(\omega t + \delta) + \alpha_{DC}) \tag{1}$$

where M and α_{DC} is the amplitude of AC and DC modulation indices, respectively. Modulation index M defines the amplitude of fundamental AC voltage, and it varies in the range $0 < M < 1$. The DC modulation index α_{DC} varies with the input DC voltage and defines the amount of negative voltage to be produced by each arm, according to the blocking voltage of the installed FB cells. In the CMMC, the DC modulation is selected for a bespoke control range. The relationship between the range of α_{DC}, the DC voltage range V_{DC} and the average virtual DC voltage of each arm $\overline{V}_c$ is shown in (2), while the DC modulation index varies within the range of $-\alpha_{DC-min} < \alpha_{DC} < 1$:

$$\alpha_{DC} = \frac{V_{DC}}{\overline{V}_c} \tag{2}$$

The relationship between the minimum DC modulation index and FB chainlink blocking voltage per

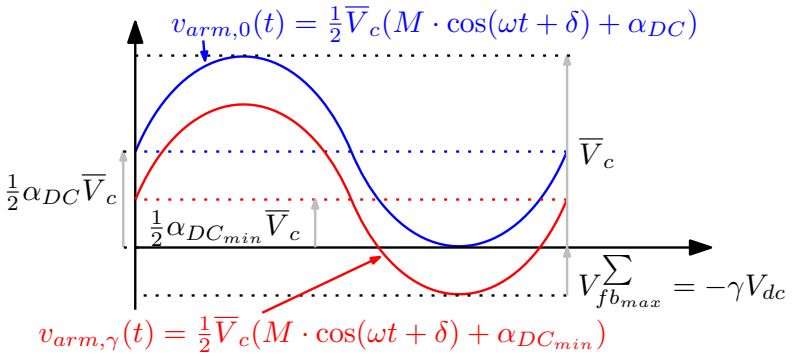


Figure 2: Arm modulation signals of CMMC.

arm is:

$$\alpha_{DC-min} = 1 - 2\gamma \tag{3}$$

where α_{DC-min} is the minimum DC modulation index for given a $\gamma = \frac{V^{\sum}_{fb}}{V_{DC}}$ which is the ratio of FB cells per arm to total number of cells per arm.

The general relationship that describes the range of DC link voltages in which the CMMC can still remain controllable for a given γ is:

$$(1 - 2\gamma)\overline{V_c} < V_{DC} < \overline{V_c} \tag{4}$$

Fig. 2 shows generic arm voltages of the CMMC for two different DC modulation indices ($v_{arm,0}$ when γ = 0 and $v_{arm,\gamma}$ for a given value of γ) when the combined blocking voltage of each CMMC arm is regulated at the nominal DC link voltage $\overline{V_c} = V_{DC}$. Thus, the CMMC can synthesize the AC voltage imposed by the AC grid as long as the DC link voltage remains within the range defined by the above inequality.

2.2. Control systems

This section provides a brief description of the CMMC control systems.Subscript j defines the phase index (i.e. j = a, b, c) and k defines the upper and lower position of the arm (i.e. k = u for the upper arm and k = l for the lower arm). A generic arm of the CMMC is considered, where the current of each cell capacitor of the FB and HB cells can be described in terms of arm current and their respective switching functions as:

$$i_{cell,hb,k} = S_{cell,hb,k} \cdot i_{arm,k} \tag{5}$$

$$i_{cell,fb,k} = S_{cell,fb,k} \cdot i_{arm,k} \tag{6}$$

where $S_{cell,fb,k}$ and $S_{cell,hb,k}$ are switching functions of arbitrary FB and HB cells, which have values of 0 or 1.

It is assumed that the HB and FB cells of the CMMC employ the same cell capacitance, which is sized on similar basis as the conventional MMC as described in (7).

$$C_{cell} = \frac{N \cdot S_n \cdot H}{3 \cdot V_{DC}^2} \tag{7}$$

where N is the total number of HB or FB cells per arm, S_n is the nominal apparent power, H is the converter inertia or time constant, which typically ranges from 30 ms to 40 ms (in other words 30 kJ/MVA to 40 kJ/MV).

Each arm voltage v_{arm} comprises of a summation of the FB and HB chainlink voltages $V_{fb,CL}(t)$ and $V_{hb,CL}(t)$, as a function of the cell current $i_{cell,k}$ and the cell capacitance C_{cell} as follows:

$$v_{cell,hb,k}(t) = \frac{1}{C_{cell}} \cdot \int \left(i_{cell,hb,k}(t) \right) dt \tag{8}$$

$$v_{cell,fb,k}(t) = \frac{1}{C_{cell}} \cdot \int \left(i_{cell,fb,k}(t) \right) dt \tag{9}$$

$$v_{arm,k} = \sum_{n=1}^{N_{hb}} \left[s_{cell,hb,k} \cdot v_{cell,hb,k} \right] + \sum_{n=1}^{N_{fb}} \left[s_{cell,fb,k} \cdot v_{cell,fb,k} \right] \tag{10}$$

or simply:

$$v_{arm,k} = V_{hb,CL,k} + V_{fb,CL,k} \tag{11}$$

As in conventional MC-MMC, the DC link voltage, V_{DC}, and phase AC voltage, V_{AC}, can be described in terms of instantaneous upper and lower arm voltages of the same phase leg as:

$$V_{DC} = v_{arm,u} + v_{arm,l} \tag{12}$$

$$V_{AC} = v_{arm,u} - v_{arm,l} \tag{13}$$

where $v_{arm,u}$ and $v_{arm,l}$ are the upper and lower arms of the same phase.

In the conventional MMC, the horizontal energy/voltage controller regulates the average energy/voltage of each arm and therefore, it allows the cell capacitor voltages to be decoupled from the DC link voltage[28]. However, adoption of such an approach in CMMC that is characterized by unequal blocking voltages of the HB and FB chainlinks, may lead to incorrect voltage distribution between the arm HB and FB chainlinks. Therefore, an alternative horizontal controller is employed, which regulates explicitly the total DC voltages across the HB and FB chainlinks of each arm at $(1-\gamma)V_{DC}$ and γV_{DC} respectively. A zero energy exchange between the HB and FB chainlinks and AC and DC sides is achieved, as described in (14) and (15).

$$E_{hb,k} = \int_0^T \left(V_{hb,CL,k} \cdot i_{arm,k}(t) \right) dt = 0 \tag{14}$$

$$E_{fb,k} = \int_0^T \left(V_{fb,CL,k} \cdot i_{arm,k}(t) \right) dt = 0 \tag{15}$$

The DC offsets of the modulating signals of the HB and FB chainlinks, m_{hb} and m_{fb}, are manipulated through the proposed HB and FB capacitor voltage controllers to ensure zero net energies are exchanged with both AC and DC sides. The modulation indices m_{hb} and m_{fb} are adjusted according to the ratios $1-\gamma$ and γ, corresponding to HB and FB chainlinks contribution to the total arm voltage, consisting of the total HB $V_{hb}^{\sum}$ and FB $V_{fb}^{\sum}$ chainlink voltages as described in (16) and (17).

$$V_{hb,k}^{\sum} = \sum_{i=1}^{N_{hb}} v_{cell,hb,k} \tag{16}$$

$$V_{fb,k}^{\sum} = \sum_{i=1}^{N_{fb}} v_{cell,fb,k} \tag{17}$$

The required measured quantities for the control of the FB and HB chainlinks are calculated as follows:

$$V_{arm.k}^{\sum} = V_{hb,k}^{\sum} + V_{fb,k}^{\sum} \tag{18}$$

$$V_{diff}^{\Delta} = V_{arm,u}^{\sum} - V_{arm,l}^{\sum} \tag{19}$$

$$\overline{V}_c = \frac{1}{2}(V_{arm,u}^{\sum} + V_{arm,l}^{\sum}) \tag{20}$$

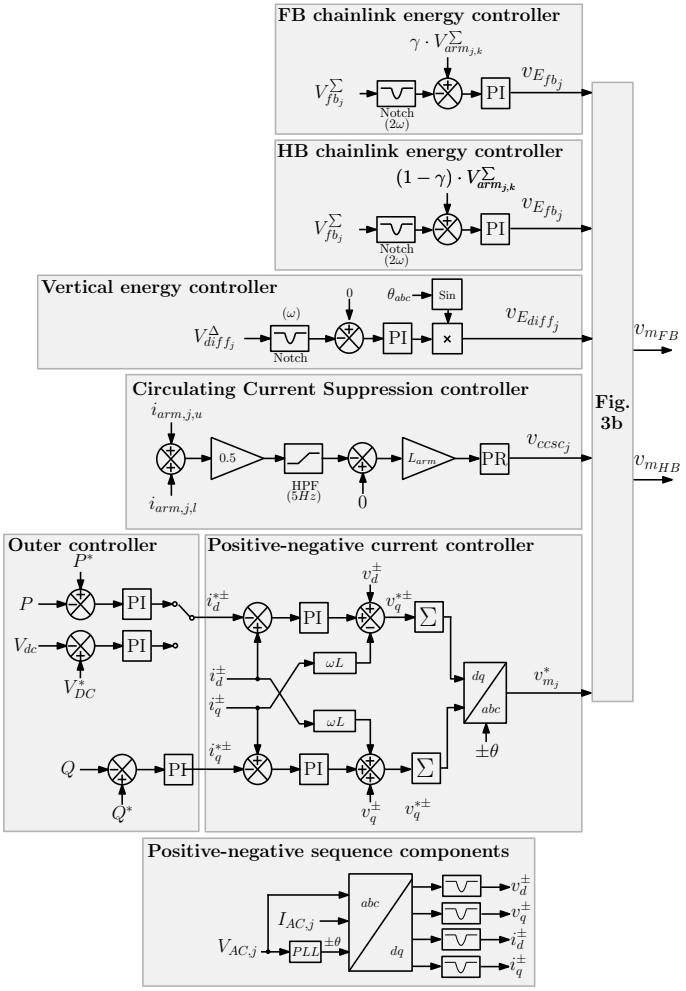
Where $V_{arm,u}^{\sum}$ and $V_{arm,l}^{\sum}$ are the sum of the capacitor voltages for the upper and lower arms. In summary, the overall control system in Fig. 3 is described as follows:

The top two subsystems in Fig. 3(a) are the controllers that allow the total DC voltage across the HB and FB chainlinks of each arm to be regulated individually, replacing the conventional implementation of horizontal voltage controllers. The third subsystem in Fig. 3(a) from the top is the per phase vertical voltage controller that ensures that the total DC voltages across the upper and lower arms of each phase-leg are equal. This controller injects a small fundamental current into common-mode loop to interact with the fundamental voltage of the arm and produce the required active power to force equalization of the upper and lower arm voltages. The fourth subsystem in Fig. 3(a) from the top is the per phase circulation current suppression controller, which is tuned to target the second-order harmonic currents in each arm of the CMMC. The bottom subsystem in Fig. 3(a) depicts the outer controllers (active power/DC voltage and reactive power) and inner positive and negative current controllers that define the phase and magnitude of AC modulating functions to be used to control the HB and FB chainlinks. The subsystems in Fig. 3(b) show the synthesis and normalization of the modulation functions of the HB and FB chainlinks, in which adjustment of DC offsets is carried out with the aid of the controllers that regulate the total DC voltage across the HB and FB chainlinks.

3. DC Faults Handling in CMMC

3.1. DC Ground-to-pole fault

Assuming that the voltage measured from the positive and negative DC P2G of a symmetrical monopole HVDC systems are $V_{DC,P}$ and $V_{DC,N}$ respectively, the output phase AC voltage relative to grounding $V_{AC,0}$



(a)

(b)

Figure 3: Proposed controller for CMMC with asymmetrical ratio of HB and FB chainlinks (a) Main controller, (b) Normalization.

can be expressed as:

$$V_{DC-P} = v_{arm,u} + L_{arm} \cdot \frac{di_{arm,u}}{dt} + V_{AC,0} \tag{21}$$

$$V_{DC-N} = v_{arm,l} + L_{arm} \cdot \frac{di_{arm,l}}{dt} - V_{AC,0} \tag{22}$$

Subtracting (22) from (21) and neglecting the voltage drops in the upper and lower arm reactors yields:

$$V_{AC} = \frac{1}{2}(V_{DC,P} - V_{DC,N}) - \frac{1}{2}(v_{arm,u} - v_{arm,l}) \tag{23}$$

A P2G DC fault on the negative pole of a DC cable will force $V_{DC,N}$=0 and $V_{DC,P} = V_{DC}$, thus (23) becomes:

$$V_{AC} = \frac{1}{2}V_{DC} - \frac{1}{2}(v_{arm,u} - v_{arm,l}) \tag{24}$$

Expression (24) indicates that the output phase AC phase voltage $V_{AC,0}$ develops a DC bias of $\frac{1}{2}V_{DC}$, which exposes the interface transformer to increased stresses and risk of insulation failure. This phenomenon appears during a P2G DC fault, regardless of grounding arrangement and transformer connection[29].

To relief the healthy pole and converter transformer from excessive DC voltage stresses, the DC modulation index of the CMMC is autonomously adjusted, dominantly by the controllers that exclusively regulate the total DC voltage across the FB chainlinks, and the P2P DC voltage is halved during P2G DC faults. Based on Eq. (4), $\gamma = 0.25$ is the minimum ratio required to facilitate continuous P2G DC fault operation. After normalization of Eq. (1) by $\overline{V}_c$, the upper and lower arm modulation functions become:

$$\begin{cases} m_{arm,u}(t) = \frac{1}{2}(M\cos(\omega t) + \alpha_{DC}) \\ m_{arm,l}(t) = \frac{1}{2}(M\cos(\omega t + \pi) + \alpha_{DC}) \end{cases} \tag{25}$$

This entails that the DC modulation corresponding to 50% reduction in DC voltage is $\alpha_{DC} = 1 - 2\gamma = 0.5$.

3.2. Pole-to-pole DC fault

This section puts forward a P2P DC fault ride-through method for the CMMC that aims to facilitate continuous operation of DC grids where is possible, primarily by extending the fault clearance times for the remote converters from the fault point. The enhanced DC fault ride-through of the CMMC is realized through the customized design of γ, from which the FB chainlinks reverse voltage capabilities are exploited to reduce the required current breaking capability of the DC circuit breakers and the current stresses in the converter semiconductor switches. The response of the CMMC to a P2P DC fault can be characterized by three stages:

1) The first stage covers the period from fault inception to the point at which the converter loses control, when its input DC link voltage drops below the peaks of the AC line-to-line voltages. The fault current in

this stage is largely dominated by transient discharge currents originating from the distributed capacitors of the DC lines or cables plus the HB and FB cell capacitors. In a typical multi-terminal HVDC grid, this stage can be extremely short for the converters near to the fault, and relatively longer for converters far from the fault point. It is possible to extend this stage further by installing large current limiting DC inductors at strategic locations in the DC grid to slowdown the rate-of-rise of fault currents.

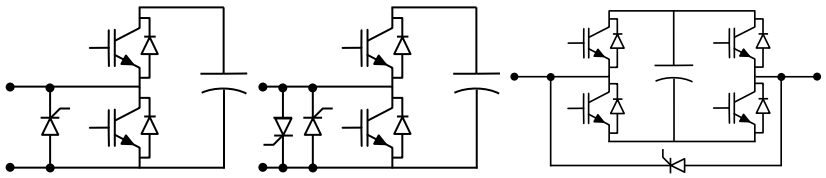
2) The second stage starts with the blocking of the fractionally rated FB chainlinks and HB chainlinks, in an effort to suppress the fault currents in the converter arms, while the DC current is interrupted by the DC circuit breakers. This stage ends with the bypass of the FB chainlinks when the FB cell capacitor voltages hit a predefined overvoltage threshold. Two variants on the HB cell bypass configuration provide different current profile behavior:

- The composite IGBT that bypasses the capacitor of each HB cell is reinforced by a diode or thyristor, as shown in Fig. 4(a). In this case the rectified AC side currents contribute to the magnitude of the DC fault currents.

- The composite IGBT that bypasses the capacitor of each HB cell is reinforced by back-to-back thyristors, as shown in Fig. 4(b). The arm currents remain largely AC side currents, and therefore do not contribute significantly to DC fault currents. However it requires additional number of semiconductors.

In both implementations, the HB cell capacitors maintain the voltage constant blocking, while the FB cells will be charged to $\frac{\sqrt{3}\hat{V}_{AC}}{\gamma N_{fb}}$ if no counter measures are put in place.

3) The third stage will be initiated only when the FB capacitor voltages exceed a specified overvoltage threshold that will trigger the FB cells bypass as shown in Fig. 4(c). This stage represents a last resort protection for the converter semiconductors and capacitors against overvoltages.



(a) (b) (c)

Figure 4: Cell topologies with bypass thyristors (a) HB cell with single bypass thyristor, (b) HB cell with back-to-back thyristor, (c) FB cell.

An approximate analysis for stage two, in which the FB chainlinks are blocked and each HB cell of the HB chainlinks employs the configuration in Fig. 4(a) is presented here. It is assumed that, the overvoltages

due to the blocking process are neglected, and when the $V_{LL} > v_{arm}$ the FB chainlinks conduct. On this basis, the larger the voltage difference between the sum of the upper and lower FB chainlink blocking voltages and the line-to-line AC voltage the AC grid imposes at the CMMC AC terminals, the larger the fault currents. In contrast, the higher the FB chainlink blocking voltage, the smaller the fault currents. Theoretically, if the arm and transformer impedance are neglected, the fault currents drop to zero when the voltage differences that drive the fault currents become zero (when the voltages of the two FB chainlinks in conduction path add to the peak of line-to-line voltage); and beyond this point, controlled operation as typical voltage source converter (VSC) can be achieved. Based on the above premises, the differential equation that describes the electromagnetic transient of the two phases of the CMMC that conduct in each instant in mode 2 is:

$$\sqrt(3)\hat{V}_{AC}sin\omega t - 2v_{fb}^{\sum}(t) = 2(R_T + R_{arm})i_a + 2(L_T + L_{arm})\frac{di_a}{dt} \tag{26}$$

where R_T and R_{arm}, and L_T and L_{arm} are transformer leakage and arm reactor resistances and inductances respectively, $v_{fb}^{\sum}(t)$ is the total voltage of the FB chainlink of each arm, and $\hat{V}_{AC}$ is the peak of the phase voltage. Note that (26) is valid for intervals in which the line voltage such as $v_{ab} = sqrt(3)\hat{V}_{AC}sin\omega t$ is greater than the combined DC voltage that the FB chainlinks present in the conduction path.

From (26), it can be observed that the higher the blocking voltage of the FB chainlinks, the lower the fault current that will be driven towards the converter from the AC grid. Recall that the FB chainlink blocking voltage is equal to the total capacitor voltage per arm and can be expressed as:

$$i_a = C_e\frac{dv_{fb}^{\sum}(t)}{dt} \tag{27}$$

where C_e is the equivalent capacitance per FB chainlink and is given by: $C_e = \frac{C_{fb}}{N_{fb}}$ in which C_{fb} is the capacitance of a single FB cell, and N_{fb} is the number of FB cells per chainlink.

After substituting (27) in (26), the following expression is obtained:

$$\sqrt(3)\hat{V}_{AC}sin\omega t - 2v_{fb}^{\sum}(t) = 2(R_T + R_{arm})C_e\frac{dv_{fb}^{\sum}(t)}{dt} + 2(L_T + L_{arm})C_e\frac{d^2v_{fb}^{\sum}(t)}{dt^2} \tag{28}$$

After solving (27) for complementary and particular solutions and ensuring that the Wronskian exists and that $\frac{4}{L_xC_e} > \frac{R_x^2}{L_x^2}$, the general solution of (28) is:

$$v_{fb}(t) = Ae^{-R_x/L_xt}\sin\omega_0 t + \frac{\sqrt{3}\hat{V}_{AC}\sin(\omega t + \varphi)}{2\omega L_xC_e\sqrt{\left[\omega^2 - \omega_0^2 + \frac{2}{L_xC_e} + \frac{1}{\omega^2L_x^2c_e^2}\right]}} \tag{29}$$

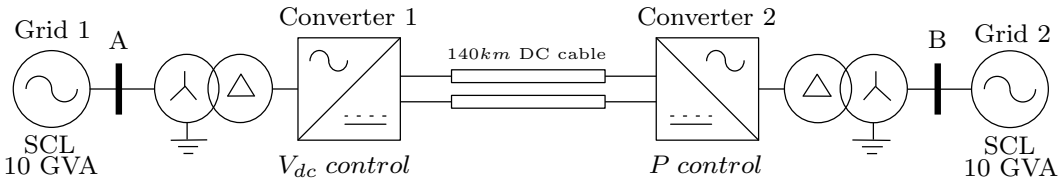


Figure 5: Simulated DC network.

where $\omega_0^2 = \frac{4}{L_x C_e} - \frac{R_x^2}{L_x^2}$, $\phi = tan^-1[\frac{\omega R_x C_e}{\omega^2 L_x C_e - 1}]$ and $R_x = R_T + R_{arm}$ and $L_x = L_T + L_{arm}$. The constants A and B can be determined from the initial conditions.

From 29, the effective resistance and inductance of the conduction path determine the rise time of the capacitor voltages from the base value for given γ; while the inductance and capacitance determine the oscillation frequency during blocking. The arm or phase current in a particular conduction interval can be calculated from (27), in which the rise time and oscillation frequency are influenced by the same parameters highlighted above. The second term, which represents the steady-state component, shows that the final settling point is marginally influenced by the passive parameters (voltage drops in the transformer and arm reactors).

4. Simulation test

Fig. 5 shows a two-terminal HVDC transmission which is used to assess the claimed advantages of the CMMC, using the parameters shown in Table 1. The test system in Fig. 5 is modelled in EMTP-RV, in which converters 1 and 2 are modelled as CMMCs with 20 cells per arm, including all the necessary controllers for ensuring correct operation during normal and abnormal conditions, while frequency dependent model is used for the cables.

To demonstrate the potential benefits that the CMMC can bring to DC fault performance of future DC grids and to the operation of HVDC converters in weak AC grids, the following test scenarios will be discussed in this section:

- Facilitation of continued operation during P2G DC fault.
- Extension of fault clearance time and reduction of fault current during P2P DC faults.
- Extension of converter P-Q envelope and active power limits in weak AC grids.

4.1. Pole-to-ground DC fault

This section presents simulation results that aim to demonstrate the performance of the CMMC with $\gamma = \{0, 0.15, 0.25, 0.5\}$ when a P2G DC fault is applied at the mid-point of the DC cables at t = 1 s. The

Table 1: Rating and design specifications

Parameter	MMC
Apparent power	1045 MVA
DC voltage	640 kV
Grid/Converter LL voltage	400/320 kV
Arm inductance	58.7 mH (18%)
DC inductance	100 mH
Cell capacitor energy	40 kJ/MVA

P2G simulation cases highlighted above are summarized in Table 2 and shown in Fig. 6 and 7.

In order to retain significant power transfer across the link, at least 50% of the rated power at rated current of the DC cable, the DC link voltage of the CMMC with various γ is adjusted according to the minimum DC modulation index for a given γ ($\alpha_{DC-min} \geq 1 - 2\gamma$), which is 640 kV, 448 kV, 320 kV and 320 kV for $\gamma = \{0, 0.15, 0.25, 0.5\}$.

The plots in Fig. 6(a) and (b) show the positive and negative DC cable voltages relative to ground, measured at the fault point. The faulty (positive) pole DC voltage falls to zero during P2G DC fault, while the voltage stress across the healthy (negative) pole varies significantly with γ. The worst-case DC voltage stress on the healthy pole is observed when γ = 0 (typical HB-MMC), and followed by the CMMC with γ = 0.15, where the voltage stress on the healthy pole is increased to 448 kV (1.4 times the rated DC voltage of the cable). While the CMMC with γ = 0.25 and 0.5 (typical MC-MMC) exhibits no overvoltage on the healthy pole. Fig. 6(c) shows the pole-to-pole voltage, where higher values of γ allow increased range of control, and the DC voltage can attain values lower than the peak line-to-line AC voltage. In Fig. 6(d) shows that the DC voltage stress on the insulation of the interfacing transformer varies with γ, and the CMMC with γ = 0 (typical HB-MMC) exhibits the largest DC voltage stress, which amounts to $\frac{1}{2}V_{DC}$ = 320 kV. The CMMCs with γ = 0.15 and 0.25 present DC voltage stresses equal to $\frac{V_{DC}}{2}\alpha_{DC-min}$ = 224 kV and 160 kV

Table 2: Cases for DC pole-to-ground fault.

Case study	Description
S1	0% CMMC (HB-MMC)
S2	15% CMMC at 0.7 p.u. DC voltage adjustment
S3	25% CMMC at 0.5 p.u. DC voltage adjustment
S4	25% CMMC (MC-MMC) at 0.5 p.u. DC voltage adjustment

on the insulations of their respective interfacing transformers. The reductions observed in the transformer DC stresses are due to equal handling of the DC modulation indices of all arms. The MC-MMC achieves complete nullification of the interfacing transformer DC stresses through independent pole control.

Fig. 7 shows the upper and lower voltages of the HB-MMC, CMMC with γ = 0.15 and 0.25 and typical MC-MMC. The results show that the CMMC with γ = 0.15 and 0.25 exploit their limited FB cells to enable operation in over-modulation region, in which the FB cells are used to generate negative voltage levels to be able to recreate any DC voltage between $\frac{V_{DC}}{2}\alpha_{DC-min}$ and V_{DC}. The HB-MMC which uses only unipolar HBs is unable to manipulate its arm voltages to reduce the DC stress on the converter transformer. In contrast, the MC-MMC fully exploits its large number of FB cells to eliminate the converter transformer DC stress by controlling the DC offset of the arm connected to the faulty pole (upper arm) at zero, and the arm which is connected to healthy pole at nominal setpoint. One of the MC-MMC arms generates substantial negative voltages, which can reach $\frac{V_{DC}}{2}$.

In summary, the above analysis, discussion and the results of Fig. 6 and 7 collectively, demonstrate the sufficiency of $\gamma \geq 0.25$ for successful healthy pole-restraining and continued operation when the HVDC system is subject to permanent P2G DC faults, during which the transformer DC stress is greatly reduced,

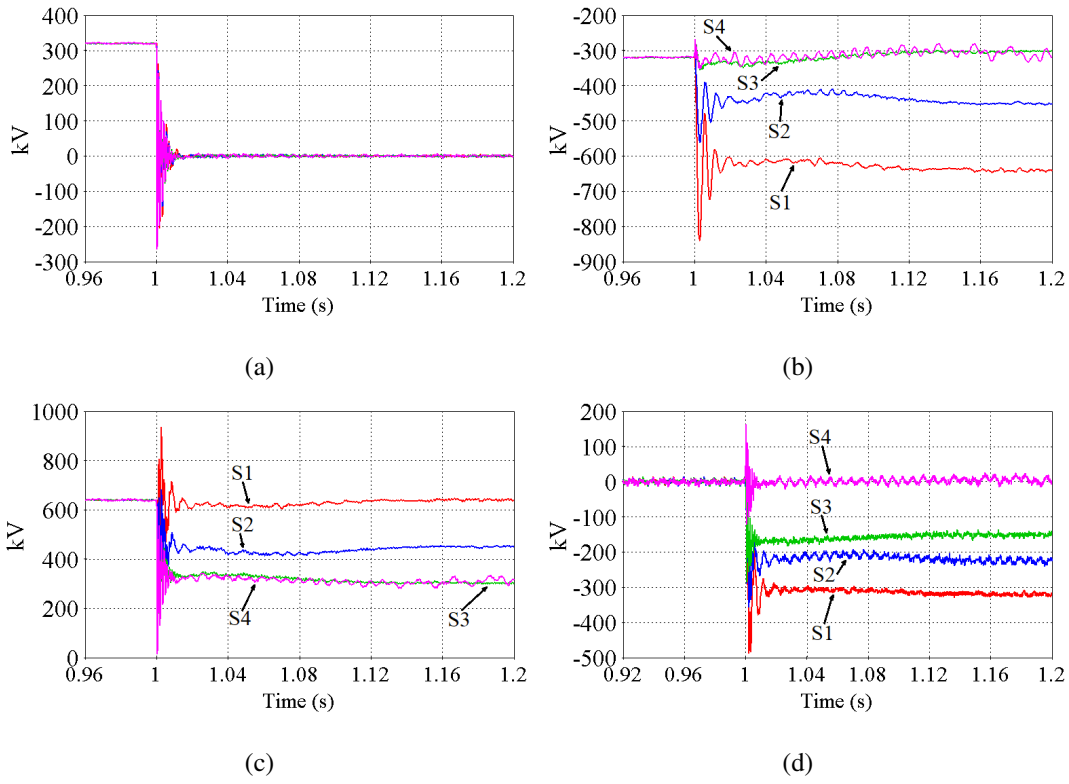


Figure 6: P2G DC fault simulation waveforms for cases highlighted in Table 2: (a) positive pole-to-ground DC voltage (faulty pole), (b) negative pole-to-ground voltage (healthy pole), (c) pole-to-pole DC voltage, (d) DC voltage stresses on the interfacing transformer.

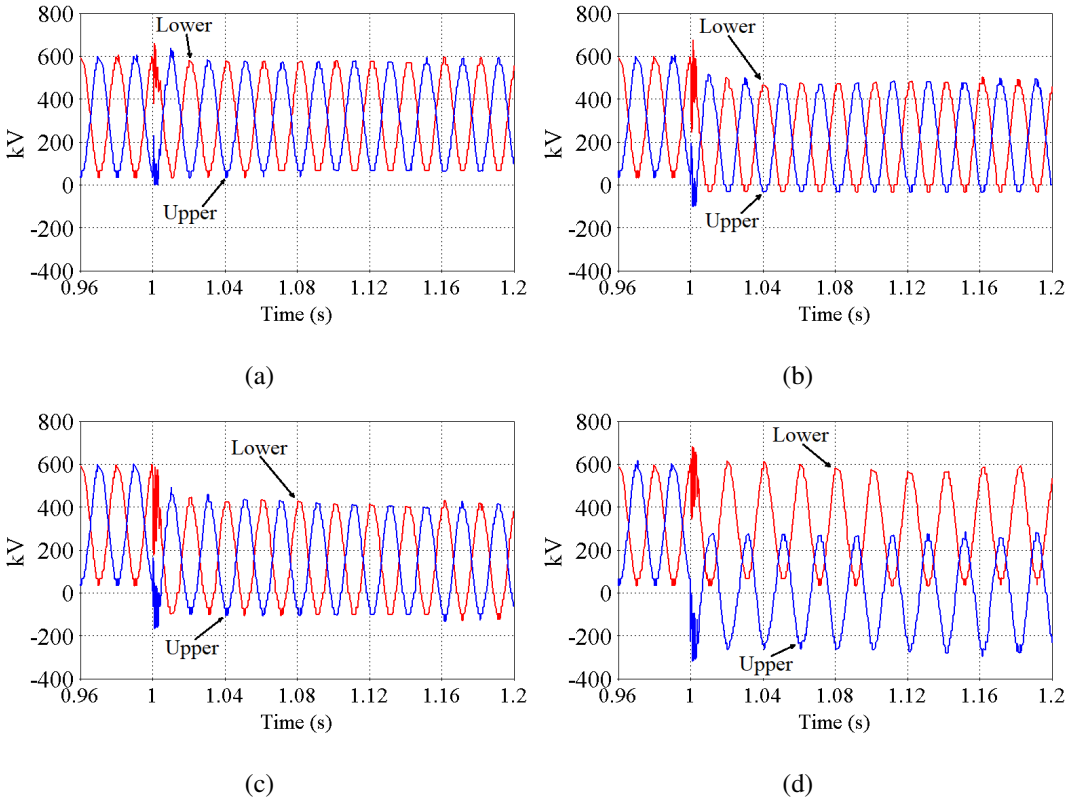


Figure 7: Arm voltages during P2G DC fault for cases highlighted in Table 2: (a) 0% CMMC (HB-MMC), (b) 15% CMMC at 0.7 pu DC voltage adjustment, (c) 25% CMMC at 0.5 pu DC voltage adjustment, (d) 50% CMMC (MC-MMC) at 0.5 pu DC voltage adjustment.

while the use of DC choppers to protect the DC cables is avoided.

4.2. DC pole-to-pole fault

This section assesses the effectiveness of CMMCs in reducing the design requirements of DC circuit breakers, particularly with regards to extension of fault clearance time and reduction of the let-through current and current breaking capacity. The two presented assessment scenarios in this section aim to establish the following:

1) The minimum practical range for γ, beyond which the CMMC can provide meaningful contribution to overall effort with regard to the relaxation of DC circuit requirements stated above. 2) The extent at which the fault critical clearance time can be extended, and the DC circuit breaker fault current breaking capacity can be reduced for various γ ratios.

The arm currents and cell capacitor voltages are normalized by the peak of the rated output phase current $\sqrt{\frac{2}{3}}\frac{S_n}{V_{LL}}$, and rated cell capacitor voltage $\frac{V_{DC}}{N}$ respectively, where V_{LL} represents line-to-line AC voltage at the converter side. In these illustrative scenarios, the performance of γ is assessed according to specified arm over-current and cell capacitor overvoltage thresholds which are set at 1.5 pu and 1.8 pu respectively.

This paper uses arm overcurrent threshold to initiate blocking of the FB and HB chainlinks, and FB cell voltage overvoltage threshold to initiate bypass of the FB chainlinks. Simulation results of converters 1 and 2 are provided, when the HVDC system in Fig. 5 is simulated with the HB chainlinks equipped with single and back-to-back bypass thyristors as shown in Fig. 4:

4.2.1. HB cells with single bypass thyristor

Fig. 8(a) and (b) show the worst-case peak arm currents of converter 1 (75 km from the fault point) and converter 2 (140 km from the fault point), in which the CMMCs with various γ, $(0.25 \leq \gamma \leq 0.5)$ are employed. These plots show that the number of inserted FB cells per arm, which is signified by γ, has a marginal effect on limiting the rate-of-rise of the fault current during the initial period from fault inception. In this period, the transient discharge fault currents from the DC line/cable distributed capacitors dominate converter arm and DC side fault currents. The peak arm currents of the distant converter rise later compared to that of the near converter from the fault point, due to the fault propagation delay as the effective line inductance is of a higher value, which indicates extension of the time for initiating blocking of HB and FB chainlinks.

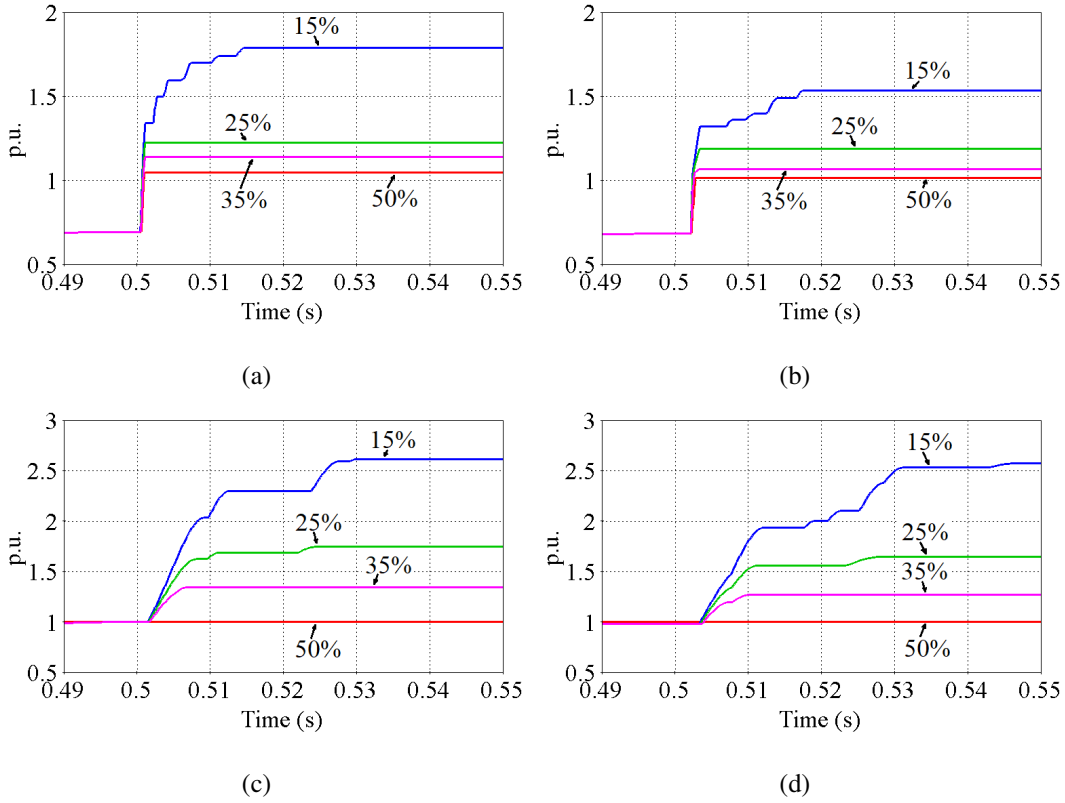


Figure 8: The effect of constant various ratio of FB cells during DC fault with rectified HB cells (a) Maximum values of arm currents of converter 1, (b) Maximum values of arm currents of converter 2, (c) Maximum values of cell voltages of converter 1, (d) Maximum values of cell voltages of converter 2.

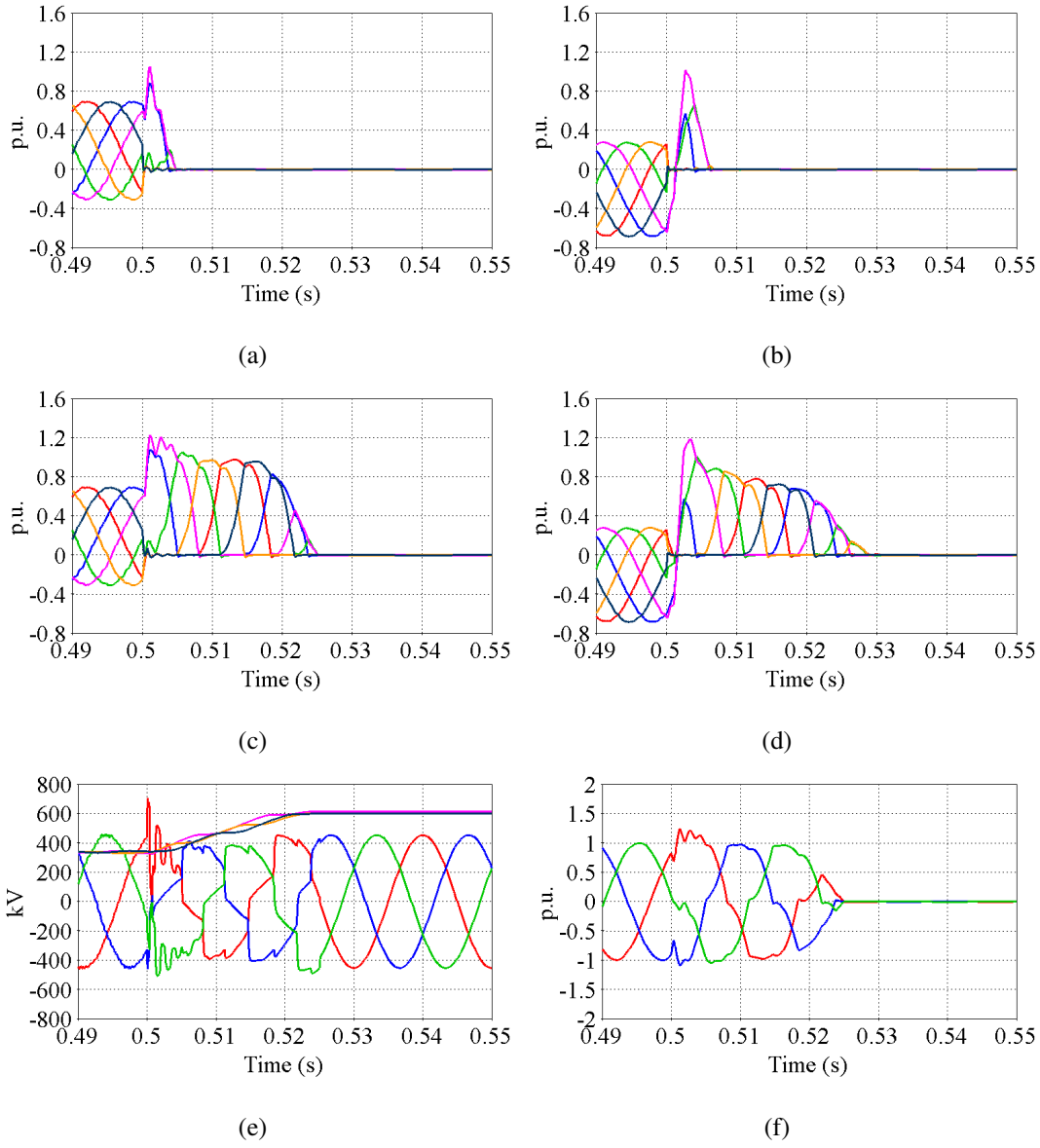


Figure 9: Arm currents during the DC fault for different FB ratios with rectified HB cells (a) 50% FB ratio converter 1, (b) 50% FB ratio converter 2, (c) 25% FB ratio converter 1, (d) 25% FB ratio converter 2, (e) AC Line-to-Line voltage superimposed with the FB cell voltages, (f) Converter side AC currents.

The times converters spent in current limiting mode (second stage) before transitioning to third stage, in which protection of the semiconductor switches is prioritized, are extended as γ increases as shown in Fig. 8(c) and (d).

Fig. 9(a) and (b) show the arm currents of converters 1 and 2 with $\gamma = 0.5$, which correspond to the conventional MC-MMC, in which the arm currents are well controlled to zero during P2P DC fault. In contrast, Fig. 9(c) and (d) show the arm currents of converters 1 and 2 for $\gamma = 0.25$. The arm currents are rectified and exhibit a brief overcurrent period followed by a sustained period of decreasing magnitudes as the FB cells continue to present rising DC voltages, which increasingly oppose the current flow through

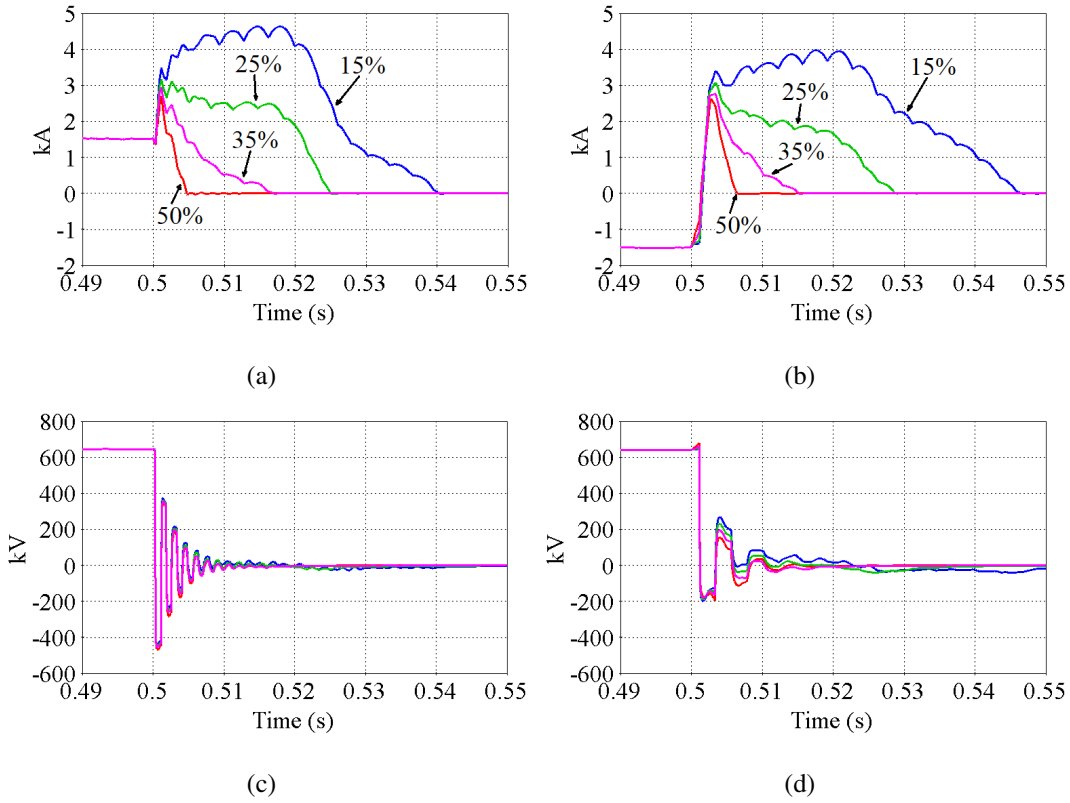


Figure 10: DC voltages and currents for different FB ratios with rectified HB cells (a) DC currents converter 1, (b) DC currents converter 2, (c) DC voltage converter 1, (d) DC voltage converter 2.

the arms of converters 1 and 2. If no overvoltage restriction is imposed, the FB cell capacitor voltages will charge until the arm and DC currents drop to zero when the total of each FB chainlink is equal to the peak of line voltage $\sqrt{(3)}\hat{V}_{AC}$. For completeness, Fig. 9(e) and (f) display the sums of the upper and lower arm FB capacitor voltage sums superimposed on the line-to-line AC voltages measured at the interfacing transformer, and three-phase output currents of the converter 2. These results indicate the decreasing trend of the DC link currents, which is in line with the arm currents displayed in Fig. 9 and 10. Observe that the significant effective inductance in the DC loop contributed by the DC cable and arm reactors delays the fall of DC link currents to zero compared with that of the three-phase output currents. Although ideally, the sums of the FB capacitor voltage sums per leg are expected to charge to the peak of the line-to-line voltage, 452 kV, the slow decay of the DC and arm currents have led to overcharge of the FB chainlinks to near 610 kV (1.9 times the rated DC voltage). Fig. 10(a) and (b) exhibit clear and speedy drop of the DC currents of converters 1 and 2 to zero as γ increases. Fig. 10(c) and (d) present the DC voltages of converters 1 and 2 for various γ. These plots show that γ has negligible impact on residual DC voltages of converters 1 and 2. It must be stressed that the illustrative results which do not account for potential actions of protection systems and exploratory discussions presented in this section aim to build-up a better understanding of the

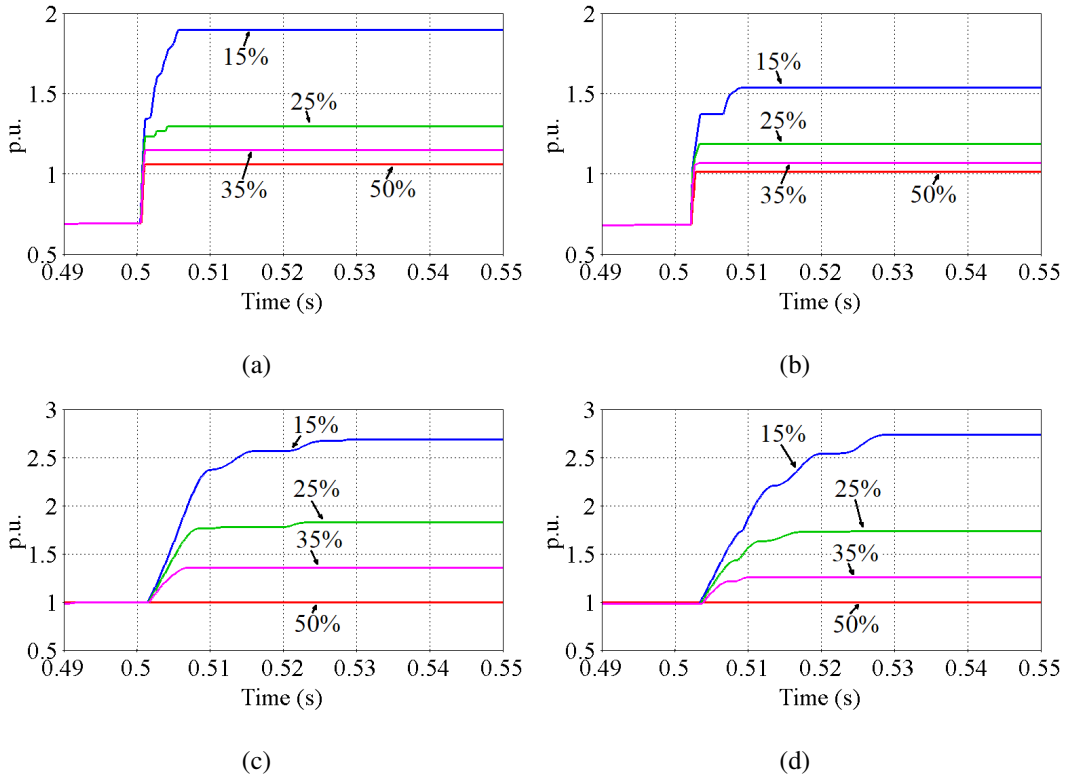


Figure 11: The effect of constant various ratio of FB cells during DC fault with fully bypassed HB cells (a) Maximum values of arm currents of converter 1, (b) Maximum values of arm currents of converter 2, (c) Maximum values of cell voltages of converter 1, (d) Maximum values of cell voltages of converter 2.

behavior of the CMMC and the possible opportunities it offers to DC fault protection.

4.2.2. HB cells with back-to-back bypass thyristors

Fig. 11 displays the worst-case peak arm currents and cell capacitor voltages of converters 1 and 2 for $0.25 < \gamma < 0.5$. These results indicate that the overall trends and magnitudes of arm and DC fault currents and capacitor voltages of both converters are greatly influenced by the number of FB cells per arm as signified by γ. The worst-case peaks of currents and cell capacitor voltages are similar to previous case. However, the arm currents of this case remain unrectified sinusoid superimposed on decaying DC components. The DC fault current starts to decay once the current limited mode (second stage) of the CMMC is activated through blocking of the FB cells and bypass of the HB cells, as shown in Fig. 4(b), and Fig. 13. The DC fault in this case falls faster than the previous case with the single bypass thyristor. In the latter case, the DC fault currents of both converters, 1 and 2, drop to zero in less than 8 ms, following a brief rise, which is largely driven by the transient discharge of the DC line/cable distributed capacitors.

Also, the magnitudes of the arm currents during faults are limited within the tolerable levels of present technologies for semiconductor switches. Moreover, it is shown in Fig. 11(c) and (d), that for $0.25 \leq \gamma \leq$

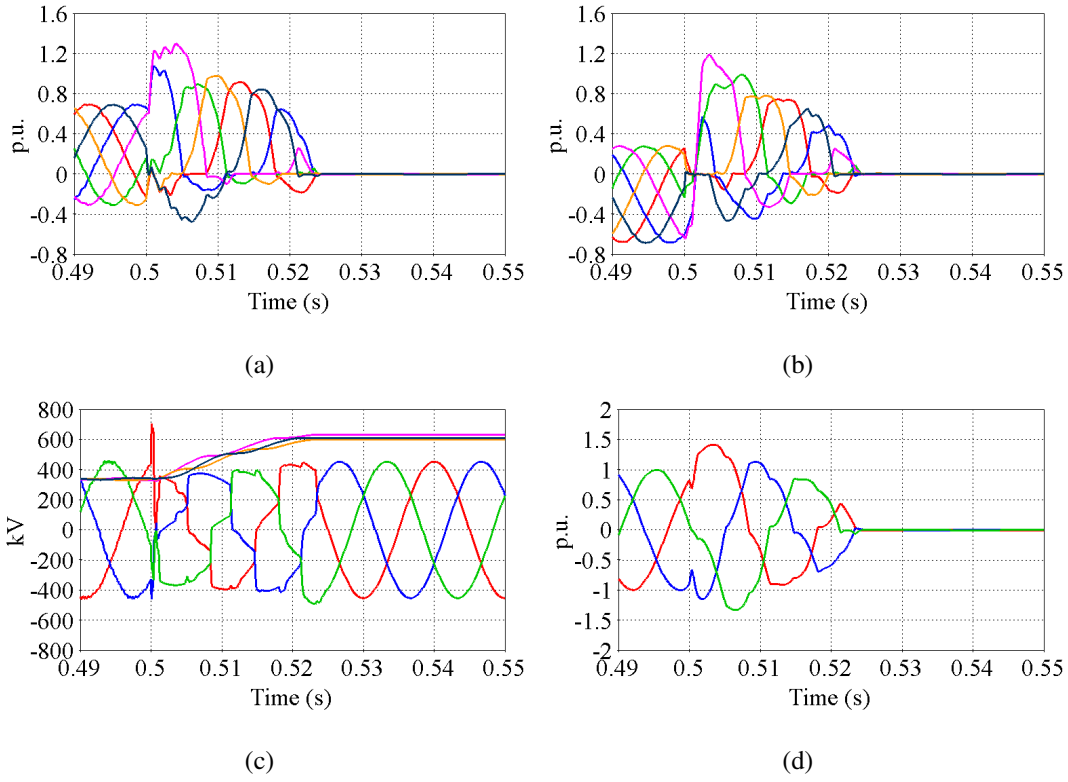


Figure 12: Arm currents during the DC fault for different FB ratios with fully bypassed HB cells (a) 50% FB ratio converter 1, (b) 50% FB ratio converter 2, (c) 25% FB ratio converter 1, (d) 25% FB ratio converter 2, (e) AC Line-to-Line voltage superimposed with the FB cell voltages, (f) Converter side AC currents.

0.5) the FB cell capacitor voltages remain below the threshold that trigger fully block mode (third stage). Also, Fig. 11(a) and (b) show that the peak of the currents of both converters for $\gamma \geq 0.25$ remain below 1.5 pu, which is the current limit threshold. The fault DC line could be isolated using mechanical DC circuit breakers or DC switches within 8 ms, without fully blocking the converter. Therefore, in cases of multi-terminal DC grids with multiple DC lines, faster resumption of power transfer could be achieved.

The arm and output phase currents in Fig. 12 are suppressed toward zeros much faster in this case (with HB cells back-to-back thyristor bypasses) than the previous case with no or single thyristor.

4.2.3. Illustrative DC fault Simulation

To demonstrate the benefits of the CMMC to wider HVDC grids, the four-terminal DC grid in Fig. 14 with the parameters of Table 1 is simulated, in which a permanent P2P DC fault is applied at location F1 at t=1 s. Selected simulation waveforms are displayed in Fig. 15.

From the active powers and DC voltages of the four converters displayed in Fig. 15(a) and (b), the converters 1 and 2 are least affected and followed by converter 3, with the converter 4 is the most affected. As illustrated in Fig. 15(c), the AC voltage at the PCC of converter 1 shows that the impact of P2G DC fault

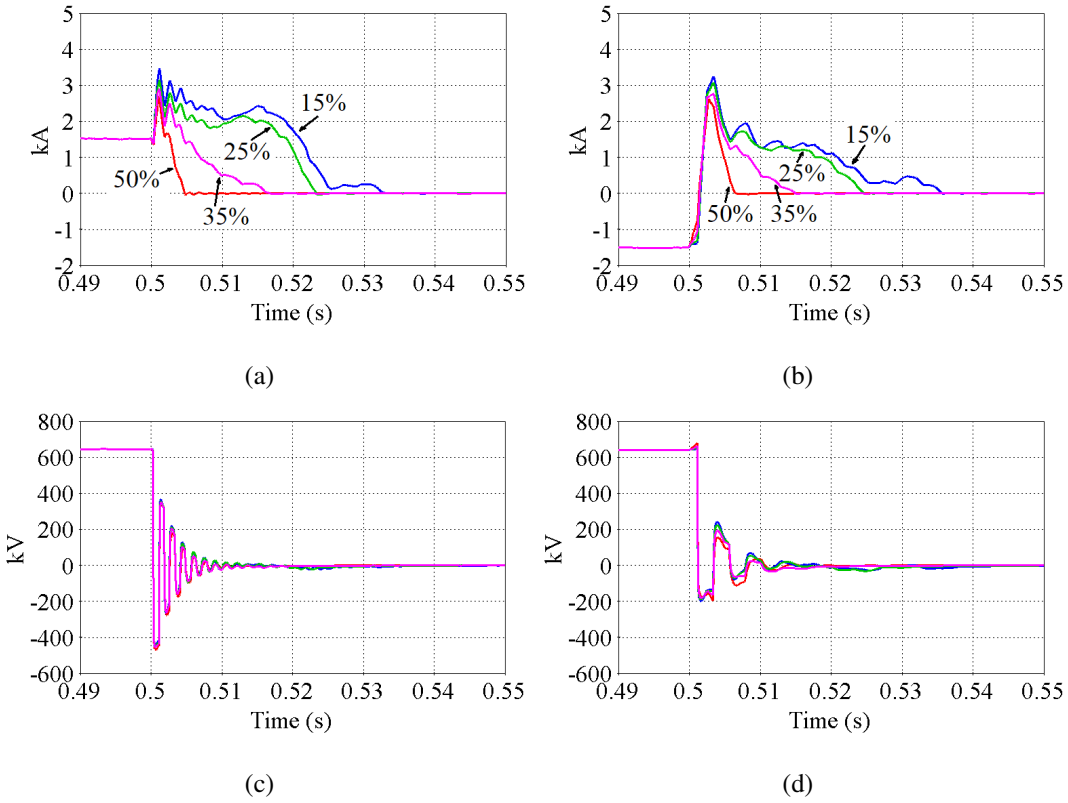


Figure 13: DC voltages and currents for different FB ratios with fully bypassed HB cells (a) DC currents converter 1, (b) DC currents converter 2, (c) DC voltage 1, (d) DC voltage converter 2.

on the AC grid which hosts the converter 1 is minimal. The period of power flow interruption across the DC grid is brief, and followed by swift system recovery to pre-fault power flows and DC link voltage once the faulted DC cable is isolated. Fig. 15(d) shows the total DC voltages across the HB and FB chainlinks of the six arms of the converter 1 are shared correctly in pre-fault and post-fault conditions. The total voltages across the HB chainlinks remain flat as the HB cell capacitors are bypassed when the CMMC operates in

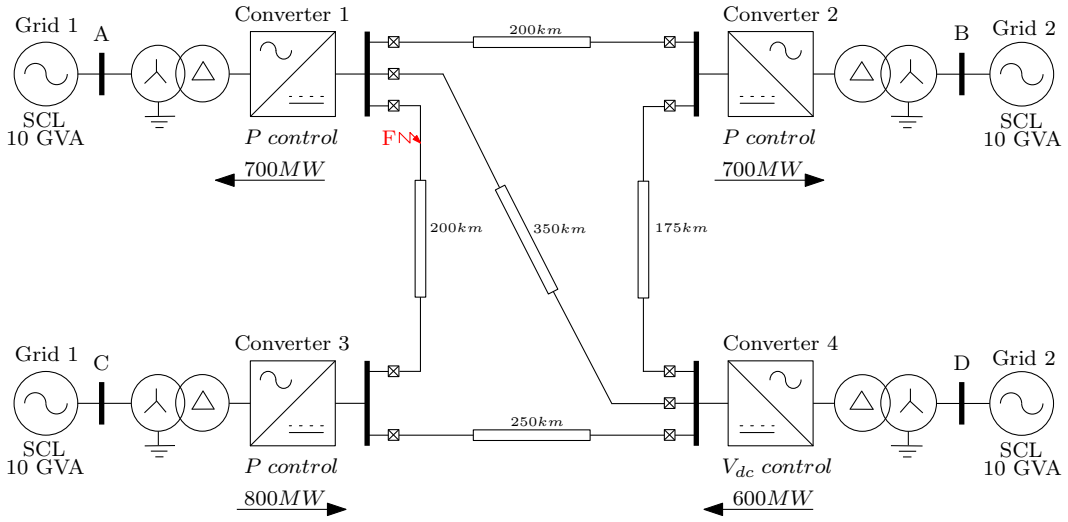


Figure 14: Simulated DC network.

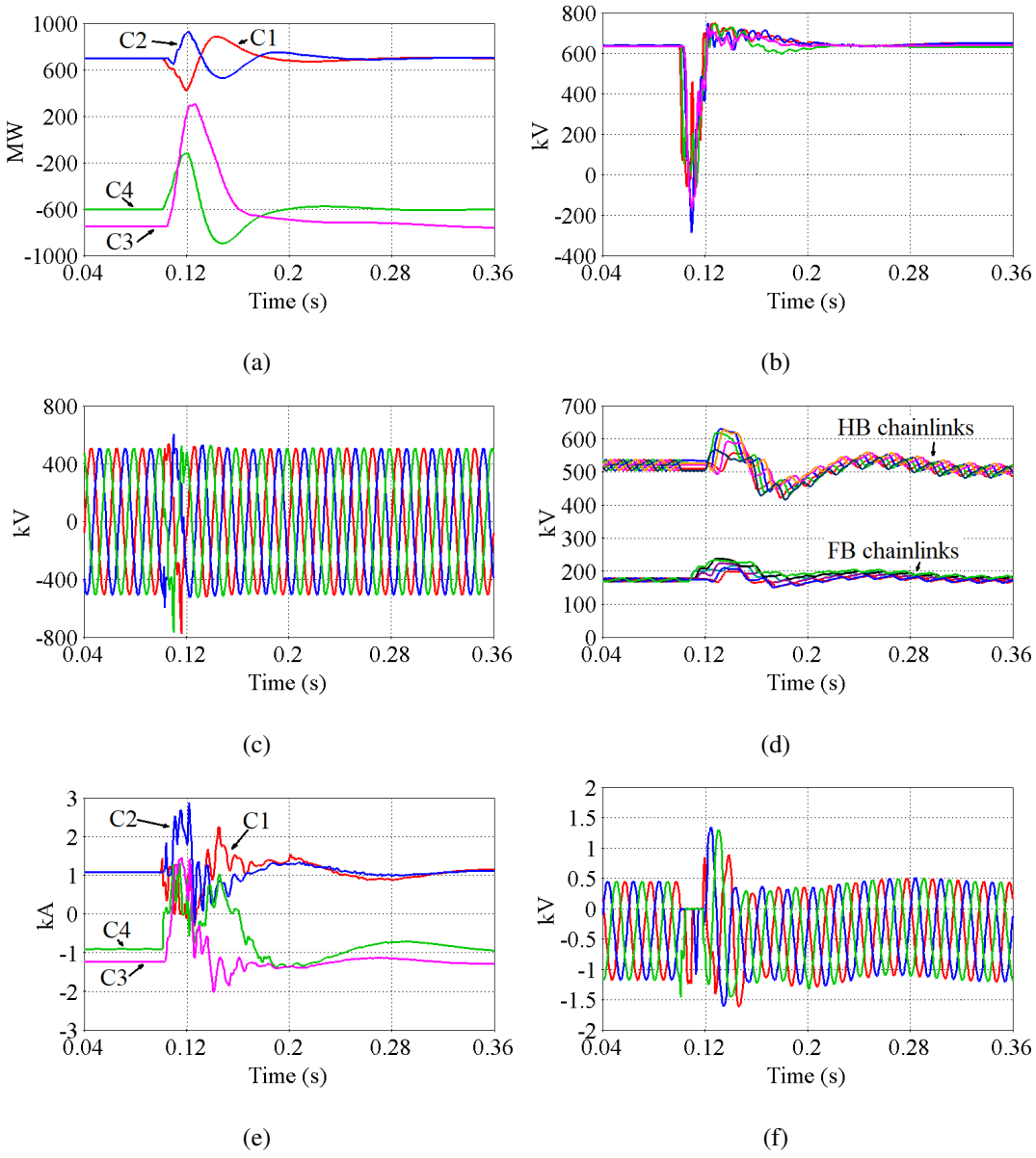


Figure 15: Illustrative operation of a four terminal system (a) Active powers, (b) DC voltages, (c) Converter 1 AC side voltages, (d) Converter 1 Capacitor voltages, (e) DC currents, (f) Converter 1 upper arm currents.

current limiting mode, in which the FB chainlinks are blocked. As a result near 45% overvoltages appear across the FB chainlinks of converter 1. At the instant of de-blocking, the HB chainlinks exhibit near 33% overvoltage. These overvoltages are well within the safe limits for semiconductor switches and cell capacitors. The DC current plots of the four converters displayed in Fig. 15(e) confirm the substantial reduction achieved in the magnitude of the fault currents in the DC side due to current limiting mode of the CMMC, regardless the distant from the fault. The arm currents shown in Fig. 15(f), further demonstrate the effectiveness of CMMC in suppression of AC side currents and current stresses in semiconductor switches.

Fig. 16 presents focused snapshots of the DC voltages of converters C1 to C4, AC voltage of converter

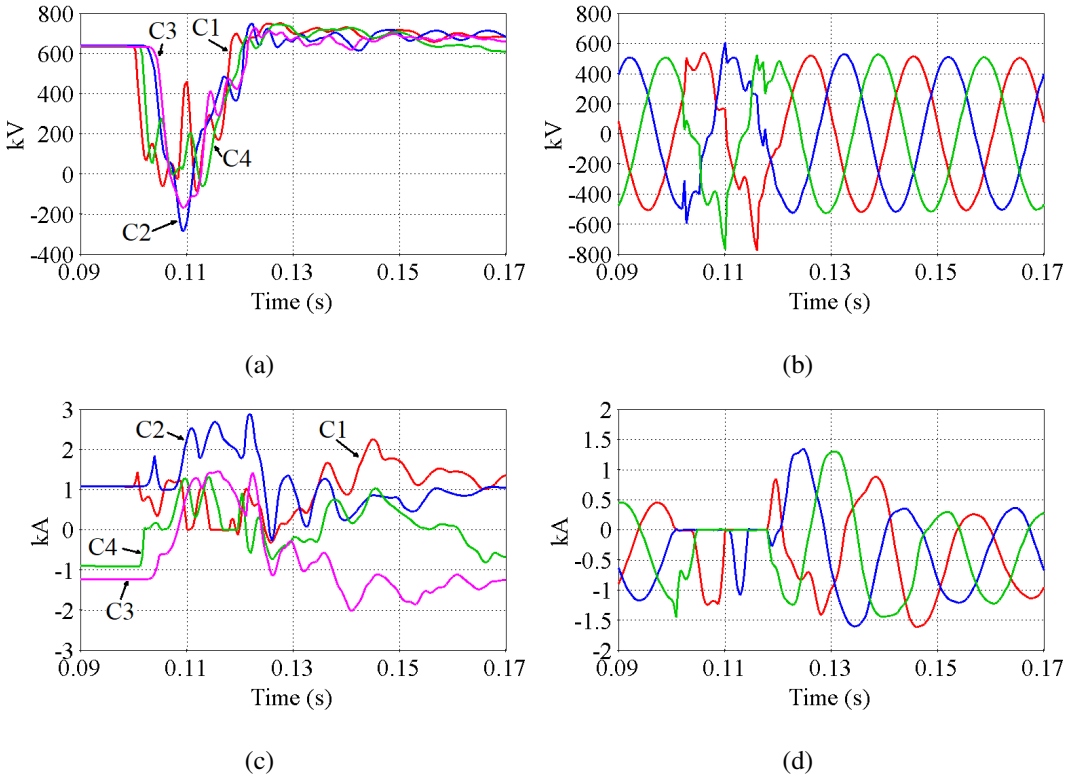


Figure 16: Focused illustrative operation of a four terminal system (a) DC voltages, (b) Converter 1 AC side voltages, (c) DC currents, (d) Converter 1 upper arm currents.

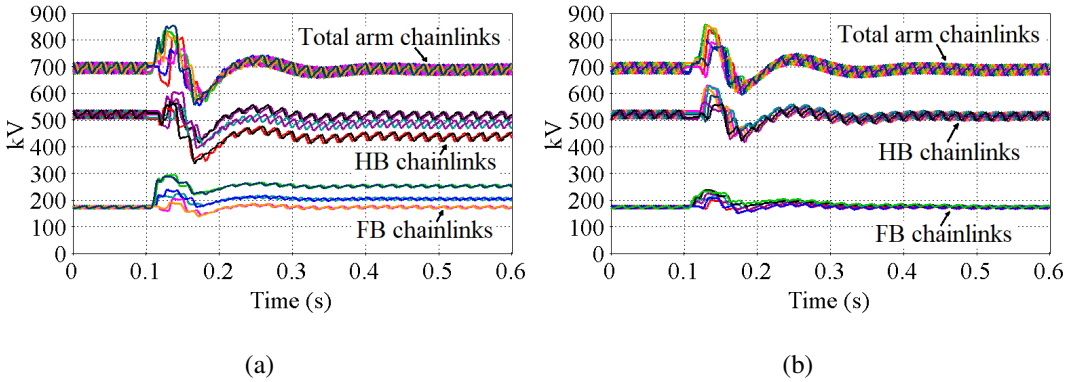


Figure 17: The effect of horizontal controller under disturbance on the capacitor voltages (a) Conventional, (b) Modified.

C2, DC currents of converters C1 to C4 and arm currents of C2, originally displayed in Fig. 15. These expanded plots confirm the effectiveness of the CMMC in driving down the faults currents in AC and DC sides, where the converters' semiconductors and DCCBs are affected.

Fig. 17(a) and (b) show the HB and FB capacitor voltage sums of converter C2 when the conventional and the proposed horizontal capacitor voltage controllers are used. Although the conventional implementation ensures correct voltage sharing between HB and FB chainlinks during normal operation, it fails during major transients. Whilst the proposed alternative manages to ensure correct voltage sharing between the

HB and FB chainlink of th arms, before and after network disturbances.

4.3. Expansion of P-Q envelope

In addition to enhanced DC fault performance, the CMMC can extend the modulation index control range and therefore the PQ envelope, without exposing the HB and FB chainlinks to high voltage stresses. According to the analysis on Section 2.1. the CMMC can offer customized over-modulation depending on γ, which defines the amount of negative voltage each CMMC can generate and thus, the theoretical maximum achievable output voltage. However, in typical operation of HVDC converters, including the CMMC, the current and voltage limits define the converter P-Q envelope. In over-excitation region, the over-modulation feature helps with the generation of extra capacitive reactive power that is especially needed in weak AC grids, without exceeding the specified current limit.

4.3.1. Limited extension of the PQ envelope and applications in weak AC grids

The limited extension of CMMC operation into over-modulation region permits the use of negative output voltages of the FB cells. The extension of modulation linear range facilitates arm voltages to over-modulate in order to achieve higher AC voltages and expansion of the P-Q envelope in the over-excitation

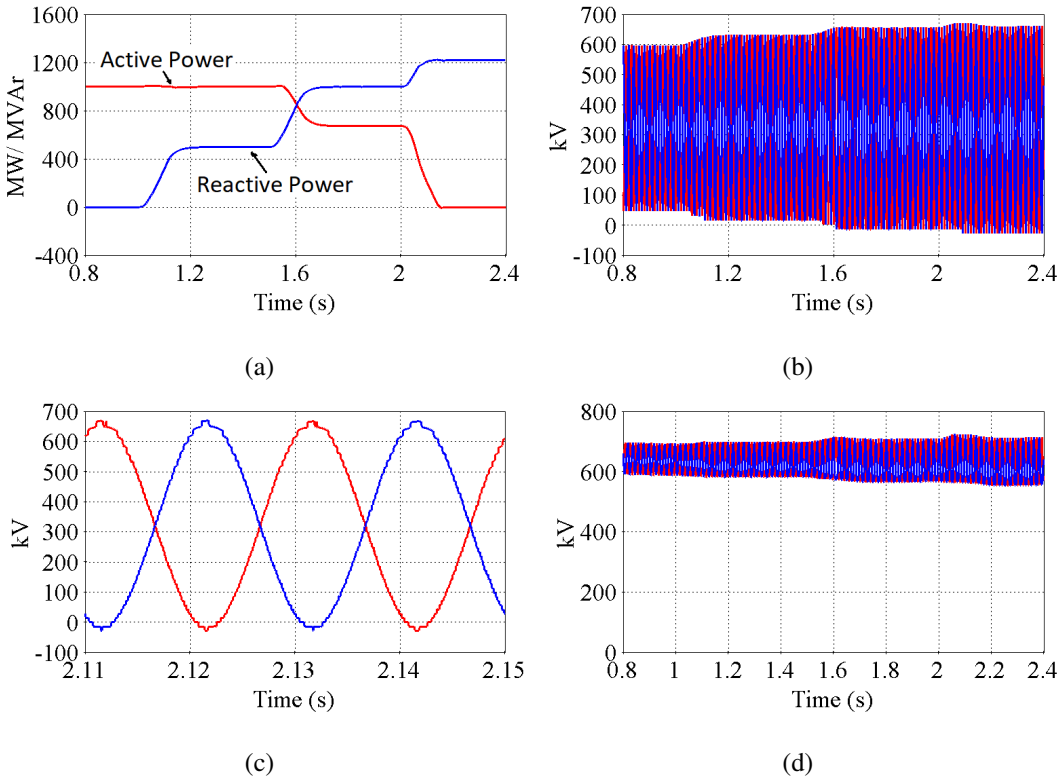


Figure 18: Expansion of the PQ capability (a) Active and Reactive power, (b) Arm voltages, (b) Focused arm voltages, (d) Total capacitor voltages.

region, in which a leading reactive power is generated. In this way, more reactive power can be provided without the need for additional equipment such as STATCOM [30].

Fig. 18 shows selected results when the CMMC varies its active and reactive power until the current or voltage limits are hit, with priority given to the reactive current i_q. The results in Fig. 18(a) show that at zero active power, the maximum achievable reactive power output of the CMMC with $\gamma = 0.25$ is 1330 MVAr. Fig. 18(b) shows that the upper and lower arm voltages of the CMMC cross the zero level to negative values from the bottom, while from the top they remain within the envelope defined by the input DC link voltage as depicted by the capacitor voltage sums in Fig. 18(d), indicating a brief period of operation in over-modulation region.

To further demonstrate the added benefits of the CMMC, particularly, in extension of active power sourcing and sinking in weak AC grids, this part presents comparative simulations for an CMMC with $\gamma = 25\%$, for the base-case with a conventional HB-MMC and for a HB-MMC with a STATCOM. In this demonstration, the CMMC uses generic model with γ varying between 0 and 1, when the AC grid short circuit ratio (SCR) is 1.1. For simplicity and illustration purposes, the rated power and DC voltage of the MMC STATCOM are 1045 MVA and 640 kV respectively, and the rest of parameters remain the same as the converter terminals of Fig. 5. Both converters regulate their PCC AC voltage at 400 kV.

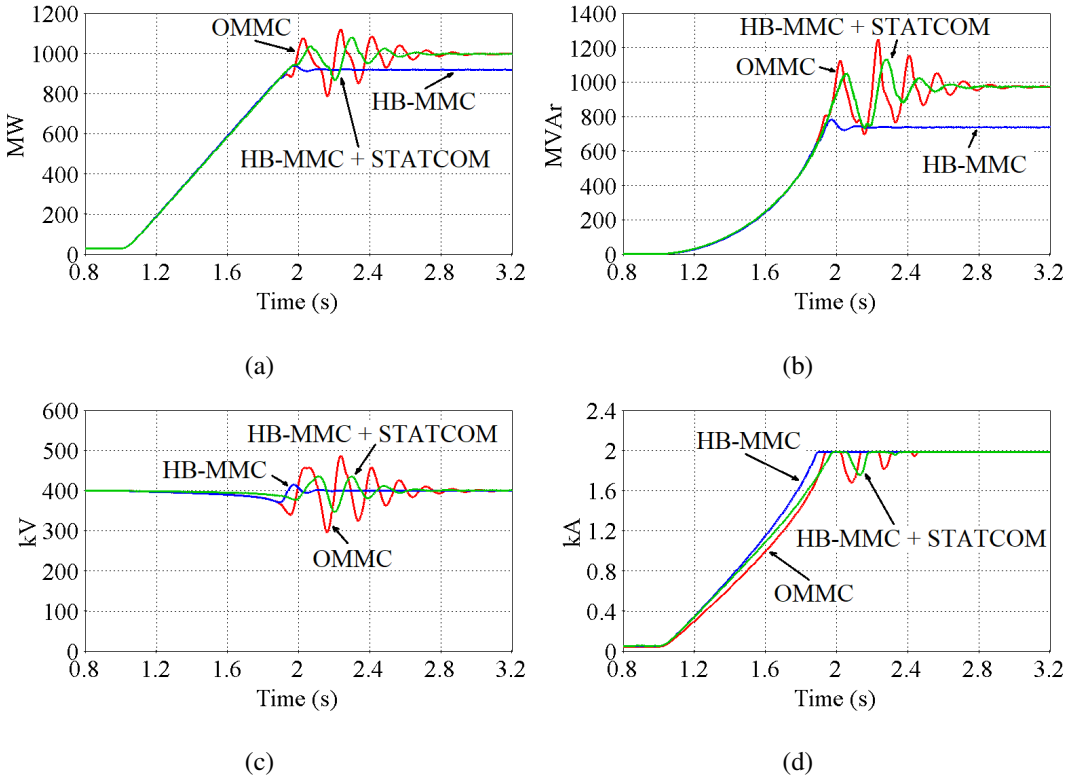


Figure 19: Expansion of the PQ capability in a weak network (a) Active power, (b) Reactive power, (c) Grid RMS voltage, (d) Converter RMS current.

Fig. 19(a) and (b) display the maximum achievable active and reactive powers for the three scenarios described earlier, in which the maximum active power that the conventional HB-MMC can inject into the AC grid is less than the rated, while the other two cases are able to inject their rated active powers. The CMMC is able to source its rated active power after sourcing extra reactive power amounts to near 200 MVAr compared to the conventional HB-MMC. Also, besides the conventional HB-MMC, a separate STATCOM with minimum rated power of near 200 MVA is required to facilitate injection of 1000 MW in the same weak AC grid.

Fig. 19(c) shows the measured AC voltages of converter 1 when it is modelled as the conventional HB-

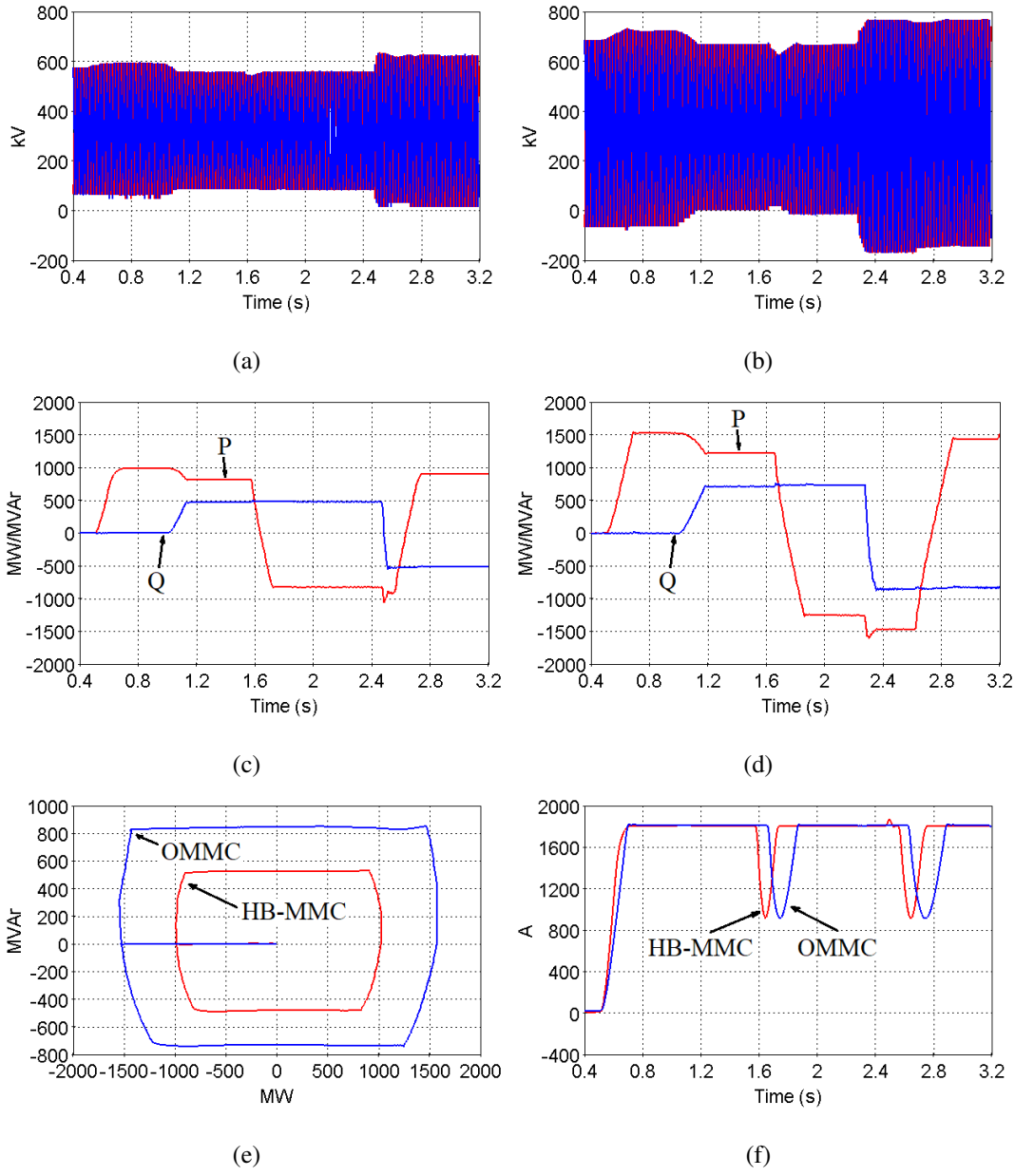


Figure 20: Expansion of the PQ capability achieving higher V_{AC} from V_{DC} (a) PQ envelopes, (b) Converter RMS AC current, (b) HB-MMC arm voltages, (d) CMMC arm voltages.

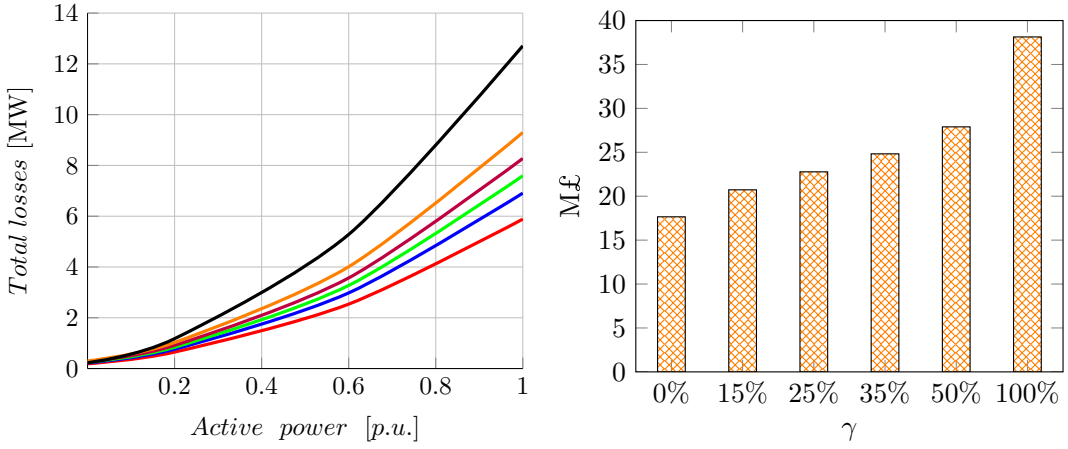
MMC, CMMC and HB-MMC plus a STATCOM. In all three cases, substantial reactive power is needed to facilitate transmission of rated active power and maintain the magnitudes of AC voltages at rated. To provide fair comparison, the current limitation of all cases in the same as shown in Fig. 19(d).

4.3.2. Extreme case of PQ expansion

Fig. 20 shows the extended PQ envelope of the CMMC relative to that of the HB-MMC, in which the CMMC over-modulation capability is exploited as evident in Fig. 20(a) and (b), where the CMMC arm peak voltages surpass the pole-to-pole DC voltage, V_{DC}=640 kV. Fig. 20(e) shows a comparison between PQ envelopes of the HB-MMC and the CMMC with γ = 0.25, in which it is assumed that the CMMC and the HB-MMC have the same current limits, see Fig. 20(f). Observe that the CMMC uses its over-modulation capability to increase the output AC voltage in order to generate more active and reactive powers, see Fig. 20(c) and (d). The results presented in this case demonstrate that the CMMC inherent over-modulation capability of typical converters that employ bipolar cells such as the MC-MMC and FB-MMC.

5. Comparison of Semiconductor Losses

Fig. 21(a) and (b) summarize the semiconductor losses of CMMCs for selected γ in the range $0 \leq \gamma \leq 1.0$ and their corresponding annual costs. The semiconductor loss estimates in Fig. 21(a) were calculated using the detailed loss-model presented in [9], while the annual cost of the losses is taken from [10]. The results reveal that the semiconductor losses and the corresponding costs incurred by the CMMC with $\gamma = 25\%$ are marginally higher than that of the conventional HB-MMC (CMMC with $\gamma = 0$).



(a) (b)

Figure 21: Investment comparison for variable installed ratios of FB cells (a) Semiconductor losses, (b) Cost of losses.

6. Discussion

The CMMC is motivated by an attempt to lower the cost associated with protection of HVDC grids, by devising alternative ways in which the expensive hybrid DC circuit breakers can be replaced with relatively cheaper and slower mechanical DCCBs, which can interrupt DC faults within 8 ms to 12.5 ms. To achieve such vision and mitigate the significant running cost associated with the converters semiconductor losses over the project life-cycle, the CMMC is put forward. The number of FB cells or converter losses can be traded for high value features: control range, resiliency to DC fault, and overall time-scale for fault clearance without significantly compromising the continued operation during P2G and P2P DC faults. Comparative summary of the attributes is visualized and presented in Fig. 22.

The CMMC with $\gamma > 0.25$ represents an attractive option for the practical realization of HVDC grids, in which a better performance in terms of resiliency to P2P and P2G DC faults is achieved at the expense of additional running cost. Nevertheless, CMMC with $\gamma = 0.25$ represents a minimum requirement for achieving most of the desirable functionalities for cost-effective HVDC grids. However, the final project design may differ depending on the required balance between practical design considerations and broader system operational objectives and priorities. Consequently, the CMMC with $\gamma < 0.25$ can still offer extended control range and P-Q envelopes, and partial controllability of DC fault current during P2P faults

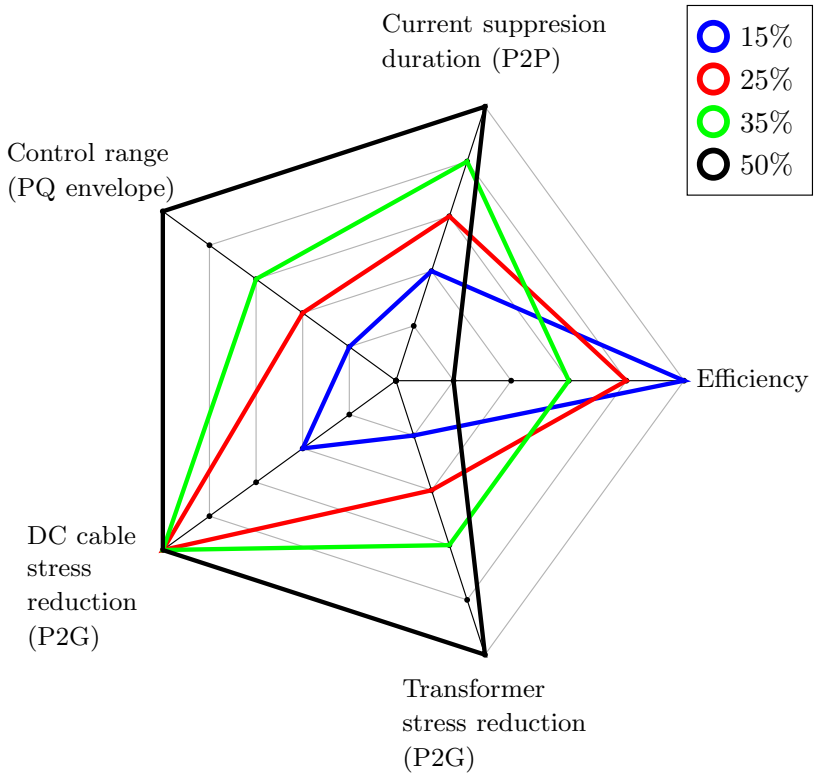


Figure 22: Comparison between different γ of the CMMC.

which leads to reduced DCCB design requirements, for even lower running costs.

In conclusion, the CMMC offers customized design, which can be tailored according to the HVDC grid requirements on case-by-case basis, while considering the trade-offs between capital, operation costs, and the desired degree of controllability during DC faults.

7. Conclusions

This paper has conducted a comprehensive investigation to establish the minimum amount of FB cells required per arm of the CMMC in order to achieve several meaningful design trade-offs for future DC grids, in which the cost of semiconductor losses over the lifetime of the HVDC grid project is traded for enhanced system resiliency against P2P and P2G DC faults, and reduced capital cost of DCCBs. This investigation was motivated by the desire to avoid the prohibitive costs of established approaches for realization of DC grids, which rely on highly selective protection systems and expensive fast acting DC circuit breakers.

From extensive quantitative investigations, it has been found that 25% is the minimum and sufficient percentage for the blocking voltage of the FB chainlink relative to the total blocking voltage of the CMMC arm to facilitate healthy pole-restraining and continued operation during a P2G DC fault. In addition, for P2P faults, this ratio provides sufficient suppression of the AC and DC fault currents to allow the use of relatively slow mechanical DCCBs or even DC switches for fault isolation. These benefits of the CMMC can reduce the magnitude of DC circuit breakers let-through currents and current breaking capacities. Additional benefit of the proposed CMMC is the extension of active and reactive power control range in general and in weak AC grids.

Detailed simulations indicate the necessity for the proposed alternative implementation of the horizontal capacitor voltage controllers to ensure correct voltage sharing between HB and FB chainlinks.

8. Declaration of Competing Interest

The authors declare that they have no known competing financial interest or personal relationships that could have appeared to influence the work reported in this paper

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