Adaptive-Filter PMU Hardware Validation to IEEE C37.118.1a Requirements

Strathclyde ENG52 REG D6 Report

February 2017

Dr Steven Blair, Dr Andrew Roscoe

University of Strathclyde
Glasgow, UK

EMRP Joint Research Project
ENG52 Smart Grids II
“Measurement tools for Smart Grid stability and quality”

Abstract

This report documents the implementation and testing of a hardware Phasor Measurement Unit (PMU) prototype, using a Beckhoff-based hardware platform. This platform offers several convenient features for PMU development, such as hardware modularity, support for integrating C++ and Simulink models, IEEE 1588 support, and scalability to multiple measurement locations. The Strathclyde M-class PMU algorithm can be deployed on this platform requiring less than 8% of the CPU time of a single CPU core, with 10 kHz analogue sampling.

A closed-loop testing procedure, using RTDS hardware and software, has been used to quantify the performance of the Strathclyde PMU algorithm. With proper calibration of the analogue system, as would be the case for a PMU to be deployed in the field, the PMU can achieve relatively low error metrics according to the Synchrophasor standard requirements. For example, for the “static” PMU tests, Total Vector Error (TVE) values as low as 0.01% can be achieved (where the Synchrophasor standard requires a maximum TVE of 1%).

Additional tests with multiple disturbances and with emulation of a power system fault have been conducted to demonstrate that PMU algorithms require resilience under realistic worst-case scenarios – and to make a case for testing all PMUs in this way.

A new method has been devised for accurately and conveniently characterising the reporting latency of PMUs. This method can also be used to measure the end-to-end performance of transmitting PMU data over wide-area communications networks, thereby providing more accurate knowledge of the actual latency of the measurement systems used to implement novel power system control and protection schemes.

The algorithm will be integrated within Synaptec’s passive and distributed optical sensing platform for wide area synchrophasor-based monitoring, protection, and control.

Contents

Abbreviations

ADC	Analogue-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
CPU	Central Processing Unit
CT	Current Transformer
E2E	End-to-End
FE	Frequency Error
FPGA	Field-Programmable Gate Array
FRACSEC	Fraction of Second
IDE	Integrated Development Environment
IO	Input or Output
IP	Internet Protocol
LAN	Local Area Network
LV	Low Voltage (typically 400 V, three-phase)
MU	Merging Unit
OOB	Out-of-Band
PC	Personal Computer
PMU	Phasor Measurement Unit
PTP	Precision Time Protocol
RFE	Rate of Change of Frequency Error
ROCOF	Rate of Change of Frequency
RTDS	Real Time Digital Simulator
SOC	Second of Century
TCP	Transmission Control Protocol
TIA	International Atomic Time
TVE	Total Vector Error
UDP	User Datagram Protocol
UTC	Coordinated Universal Time
VT	Voltage Transformer

1 Introduction

This report documents the performance validation of a hardware Phasor Measurement Unit (PMU) prototype for the D6 REG(STRAT) deliverable within the EMRP ENG52 “Smart Grids II” project. The report includes details of the hardware, software, IEEE C37.118.2 communications, system validation, and detailed analysis of measurement performance.

The PMU algorithm under test is described in general in [1], with further details in [2], [3]. The prototype has been implemented using a Beckhoff hardware platform. This platform has several characteristics – such as modular hardware and support for IEEE 1588-based time synchronisation – which make it very convenient for prototyping PMU algorithms. A separate document has been prepared to describe the practical details of using the Beckhoff hardware and software platform, which is available at [4].

The Real Time Digital Simulator (RTDS) PMU Test Utility [5] has been used to perform most of the PMU measurement performance testing. This software provides automated closed-loop testing of PMU performance according to IEEE C37.118.1a (2014) [6] and the IEEE Synchrophasor Measurement Test Suite Specification (2015) [7], using RTDS hardware to supply known analogue signals to the PMU. Although this testing environment does have the same accuracy as a dedicated PMU calibrator (such as [8]), it provides a convenient method for characterising PMU performance using existing equipment available at Strathclyde and many other power system R&D facilities.

There is one test which cannot be performed by the RTDS PMU Test Utility: measuring PMU reporting latency. However, a very accurate, convenient, and cost-effective method of measuring PMU reporting latency has been developed, with the results given in Section 6.2.

2 Overview of PMU Platform

2.1 Beckhoff hardware platform

Beckhoff devices are generally designed for industrial automation systems. A Beckhoff hardware configuration typically consists of a power supply, a “controller” unit, a set of local IO modules, and a set of distributed IO modules. Each controller unit has at least two Ethernet ports, which are typically intended to be used to create an EtherCAT [9] network to connect to distributed IO modules. Figure 1 shows the hardware configuration for the prototype PMU.

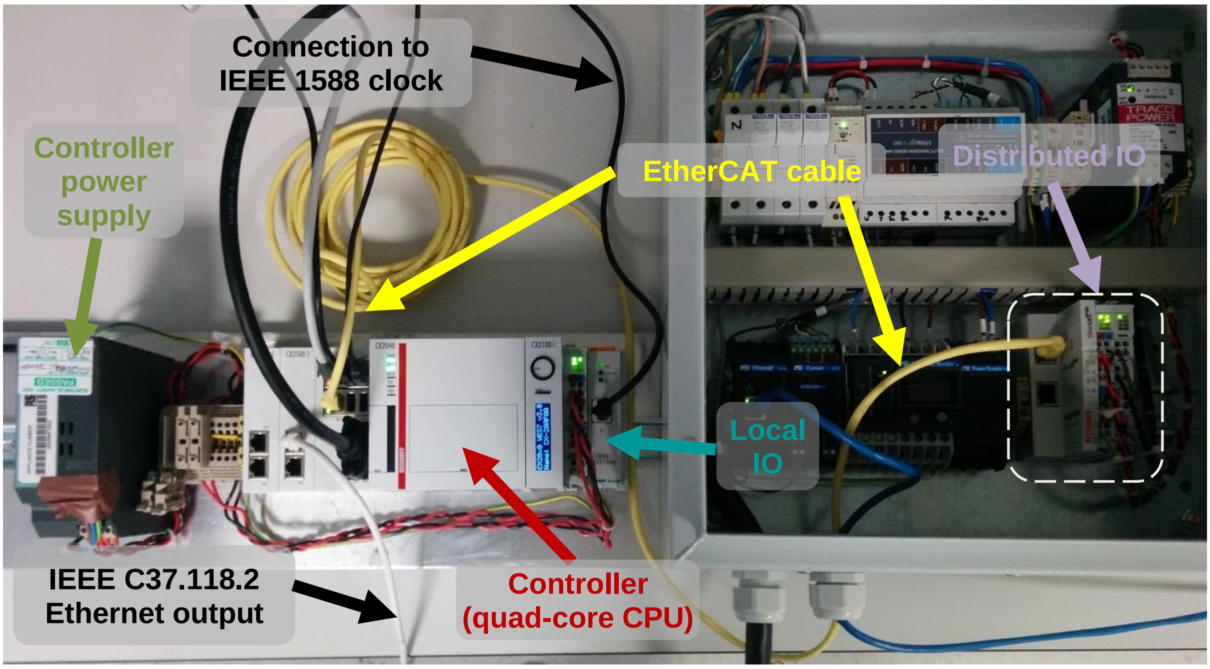

Figure 1: Typical Beckhoff hardware configuration

A host PC, running the TwinCAT 3 development software, is required for configuring, uploading, and debugging the control software. After the system development is complete, the software can be deployed to the controller unit which automatically executes the control software when booted.

The controller units generally use Intel x86 Central Processing Units (CPUs) and run a Windows Embedded operating system. The main algorithm for a given application (in this case, a PMU) should execute on the controller’s CPU. Due to the use of an x86 architecture, the main algorithm processing is limited to a minimum cycle period of approximately 50 µs, with a jitter of approximately 1-5 µs. However, time-critical IO modules are operated more accurately using dedicated hardware clocks (see Section 2.2), so that hard real-time applications are possible. Controllers with multi-core CPUs can be used to execute software in parallel, with each core allocated to a specific thread of execution.

In summary, although it was originally designed for other applications (such as industrial process control), a Beckhoff platform is also well-suited for prototyping PMUs in a relatively cost-effective manner:

- There is a variety of analogue voltage input modules which support 16-bit sampling at 10 kHz, which is in the order of the performance required for the REG(STRAT)

PMU algorithm. A combination of IO modules can be connected to a Beckhoff system, depending on the requirements of the application.

- The IEEE 1588 standard [10] is supported for time-synchronisation to a Coordinated Universal Time (UTC) clock source, using an Ethernet network.
- The use of a modern x86 CPU architecture allows relatively complex algorithms (implemented in C, C++, or Simulink) to be executed in real-time and using native 64-bit double-precision floating-point arithmetic, which many not be possible on less powerful embedded platforms or using a Field-Programmable Gate Array (FPGA).
- Distributed Clocks ensure that time-sensitive IO modules are handled appropriately in real-time (see Section 2.2).
- EtherCAT allows multiple measurement modules to be distributed (i.e. physically separated from the controller CPU) at multiple locations without affecting measurement fidelity or timing accuracy.

2.2 Distributed Clock concept

Although the main algorithm processing is executed with some jitter (see Section 6.2) due to the nature of an x86 architecture, the IO hardware is more tightly synchronised using the Distributed Clock (DC) technique [11], [12]. DC enables the IO functionality – such as sampling an analogue value, or actuating a digital output – to be synchronised precisely with a jitter of less than 100 ns. This is important for industrial automation systems, but is also beneficial for power system measurement applications such as a PMU.

The DC is implemented as 64-bit value with 1 ns resolution. One of the hardware modules (which can be referred to as an “EtherCAT slave” device) is responsible for defining the reference DC value. All other modules are synchronised to this reference. Synchronisation is achieved using “synchronisation datagrams”, which are sent through the EtherCAT bus. These datagrams are processed by an Application-Specific Integrated Circuit (ASIC) or FPGA in each hardware module.

An external time source can be integrated with a Beckhoff system to provide an absolute time reference [13]. For example, the EL6688 module can be used to connect a system to an IEEE 1588 grandmaster clock. This provides a mapping from the DC value to an absolute time reference (i.e. UTC).

2.3 TwinCAT 3 development software

TwinCAT is the Integrated Development Environment (IDE) for configuring Beckhoff hardware and software. TwinCAT 3 is presently the most recent version, and it is integrated within Microsoft Visual Studio. TwinCAT typically runs on the host PC for development, but just the TwinCAT “runtime” executes on the target Beckhoff controller unit. The host PC and the target controller unit can be directly connected with an Ethernet cable, or they can be connected to the same LAN.

TwinCAT 3 supports a variety of different software “modules” which can be implemented in, for example, IEC 61131-3 (for programmable logic controllers), C++, or Simulink. The TwinCAT interface allows software module IO (e.g. inputs defined in a Simulink model) to be linked to hardware IO, depending on the configuration of the target hardware.

In some cases, TwinCAT projects can be compiled and executed on the host PC. This is useful for testing purposes, but clearly the host PC will not have the same hardware IO capabilities as the target Beckhoff controller.

The TwinCAT software tools can be used free of charge for testing purposes. Trial licenses can be perpetually renewed.

3 Prototype PMU Implementation

3.1 Overall system architecture

Figure 2 illustrates the hardware and software configuration of the prototype PMU. A CX2040 controller, with a quad-core Intel Core i7 2.1 GHz CPU, has been used. The associations of hardware components (the EL3773 module and Ethernet Port 1) to software tasks are shown by dashed light-grey lines.

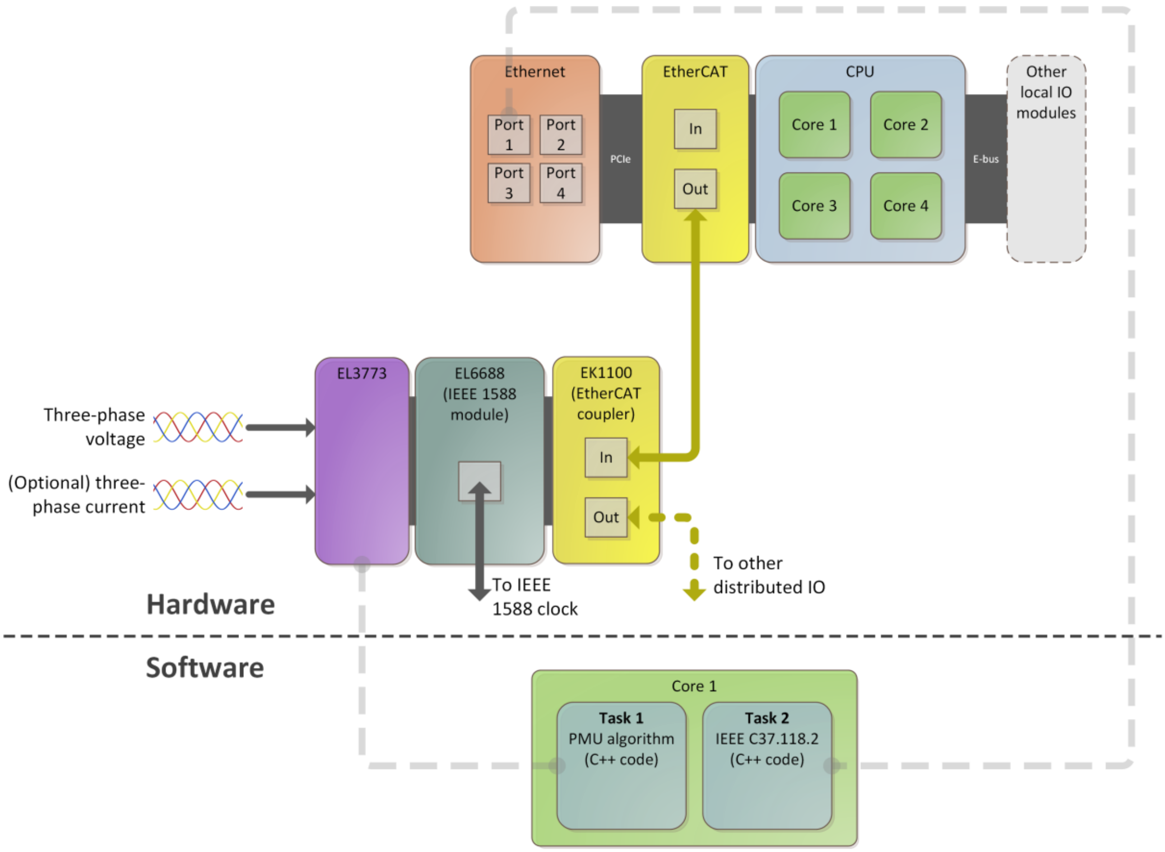

Figure 2: Overview of system hardware and software

The use of a quad-core CPU allows at least four independent PMU instances (and corresponding IEEE C37.118.2 communications) on the same hardware. Similarly, the modularity of EtherCAT enables additional measurement modules – at multiple, distributed locations – to be connected. Each PMU instance can be assigned to separate (or to the same) Ethernet network interface. Only one EL6688 module is required for the entire EtherCAT network i.e. other distributed monitoring locations can "daisy-chained" using additional EK1100 modules, which will all use a common timing reference.

3.2 Simulink PMU algorithm

The REG(STRAT) PMU algorithm (available in executable form at [14]) has been implemented in Simulink, with performance-critical sections written in C code [15]. Simulink Coder [16] has been used to automatically generate a C++ code implementation of the PMU Simulink model.

The generated C++ code can be included in a TwinCAT 3 project as a software module, and associated with a TwinCAT "task". Each task should be configured to execute on a particular cycle time-base, such as 1 ms or 100 µs, on a specific CPU core. The REG(STRAT) PMU algorithm uses a 10 kHz sampling frequency which requires a cycle time of 100 µs (except when ADC oversampling is used, as discussed in Section 3.4). The supports both M-class and P-class configuration with a 50 Hz nominal frequency and a reporting rate of 50 Hz; however, other configurations can also be used and the reporting rate can be changed dynamically at run-time.

3.3 Time synchronisation

The Beckhoff EL6688 module allows a Beckhoff hardware configuration to be synchronised with an IEEE 1588 (PTP) timing source (as shown in Figure 2). The module can function as a PTP slave or master and, with some limitations, can support PTPv1 and PTPv2.

The use of the EL6688 module allows the DC within a Beckhoff hardware configuration to be synchronised to an absolute time reference, i.e. the EL6688 module is the reference clock within the system. The various devices connected to an EtherCAT network are synchronised to this reference with an accuracy of less than 100 ns.

The EL6688 module configuration is given in Table 1, although other configurations are also supported.

Parameter	**Value**
IEEE 1588 mode	PTPv2, slave only
Transport type	Layer 3 (PTP over UDP)
Domain number	0x0000
Sync interval:	1 s
Delay request interval	1 s
Announce interval	2 s
Announce interval timeout	3 s
Delay mechanism	E2E
Internet Protocol (IP) address and subnet mask	As appropriate for grandmaster clock configuration

Table 1: EL6688 module configuration

The following requirements should be noted when using an EL6688 module:

- The epoch used by Beckhoff hardware is the year 2000 [17], rather than 1970 as defined in IEEE C37.118.2.
- The time value provided in software must be adjusted for leap seconds, i.e. converted from TIA to UTC.
- There is an issue where the EL6688 only synchronises with the IEEE 1588 grandmaster clock if the network interface is disconnected and reconnected (i.e. the Ethernet cable is unplugged and reconnected) *after* the Beckhoff controller has been initialised with the PMU program. This issue is under investigation with Beckhoff.
- The EL6688 module must connect to the IEEE 1588 grandmaster clock via and Ethernet switch which acts as an IEEE 1588 transparent clock (or boundary clock) to ensure proper timing accuracy. Alternatively, a direct connection between the clock and EL6688 module with a cross-over Ethernet cable can be used.

3.4 Voltage input sampling

Three approaches can be used for obtaining measurements of analogue three-phase voltage (and potentially for monitoring current):

1. Direct three-phase 400 V (LV) measurements using the EL3773 module. This allows testing of the PMU prototype within the Dynamic Power Systems laboratory at the University of Strathclyde.

   However, it should be noted that although the module supports 10 kHz sampling with 16-bit resolution, there is an integrated filtering stage which cannot be disabled. The REG(STRAT) PMU algorithm includes provisions for compensating for anti-aliasing filter magnitude and phase responses (and VT/CT responses, if required). However, these settings have not yet been validated and it is possible that calibration of the filter may be required. Similarly, the EL3773 ADC sampling time of 3.4 μs is also accommodated by the PMU algorithm.

   There is a further caveat that the measurement timestamp can only be accurately acquired for 10 kHz analogue sampling if the oversampling feature is used. For example, an oversampling factor of 2 means that 2 measurement samples are delivered to the software task each cycle (at 5 kHz instead of 10 kHz). This can be accommodated by simply executing multiple iterations of the REG(STRAT) PMU algorithm, with the appropriate input values, depending on the oversampling factor.

2. ±10 V testing using the EL3102 module. This approach is useful for interfacing with equipment such as an RTDS. Each EL3102 module provides two differential inputs with 16-bit resolution, with a sampling rate of up to 10 kHz. Within each module, the two inputs each have a dedicated ADC and are sampled at the same instant.

3. Using the IEC 61850-9-2 Sampled Value (SV) protocol [18] to acquire digital signals from a Merging Unit (MU) or other data source. This has been implemented using the efficient software library described in [19] and available at [20]. For convenience of testing the PMU with an RTDS, a sampling rate of 12.8 kHz has been used, but other sampling rates are supported (or will be supported in the future).

3.5 IEEE C37.118.2 communications output

The prototype PMU outputs IEEE C37.118.2 format data as either User Datagram Protocol (UDP) unicast, or UDP multicast with periodic transmission of configuration frames (e.g. once per second). The communications stack is based on a UDP implementation previously created for “tunnelling” IEC 61850 Ethernet traffic, which is available at [21]. This implementation requires the UDP payload (in a valid IEEE C37.118.2 format) to be provided as an input, and returns a properly-encoded Ethernet frame containing the Ethernet, IP, and UDP headers. This frame can be passed to a platform-specific function for transmitting an Ethernet frame on a specific hardware network interface.

Several C++ classes have been defined to manage the PMU configuration and generate valid UDP payloads for the IEEE C37.118.2 “Data Frame” and “Configuration Frame 2” formats. Additional PMUs or data values (such as per-phase phasors) can be added to the configuration with relatively few changes to the code.

It should be noted that TwinCAT 3 includes C++ libraries for Ethernet, IP, UDP, and TCP communications. However, for simplicity, these have not been used in the PMU prototype.

4 Laboratory Testing Configuration

4.1 Configuration for PMU Measurement Performance

An RTDS has been used to supply controllable signals to the PMUs under test, as shown in Figure 3. The RTDS supplies analogue waveforms (representing signals from voltage and current transformers) to the PMU inputs, with new values being calculated every 10 µs (which is the minimum possible simulation time-step).

An Arbiter 1201C GPS clock with 100 ns accuracy has been used to synchronise both the PMU and the RTDS. Within the RTDS, time synchronisation is managed by a “GTSYNC” card, which supports IRIG-B and PTP inputs, and can be used to distribute time to other devices using (e.g. using IRIG-B or 1 PPS signals).

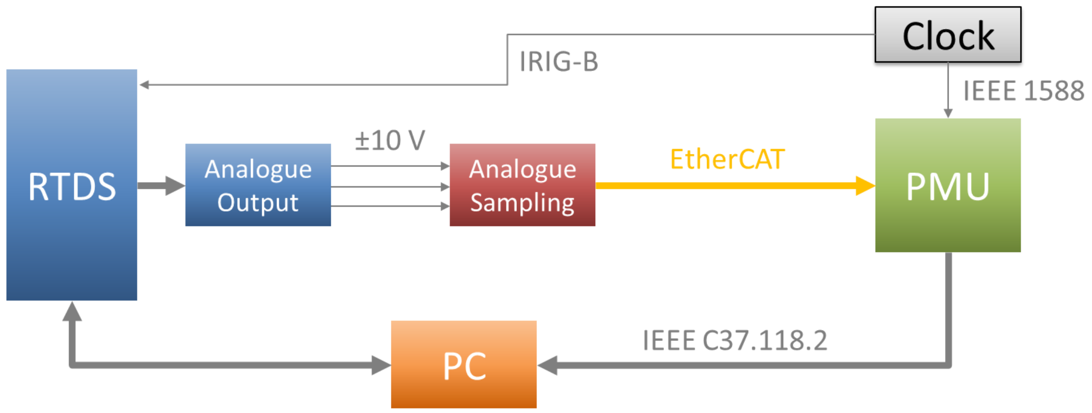

Figure 3: PMU closed-loop testing configuration

The RTDS also has the ability to digitally output the voltage and current signals using the IEC 61850-9-2 SV protocol, using the “GTNET” hardware card to emulate a Merging Unit (MU), as illustrated in Figure 4. Note that the PMU does not necessarily need to be synchronised, as long as the Second of Century (SOC) value is encoded in the SV frames. This significantly simplifies the PMU architecture, because the analogue processing and associated time synchronisation is delegated to the MU. However, it should be noted that this testing configuration does not involve analogue sampling because the MU is emulated and samples are passed to the PMU digitally; therefore, the PMU performance results would be expected to be better than for a real application.

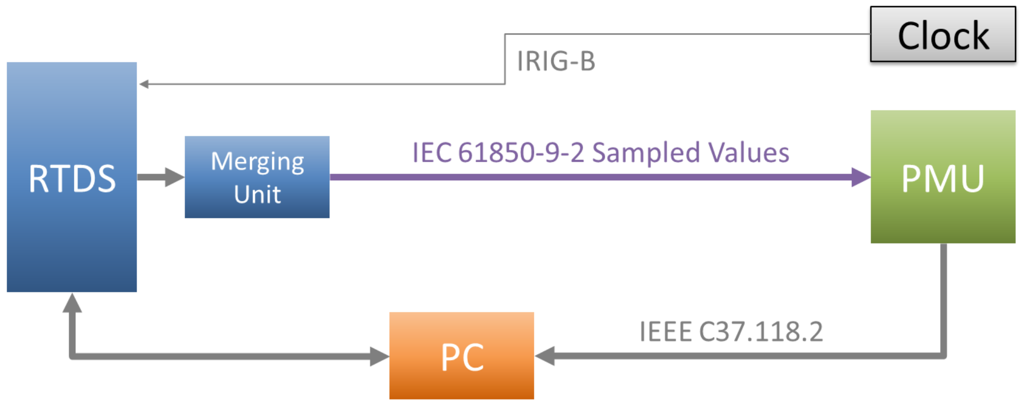

Figure 4: PMU testing using IEC 61850-9-2 SV protocol

The laboratory configuration is shown in Figure 5.

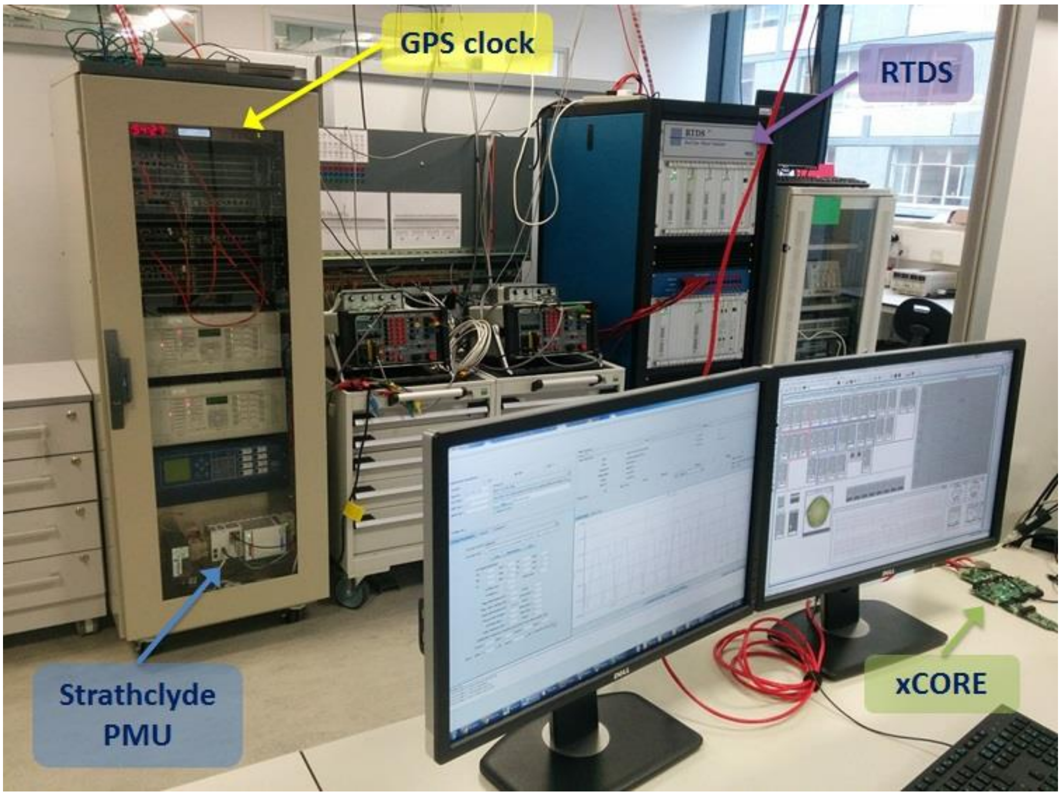

Figure 5: Laboratory testing configuration

It should be noted that this is a somewhat idealised testing arrangement; in particular, sensors (i.e. VTs or CTs) and the associated impact on magnitude and phase is not included. However, there are other factors which may introduce error, such as the lack temperature compensation for the analogue system.

The RTDS software application, called RSCAD, provides a script to automate PMU testing. However, the following changes have been made to the script for the purposes of this report:

- Added support for M-class PMUs.
- Added support for out-of-band (OOB) tests.
- Ensured correct observation of the settling period required for the static PMU tests (e.g. harmonics).
- The exclusion zone defined for frequency ramp tests has been revised according to the recommendation in [7], and to correctly distinguish between P-class and M-class PMU requirements.

4.2 Measuring PMU Reporting Latency

A new method for accurately determining the reporting latency of a PMU has been developed, which is illustrated in Figure 6. This method relies upon a receiving device, connected directly using an Ethernet to the PMU under test, which is synchronised to the same clock source as the PMU. Hardware timestamping within the Ethernet interface of the receiving devices allows for very accurate comparisons of the common time source to the timestamps in PMU output data stream.

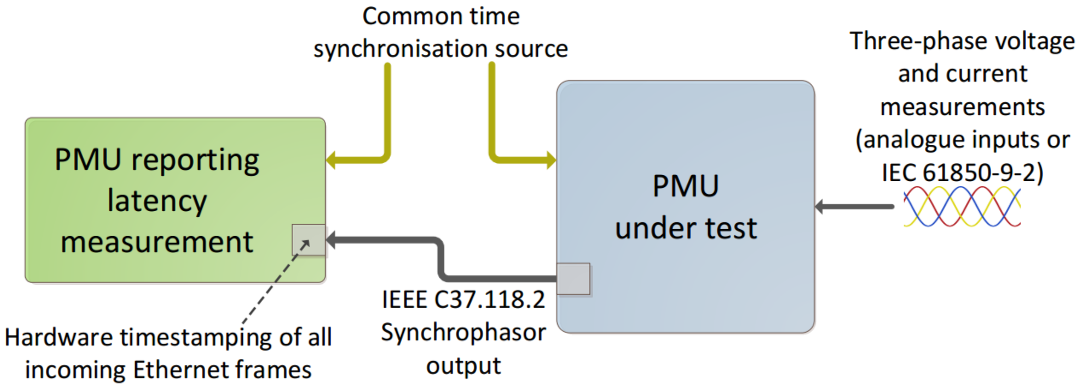

Figure 6: Overview of PMU reporting latency measurement method

The method operates in real-time, works passively for any existing PMU without requiring changes to the PMU hardware or software, and is very accurate — within the accuracy of the IEEE 1588 standard for time synchronisation, providing a measurement uncertainty of <500 ns in many cases, significantly surpassing the 0.002 s accuracy requirement in the most recent Synchrophasor standard.

The XMOS xCORE microcontroller platform has been used to implement the PMU reporting latency measurement method. This hardware platform is well-suited to real-time, deterministic applications involving Ethernet [22], has been previously demonstrated for use as real-time Ethernet delay emulation for time-critical protection applications [23] and IEC 61850-9-2 Sampled Value encoding performance analysis [24]. This is also a relatively low-cost hardware, at approximately €150. All software required has been open sourced and is available at [25].

It is particularly important to understand full system latency, including the impact of local or wide-area communications, rather than just the latency of the PMU device; the proposed method also supports such latency measurements.

5 System Validation and Calibration

5.1 Calibration of Magnitude and Timing Accuracy

The analogue output signals from the RTDS, which supply signals to the PMU, are not well-calibrated and are likely to be temperature-dependent (and temperature cannot be controlled without more specialised equipment). Furthermore, there is some uncertainty relating to exact time when analogue signals are sampled.

To compensate for these issues, the RTDS is configured to generate a “perfect” output i.e. a 1 pu balanced three-phase signal at nominal frequency and with zero phase shift. The PMU output can be monitored, with calibration values adjusted until the PMU output closely matches the expected value. A scaling factor is used to correct the magnitude output, and a phase offset is applied to the analogue sampling timestamps. Furthermore, the magnitude calibration is conducted per-phase. The calibration process is conducted before each PMU test.

5.2 Computational Performance

The PMU algorithm time processing time, for the P-class and M-class variants, is illustrated in Figure 7. This includes only the algorithm computation, not other aspects such as capturing analogue signals or communications. For this test, an input signal of 50 Hz and a reporting rate of 50 Hz have been used. Figure 7 highlights that the algorithm is relatively efficient, and M-class PMU computation consumes approximately 6-8% of the 100 µs cycle time (for an analogue sampling rate of 10 kHz).

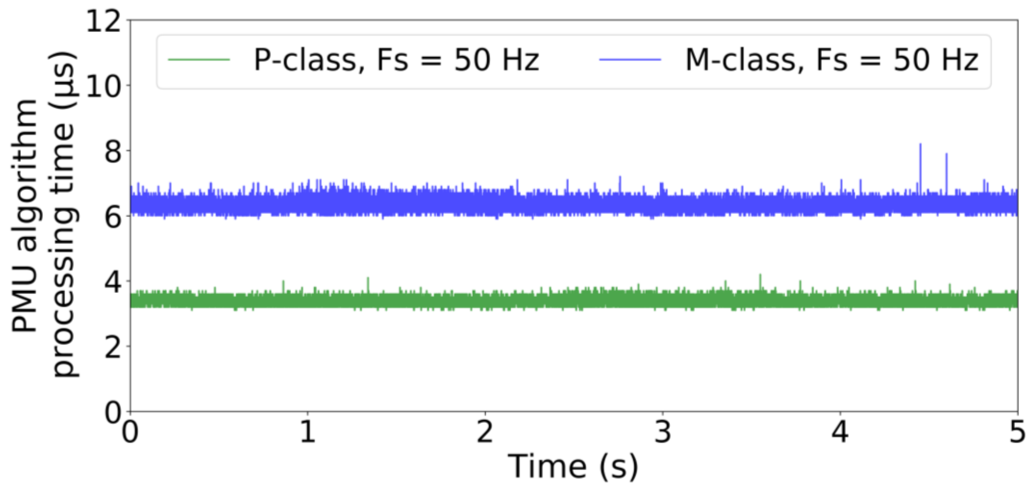

Figure 7: PMU algorithm processing time

Table 2 summarises the total CPU usage (as a percentage of a single core) for three different options, considering both the PMU algorithm computation and the IEEE C37.118.2 communications output. For the M-class PMU, these tasks require approximately 19.9 µs and 2.5 µs of CPU time, respectively. Equivalent results for the P-class PMU illustrate the slightly lower performance requirements. The use of the SV protocol as the data input for the PMU overall reduces the computational requirements, despite the additional processing required to read the SV Ethernet frames (e.g. 1600 frames per second, each containing 8 samples). This is due to the fact that the Beckhoff platform does not need to process the analogue signals, and is facilitated by the use of a very efficient SV protocol stack [19].

	Input type	Sampling rate	PMU algorithm computation	IEEE C37.118.2 communications output	Total CPU time (one core)
M-class PMU	Analogue	10 kHz	19.9%	2.5%	22.8%
P-class PMU	Analogue	10 kHz	16%	2.4%	18.8%
M-class PMU	SV	12.8 kHz	~13%	n/a – included in PMU algorithm	~13%

Table 2: Summary of PMU CPU usage

These results confirm that the platform provides sufficient performance to implement the full PMU architecture in real-time. Note that these results are for a single iteration of the PMU algorithm using a 100 µs cycle time; depending on the configuration of analogue input modules, a different cycle time may be used.

6 PMU Measurement Performance

6.1 Summary of Standard Measurement Tests

6.1.1 Strathclyde PMU Performance

The requirements and procedures defined in [6] and [7] require many individual tests to be executed and analysed to determine the performance of a PMU. To reduce the amount of data presented in this section, the results show only the *maximum* error value across all tests of a particular type, in order to give a conservative impression of the PMU performance in the worst case. The full results are given in Appendix A.

The M-class and P-class results for the RTDS testing method described in Section 4.1 are given in Table 3 and Table 4, respectively. Total Vector Error (TVE) values are given per-phase (e.g. "TVE-Va" refers to the phase A TVE). For convenience, each table also shows how the results compare to the appropriate standard requirements. Note that P-class PMUs do not need to pass the OOB tests to comply with the standard. The PMU prototype does not have current inputs, so the current magnitude tests are not performed.

In all cases, the PMU results are well within the standard requirements. In particular, the M-class algorithm can achieve TVE values as low as approximately 0.01% in the static tests (where the requirement is 1%). The TVE in the static tests (i.e. Frequency Range, Voltage Magnitude, and Harmonic Distortion) is dominated by magnitude error, rather than phase error. The TVE differs across the three phases and this behaviour is due to slightly differing analogue noise for each phase. The P-class algorithm has generally slightly higher errors, as would be expected due to the shorter measurement window used.

	FE (Hz)	**RFE (Hz/s)**	**TVE-Va (%)**	**TVE-Vb (%)**	**TVE-Vc (%)**
Frequency Range	0.000172	0.006656	0.0118	0.007	0.0094
Voltage Magnitude	n/a	n/a	0.0095	0.0056	0.007
Harmonic Distortion	0.000092	0.003638	0.0129	0.0058	0.009
Measurement Bandwidth: Magnitude Modulation	0.000191	0.01732	0.2688	0.271	0.2712
Measurement Bandwidth Test: Phase Modulation	0.008584	0.337966	0.2543	0.2514	0.2537
Frequency Ramp	0.000193	0.005492	0.1316	0.1227	0.1199
OOB	0.000587	0.049334	0.0594	0.0515	0.0523
Results as percentage of standard requirements:					
	FE	**RFE**	**TVE-Va**	**TVE-Vb**	**TVE-Vc**
Frequency Range	3.4%	6.7%	1.2%	0.7%	0.9%
Voltage Magnitude	n/a	n/a	1.0%	0.6%	0.7%
Harmonic Distortion	0.4%	n/a	1.3%	0.6%	0.9%
Measurement Bandwidth: Magnitude Modulation	0.1%	0.1%	9.0%	9.0%	9.0%
Measurement Bandwidth Test: Phase Modulation	2.9%	2.4%	8.5%	8.4%	8.5%
Frequency Ramp	1.9%	2.7%	13.2%	12.3%	12.0%
OOB	5.9%	n/a	4.6%	4.0%	4.0%

Table 3: M-class PMU performance (maximum error for each test)

	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
Frequency Range	0.000626	0.053213	0.0125	0.0066	0.0088
Voltage Magnitude	n/a	n/a	0.0109	0.0059	0.0072
Harmonic Distortion	0.000614	0.048039	0.0137	0.0072	0.0086
Measurement Bandwidth: Magnitude Modulation	0.000637	0.045872	0.0723	0.0556	0.0549
Measurement Bandwidth Test: Phase Modulation	0.000724	0.331063	0.0565	0.0595	0.0619
Frequency Ramp	0.000603	0.04974	0.0367	0.0292	0.0282
OOB	n/a	n/a	n/a	n/a	n/a
Results as percentage of standard requirements:					
	FE	**RFE**	**TVE-Va**	**TVE-Vb**	**TVE-Vc**
Frequency Range	12.5%	13.3%	1.3%	0.7%	0.9%
Voltage Magnitude	n/a	n/a	1.1%	0.6%	0.7%
Harmonic Distortion	12.3%	12.0%	1.4%	0.7%	0.9%
Measurement Bandwidth: Magnitude Modulation	1.1%	2.0%	2.4%	1.9%	1.8%
Measurement Bandwidth Test: Phase Modulation	1.2%	14.4%	1.9%	2.0%	2.1%
Frequency Ramp	6.0%	12.4%	3.7%	2.9%	2.8%
OOB	n/a	n/a	n/a	n/a	n/a

Table 4: P-class PMU performance (maximum error for each test)

From the full OOB results given in Appendix A, it can be observed that that – as would be expected – interharmonics closer to $\frac{F_S}{2}$ or $F_S + \frac{F_S}{2}$ tend to result in slightly higher TVE; however, the differences are relatively small.

Table 5 summarises the performance of the M-class PMU algorithm for step response tests. The results are well with the standard requirements.

	Response time	Delay time	Maximum overshoot/undershoot
Positive Step: Magnitude	0.050515 s	0.000758 s	1.11%
Negative Step: Magnitude	0.054151 s	0.000763 s	1.11%
Positive Step: Phase	0.066457 s	0.002527 s	0.68%
Negative Step: Phase	0.066312 s	0.002449 s	0.68%

Table 5: Summary of step reponse tests (maximum for all phases)

6.1.2 Comparison to IEEE C37.118.1 Annex C Implementation

The RTDS GTNET card can be used to emulate a PMU, according to the IEEE C37.118.1 Annex C reference PMU. Appendix B provides the results for the M-class version, but it must be remembered that the samples are transferred digitally from the RTDS simulation to the GTNET i.e. there is no analogue system. Despite this advantage, comparing the results in Table 3 and Table 8 show that the Strathclyde PMU algorithm achieves better results for the OOB and Frequency Range tests. Furthermore, in the Frequency Range tests, the reference PMU performance is worse for tests further from the nominal frequency; the Strathclyde PMU performs similarly across all tested frequencies.

6.2 PMU Reporting Latency

Using the method described in Section 4.2, the measured PMU reporting latency results are summarised in Table 6. Two PMU implementations have been used: the RTDS GTNET

Simulated PMU and the Strathclyde PMU implementation. In all cases, 7000 samples have been taken. For convenience, a non-PTP Ethernet switch has been used for some of the tests involving the Strathclyde PMU. This means that these latency measurements have an error of approximately 10 μs, but this is well within the Synchrophasor standard requirements and only comprises a small proportion of the actual measurement values. In all cases, a 50 Hz nominal power system frequency is used, and the measured reporting latency is well within the standard requirements of $2/F_s$ (for P class) or $7/F_s$ (for M class), where F_s is the PMU reporting rate. Note that the two-rack RTDS configuration used in these tests incurs an inherent inter-rack delay of one simulation time-step, or 50 μs, but this does not significantly affect the results.

PMU device	PMU input type	Signal input (Hz)	Reporting rate, F_s (Hz)	PMU class	Mean latency (ms)	Std. dev. of latency (μs)	Theoretical latency, based on window length (ms)	Difference between measured mean latency and theoretical latency length (ms)
RTDS GTNET	Digital	50	50	P	21.595	8.7	20.0	1.595
RTDS GTNET	Digital	50	50	M	91.846	8.0	88.75	3.096
RTDS GTNET	Digital	50	100	P	21.594	6.4	20.0	1.594
RTDS GTNET	Digital	50	100	M	44.344	6.4	41.25	3.094
Strathclyde	Analogue	50	50	P	20.234	28.9	20.0	0.234
Strathclyde	Analogue	50	50	M	100.231	29.3	100.0	0.231
Strathclyde	Analogue	50	100	P	20.240	27.6	20.0	0.240
Strathclyde	Analogue	50	100	M	60.230	32.4	60.0	0.230
Strathclyde	IEC 61850 Sampled Values	50	50	M	101.001	29.6	100.0	1.001
Strathclyde	Analogue	55	100	M	54.780	31.8	54.545	0.234
Strathclyde	Analogue	45	100	M	66.898	24.9	66.667	0.232

Table 6: PMU reporting latency results

This method can also be used to estimate the impact of the processing time of the PMU under test. For example, the Strathclyde M-class PMU algorithm uses a ten-cycle window length (i.e. the total filter group delay) for a 50 Hz reporting rate, which equates to 200 ms at nominal frequency. The Synchrophasor report timestamp is defined as corresponding to the middle of the window; therefore, the theoretical PMU reporting latency, at nominal frequency, is 200 ms / 2 = 100 ms. From the measured reporting latency results in Table 6, it can be calculated that the additional latency due to measurement acquisition, algorithm processing, and generating valid PMU report Ethernet frames is approximately 100.231 ms - 100 ms = 0.231 ms. The results for each test are given in the final column in Table 6; the range in values illustrates that the choice of the implementation platform and protocols can significantly impact the overall latency.

The reporting latency can also be calculated internally within the Strathclyde PMU software, albeit without the same level of accuracy due to the lack of Ethernet hardware timestamping. This yields results that are consistent with Table 6.

6.3 Impact of IEC 61850-9-2 Sampled Value Inputs

Table 7 summarises the performance of the M-class PMU using the SV protocol to obtain input data, rather than analogue inputs. As would be expected for such non-realistic conditions (due to the lack of any analogue system), the results are better than those given in Table 3. This highlights the importance of including the full analogue system (i.e. 16-bit ADC quantisation errors, and other factors) when conducting realistic PMU performance testing.

	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
Frequency Range	0.000004	0.000163	0.0005	0.0006	0.0006
Voltage Magnitude	n/a	n/a	0.0002	0.0004	0.0002
Harmonic Distortion	0	0	0.0002	0.0002	0.0003
Measurement Bandwidth: Magnitude Modulation	0.000004	0.000155	0.2694	0.2694	0.2694
Measurement Bandwidth Test: Phase Modulation	0.008581	0.335933	0.2507	0.2508	0.2507
Frequency Ramp	0.000043	0.000118	0.1197	0.1197	0.1197
OOB	0.000496	0.046172	0.0511	0.0512	0.0511
Results as percentage of standard requirements:					
	FE	**RFE**	**TVE-Va**	**TVE-Vb**	**TVE-Vc**
Frequency Range	0.1%	0.2%	0.1%	0.1%	0.1%
Voltage Magnitude	n/a	n/a	0.0%	0.0%	0.0%
Harmonic Distortion	0.0%	n/a	0.0%	0.0%	0.0%
Measurement Bandwidth: Magnitude Modulation	0.0%	0.0%	9.0%	9.0%	9.0%
Measurement Bandwidth Test: Phase Modulation	2.9%	2.4%	8.4%	8.4%	8.4%
Frequency Ramp	0.4%	0.1%	12.0%	12.0%	12.0%
OOB	5.0%	n/a	3.9%	3.9%	3.9%

Table 7: M-class PMU performance using SV input (maximum error for each test)

6.4 Extended Harmonics, Interharmonics, and Unbalance Testing

The Synchrophasor standard only requires that each disturbance type (harmonics, off-nominal frequency, etc.) is tested in isolation. However, real power systems may experience multiple simultaneous issues – and it is during these conditions that measurement accuracy is most critical. A test with multiple disturbances has been conducted to illustrate resilience under realistic worst-case scenarios. The following test parameters have been chosen (within the capabilities of the RTDS PMU test software):

- Actual system frequency: 50.04 Hz.
- Harmonics: 7^{th} and 11^{th}, 0.05 pu magnitude each.
- Unbalance: phase A at 1.0 pu, phase B at 0.9 pu, and phase C at 0.8 pu.
- Interharmonic: 79.5 Hz at 0.01 pu magnitude.
- Frequency drop: 50.04 Hz to 49.4 Hz with ROCOF of 1 Hz/s.

Figure 8 shows a sample of the waveform injected into the PMU, which clearly illustrates the harmonics and unbalance.

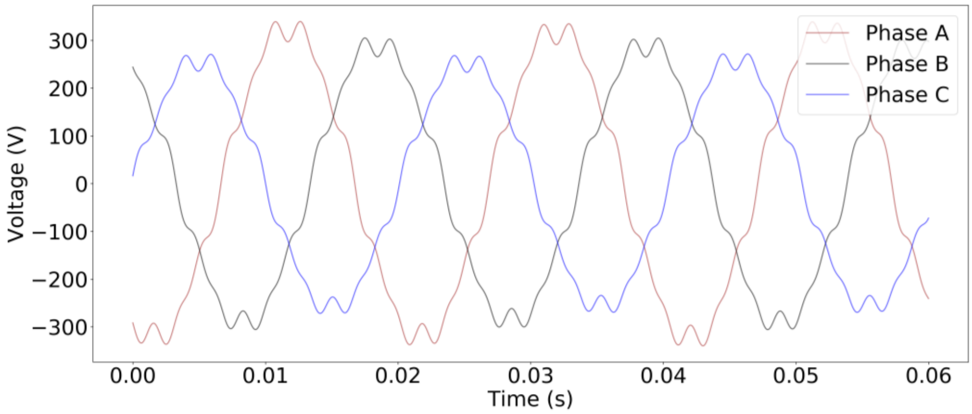

Figure 8: Generated waveform

Figure 9 compares the results for frequency (and other parameters) under these conditions, using an M-class PMU. Only phase A is shown for simplicity. Although it may appear that the PMU is reacting to changes in frequency and ROCOF in advance of the drop being applied, this is correct behaviour which is due to intentional correction of the measurement timestamps by the PMU algorithm. The maximum TVE during the test is approximately 0.1%. The maximum FE (which occurs at the start of the frequency drop, which would normally be exempt by the standard requirements) is approximately 0.01 Hz. These results, while somewhat arbitrary, illustrate that the PMU algorithm is highly resilient to significant disturbances.

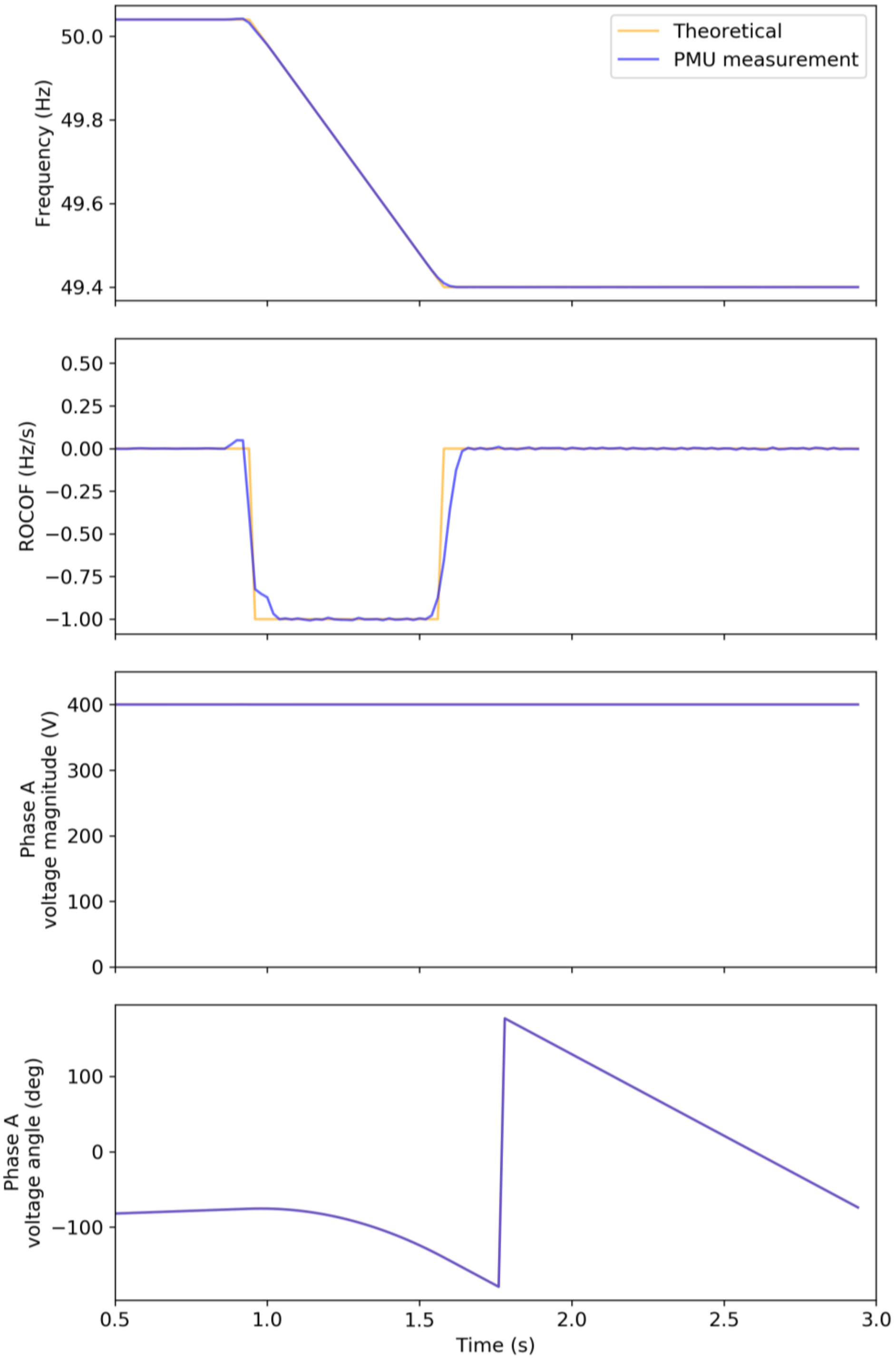

Figure 9: Comparison of theoretical and measured parameters

6.5 Behaviour During Simulated Power System Fault

It is possible to emulate the impact of a three-phase fault on voltage signals by applying a significant voltage magnitude step using the RTDS PMU Test Utility. This means that it is convenient to compare the theoretical and measured parameters; for arbitrary fault waveforms, it is more complicated to quantitatively determine the PMU performance. Figure 10 compares the performance of the M-class Strathclyde PMU algorithm for a voltage magnitude step change from 1.0 pu to 0.1 pu. All other parameters are at nominal values.

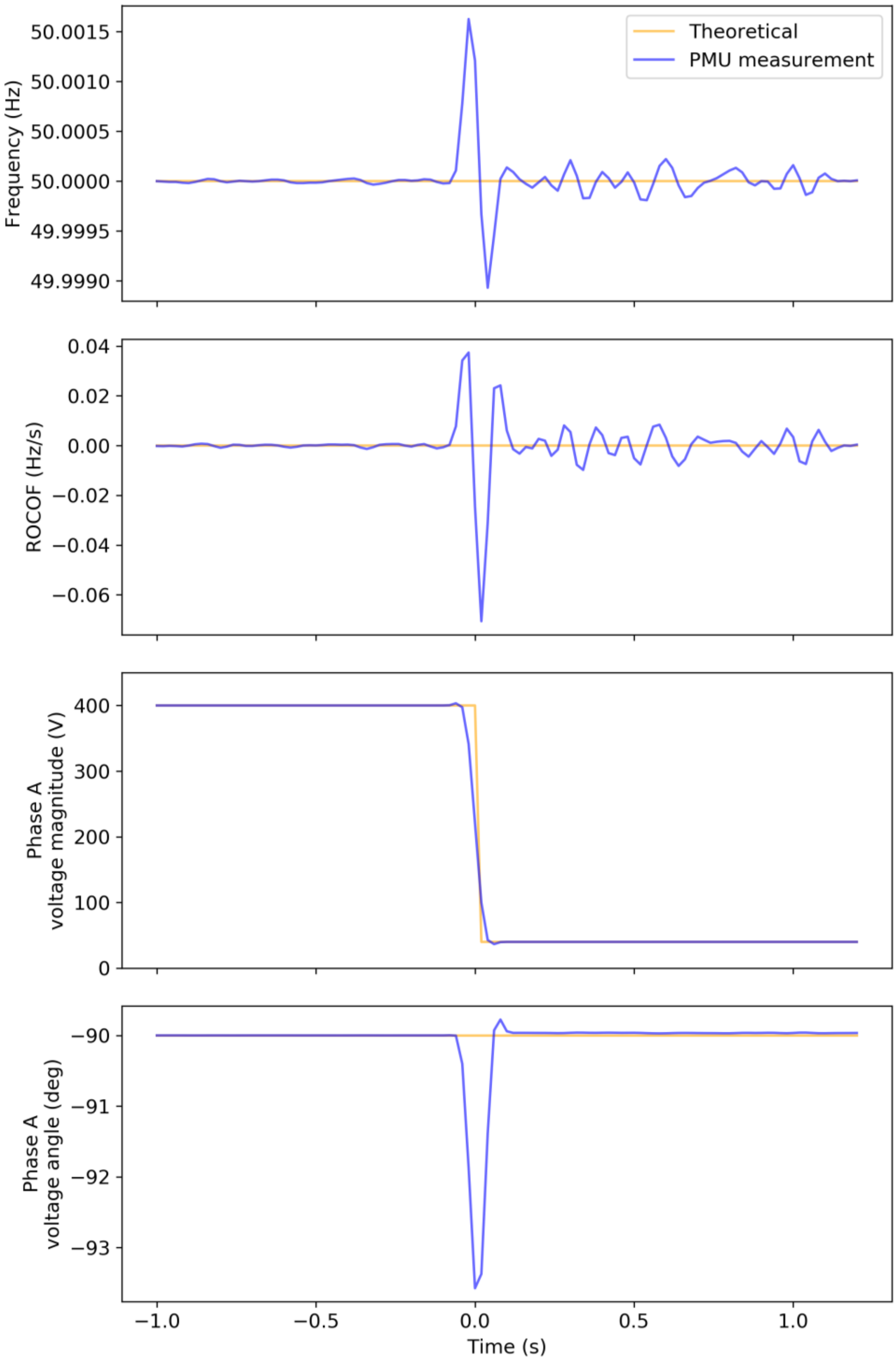

Figure 10: Comparison of theoretical and measured parameters during emulated fault

While the PMU exhibits only a relatively small FE during this event, and other PMUs would be expected to perform similarly under such extreme dynamic conditions, it is clear that the temporary deviation in phase could be misleading. Similarly, step changes in phase create temporary deviations in PMU frequency output. Real-time systems which use PMU data, such as for enabling faster frequency response schemes [26], must cater for these characteristics; alternatively, new measurands are required which adapt to dynamic events.

7 Conclusions

This report has documented the implementation and testing of a hardware PMU prototype, using a Beckhoff-based hardware platform. This platform offers several convenient features for PMU development, such as hardware modularity, support for integrating C++ and Simulink models, IEEE 1588 support, and scalability to multiple measurement locations. The Strathclyde M-class PMU algorithm can be deployed on this platform requiring less than 8% of the CPU time of a single CPU core, with 10 kHz analogue sampling. The platform could be used for other applications such as power quality monitoring or integration of control algorithms.

A closed-loop testing procedure, using RTDS hardware and software, has been used to quantify the performance of the Strathclyde PMU algorithm, and for comparison to a reference PMU implementation. With proper calibration of the analogue system, as would be the case for a PMU to be deployed in the field, the PMU can achieve relatively low error metrics according to the Synchrophasor standard requirements.

Additional tests with multiple disturbances and with emulation of a power system fault have been conducted to demonstrate that PMU algorithms require resilience under realistic worst-case scenarios – and to make a case for testing all PMUs in this way.

A new method has been devised for accurately and conveniently characterising the reporting latency of PMUs. Although the Synchrophasor standard prescribes relatively simple requirements for PMU reporting latency, and PMUs are obliged to merely meet the maximum latency threshold over 1000 samples, there are many emerging power system protection and control applications which could benefit from faster-acting measurements and more accurate knowledge of the actual latency of the PMUs used to implement novel control and protection schemes.

Future work will integrate the algorithm within Synaptec’s passive and distributed optical sensing platform to deliver high-quality P-class and M-class synchrophasor measurements from a wide area of a power system.

8 Appendix A: Full PMU Performance Testing Results

8.1 M-class

Frequency Range Test					

Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
45	0.000111	0.004271	0.0114	0.0036	0.0044
45.5	0.000114	0.003555	0.0096	0.0033	0.0059
46	0.000134	0.003596	0.0095	0.0039	0.0062
46.5	0.000092	0.0027	0.0101	0.0029	0.0054
47	0.000118	0.003527	0.0096	0.0039	0.007
47.5	0.000107	0.00348	0.0093	0.0042	0.0073
48	0.000076	0.002867	0.0094	0.007	0.0094
48.5	0.00008	0.002578	0.0105	0.0029	0.0069
49	0.000084	0.003436	0.0113	0.003	0.0054
49.5	0.000065	0.002982	0.0108	0.0032	0.0052
50	0.000088	0.003178	0.0118	0.0033	0.0066
50.5	0.000084	0.0033	0.0097	0.0043	0.0069
51	0.000114	0.004822	0.0092	0.0049	0.0077
51.5	0.000099	0.00362	0.0089	0.0054	0.0088
52	0.000107	0.005282	0.0105	0.0062	0.0089
52.5	0.000114	0.004861	0.0106	0.0025	0.0048
53	0.00013	0.006478	0.0094	0.0057	0.0088
53.5	0.000122	0.004763	0.0104	0.0036	0.0066
54	0.000122	0.005938	0.01	0.0056	0.0087
54.5	0.000172	0.005236	0.0091	0.0037	0.0068
55	0.000145	0.006656	0.0094	0.0055	0.0073
Result	Pass	Pass	Pass	Pass	Pass
Voltage Magnitude Test					

Voltage (pu)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)		
0.8	0.0093	0.0045	0.007		
0.9	0.0077	0.0026	0.0068		
1	0.0095	0.0036	0.0054		
1.1	0.009	0.0056	0.0067		
1.2	0.005	0.0034	0.0068		
Result	Pass	Pass	Pass		
Current Magnitude Test					

Current (pu)	TVE-Ia (%)	TVE-Ib (%)	TVE-Ic (%)	TVE-I+ (%)	
0.1	0	0	0	0	
0.2	0	0	0	0	
0.3	0	0	0	0	
0.4	0	0	0	0	
0.5	0	0	0	0	
0.6	0	0	0	0	
0.7	0	0	0	0	
0.8	0	0	0	0	
0.9	0	0	0	0	
1	0	0	0	0	
1.1	0	0	0	0	
1.2	0	0	0	0	
1.3	0	0	0	0	
1.4	0	0	0	0	
1.5	0	0	0	0	
1.6	0	0	0	0	
1.7	0	0	0	0	
1.8	0	0	0	0	
1.9	0	0	0	0	
2	0	0	0	0	
Result	Pass	Pass	Pass	Pass	
Harmonic Distortion Test					

Harmonic No.	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
2	0.000069	0.002702	0.009	0.0042	0.0068
3	0.00008	0.003048	0.0093	0.0057	0.0067
4	0.000092	0.003397	0.0103	0.0037	0.0072
5	0.000084	0.003282	0.0118	0.004	0.0062
6	0.000076	0.003387	0.0103	0.0034	0.0046
7	0.000076	0.003358	0.0101	0.004	0.009
8	0.00008	0.003638	0.0084	0.0044	0.0077
9	0.000076	0.002876	0.0129	0.0058	0.0059
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Magnitude Modulation					

Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0.000084	0.003405	0.0112	0.0056	0.0087
0.3	0.000092	0.004508	0.0142	0.0085	0.0094
0.5	0.000069	0.003218	0.0259	0.0174	0.0185

0.7	0.00008	0.00333	0.0386	0.0347	0.035
0.9	0.00008	0.003219	0.0618	0.0559	0.057
1.1	0.000191	0.01732	0.0913	0.0834	0.0837
1.3	0.000095	0.003397	0.1237	0.1154	0.1155
1.5	0.000084	0.003534	0.1563	0.1545	0.1539
1.7	0.000076	0.002814	0.1987	0.1973	0.197
1.9	0.000061	0.002588	0.254	0.2463	0.2465
2	0.000084	0.003434	0.2688	0.271	0.2712
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Phase Modulation					
--					
Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0.000094	0.00432	0.014	0.005	0.0048
0.3	0.000116	0.004277	0.0177	0.0075	0.0086
0.5	0.000194	0.008144	0.018	0.0215	0.025
0.7	0.000451	0.016711	0.0338	0.0311	0.0334
0.9	0.000832	0.031737	0.054	0.0521	0.0543
1.1	0.001501	0.057173	0.0818	0.0794	0.0803
1.3	0.00243	0.091762	0.1115	0.1069	0.1084
1.5	0.003668	0.13994	0.1482	0.1416	0.1422
1.7	0.005307	0.20586	0.1838	0.183	0.185
1.9	0.007389	0.289136	0.2335	0.2309	0.2325
2	0.008584	0.337966	0.2543	0.2514	0.2537
Result	Pass	Pass	Pass	Pass	Pass
Frequency Ramp Test					

Frequency Ramp(Hz/s)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
1	0.000156	0.003728	0.1316	0.1227	0.1199
-1	0.000193	0.005492	0.0958	0.0961	0.0977
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Magnitude					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.050515	0.05044	0.050444
Delay time (s)			0.000128	0.000742	0.000758
Maximum overshoot/undershoot (%)			1.07	1.11	1.09
Result	Pass	Pass	Pass	Pass	Pass

Negative Step Response Test : Magnitude					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.051494	0.051798	0.054151
Delay time (s)			0.000034	0.000736	0.000763
Maximum overshoot/undershoot (%)			1.04	1.11	1.09
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Phase					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0.133173	0.17163	0.062476	0.066457	0.062769
Delay time (s)			0.001035	0.002527	0.000735
Maximum overshoot/undershoot (%)			0.68	0.66	0.67
Result	Pass	Pass	Pass	Pass	Pass
Negative Step Response Test : Phase					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0.133153	0.171678	0.062457	0.066312	0.063275
Delay time (s)			0.000808	0.002335	0.002449
Maximum overshoot/undershoot (%)			0.68	0.67	0.67
Result	Pass	Pass	Pass	Pass	Pass
OOB Test					

Frequency Ramp(Hz/s)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
50.0Hz_24.9Hz	0.000072	0.003134	0.0479	0.0398	0.0404
50.0Hz_24.8Hz	0.000076	0.004075	0.0384	0.0401	0.0395
50.0Hz_24.6Hz	0.000103	0.004976	0.0364	0.0392	0.0383
50.0Hz_24.2Hz	0.000126	0.006968	0.0354	0.0369	0.0363
50.0Hz_23.4Hz	0.000252	0.019631	0.0434	0.0332	0.0341
50.0Hz_21.8Hz	0.000511	0.043837	0.0306	0.0322	0.0307
50.0Hz_18.6Hz	0.000351	0.028734	0.0219	0.0182	0.0184
50.0Hz_12.2Hz	0.00013	0.009472	0.0074	0.0041	0.0058
50.0Hz_10.0Hz	0.000088	0.003338	0.0099	0.0046	0.0056
50.0Hz_75.1Hz	0.00008	0.003587	0.0379	0.0403	0.0402
50.0Hz_75.2Hz	0.00008	0.004023	0.0451	0.039	0.0385
50.0Hz_75.4Hz	0.000088	0.004424	0.0454	0.0374	0.0371
50.0Hz_75.8Hz	0.000141	0.008086	0.0443	0.0371	0.0369
50.0Hz_76.6Hz	0.000248	0.018746	0.0424	0.0332	0.0334

50.0Hz_78.2Hz	0.000511	0.04117	0.0346	0.0309	0.0309
50.0Hz_81.4Hz	0.000355	0.026918	0.025	0.0177	0.0178
50.0Hz_87.8Hz	0.000134	0.008818	0.0142	0.0052	0.0057
50.0Hz_100.0Hz	0.000076	0.002983	0.0119	0.0052	0.0056
52.5Hz_27.4Hz	0.000229	0.015916	0.0584	0.0515	0.0509
52.5Hz_27.3Hz	0.000259	0.013878	0.0594	0.0496	0.05
52.5Hz_27.1Hz	0.000172	0.011985	0.0555	0.048	0.0479
52.5Hz_26.7Hz	0.00016	0.005639	0.0532	0.0453	0.0447
52.5Hz_25.9Hz	0.000118	0.004376	0.0484	0.0395	0.0397
52.5Hz_24.3Hz	0.000343	0.02686	0.0427	0.0348	0.0352
52.5Hz_21.1Hz	0.000587	0.048693	0.034	0.0269	0.0276
52.5Hz_14.7Hz	0.000244	0.016951	0.0151	0.0082	0.0087
52.5Hz_10.0Hz	0.000122	0.004747	0.0114	0.0041	0.0041
52.5Hz_77.6Hz	0.000233	0.014739	0.0586	0.0514	0.0523
52.5Hz_77.7Hz	0.000214	0.013824	0.0577	0.0508	0.0505
52.5Hz_77.9Hz	0.000221	0.010209	0.0551	0.0487	0.0491
52.5Hz_78.3Hz	0.000122	0.004765	0.0522	0.0465	0.0458
52.5Hz_79.1Hz	0.000122	0.00464	0.047	0.0412	0.041
52.5Hz_80.7Hz	0.000347	0.02594	0.0412	0.0357	0.0359
52.5Hz_83.9Hz	0.000557	0.049334	0.0328	0.0285	0.0292
52.5Hz_90.3Hz	0.000252	0.016033	0.0154	0.0086	0.0091
52.5Hz_103.1Hz	0.000134	0.0046	0.0114	0.0035	0.006
52.5Hz_105.0Hz	0.000118	0.003609	0.0093	0.0059	0.0087
47.5Hz_22.4Hz	0.000233	0.014202	0.0428	0.0385	0.0376
47.5Hz_22.3Hz	0.000256	0.015875	0.0423	0.0386	0.0373
47.5Hz_22.1Hz	0.000309	0.019039	0.0428	0.0372	0.0365
47.5Hz_21.7Hz	0.000347	0.024775	0.0413	0.0373	0.0351
47.5Hz_20.9Hz	0.000511	0.036306	0.0401	0.0359	0.0345
47.5Hz_19.3Hz	0.000546	0.040468	0.0357	0.031	0.0291
47.5Hz_16.1Hz	0.000122	0.004925	0.0165	0.0132	0.0115
47.5Hz_10.0Hz	0.000111	0.003377	0.0101	0.0052	0.0065
47.5Hz_72.6Hz	0.000229	0.014202	0.0426	0.0394	0.0376
47.5Hz_72.7Hz	0.000256	0.015369	0.042	0.0391	0.0377
47.5Hz_72.9Hz	0.000282	0.018474	0.042	0.0391	0.0367
47.5Hz_73.3Hz	0.000359	0.024049	0.0403	0.038	0.0368
47.5Hz_74.1Hz	0.000481	0.036143	0.0397	0.0373	0.0353
47.5Hz_75.7Hz	0.000534	0.04158	0.0342	0.0305	0.0306
47.5Hz_78.9Hz	0.00013	0.00577	0.0175	0.0136	0.0119
47.5Hz_85.3Hz	0.000111	0.003319	0.0108	0.007	0.0068
47.5Hz_95.0Hz	0.000092	0.003132	0.0116	0.0047	0.0061
Result	Pass	Pass	Pass	Pass	Pass

8.2 P-class

Frequency Range Test					

Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
45	0.000431	0.021803	0.0104	0.0053	0.0068
45.5	0.00045	0.027769	0.0103	0.004	0.0054
46	0.00032	0.022161	0.011	0.0052	0.0063
46.5	0.00037	0.027865	0.0124	0.0061	0.0052
47	0.000366	0.029027	0.01	0.0051	0.0067
47.5	0.000336	0.025947	0.0093	0.0062	0.0088
48	0.000393	0.03062	0.0106	0.005	0.0077
48.5	0.000401	0.029834	0.0108	0.0062	0.0076
49	0.000465	0.033774	0.0118	0.0051	0.0064
49.5	0.00045	0.025846	0.0114	0.0056	0.0058
50	0.000538	0.039931	0.0109	0.0057	0.0071
50.5	0.000362	0.033958	0.0108	0.0044	0.0071
51	0.00042	0.031853	0.0115	0.004	0.0064
51.5	0.000549	0.035674	0.0108	0.0058	0.0079
52	0.000542	0.043192	0.0098	0.0066	0.0072
52.5	0.000496	0.035721	0.0105	0.0049	0.0073
53	0.000462	0.043929	0.0107	0.0046	0.006
53.5	0.000462	0.045094	0.0104	0.0054	0.0077
54	0.00061	0.043322	0.0108	0.0046	0.0082
54.5	0.000515	0.041869	0.0125	0.0054	0.0065
55	0.000626	0.053213	0.0115	0.0063	0.0079
Result	Pass	Pass	Pass	Pass	Pass
Voltage Magnitude Test					

Voltage (pu)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)	TVE-V+ (%)	
0.8	0.0096	0.0059	0.0072	0	
0.9	0.0109	0.0052	0.0071	0	
1	0.0068	0.0057	0.0067	0	
1.1	0.0096	0.0047	0.006	0	
1.2	0.0087	0.0042	0.0067	0	
Result	Pass	Pass	Pass	Pass	
Current Magnitude Test					

Current (pu)	TVE-Ia (%)	TVE-Ib (%)	TVE-Ic (%)	TVE-I+ (%)	
0.1	0	0	0	0	
0.2	0	0	0	0	
0.3	0	0	0	0	
0.4	0	0	0	0	

0.5	0	0	0	0	
0.6	0	0	0	0	
0.7	0	0	0	0	
0.8	0	0	0	0	
0.9	0	0	0	0	
1	0	0	0	0	
1.1	0	0	0	0	
1.2	0	0	0	0	
1.3	0	0	0	0	
1.4	0	0	0	0	
1.5	0	0	0	0	
1.6	0	0	0	0	
1.7	0	0	0	0	
1.8	0	0	0	0	
1.9	0	0	0	0	
2	0	0	0	0	
Result	Pass	Pass	Pass	Pass	
Harmonic Distortion Test					

Harmonic No.	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
2	0.0005	0.0324	0.0082	0.0044	0.0068
3	0.000614	0.048039	0.0125	0.0059	0.0056
4	0.000484	0.036759	0.0077	0.0052	0.0066
5	0.000538	0.034382	0.0102	0.0064	0.0086
6	0.000427	0.030211	0.0137	0.0072	0.0053
7	0.000542	0.040948	0.0128	0.0063	0.0069
8	0.00045	0.033946	0.0086	0.0062	0.0086
9	0.000465	0.035101	0.008	0.0052	0.007
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Magnitude Modulation					

Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0.000637	0.045872	0.0119	0.007	0.0084
0.3	0.000576	0.040801	0.0091	0.0056	0.0074
0.5	0.000534	0.03565	0.011	0.0058	0.0082
0.7	0.000519	0.030477	0.0169	0.0095	0.0085
0.9	0.000427	0.033736	0.0196	0.0129	0.0126
1.1	0.000534	0.045015	0.0219	0.018	0.018
1.3	0.000401	0.035409	0.0343	0.0237	0.0247
1.5	0.000572	0.039182	0.036	0.0312	0.0316

1.7	0.000465	0.031011	0.0484	0.0402	0.0422
1.9	0.000519	0.031568	0.0606	0.0511	0.0508
2	0.000416	0.03466	0.0723	0.0556	0.0549
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Phase Modulation					

Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0.000592	0.043974	0.0088	0.0056	0.008
0.3	0.000485	0.043962	0.0079	0.0057	0.0078
0.5	0.000492	0.032705	0.0081	0.01	0.0085
0.7	0.000458	0.037116	0.0089	0.0095	0.0103
0.9	0.000417	0.056386	0.0194	0.0151	0.0164
1.1	0.00051	0.07538	0.0241	0.0194	0.0202
1.3	0.000516	0.106849	0.026	0.0285	0.0301
1.5	0.000539	0.151275	0.0371	0.034	0.0371
1.7	0.000632	0.213543	0.0409	0.042	0.0451
1.9	0.000662	0.286285	0.0486	0.0524	0.0549
2	0.000724	0.331063	0.0565	0.0595	0.0619
Result	Pass	Pass	Pass	Pass	Pass
Frequency Ramp Test					

Frequency Ramp(Hz/s)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
1	0.000534	0.04248	0.0367	0.0292	0.0271
-1	0.000603	0.04974	0.0236	0.0242	0.0282
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Magnitude					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.025023	0.021295	0.021201
Delay time (s)			0.000027	0.000785	0.000786
Maximum overshoot/undershoot (%)			0.08	0.02	0.02
Result	Pass	Pass	Pass	Pass	Pass
Negative Step Response Test : Magnitude					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.025858	0.021768	0.021716
Delay time (s)			0.000075	0.000784	0.00079

Maximum overshoot/undershoot (%)			0.07	0.03	0.03
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Phase					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0.059818	0.059873	0.023659	0.029033	0.028432
Delay time (s)			0.000163	0.001426	0.001272
Maximum overshoot/undershoot (%)			0.01	0.01	0.02
Result	Pass	Pass	Pass	Pass	Pass
Negative Step Response Test : Phase					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0.059821	0.059877	0.023538	0.028383	0.028863
Delay time (s)			0.000147	0.001271	0.001399
Maximum overshoot/undershoot (%)			0.01	0.01	0.01
Result	Pass	Pass	Pass	Pass	Pass

9 Appendix B: IEEE C37.118.1 Reference PMU Implementation Performance Testing Results

The following results are for the RTDS GTNET card PMU implementation, which is based on the IEEE C37.118 reference PMU algorithm. These are provided results for comparison with Appendix A, and have been generated using the same test environment. Note that several of the OOB tests fail the FE standard requirements.

	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
Frequency Range	0	0.000009	0.202	0.2047	0.2012
Voltage Magnitude	n/a	n/a	0.0005	0.0571	0.0575
Harmonic Distortion	0.003212	2.96857	0.0031	0.0644	0.0647
Measurement Bandwidth: Magnitude Modulation	0	0.000007	0.0059	0.0627	0.0602
Measurement Bandwidth Test: Phase Modulation	0.000053	0.020336	0.007	0.0606	0.0632
Frequency Ramp	0.00004	0.000017	0.1817	0.1886	0.1751
OOB	0.081203	n/a	0.5404	0.5339	0.541
Results as percentage of standard requirements:					
	FE	**RFE**	**TVE-Va**	**TVE-Vb**	**TVE-Vc**
Frequency Range	0.0%	0.0%	20.2%	20.5%	20.1%
Voltage Magnitude	n/a	n/a	0.1%	5.7%	5.8%
Harmonic Distortion	12.8%	n/a	0.3%	6.4%	6.5%
Measurement Bandwidth: Magnitude Modulation	0.0%	0.0%	0.2%	2.1%	2.0%
Measurement Bandwidth Test: Phase Modulation	0.0%	0.1%	0.2%	2.0%	2.1%
Frequency Ramp	0.4%	0.0%	18.2%	18.9%	17.5%
OOB	812.0%	n/a	41.6%	41.1%	41.6%

Table 8: M-class reference PMU performance (maximum error for each test)

Frequency Range Test					

Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
45	0	0.000007	0.1728	0.1728	0.174
45.5	0	0.000007	0.0937	0.0937	0.0937
46	0	0.000005	0.0809	0.081	0.081
46.5	0	0.000009	0.0843	0.0843	0.0843
47	0	0.000005	0.0905	0.0905	0.0904
47.5	0	0.000005	0.0948	0.0947	0.0953
48	0	0.000001	0.0973	0.0972	0.0973
48.5	0	0.000005	0.0958	0.0958	0.0957
49	0	0.000005	0.0899	0.0899	0.0898
49.5	0	0.000004	0.0798	0.0798	0.0798
50	0	0	0.0005	0.0571	0.0575
50.5	0	0.000004	0.0502	0.0502	0.0502

51	0	0.000004	0.0333	0.0333	0.0333
51.5	0	0.000006	0.0506	0.0506	0.0506
52	0	0.000004	0.0669	0.0669	0.0669
52.5	0	0.000004	0.0814	0.082	0.0816
53	0	0.000003	0.0953	0.0954	0.0953
53.5	0	0.000007	0.1069	0.1069	0.1069
54	0	0.000005	0.1197	0.1197	0.1195
54.5	0	0.000009	0.1457	0.1457	0.1457
55	0	0.000001	0.202	0.2047	0.2012
Result	Pass	Pass	Pass	Pass	Pass
Voltage Magnitude Test					

Voltage (pu)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)	TVE-V+ (%)	
0.8	0.0005	0.0571	0.0575	0	
0.9	0.0004	0.0571	0.0575	0	
1	0.0005	0.0571	0.0575	0	
1.1	0.0005	0.0571	0.0575	0	
1.2	0.0005	0.0571	0.0575	0	
Result	Pass	Pass	Pass	Pass	
Current Magnitude Test					

Current (pu)	TVE-Ia (%)	TVE-Ib (%)	TVE-Ic (%)	TVE-I+ (%)	
0.1	0	0	0	0	
0.2	0	0	0	0	
0.3	0	0	0	0	
0.4	0	0	0	0	
0.5	0	0	0	0	
0.6	0	0	0	0	
0.7	0	0	0	0	
0.8	0	0	0	0	
0.9	0	0	0	0	
1	0	0	0	0	
1.1	0	0	0	0	
1.2	0	0	0	0	
1.3	0	0	0	0	
1.4	0	0	0	0	
1.5	0	0	0	0	
1.6	0	0	0	0	
1.7	0	0	0	0	
1.8	0	0	0	0	
1.9	0	0	0	0	

2	0	0	0	0	
Result	Pass	Pass	Pass	Pass	
Harmonic Distortion Test					

Harmonic No.	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
2	0.003212	1.630787	0.0031	0.0644	0.0647
3	0	0	0.0008	0.0572	0.0574
4	0.003212	1.630694	0.0006	0.0527	0.053
5	0.00214	2.96857	0.0006	0.0528	0.0533
6	0	0	0.0003	0.0569	0.0577
7	0.00214	2.968518	0.0006	0.0611	0.0617
8	0.001144	1.744238	0.0003	0.0613	0.0615
9	0	0	0.0007	0.0574	0.0572
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Magnitude Modulation					

Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0	0.000007	0.0008	0.0573	0.0575
0.3	0	0.000006	0.0014	0.0579	0.0576
0.5	0	0.000005	0.0021	0.0584	0.0578
0.7	0	0.000004	0.0027	0.059	0.0579
0.9	0	0.000005	0.0033	0.0595	0.0581
1.1	0	0.000006	0.0039	0.0601	0.0584
1.3	0	0.000004	0.0044	0.0607	0.0587
1.5	0	0.000005	0.0049	0.0613	0.0591
1.7	0	0.000006	0.0053	0.0618	0.0595
1.9	0	0.000004	0.0057	0.0624	0.0599
2	0	0.000003	0.0059	0.0627	0.0602
Result	Pass	Pass	Pass	Pass	Pass
Measurement Bandwidth Test : Phase Modulation					

Modulation Frequency (Hz)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
0.1	0.000002	0.000007	0.007	0.0601	0.0605
0.3	0.000003	0.000072	0.007	0.0602	0.0606
0.5	0.000005	0.00032	0.0069	0.0603	0.0609
0.7	0.000008	0.000876	0.0068	0.0604	0.0612
0.9	0.000012	0.00186	0.0067	0.0605	0.0615
1.1	0.000017	0.003391	0.0065	0.0605	0.0618

1.3	0.000023	0.005596	0.0064	0.0606	0.0622
1.5	0.00003	0.008594	0.0063	0.0606	0.0625
1.7	0.000039	0.012514	0.0063	0.0606	0.0628
1.9	0.000048	0.017468	0.0063	0.0606	0.0631
2	0.000053	0.020336	0.0064	0.0606	0.0632
Result	Pass	Pass	Pass	Pass	Pass
Frequency Ramp Test					

Frequency Ramp(Hz/s)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
1	0.00004	0.000017	0.1618	0.162	0.1708
-1	0.00004	0.000015	0.1817	0.1886	0.1751
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Magnitude					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.029907	0.029635	0.029615
Delay time (s)			0.000081	0.000186	0.001112
Maximum overshoot/undershoot (%)			5.97	6.28	6.54
Result	Pass	Pass	Pass	Pass	Pass
Negative Step Response Test : Magnitude					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0	0	0.030759	0.030169	0.030173
Delay time (s)			0.000123	0.000441	0.000965
Maximum overshoot/undershoot (%)			5.97	6.48	6.24
Result	Pass	Pass	Pass	Pass	Pass
Positive Step Response Test : Phase					
--					
	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc
Response time (s)	0.176927	0.181842	0.072565	0.05207	0.052125
Delay time (s)			0.00063	0.001589	0.001221
Maximum overshoot/undershoot (%)			1.47	1.55	1.56
Result	Pass	Pass	Pass	Pass	Pass
Negative Step Response Test : Phase					

	FE	RFE	TVE-Va	TVE-Vb	TVE-Vc

Response time (s)	0.176927	0.181842	0.072674	0.06843	0.068193
Delay time (s)			0.00044	0.00136	0.001319
Maximum overshoot/undershoot (%)			1.46	1.49	1.49
Result	Pass	Pass	Pass	Pass	Pass
OOB Test					

Frequency Ramp(Hz/s)	FE (Hz)	RFE (Hz/s)	TVE-Va (%)	TVE-Vb (%)	TVE-Vc (%)
50.0Hz_24.9Hz	0.004326	0.682205	0.0246	0.0666	0.0687
50.0Hz_24.8Hz	0.003208	0.506995	0.0198	0.0623	0.0644
50.0Hz_24.6Hz	0.001213	0.19312	0.0113	0.0577	0.0598
50.0Hz_24.2Hz	0.001869	0.30252	0.0141	0.0683	0.0703
50.0Hz_23.4Hz	0.005245	0.874978	0.0232	0.0774	0.0794
50.0Hz_21.8Hz	0.00621	1.097725	0.0284	0.0725	0.0746
50.0Hz_18.6Hz	0.003941	0.775559	0.018	0.0639	0.066
50.0Hz_12.2Hz	0.004574	1.082112	0.0141	0.0674	0.0694
50.0Hz_10.0Hz	0.00124	0.307363	0.0125	0.0624	0.0644
50.0Hz_75.1Hz	0.004326	0.682206	0.0237	0.0778	0.0799
50.0Hz_75.2Hz	0.003208	0.507003	0.0193	0.0734	0.0755
50.0Hz_75.4Hz	0.001213	0.193118	0.0115	0.0656	0.0677
50.0Hz_75.8Hz	0.001869	0.302524	0.0126	0.0586	0.0607
50.0Hz_76.6Hz	0.005245	0.874976	0.025	0.0713	0.0734
50.0Hz_78.2Hz	0.00621	1.097723	0.0246	0.0765	0.0786
50.0Hz_81.4Hz	0.003941	0.775563	0.0195	0.0736	0.0757
50.0Hz_87.8Hz	0.004574	1.082109	0.0187	0.0729	0.075
50.0Hz_100.0Hz	0.002766	0.194919	0.0035	0.0493	0.0508
52.5Hz_27.4Hz	0.081203	12.763878	0.5264	0.5265	0.5297
52.5Hz_27.3Hz	0.076084	11.992418	0.5069	0.507	0.5077
52.5Hz_27.1Hz	0.066277	10.533021	0.466	0.4655	0.4669
52.5Hz_26.7Hz	0.049088	7.929525	0.3951	0.3959	0.3963
52.5Hz_25.9Hz	0.023495	3.91611	0.2933	0.2938	0.2942
52.5Hz_24.3Hz	0.001316	0.232986	0.2103	0.2089	0.2101
52.5Hz_21.1Hz	0.006321	1.243582	0.226	0.2263	0.2268
52.5Hz_14.7Hz	0.004215	0.997421	0.219	0.2192	0.2199
52.5Hz_10.0Hz	0.001312	0.346512	0.2097	0.2128	0.2122
52.5Hz_77.6Hz	0.005753	0.907457	0.224	0.2248	0.2275
52.5Hz_77.7Hz	0.005772	0.91195	0.2268	0.2262	0.2273
52.5Hz_77.9Hz	0.005753	0.916152	0.2265	0.2258	0.2269
52.5Hz_78.3Hz	0.005627	0.910382	0.2254	0.2246	0.2258
52.5Hz_79.1Hz	0.005219	0.870661	0.2231	0.2217	0.2232
52.5Hz_80.7Hz	0.00425	0.751379	0.219	0.2177	0.2187

52.5Hz_83.9Hz	0.000729	0.143538	0.2062	0.2053	0.2066
52.5Hz_90.3Hz	0.00201	0.475947	0.2087	0.2074	0.2087
52.5Hz_103.1Hz	0.005455	1.722921	0.2149	0.2136	0.2147
52.5Hz_105.0Hz	0.004131	1.349507	0.2105	0.2105	0.2041
47.5Hz_22.4Hz	0.005753	0.90746	0.239	0.2319	0.2392
47.5Hz_22.3Hz	0.005772	0.911952	0.239	0.2399	0.2391
47.5Hz_22.1Hz	0.005753	0.916153	0.239	0.2399	0.2389
47.5Hz_21.7Hz	0.005627	0.910381	0.2386	0.2395	0.2384
47.5Hz_20.9Hz	0.005219	0.870665	0.2375	0.2381	0.2369
47.5Hz_19.3Hz	0.00425	0.751373	0.2328	0.2336	0.2324
47.5Hz_16.1Hz	0.000729	0.14354	0.2228	0.224	0.2233
47.5Hz_10.0Hz	0.001163	0.269182	0.223	0.2259	0.2205
47.5Hz_72.6Hz	0.081203	12.763895	0.5404	0.5339	0.541
47.5Hz_72.7Hz	0.076084	11.992441	0.5181	0.5192	0.5185
47.5Hz_72.9Hz	0.066277	10.532994	0.4769	0.4787	0.4779
47.5Hz_73.3Hz	0.049088	7.929498	0.4066	0.4081	0.4076
47.5Hz_74.1Hz	0.023495	3.916123	0.3044	0.3059	0.3051
47.5Hz_75.7Hz	0.001316	0.23298	0.2224	0.2234	0.2226
47.5Hz_78.9Hz	0.006321	1.243586	0.2359	0.2371	0.2367
47.5Hz_85.3Hz	0.004215	0.997423	0.227	0.2286	0.2281
47.5Hz_95.0Hz	0.000908	0.268283	0.218	0.2181	0.2174
Result	Fail	Pass	Pass	Pass	Pass

10 References

[1] A. J. Roscoe, I. F. Abdulhadi, and G. M. Burt, “P and M Class Phasor Measurement Unit Algorithms Using Adaptive Cascaded Filters,” *IEEE Trans. Power Deliv.*, vol. 28, no. 3, pp. 1447–1459, Jul. 2013.

[2] A. J. Roscoe, T. Sklaschus, G. Oldroyd, S. M. Blair, and G. M. Burt, “Measurement of 40 power system harmonics in real-time on an economical ARM Cortex-M3 platform,” *Electron. Lett.*, vol. 49, no. 23, pp. 1475–1476, Nov. 2013.

[3] A. J. Roscoe and S. M. Blair, “Choice and properties of adaptive and tunable digital boxcar (moving average) filters for power systems and other signal processing applications,” in *2016 IEEE International Workshop on Applied Measurements for Power Systems (AMPS)*, 2016, pp. 1–6.

[4] S. M. Blair, “Beckhoff and TwinCAT 3 System Development Guide,” 2015. [Online]. Available: http://strathprints.strath.ac.uk/55254/1/Blair_2015_Beckhoff_and_TwinCAT_3_System_Development_Guide.pdf.

[5] D. R. Gurusinghe, D. Ouellette, and A. D. Rajapakse, “Development of a test platform for synchrophasor applications with real-time digital simulator,” in *2016 Electrical Engineering Conference (EECon)*, 2016, pp. 13–18.

[6] Synchrophasor Measurements for Power Systems Working Group, “C37.118.1a-2014 - IEEE Standard for Synchrophasor Measurements for Power Systems -- Amendment 1: Modification of Selected Performance Requirements,” 2014.

[7] IEEE Conformity Assessment Program, *IEEE synchrophasor measurement test suite specification -- Version 2*. .

[8] J. P. Braun and S. Siegenthaler, “The calibration of static and dynamic performances of PMUs,” in *17th International Congress of Metrology*, 2015, p. 12002.

[9] Beckhoff Automation GmbH & Co. KG, “EtherCAT: Highlights,” 2015. [Online]. Available: http://www.beckhoff.com/english.asp?ethercat/highlights.htm?id=20433492043386.

[10] IEEE, “1588-2008 IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.” 2008.

[11] Beckhoff Automation GmbH & Co. KG, “EtherCAT: Topology, Distributed Clock,” 2015. [Online]. Available: http://www.beckhoff.com/english.asp?ethercat/aufbau2.htm?id=20433492043359.

[12] G. Cena, I. Cibrario Bertolotti, S. Scanzio, A. Valenzano, and C. Zunino, “Synchronize Your Watches: Part II: Special-Purpose Solutions for Distributed Real-Time Control,” *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 27–39, Jun. 2013.

[13] Beckhoff Automation GmbH & Co. KG, “Internal and external EtherCAT synchronization,” 2015. [Online]. Available: https://infosys.beckhoff.com/english.php?content=../content/1033/ethercatsystem/html/bt_ethercat_dc_synchronization.htm&id=.

[14] A. J. Roscoe, “Frequency tracking, C37.118.1a compliant, P and M class PMU (Phasor Measurement Unit) algorithm examples for MATLAB Simulink,” May-2014. [Online]. Available: https://pure.strath.ac.uk/portal/en/publications/frequency-tracking-c371181a-compliant-p-and-m-class-pmu-phasor-measurement-unit-algorithm-examples-for-matlab-simulink(64ea57b3-78db-405d-9f09-23bbb6d3cd3a).html.

[15] A. J. Roscoe, S. M. Blair, and G. M. Burt, “Benchmarking and optimisation of Simulink code using Real-Time Workshop and Embedded Coder for inverter and microgrid

control applications," in *Universities Power Engineering Conference (UPEC)*, 2009, pp. 1–5.

[16] MathWorks, "Simulink Coder - Generate C and C++ code from Simulink and Stateflow models," 2012. [Online]. Available: http://www.mathworks.co.uk/products/simulink-coder/.

[17] M. J. Kiekebusch, N. Di Lieto, S. Sandrock, D. Popovic, and G. Chiozzi, "MathWorks Simulink and C++ integration with the new VLT PLC-based standard development platform for instrument control systems," in *SPIE Astronomical Telescopes + Instrumentation*, 2014, p. 91522B.

[18] IEC TC 57, "Communication networks and systems in substations Part 9-2: Specific Communication Service Mapping (SCSM) - Sampled values over ISO/IEC 8802-3 (IEC 61850-9-2:2011)." 2011.

[19] S. M. Blair, F. Coffele, C. D. Booth, and G. M. Burt, "An Open Platform for Rapid-Prototyping Protection and Control Schemes with IEC 61850," *IEEE Trans. Power Deliv.*, vol. 28, no. 2, pp. 1103–1110, 2013.

[20] S. M. Blair, "rapid61850," 2012. [Online]. Available: https://github.com/stevenblair/rapid61850.

[21] S. M. Blair, "tunnel61850," 2012. [Online]. Available: https://github.com/stevenblair/tunnel61850.

[22] G. Martins, D. Lacey, A. Moses, M. J. Rutherford, and K. P. Valavanis, "A case for I/O response benchmarking of microprocessors," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 3018–3023.

[23] S. M. Blair *et al.*, "Validating Secure and Reliable IP/MPLS Communications for Current Differential Protection," in *Developments in Power System Protection (DPSP)*, 2016.

[24] S. M. Blair, A. J. Roscoe, and J. Irvine, "Real-time compression of IEC 61869-9 sampled value data," in *2016 IEEE International Workshop on Applied Measurements for Power Systems (AMPS)*, 2016, pp. 1–6.

[25] S. M. Blair, "Real-time measurement of PMU reporting latency," 2017. [Online]. Available: https://doi.org/10.5281/zenodo.400934.

[26] P. Wall *et al.*, "Smart frequency control for the future GB power system," in *IEEE PES ISGT Europe*, 2016.