DC Fault Protection Algorithms of MMC HVDC Grids: Fault Analysis, Methodologies, Experimental Validations and Future Trends

Wang Xiang, *Member, IEEE*, Saizhao Yang, Grain Philip Adam, *Member, IEEE*, Haobo Zhang, Wenping Zuo, Jinyu Wen, *Member, IEEE*

***Abstract*- To protect the converters and minimize the power transmission interruption during DC line faults, it is necessary to detect the faults at ultra-high-speed for the MMC based HVDC grids. This paper reviews the state-of-the-art of DC fault protection methods of MMC HVDC grids, and summarizes the underlying principles of each method. On this basis, the DC fault characteristics analysis in terms of modal-domain, time-domain and frequency-domain are analyzed, which direct the protection design. Typical boundary protection and non-boundary protection schemes are reviewed. The advantages and disadvantages of existing fault protection methods are compared. A two-terminal MMC-HVDC prototype is developed to test the effectiveness of three fault protection methods. Comprehensive quantitative assessments of the protection methods discussed above are carried out in a four-terminal MMC HVDC grid. Finally, the future trends of the protection schemes are discussed and the findings are concluded.**

***Index Terms*- DC grid, DC fault, fault protection, HVDC transmission, modular multilevel converter, renewable energy.**

I. Introduction

With the increasing energy consumption and growing concerns on environmental degradation, renewable energy integration is receiving increased attention in decarbonizing the power sectors and slowing down the pace of climate change. Many countries set their goals to produce more renewable energy and reduce carbon emissions. In the *United Kingdom*, half of the UK's electricity will come from renewable sources by 2025. It also became the first major economy in the world to pass laws to end its contribution to global warming by 2050.

Due to the intermittent nature of renewable energy resources, they impose new technical challenges for integration into power systems. With the merits of self-commutation, decoupled active and reactive power control and black start capabilities, the modular multilevel converter (MMC) based DC grid technology is widely recognized as a suitable approach for long-distance power transmission [1]-[3]. To utilize the diversity of renewable energy resources across different regions, such as the North Sea in Europe, the inland areas in USA, China and India, the multi-terminal MMC HVDC grid is the most cost-effective solution. It allows massive integration of renewable energy sources and flexible infeed of local AC grids. In 2020, the world's first MMC HVDC grid project (*Zhangbei project*) is commissioned in *Beijing -Tianjin-Hebei* area of China, which transmits 4500 MW wind and solar power to the Beijing load center [4][5].

When the MMC HVDC grid is subject to short-circuit faults on the transmission lines, all the sub-module (SM) capacitors discharge rapidly, leading to a high fault current. Due to the low inertia of the DC networks, the DC fault propagation speed is much faster than the AC fault [6]. To protect the converters, double thyristor switches can be connected in parallel with the half-bridge sub-modules to isolate the fault lines by turning on the firing signals [7]. However, the fault clearance time is partially determined by the current decaying time. And the AC grid protection will be interrupted under some extreme cases. To interrupt the DC faults, various DC fault-tolerant MMC topologies have been proposed, which can be classified into DC fault blocking [8]-[12] and DC fault ride-through (without blocking) approaches [13]-[23]. For the blocking approach, references [16]-[19] proposed various improved SM topologies to block the DC fault current by switching off the power electronic devices. For the latter approach, references [20]-[22] utilized the cell topologies which can output negative voltage to ride through DC faults and maintain continuous operation during DC faults. However, these solutions are non-selective or partially selective [24], which will interrupt the power transmission of healthy parts. Thus, they are only suitable for point-to-point HVDC transmission.

To facilitate fully selective DC fault protection, the high voltage DC circuit breakers (DCCBs) should be applied to both ends of each protection zone to disconnect the faulty zone [25]. Thus, the impact of the fault condition is minimized and the healthy parts of the system continue transmitting power, which is similar to the traditional AC protection strategies. Due to the fast fault current rise rate in HVDC grids, the DCCBs are required to be tripped in a range of time shorter than 10ms [26] [27], leading to an ultra-fast requirement for DC fault protection algorithms. Taking the *Zhangbei project* as an example, the DC fault protection algorithms need to detect different faults within 2-3ms [28].

One of the major challenges in the practical operation of DCCBs is the dependence on ultra-high-speed protection algorithms. Local measurement-based algorithms are considered to accelerate the detection speed, such as the conventionally overcurrent, low-voltage, the rate of change of current or voltage algorithms. To guarantee high selectivity and

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reliability under different fault types, fault resistances and noise disturbance, many improved algorithms have been proposed. Aimed at investigating the most competitive and promising fault protection methods, this paper carries out the review of the state-of-the-art of DC fault protection algorithms for the MMC based HVDC grids, with a focus on their functions, technical advantages and disadvantages.

The outline of this paper is organized as shown in Fig. 1. In Section II, the technical requirements of the MMC HVDC protection are introduced, so as to provide a basis for performance evaluation of DC fault protection schemes. Sections III-V carry out the fault characteristic analysis of MMC HVDC grids in modal-domain, time-domain and frequency-domain, providing the theoretical foundation for the design of protection methodologies. Section VI summarizes the advantages and disadvantages of existing fault protection algorithms. And a comprehensive comparison is carried out for the mentioned schemes. The performance of three typical protection algorithms is validated by experimental tests and evaluated in a four-terminal MMC HVDC grid in Section VII and VIII, respectively. Section IX discusses the future trends of the HVDC grid protection schemes. Section X concludes the founding in this paper.

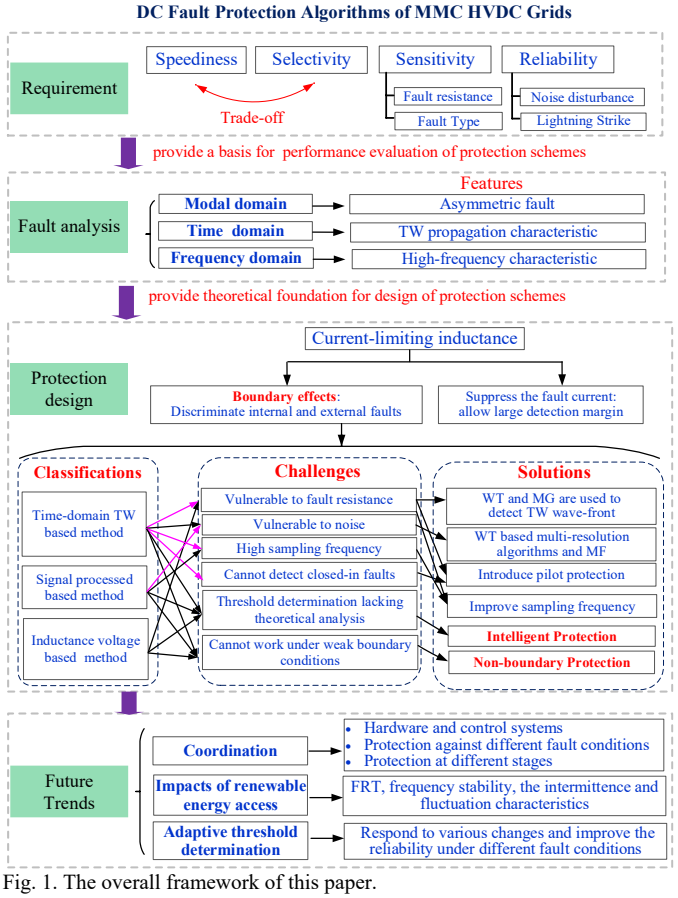


Fig. 1. The overall framework of this paper.

II. Specificity of Fault Protection Scheme for MMC Based HVDC Grid

A. Topology and Protection Configuration of a Typical MMC HVDC Grid

Fig. 2 shows the topology of a typical four-terminal meshed HVDC grid, where each converter employs the half-bridge sub-modules based MMC technology. The DC circuit breakers are installed on both ends of the transmission lines to protect the lines. In the meshed HVDC grid, multiple converters will feed current to the fault point during DC short circuit faults. Thus, large current limiting inductances are implemented at the terminals of each line.

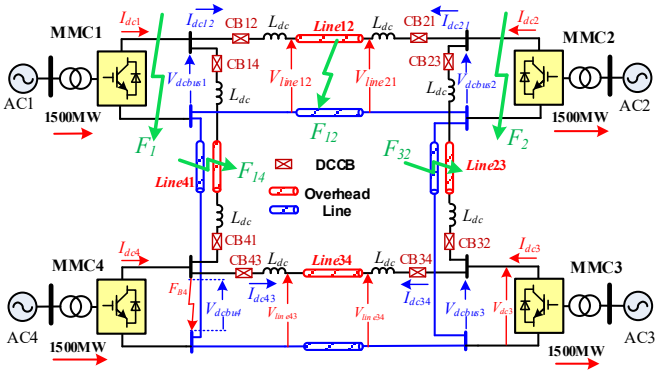


Fig. 2. The structure of a four-terminal MMC-based DC grid with DCCB.

For the meshed HVDC grid shown in Fig. 2, the protection zones can be configured as shown in Fig. 3, namely, the AC yard protection zone, the converter protection zone and the DC yard protection zone [29][30]. The DC transmission lines are exposed to air and the probability of faults is high. To prevent converters from overcurrent, a comprehensive DC line fault protection algorithm is required.

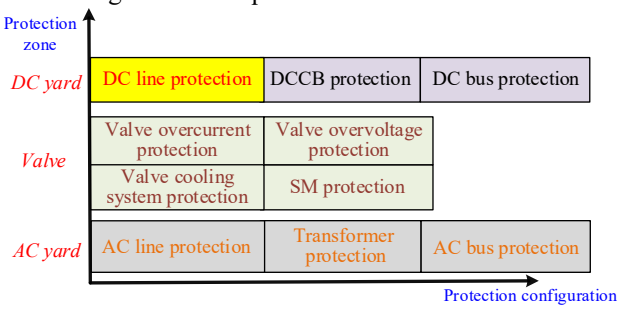


Fig. 3. The protection zones of meshed MMC HVDC grids.

B. Technical Requirements of DC Fault Protection Algorithm

1) Speediness

When a short-circuit fault occurs on the DC transmission line, multiple converters will feed fault current, leading to a high amplitude of fault current. To protect the semiconductors from overcurrent, the fault is desired to be detected and interrupted within several milliseconds. Taking the four-terminal *Zhangbei* HVDC grid project as an example, the fault protection time is less than 3ms while the total fault clearing time is less than 6ms [31].

As pointed out in [32][33], the speed of fault protection depends on used signals and the delay introduced by the measurement unit. Thus, single-end measurement is recommended to avoid communication delay. Also, the algorithms involved in the data processing should not be too complicated, otherwise, it will increase the calculation burden and delay of the hardware processor. A simple and feasible data processing algorithm should be selected to reduce the computation burden and time cost.

2) Selectivity

Selectivity implies that the protection relay should detect the

faults in its coverage zone of the HVDC system and do not operate out of its coverage zone. Taking protection CB12 shown in Fig. 2 as an example, F_{12} is an internal fault for CB12 while F_1, F_2, F_{14} and F_{32} are deemed as external faults for CB12. The selectivity of the DC line protection algorithm of CB12 means that CB12 should be tripped only during internal DC line faults (F_{12}) while do not respond to external faults (F_1, F_2, F_{14} and F_{32}).

To ensure selectivity, it is possible to increase the protection thresholds to avoid tripping during external faults. However, this will reduce the endurance to high-impedance faults. The pilot protection schemes are robust to high-impedance faults. but they need to receive information from the opposite station, which increases the protection time delay. Thus, they are often used as backup protection [34].

3) Sensitivity

The sensitivity requires the protection devices to accurately detect any internal faults, regardless of fault types and fault resistances [35], e.g., the pole-to-pole (PTP) and the pole-to-ground (PTG) faults. Considering the coupling of the faulted and healthy poles, some methods have been proposed to discriminate the faulted poles, e.g., the integration of the change of pole voltages [31], the zero-mode component based methods [36], the morphological gradient based methods [37].

To improve the robustness to high-impedance faults, signal processing algorithms such as wavelet transform (WT) [31], morphological gradient (MG) [38] can be used to detect the arrival of fault traveling waves or extract high-frequency components of voltage/ current for protection design.

The sampling frequency is another factor that affects sensitivity. The higher the sampling frequency, the richer the fault data information. Thus, for most fault protection algorithms, a higher sampling frequency results in higher sensitivity. With the development of analog-to-digital converters and digital signal processors, the sampling step of the current fault protection system can reach 2μs [39].

4) Reliability

Regarding the reliable operation of protection systems, there are two aspects: dependability and security [40][41]. The dependability indicates that the protection algorithm should operate correctly under internal faults. While the security requires that the protection algorithm should not operate falsely under external faults and unfaulty operating conditions.

The main factors affecting reliability are noise disturbance and lightning strikes. For the noise disturbance, the signal-noise-ratio (SNR) is conventionally used to describe the relationship between the original signal and the noise signal, which is defined as follows:

$$SNR = 10\lg\frac{P_s}{P_{noise}}(\text{db}) \tag{1}$$

where P_s and P_{noise} represent the original and noise signal power, respectively. For the lightning strike, the IEC standard recommends that the wave-front and half-peak time of the lightning current are 1.2μs/50μs for a standard lightning current waveform [42]. It will cause a large transient in voltage and current, leading to the malfunction of protection.

Both noise disturbance and lightning strikes are high-frequency signals [42], which possess few low-frequency components. Compared with transient voltage and current during internal and external faults, noise and lightning interference have obvious differences in the frequency spectrum. Thus, the difference in frequency-domain is often adopted to design a protective algorithm for preventing noise and lightning strike interference. For example, the criteria based on high-frequency spectrum differences are proposed in [43][44] to discriminate the lightning disturbance. For the noise disturbance, wavelet transform with a multi-resolution algorithm [45] or morphological filter (MF) [46] is adopted to weaken the impacts of noise. Considering that the average value of the noise is zero, the integral process is usually employed to mitigate the impacts of noise disturbance [47].

In summary, the technical requirements for the fault protection schemes of MMC HVDC grids are concluded in Table 1 as well as the technical difficulties and objectives [48][49].

Table 1. Summary of technical requirements of MMC HVDC grid protection.

	Technical requirements	Technical difficulties	Overall objectives
Speediness	Ultra-fast, e.g. 3ms in *Zhangbei* MMC HVDC meshed grid project.	Short time window, which is difficult to ensure selectivity.	1. Investigate fast single-end protection schemes 2. Ensure the ultra-fast detection speed while remaining selectivity to different fault conditions. 3. Reduce the signal transmission and processing delay and enhance the anti-interference ability. 4. Coordinate the main protection and backup protection to improve reliability.
Selectivity	Operate under all internal faults while do not operate under all external faults.	High sampling frequency.	
Sensitivity	1. Distinguish different fault types, e.g., pole-to-ground and pole-to-pole faults. 2. Endurance to high-impedance faults.	1. Effective faulted pole selection. 2. Endurance to high-resistance faults.	
Reliability	Reliable operation against noise disturbance, lightning strike and other unfaulty operating conditions.	Lightning and noise interference can easily cause malfunction of protection.	

III. DC Fault Characteristics Analysis in Modal-Domain

A. Equivalent Circuit in Modal-Domain

Fault current calculation can be conducted to theoretically analyze the inherent fault characteristics, thereby providing a theoretical basis for some protection schemes, e.g., overcurrent protection. In addition, it can also be adopted to determine the fault detection time, thereby avoiding overcurrent. The calculation of DC fault current under PTP fault is well studied in [50] and will not be repeated in this paper. Whereas, for the PTG faults, the interactions and unbalances between the negative and positive poles impose more challenges on the calculation of fault currents [51][52].

For the line *jk*, the simplified equivalent circuit of the positive and negative overhead lines in *s*-domain can be obtained in Fig. 4. Where the ground admittance and line capacitance of the overhead line are neglected [53]. L_{dc} is the current limiting inductance. R_{jk}, L_{jk} and M_{jk} are the line resistance, self-inductance and mutual inductance of the line *jk*,

respectively. Denote V_{jk_p}(s) (V_{jk_n}(s)) and V_{kj_p}(s) (V_{kj_n}(s)) as the positive (negative) pole voltage at node j and k. And I_{jk_p}(s) and I_{jk_n}(s) are the positive and negative line currents.

According to Fig. 4, the pole voltages and currents yield:

$$\begin{bmatrix} V_{jk\_p}(s) \\ V_{jk\_n}(s) \end{bmatrix} = \begin{bmatrix} s(2L_{dc}+L_{jk}) & sM_{jk} \\ sM_{jk} & s(2L_{dc}+L_{jk}) \end{bmatrix} \begin{bmatrix} I_{jk\_p}(s) \\ I_{jk\_n}(s) \end{bmatrix} + \begin{bmatrix} R_{jk} & 0 \\ 0 & R_{jk} \end{bmatrix} \begin{bmatrix} I_{jk\_p}(s) \\ I_{jk\_n}(s) \end{bmatrix} + \begin{bmatrix} V_{kj\_p}(s) \\ V_{kj\_n}(s) \end{bmatrix} \quad (2)$$

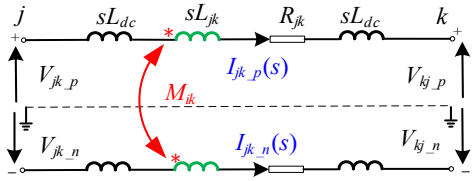
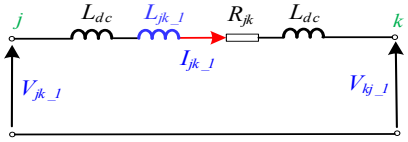


Fig. 4. Equivalent circuit of overhead line *jk* in s-domain.

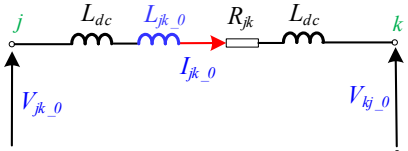
When a PTG fault occurs, it can be seen from equation (2) that there will be strong couplings between the pole voltages. Thus, to eliminate the couplings and reduce the analytical complexity, phase-modal transformation is commonly adopted, which can transform equation (2) into the following form [54]:

$$\begin{bmatrix} V_{jk\_1}(s) \\ V_{jk\_0}(s) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} V_{jk\_p}(s) \\ V_{jk\_n}(s) \end{bmatrix} = \begin{bmatrix} s(2L_{dc}+L_{jk\_1}) & 0 \\ 0 & s(2L_{dc}+L_{jk\_0}) \end{bmatrix} \begin{bmatrix} I_{jk\_1}(s) \\ I_{jk\_0}(s) \end{bmatrix} + \begin{bmatrix} R_{jk} & 0 \\ 0 & R_{jk} \end{bmatrix} \begin{bmatrix} I_{jk\_1}(s) \\ I_{jk\_0}(s) \end{bmatrix} + \begin{bmatrix} V_{kj\_1}(s) \\ V_{kj\_0}(s) \end{bmatrix} \quad (3)$$

where $V_{jk\_1}(s)$ and $V_{jk\_0}(s)$ are respectively the line-mode and zero-mode voltages of $V_{jk\_p}(s)$ and $V_{jk\_n}(s)$. $L_{jk\_1}=L_{jk}-M_{jk}$, $L_{jk\_0}=L_{jk}+M_{jk}$. Equation (3) demonstrates that the couplings between the positive and negative poles can be eliminated by the phase-modal transformation. And the line-mode and zero-mode equivalent circuits can be obtained:



(a) line-mode equivalent circuit



(b) zero-mode equivalent circuit

Fig. 5. Equivalent circuits of line *jk* in modal-domain.

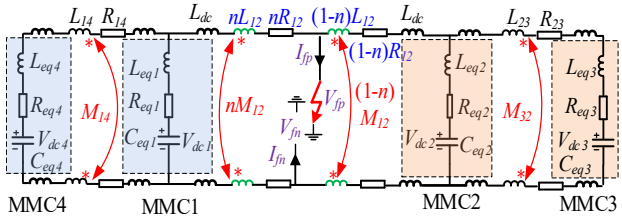
B. Fault Current Calculation under PTG Faults

As shown in Fig. 2, supposing a solid positive PTG fault happened at n% of line 12 ($0 \le n\% \le 1$). Considering that MMC3 and MMC4 are far away from the fault point, the fault current passing line 34 can be ignored [31]. Thus, the equivalent circuit of the four-terminal DC grid under a positive PTG fault can be obtained, as shown in Fig. 6(a). Where L_{eqi}, R_{eqi}, C_{eqi} respectively represent the equivalent inductance, equivalent resistance and equivalent capacitance of MMC i (i=1, 2, 3, 4). $I_{fp(n)}$ and $V_{fp(n)}$ are the positive (negative) pole current and the positive (negative) PTG voltage at the fault point, respectively.

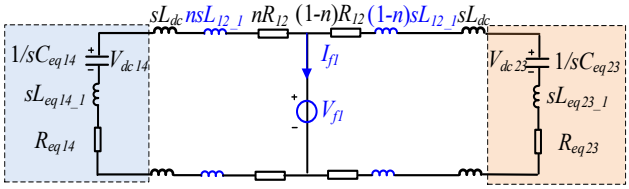
The line-mode equivalent circuit and the zero-mode equivalent circuit can be obtained, as shown in in Fig. 6 (b) and (c). Where $L_{eq14\_1(0)}=(L_{14\_1(0)}+L_{eq4}+2L_{dc})//L_{eq1}$, $C_{eq14}=C_{eq4}//C_{eq1}$ and $R_{eq14}=(R_{14}+R_{eq4})//R_{eq1}$. $I_{f1(0)}$ and $V_{f1(0)}$ are the line (zero)-mode current and line (zero)-mode voltage at the fault point, respectively. The fault boundary conditions under a positive PTG fault are V_{fp}=0, I_{fn}=0. Using phase-modal transformation, it yields:

$$\begin{cases} V_{f1}+V_{f0}=0 \\ I_{f1}=I_{f0} \end{cases} \quad (4)$$

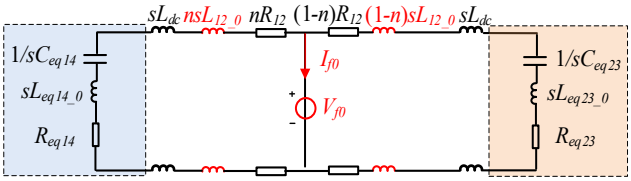
Equation (4) indicates that the line-mode fault equivalent circuit and the zero-mode equivalent circuit should be in series connection. Thus, a composite equivalent network in modal-domain can be obtained, as shown in Fig. 6 (d).



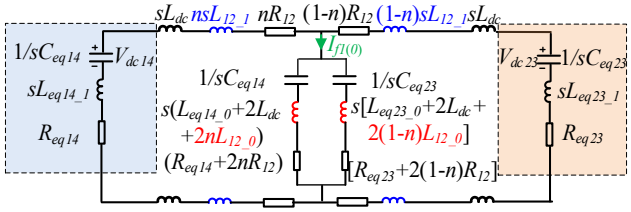
(a) equivalent circuit of four-terminal DC grid under a positive PTG fault



(b) line-mode equivalent circuit



(c) zero-mode equivalent circuit



(d) composite-mode equivalent circuit

Fig. 6. Equivalent circuits in modal-domain during a PTG fault.

From Fig. 6 (d), the fault current $I_{f1(0)}$ can be obtained:

$$I_{f1(0)} = \frac{V_{dc1}Z_{\Sigma 2}+V_{dc2}Z_{\Sigma 1}}{Z_{\Sigma 1}Z_{\Sigma 3}+Z_{\Sigma 1}Z_{\Sigma 2}+Z_{\Sigma 2}Z_{\Sigma 3}} \quad (5)$$

where $Z_{\Sigma 1}=R_{eq14}+2nR_{12}+1/(sC_{eq14})+s(2L_{dc}+L_{eq14\_1}+2nL_{12\_1})$, $Z_{\Sigma 2}=R_{eq23}+2(1-n)R_{12}+1/(sC_{eq23})+s[2L_{dc}+L_{eq23\_1}+2(1-n)L_{12\_1}]$, $Z_{\Sigma 4}=R_{eq14}+2nR_{12}+1/(sC_{eq14})+s(2L_{dc}+L_{eq14\_0}+2nL_{12\_0})$, $Z_{\Sigma 5}=R_{eq23}+2(1-n)R_{12}+1/(sC_{eq23})+s[2L_{dc}+L_{eq23\_0}+2(1-n)L_{12\_0}]$, $Z_{\Sigma 3}=Z_{\Sigma 4}||Z_{\Sigma 5}$.

Considering that $V_{dc14}(0^-)=V_{dc23}(0^-)=V_{dcn}$ (V_{dcn} is the rated DC voltage), the fault current in s-domain can be expressed as:

$$I_{fp}(s) = I_{f1} + I_{f0} = \frac{2V_{dcn}(Z_{\Sigma 2}+Z_{\Sigma 1})}{Z_{\Sigma 1}Z_{\Sigma 3} + Z_{\Sigma 1}Z_{\Sigma 2} + Z_{\Sigma 2}Z_{\Sigma 3}} \tag{6}$$

Equation (6) shows that the fault current is highly dependent on the fault distance. It is difficult to obtain a simplified expression of fault current for protection design. Thus, DC Fault characteristics analysis in other domains should be studied.

When a short-circuit fault occurs on the transmission line, the backward voltage traveling wave (TW) induced from the fault point will cause the rapid drop of DC line voltage and a drastic increase of DC line current. The time-domain together with the frequency- domain methods can be used to analyze the fault propagation characteristics and frequency information of TWs, thereby providing a theoretical basis for the DC grid protection design, which will be detailed in the following sections.

IV. DC Fault Characteristics Analysis in Time-Domain

A. Time-Domain Travelling Wave Analysis

Once a short-circuit fault occurs on the DC line, a negative voltage source is superimposed on the fault point and the voltage TW propagates towards both ends of the line. Fig. 7 shows the distributed parameter model of one pole of overhead lines, where r, L, g and C represent the resistance, inductance, conductance and capacitance of one unit segment of the overhead line. The wave impedance Z_C and propagation velocity v_p can be expressed as:

$$\begin{cases} Z_C = \sqrt{\dfrac{Z}{Y}} = \sqrt{\dfrac{r+j\omega L}{g+j\omega C}} \\ v_p = \dfrac{\omega}{\mathrm{Im}\sqrt{ZY}} = \dfrac{\omega}{\mathrm{Im}\sqrt{(r+j\omega L)(g+j\omega C)}} \end{cases} \tag{7}$$

In equation (7), Z and Y are the impedance and admittance of one segment of the overhead line, respectively.

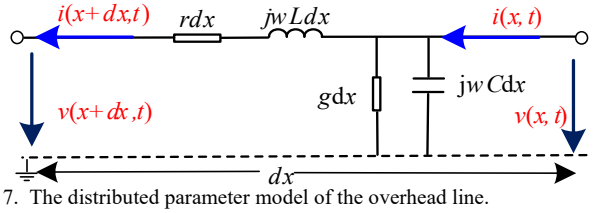
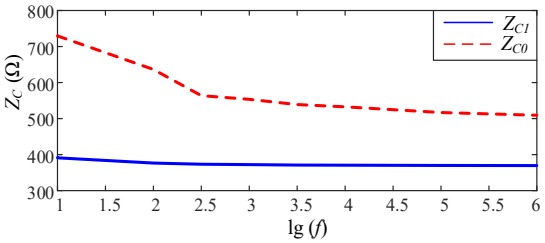


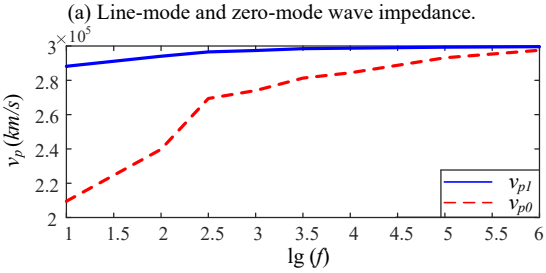
Fig. 7. The distributed parameter model of the overhead line.

For the positive and negative poles, applying the phase-modal transform to decouple the couplings between the poles. Using the overhead line parameters listed in [53], Fig. 8 depicts the frequency-magnitude characteristics of the line-mode and zero-mode wave impedances (Z_{C1} and Z_{C0}) and propagation velocity (v_{p1} and v_{p0}), respectively.

It can be seen from Fig. 8 that, compared with zero-mode wave impedances Z_{C0} and propagation velocity v_{p0}, the line-mode wave impedances Z_{C1} and propagation velocity v_{p1} are more stable, indicating that Z_{C1} and v_{p1} are less affected by the variation of frequency. Thus, Z_{C1} and v_{p1} are often adopted for fault protection design.



(a) Line-mode and zero-mode wave impedance.



(b) Line-mode and zero-mode TW propagation velocity.

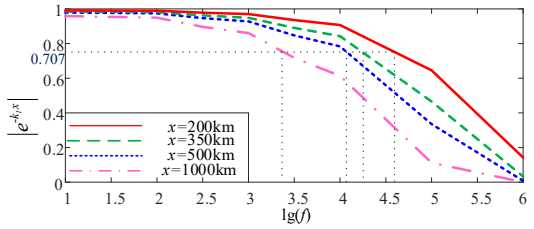
Fig. 8. Frequency-magnitude characteristics of wave impedance and propagation velocity.

Due to the attenuation effect of the transmission line, the magnitude of the fault TW will decrease when the fault TW propagates along the transmission line. The attenuation coefficient k can be expressed as:

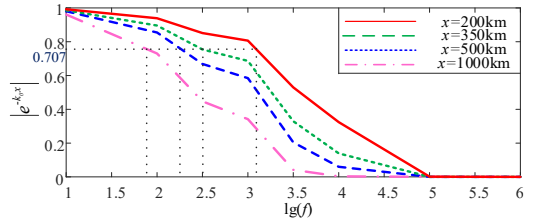
$$k = \mathrm{Re}\sqrt{(r+j\omega L)(g+j\omega C)} \tag{8}$$

Fig. 9 shows the attenuation factor $|e^{-k\,x}|$ of the TW versus different fault distances. From Fig. 9, it can be concluded that:

1) As the fault distance increases, the TW attenuation degree will be severe, and the corresponding cut-off frequency will decrease. 2) Under the same fault distance, the cut-off frequency of line-mode TW is larger than that of the zero-mode TW. 3) Under the same fault distance and frequency, the attenuation degree of zero-mode TW is more serious.



(a) line-mode attenuation factor.



(b) zero-mode attenuation factor.

Fig. 9. Attenuation characteristics of the line-mode and zero-mode TWs.

B. Characteristics of the Initial Traveling Wave

The length of the transmission line is denoted as l and the fault distance is x. Assuming that the direction from the MMC to the transmission line is positive. The initial voltage TW and current TW from the fault point are backward, denoting them as $V_{fb}(x, t)$ and $I_{fb}(x, t)$, respectively. Then, the measured backward voltage and current TWs ($V_b(x, t)$ and $I_b(x, t)$) at the terminal of the line can be expressed as:

$$\begin{cases} V_b(0,t) = V_{fb}(x,t)e^{-\gamma(x,t)x} \\ I_b(0,t) = I_{fb}(x,t)e^{-\gamma(x,t)x} \end{cases} \tag{9}$$

where $e^{-\gamma x}$ is the propagation coefficient of the TW, which is the main cause of TW distortion and dispersion [55]. Its expression in s-domain is [56]:

$$e^{-\gamma(s)x} \approx \frac{e^{-kx}}{(1+sT_a)} e^{-sx/v} \tag{10}$$

where $e^{-sx/v}$ is the phase shift factor, representing the propagation delay of the fault TW. T_a is the dispersion time constant, which represents the distortion effect of the transmission line on the TW. The farther the fault distance x, the larger the dispersion constant T_a.

Fig. 10 shows the waveform of the initial backward TW (V_b) detected at the terminal of the transmission line under different fault distances.

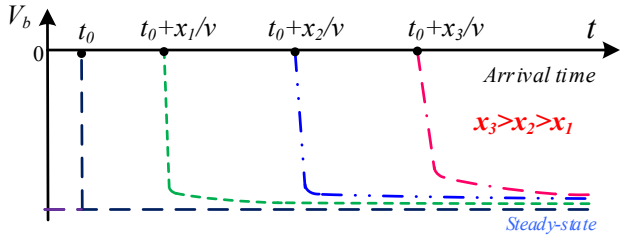


Fig. 10. Measured backward TW at the terminal of the transmission line versus different fault distances.

In Fig. 10, the arrival time t in x-axis represents the time when the initial TW arrives at the terminal of the transmission line. x_1-x_3 denote the different fault distances ($x_1 < x_2 < x_3$). It can be seen from Fig. 10 that, the farther the fault distance, the longer the propagation delay and the longer the time of TW V_b to reach steady-state.

C. Refraction and Reflection of Traveling Wave

As shown in Fig. 11, the fault TW induced from the fault point C propagates towards the terminals of the OHL and is reflected at the terminals (points A and B).

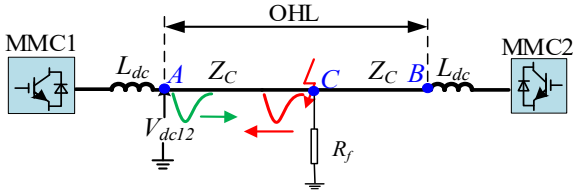


Fig. 11. Schematic diagram of traveling wave propagation.

Denote the first reflected wave at point A as V_r^1. It propagates towards the fault point and is reflected at point C, denoting as V_r^2. The reflection coefficient β_A at point A is:

$$\beta_A = \frac{Z_{T1} - Z_C}{Z_{T1} + Z_C} > 0 \tag{11}$$

where Z_{T1} is the equivalent impedance of the terminal close to MMC1.

The refraction coefficients α_C and β_C at point C are:

$$\begin{cases} \alpha_C = \dfrac{2Z_C // R_f}{Z_C + Z_C // R_f} = \dfrac{R_f}{R_f + Z_C/2} \\ \beta_C = \dfrac{Z_C // R_f - Z_C}{Z_C // R_f + Z_C} < 0 \end{cases} \tag{12}$$

where R_f is the fault resistance. As can be seen, when the fault resistance is small, $\alpha_C \approx 0$, indicating that the reflected TW at point A will not refract into the BC segment. Similarly, the reflected TW at point B will not refract into the AC segment, as shown in Fig. 12.

For the measured voltage V_{dc12} at point A, it contains multiple reflected waves from the fault point. The reflected waves V_r^2, V_r^4, V_r^6, …, V_r^{2n} from the fault point are:

$$\begin{cases} V_r^2 = \beta_A\beta_C V_{fb}, \quad V_r^4 = (\beta_A\beta_C)^2 V_{fb} \\ V_r^6 = (\beta_A\beta_C)^3 V_{fb}, \ldots, \quad V_r^{2n} = (\beta_A\beta_C)^n V_{fb} \end{cases} \tag{13}$$

Considering that the polarity of the initial TW V_{fb} is negative, the polarities of the reflected waves V_r^2, V_r^4, V_r^6, …, V_r^{2n} from the fault point are respectively positive, negative, positive, ... When the reflected waves V_r^2, V_r^4, V_r^6, …, V_r^{2n} arrive at point A, it will cause the increase or decrease of the DC line voltage, as illustrated in Fig. 13. The time interval that causes the change of the voltage V_{dc_line} is $\Delta T = 2x/v_p$.

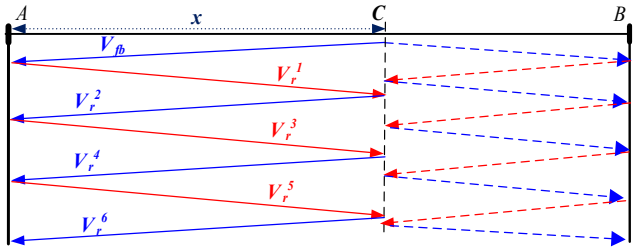


Fig. 12. Illustration of traveling wave reflection and refraction.

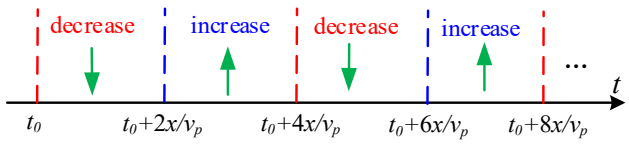


Fig. 13. Illustration of change tendency of measured voltage V_{dc_line}.

Based on the aforementioned analysis, the main frequency of the DC line voltage can be obtained as [57][58]:

$$f = \frac{1}{\Delta T} = \frac{v_p}{4x} \tag{14}$$

D. Characteristics of the Backward Traveling Wave

Fig. 14 shows two DC faults happening at the meshed grid. For the protection of line 12, F_{12} is an internal fault while F_{23} is an external fault.

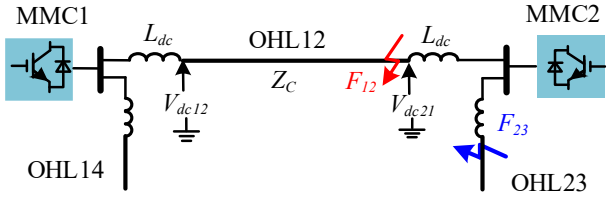


Fig. 14. Illustration of internal and external faults.

Based on the phase-modal transformation, the initial line-mode backward TW V_{fb1} superimposed on the fault point is [59] :

$$V_{fb1} = -\frac{2V_{dcn}Z_{C1}}{R_f + Z_{C1}} \tag{15}$$

For the internal faults (e.g. F_{12}), the initial line-mode backward TW (V_{b1}) measured at the terminal of line 12 is:

$$V_{b1}(F_{12}) = e^{-\gamma(s)l}V_{fb1} = -\frac{2V_{dcn}Z_{C1}e^{-kx}e^{-s/v}}{(R_f+Z_{C1})(1+sT_a)} \quad (16)$$

For the external faults (e.g. F_{23}), according to Peterson equivalent circuit shown in Fig. 15, the initial line-mode backward TW (V_{b1}) measured at the terminal of line 12 is:

$$\begin{cases} V_{b1}(F_{23}) = 2\Gamma_1\Gamma_2 e^{-\gamma(s)l}V_{fb1} \\ \Gamma_1 = \dfrac{s^2L_{eq2}C_{eq2}+sC_{eq2}R_{eq2}+1}{2(s^2L_{eq2}C_{eq2}+sC_{eq2}R_{eq2}+1)+sL_{dc}+Z_{C1}} \\ \Gamma_2 = \dfrac{Z_{C1}}{sL_{dc2}+Z_{C1}} \end{cases} \quad (17)$$

where Γ_1 is the high-frequency oscillation term and Γ_2 is the exponential decay term. Γ_2 exhibits that the sharp TW wave-front will be smoothed by the current limiting inductor.

Supposing PTP faults occur at the opposite terminal of line 12 (close to MMC2) and the terminal of line 23 (close to MMC2) at 2s, respectively. Using the parameters listed in Table 4 and Table 5. the initial line-mode backward TW (V_{b1}) measured at the terminal of line 12 is shown in Fig. 16.

As can be seen from Fig. 16, due to the smoothing effect provided by the current-limiting inductor, the wave-front of the backward TW is flattered under external faults. Thus, the rate of change of the amplitude of the backward TW can be used to distinguish internal and external faults.

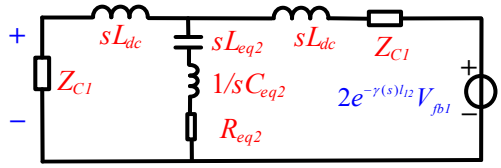


Fig. 15. Peterson equivalent circuit under an external fault F_{23}.

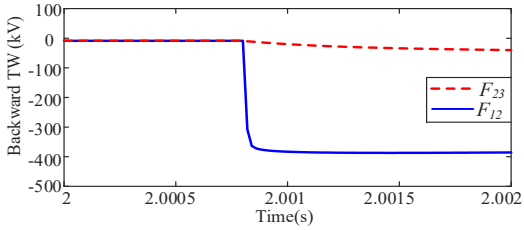


Fig. 16. Line-mode of initial backward voltage TW under an internal fault F_{12} and an external fault F_{23}.

V. DC Fault Characteristics Analysis in Frequency-Domain

A. Frequency Characteristics of Transient Voltage

As analyzed in Section IV.C, due to multiple refractions, the transient voltage possesses plentiful high-frequency components. As shown in Fig. 2, when a metallic PTP fault occurs at 25% of line 12, the FFT is performed on voltage V_{dc12}. The frequency spectrum of voltage V_{dc12} is shown in Fig. 17.

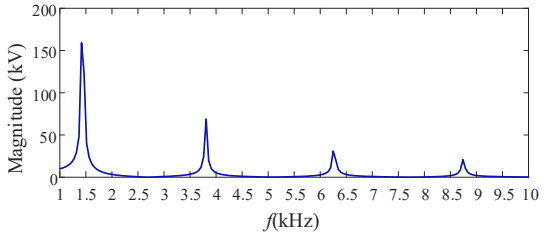


Fig. 17. Frequency spectrum of DC line voltage V_{dc12} under an internal fault.

As can be seen in Fig. 17, the main frequency in the transient voltage is around 1400 Hz, which complies with the analytical results in equation (14).

Neglecting the line capacitance, the equivalent fault circuit of the meshed DC grid is shown in Fig. 18 (a). Where Z_{jk_1} is the line-mode impedance of line jk. $Z_{jk\_1}=j\omega L_{jk\_1}+R_{jk}$.

Since MMC3 is far away from the fault point, the short-circuit current fed through line 34 is negligible [31]. Therefore, the equivalent circuit can be simplified as shown in Fig. 18 (b). The ratio between the DC line voltage V_{dc12} and the DC bus voltage V_{dc1} at MMC1 side in frequency-domain yields,

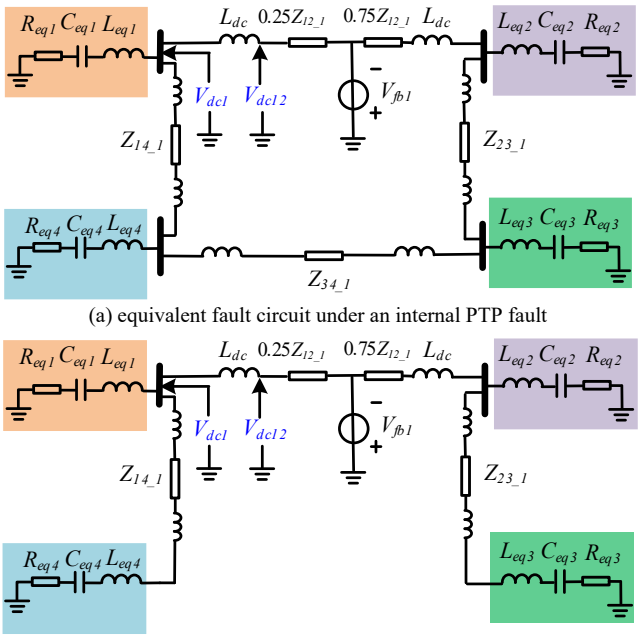


Fig. 18. Equivalent fault circuit of the HVDC grid under an internal PTP fault.

$$|H(j\omega)| = \left|\frac{V_{dc12}}{V_{dc1}}\right| = \left|\frac{2j\omega L_{dc}+Z_{eq1}//Z_{\Sigma}}{Z_{eq1}//Z_{\Sigma}}\right| \quad (18)$$

Z_{Σ} and Z_{MMC1} are:

$$\begin{cases} Z_{eq1(4)} = j(\omega L_{eq1(4)} - \dfrac{1}{\omega C_{eq1(4)}}) + R_{eq1(4)} \\ Z_{\Sigma} = Z_{eq4} + 4j\omega L_{dc} + 2Z_{L14\_1} \\ L_{eq1(4)} = \dfrac{2L_{arm1(4)}}{3};\ R_{eq1(4)} = \dfrac{2R_{arm1(4)}}{3};\ C_{eq1(4)} = \dfrac{6C_{arm1(4)}}{N} \end{cases} \quad (19)$$

where L_{armi}, R_{armi} and C_{armi} are the arm inductance, resistance and capacitance of MMC i (i=1,2,34) respectively. N is the number of sub-module per arm. According to equation (18), the frequency-amplitude characteristic of $|H(j\omega)|$ can be obtained

in Fig. 19.

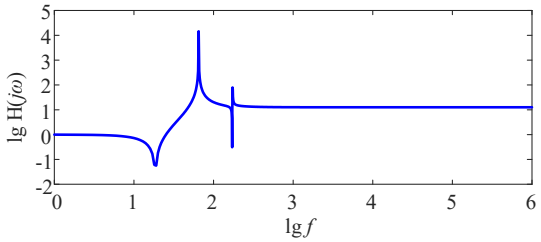


Fig. 19. Frequency-amplitude characteristics of $|H(j\omega)|$.

Fig. 19 shows that, due to the attenuation effect provided by the current-limiting inductor, the DC line voltage (V_{dc12}) possesses more high-frequency components (more 10kHz) compared to the DC bus voltage (V_{dc1}). Thus, the difference of high-frequency components in transient voltages can be used as an indicator to identify the internal and external faults.

B. Analysis of Current Frequency Characteristics

Based on the aforementioned analysis in Section III, when a metallic PTP fault occurs at n% of line 12 the fault equivalent network is depicted in Fig. 6 (b). The oscillation frequencies of currents i_{12} and i_{21} can be obtained:

$$\begin{cases} \omega_1 = \sqrt{\dfrac{1}{(L_{eq14\_1}+2L_{dc}+2nL_{12\_1})C_{eq14}} - \left(\dfrac{2nR_{12}+R_{eq14}}{L_{eq14\_1}+2L_{dc}+2nL_{12\_1}}\right)^2} \\ \omega_2 = \sqrt{\dfrac{1}{[L_{eq23\_1}+2L_{dc}+2(n\text{-}1)L_{12\_1}]C_{eq23}} - \left[\dfrac{2(n\text{-}1)R_{12}+R_{eq23}}{L_{eq23\_1}+2L_{dc}+2(n\text{-}1)L_{12\_1}}\right]^2} \end{cases} \quad (20)$$

Substituting the parameters listed in Table 4 and Table 5 into (20), the oscillation frequencies of the current can be obtained, which are within hundreds of hertz.

The differential current expression of protection CB12 is:

$$i_d = |i_{dc12} + i_{dc21}| \quad (21)$$

When internal faults occur, i_d is equal to the fault current. Its frequency is the superposition of oscillation frequencies ω_1 and ω_2. When external faults occur, the differential current i_d is equal to the current flowing through the line-to-ground capacitor. The line-to-ground capacitor current is proportional to the derivative of the line voltage. Thus, the frequency of the line-to-ground capacitor current is determined by the frequency of the voltage TW [58], which is above 10 kHz. Therefore, the high-frequency components of the differential current can also be used to identify the internal and external faults.

VI. DC Line Protection Schemes for MMC Based HVDC Grids

From the above fault characteristic analysis, it can be seen that the current limiting inductors act as a boundary element for fault protection. Therefore, most existing single-end protection schemes rely on the current-limiting inductors to design the fault protection criterion. Thus, in the following section, the impacts of current limiting inductors on fault protection algorithms are analyzed firstly. Then, the DC line protection algorithms depending on and independent of the current limit inductors will be reviewed.

A. Analysis of the Impact of Current Limiting Inductor on Fault Protection

To test the current limiting effect of different sizes of current limiting inductors, a solid PTP DC fault is applied at the terminal of line 12 (close to MMC1). The maximum arm currents of MMC1 versus different current limiting inductors are shown in Fig. 20. The rated arm current and submodule voltage of MMC 1 are 2.2kA and 4kV respectively. Thus, the 4.5kV/3kA press-pack IGBT developed by ABB is selected [60], of which the maximum allowable arm current is 6kA.

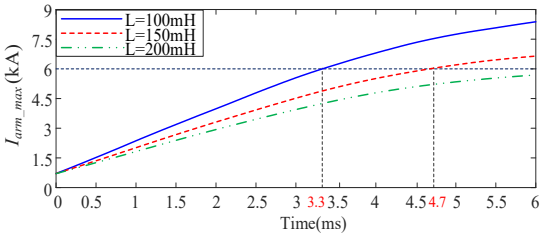


Fig. 20. Maximum arm currents of MMC1 versus different fault current limiting inductors.

Fig. 20 shows that a larger current limiting inductor has a stronger current limiting effect. As the fault distance increases, the TW propagation delay increases and the rise of arm current slows down. Supposing the operation time of DCCB is 3ms, the allowable fault detection time t_d can be obtained:

$$t_d\,(L_{dc} = 100\text{mH}) \le (3.3\text{-}3)ms + x/v_p \quad (22)$$

where x/v_p represents the TW propagation delay. Similarly, when the current-limiting inductors are 150mH and 200mH, the allowable fault detection times t_d are respectively:

$$\begin{cases} t_d\,(L_{dc} = 150\text{mH}) \le (4.7\text{-}3)ms + \dfrac{x}{v_p} \\ t_d\,(L_{dc} = 200\text{mH}) \le (6\text{-}3)ms + \dfrac{x}{v_p} \end{cases} \quad (23)$$

As can be seen from equations (22) and (23), a larger current-limiting inductance can suppress the fault current rise rate better, thereby allowing more detection time for fault identification and reducing the breaking capacity of DCCBs. However, the size of the current-limiting inductance is constrained by its cost C_L and weight M_L, which satisfy [61][62]

$$C_L, M_L \propto \sqrt{L_{dc}} \quad (24)$$

Taking the 5mH hollow inductor as an example, its weight is about 2.5 tons [63]. Therefore, there is a tradeoff between fault current limiting effect and manufacturing difficulty for the selection of current-limiting inductors.

B. Analysis of Boundary Characteristics

As a boundary element, the current-limiting inductors smooth the wave-head of traveling waves and attenuate the high-frequency components. Therefore, the amplitudes of the change rate of DC line voltage and the high-frequency components in transient voltage are much larger under internal faults than those under external faults. References [64] and [31] respectively proposed the protection algorithms based on the rate of change of DC line voltage (ROCOV) and the transient energy of DC line voltage (E_{WT}).

As shown in Fig. 2, taking CB12 as an example, the bus fault F_1 is a backward external fault while F_2 is a forward external fault. The backward external fault F_1 can be sorted out by the directional element easily. Thus, the most severe external fault is the solid PTP fault at DC bus 2 (F_2). Considering an internal fault with 300 Ω resistance happened at the end of line 12 (close to MMC2, F_{12}), the sensitivity coefficients k_{sen1} and k_{sen2} against different current-limiting inductors are compared, as shown in

Fig. 21. Where the sensitivity coefficients k_{sen1} and k_{sen2} are defined as:

$$\begin{cases} k_{sen1} = \dfrac{ROCOV(F_{12})}{ROCOV(F_2)} \\ k_{sne2} = \dfrac{E_{WT}(F_{12})}{E_{WT}(F_2)} \end{cases} \tag{25}$$

where $ROCOV$ (F_2) and $ROCOV$ (F_{12}) respectively represent the measured ROCOV under the external fault F_2 and the internal fault F_{12}. $E_{WT}(F_2)$ and $E_{WT}(F_{12})$ respectively represent the measured transient energy under faults F_2 and F_{12}.

From Fig. 21, it can be concluded that,

(1) With the increase of current-limiting inductances, the sensitivity coefficient increases. When the current-limiting inductor is selected as 50mH, both k_{sen1} and k_{sen2} are less than 1, indicating that the external and internal fault cannot be correctly detected. Therefore, protection schemes based on boundary elements rely on large current-limiting inductors to ensure selectivity.

(2) Under the same current-limiting inductance, k_{sen1} is smaller than k_{sen2}, indicating that the protection algorithm based on transient energy is more reliable than that based on ROCOV.

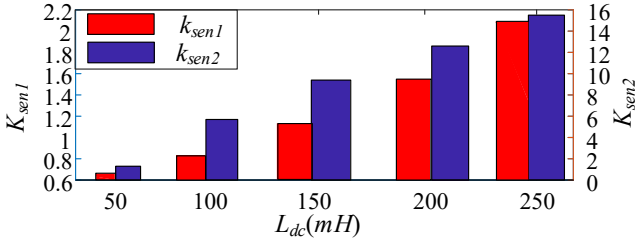


Fig. 21. Sensitivity coefficients versus different current limiting inductors.

C. Single-end Protection Schemes Relying on Boundary Elements

Regarding the classification of single-end boundary protection, it can be divided into two categories, i.e., the phase-domain and the frequency-domain based methods) [65] or three categories based on the fault protection principle. Since phase-domain and modal-domain based methods have been investigated and reviewed in [65], the latter classification is adopted to evaluate different fault protection schemes. Considering that most fault protection algorithms are applicable to both cable and overhead line based systems, the following reviewed publications contain the protection schemes for both cable and overhead line applications.

1) Time-domain TW based protection scheme

Traveling wave protection is widely used in traditional AC power systems and LCC-HVDC systems, which has a simple principle and can be easily implemented. For instance, *Siemens* proposed the TW protection scheme based on the DC voltage derivative (dV/dt), the change of DC line voltage (ΔV) and the DC current derivative (dI/dt) [66]. For the MMC HVDC systems, references [67]-[69] proposed ultra-fast TW protection schemes based on the rate of change of DC voltage (ROCOV) and the rate of change of DC current (ROCOC) respectively. A comprehensive protection scheme that contains the low-voltage criterion, the DC voltage derivative criterion and the directional overcurrent criterion is proposed in [70]. In [71], the line-mode backward voltage TW is adopted to identify the internal DC faults. When the amplitude of the line-mode backward voltage TW exceeds the threshold, it is deemed to be an internal fault. These methods have the merits of fast detection speed and no dead protection zone. However, these methods suffer from poor performances under high resistance faults and noise disturbance.

To improve reliability, reference [72] proposed a TW protection scheme with adaptive protective thresholds. The propagation characteristics of the initial zero-mode TW is analyzed to estimate the fault distance and the fault resistance, thereby adaptively adjusting the threshold to improve the endurance to fault resistances. In [73], the first peak time of the line-mode voltage TW is adopted to identify the internal and external faults. In [74], considering that distortion of the fault TW wave-front depends on the fault distance, a protection scheme using the zero-mode current waveform correlation is adopted to detect internal and external faults. References [75][76] calculated the parameters that can present the fault distance by fitting the zero-mode current TW, so as to achieve the identification of internal faults. In [77], the time interval between the sudden change point and the first peak point of the initial TW is adopted to identify internal faults. These aforementioned schemes improved the performance of endurance to large fault resistance (300Ω). However, these schemes are easily affected by noise disturbance and high sampling frequencies (100kHz or 200kHz) are required. Due to the absence of zero-mode components, the methods in [72][74] -[76] cannot identify internal PTP faults. In addition, these protection schemes cannot work well under close-in faults. To detect close-in faults, distributed sensors are adopted in [78] to protect the entire transmission line.

Based on the above literature review, for the TW protection schemes based on the voltage/current derivative, a smaller sampling frequency is required and there is no dead protection zone. But they are vulnerable to high fault resistances and noise disturbance. The protection schemes based on waveform correlation calculation or TW propagation characteristic analysis can improve the performance under high-impedance faults, but higher sampling frequency is required and they are unable to detect close-in faults.

2) Frequency- domain signal processing based protection schemes

Wavelet transform (WT) has the merits of time-frequency localization and multi-scale decomposition ability [79], which has been widely used to extract high-frequency components of signals or detect the wave-front of the initial TW. References [31][80][81] used WT to extract the high-frequency components of the DC line voltage, so as to take advantage of the boundary effect provided by the current-limiting inductor to discriminate internal and external faults. While references [82][83] used the wavelet transform modulus maxima (WTMM) to detect the arrival of the voltage TWs in the high-frequency spectrum. These protection schemes can tolerate high-impedance faults and protect the whole line. But they are easily affected by noise disturbance.

To improve the endurance to noise disturbance, the WTMM with multi-resolution algorithms are adopted to detect the line-mode TW in [38][84]. However, the multi-scale decomposition of WT requires the sampling frequency as high as 1MHz, which is difficult to be implemented in practical

applications. Reference [85] adopted the morphological gradient (MG) to detect the initial TW wave-front and the morphological filtering (MF) to resist noise disturbance. But MG also brings about a high computation burden and sampling frequency.

To be concluded, the protection schemes based on WT and MG are robust to large fault resistances and fault types. In addition, WT based on multi-resolution algorithms and MF can be adopted to improve the endurance to noise disturbance. However, they also suffer from the problems of the high sampling frequency, computation burden and difficulty in selecting the mother wavelet.

3) Current-limiting inductor voltage based protection schemes

In addition to the boundary element of the current-limiting inductor, the voltage across the inductor can also be used as indicators for fault protection [86]. Reference [87] proposed a protection scheme based on the rate of change of the current-limiting inductor voltage. The change-rate of inductor voltage is the second derivative of the line current. Compared with the protection scheme based on the change rate of current, this method is robust to large fault resistances. However, this scheme cannot identify PTG faults. In order to improve the applicability for different fault types, reference [88] used the inductor voltage differences between negative and positive poles to discriminate faulted poles. Nevertheless, similar to the current change-rate based schemes, this scheme also fails to detect high-impedance faults. In [53], based on the modal domain analysis, the line-mode inductor voltage is adopted for fault identification while the zero-mode inductor voltage is adopted for faulted pole selection. The maximum detectable resistance is 200Ω, which needs to be further improved. Besides, the above protection schemes are robust to noise disturbance.

In summary, compared with time-domain TW schemes, the inductor voltage based methods improve the robustness to noise disturbance, and there are no dead protection zones. Compared with the protection schemes based on WT and MG, the inductor voltage based methods have the advantages of low computation burden and low sampling frequency. However, the performances under high-impedance faults need to be improved.

D. Protection Schemes Independent of Boundary Elements

As pointed out in [31], for boundary protection schemes, large CLRs (over 100mH) are adopted to enable high selectivity and reliability. In addition, various simulation results also demonstrate that 200mH or larger CLRs are required to guarantee the robustness to large fault resistance and noise disturbance. However, there are several scenarios where the configured current-limiting inductors are small and cannot provide strong boundary conditions for fault protection algorithms.

(1) DC cable-based HVDC transmission system. The cable-based transmission system has a low probability of faults and most faults are permanent. Once a fault occurs, the converters will be blocked and there is no need to implement a large current limiting inductor for fault current limiting. Taking the INELFE MMC-HVDC project as an example, the current limiting inductor of the system is only 50mH [89].

(2) Fault tolerable converter based HVDC transmission systems. The fault tolerable converters, e.g., the full-bridge MMC, the hybrid MMC, can suppress the fault current via fault current limit control [90]. The *Kunliulong* three-terminal HVDC project constructed by hybrid MMC will use a current limiting reactor of 100mH for fault current limiting [91].

(3) Medium/low voltage and small capacity transmission systems. In MVDC distribution systems, the current limiting inductors are conventionally in the range of 20mH [92].

To realize reliable fault protection under weak boundary conditions, single-end protection schemes independent of boundary conditions need to be proposed. Reference [93] used the arrival time difference between line-mode and zero-mode TW to realize non-boundary protection. This scheme is robust to high-resistance faults. However, it cannot identify remote faults and PTP faults. To improve the applicability for different fault types, TW frequency characteristics which are dependent on the fault distance are adopted to identify the internal faults in [94]. The proposed method is affected by the noise and a high sampling frequency is required. These non-boundary protection schemes cannot work well for remote faults. Reference [36] introduced the distortion effects of the line-mode backward TWs to identify faults independent of boundary components. Except for [36][93][94], there are no other references concerning single-end protection schemes that independent of boundary elements for the MMC HVDC systems.

E. Intelligent Algorithm Based Protection Schemes

With the development of artificial intelligence, intelligent algorithms are gradually applied in HVDC protection. The protection schemes based on intelligent algorithms avoid the complex threshold determination process and have good performances on the speediness and selectivity.

Reference [95] used four neural networks to detect the faults, whose training workload is large and complicated. Reference [96] realizes the faulted types selection by comparing the differences in the frequency spectrum. Compared with [95], this scheme used three neural networks to sequentially implement the functions of fault identification, fault classification and fault location. The workload is reduced, but it is still very complicated. Reference [97] used the wavelet transform and fuzzy *C*-means algorithm to extract fault features. But this method did not consider the impact of fault resistances and noise disturbance. Reference [98] proposed a protection scheme based on the fuzzy control algorithm, which used a multi-layer wavelet transform to extract fault features and implemented the fault recognition function through training weights. However, the maximum detectable fault resistance is only 50Ω. Reference [99] proposed a machine learning-based protection scheme. But this method needed to install a large number of current sensors along the line, which will increase the investment cost.

Compared with the non-intelligent protection algorithm, intelligent protection methods avoid the complicated tuning and calculation process. However, it is still at the preliminary stage of research. The application in practical engineering needs to be investigated.

In summary, from the above literature review, the performances of typical boundary and intelligent protection schemes for MMC HVDC grids have been concluded in Table

2. Where '√' indicates that the method can detect both PTG and PTP fault with tolerating fault resistance larger than 300Ω, at least 20db noise disturbance. '×' indicates that the method cannot meet the technical requirements. '/' indicates that the technical requirements are not discussed in the literature.

As can be seen in Table 2, the existing boundary protection schemes suffer from some of the following problems: 1) vulnerable to fault resistances; 2) easily affected by noise disturbance; 3) cannot identify different fault types; 4) cannot work well for close-in faults. To overcome the aforementioned shortcomings, WT and MG can be adopted to detect the TW wave-front to improve the robustness to fault resistance. More importantly, a higher sampling frequency (100kHz or 200kHz) is recommended. For the close-in faults, the pilot protection can be adopted as back-up protection [100]-[104]. Regarding the robustness to noise disturbance, the WT based on multi-resolution algorithms and MF can be adopted to improve the endurance to noise disturbance. As for different fault types, it is recommended that the line-mode components are adopted for fault identification while the zero-mode components are adopted for faulted pole selection.

Table 2 The Performance evaluation of typical protection methods under different protection classifications

Performance	TW based protection scheme in time-domain					Intelligent algorithm based protection schemes				
	[64][67][68][69]	[70]	[72] [74][75][76]	[77]	[78]	[99]	[98]	[95]	[96]	[97]
Fault resistance (Ω)	Weak		√				50	50	69	10
Fault types	√		×	√		√				
Noise endurance (dB)	×		weak	×		√				
Sampling frequency (kHz)	96 in [68]	100	200	100	100	5	/			
Advantages	fast speed, simple principle		/			/				
Other disadvantages	/		Need supplementary protection to detect close-in faults		More sensors employed	Need many sensors	Applicable only in two-terminal systems	Need multiple ANNs		Difficult to extract fault features
Operability	Medium	Low				Low				

Performance	Signal processing based protection schemes						Current-limiting inductor voltage based protection schemes		
	[80] [81]	[82][83]	[31]	[38]	[84]	[85]	[87]	[88]	[53]
Fault resistance (Ω)	√					200	√	Weak	200
Fault types	√						×	√	
Noise endurance(dB)	Weak			√			√		
Sampling frequency (kHz)	10	25	20	20	1000	20	200	5	20
Advantages	/						fast speed, simple principle		
Other disadvantages	Some need high sampling frequency and computation burden						More voltage sensors		
Operability	Low						Low	High	

VII. Experimental Validations

As mentioned above, the solid bus fault at the opposite terminal is regarded as the most severe external fault. Thus, a prototype of a two-terminal MMC HVDC system can be adopted to verify the selectivity of the DC line protection schemes, as shown in Fig. 22.

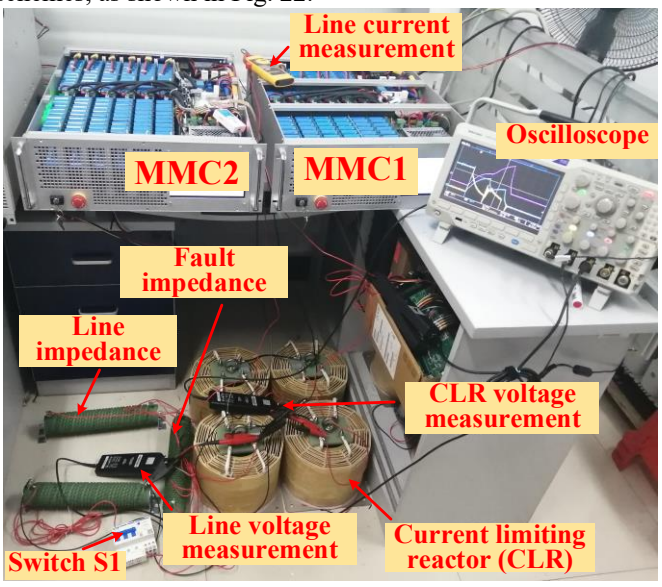


Fig. 22. The prototype of a two-terminal MMC-HVDC system.

The electrical circuit and the parameters of the test system are shown in Fig. 23 and Table 3, respectively. In Fig. 23, F_{12} represents the internal fault and R_f is the fault resistance. F_2 represents the DC bus fault on the MMC2 side.

Three typical boundary protection schemes as presented in Section VI.C will be studied, namely, the time-domain TW based protection as reported in [64] (denoted as *ROCOV* protection), the signal processing based protection using MG as reported in [38] (denoted as *MGV* protection) and the inductor voltage based protection as reported in [88] (denoted as V_L protection).

Considering that the fault impedance is usually small in low voltage DC systems, a 10Ω fault impedance is applied at the end of the transmission line (F_{12}) to test the selectivity of these protection schemes under internal faults. The measured DC line voltage V_{dc12}, the DC line current I_{dc12}, and the voltage across the current-limiting reactor V_L are shown in Fig. 24.

As can be seen in Fig. 24, under the internal fault, the DC line voltage V_{dc12} drops rapidly from the rated voltage (400V). Meanwhile, the DC line current I_{dc12} rises rapidly, leading to the fast increase of the current-limiting reactor voltage V_L.

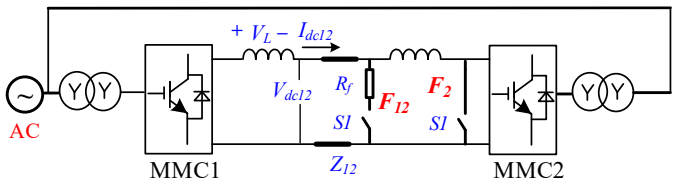


Fig. 23. The electrical circuit of the test system.

Table 3. Parameters of the test system

Parameter	Value
The rated power	2500VA
AC voltage	380V
The ratio of the AC transformer	380/220
DC voltage	400V
Arm inductance of MMC	10mH
Sub-module capacitance of MMC	6600μF
Sub-module number per arm	20
Current-limiting reactor (CLR)	30mH
Line impedance Z_{12}	0.5Ω
Fault impedance R_f	10Ω

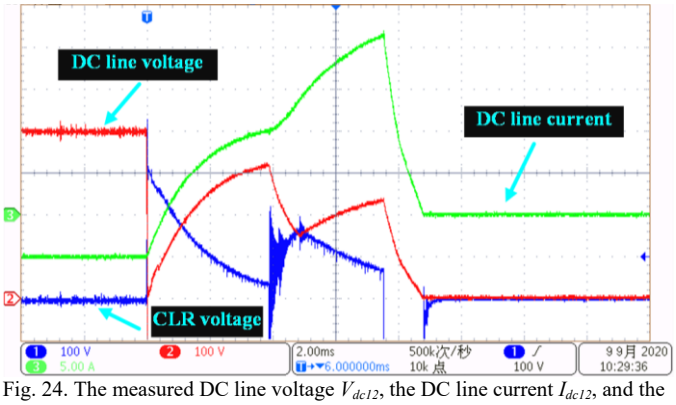


Fig. 24. The measured DC line voltage V_{dc12}, the DC line current I_{dc12}, and the current-limiting reactor voltage V_L under an internal fault F_{12}.

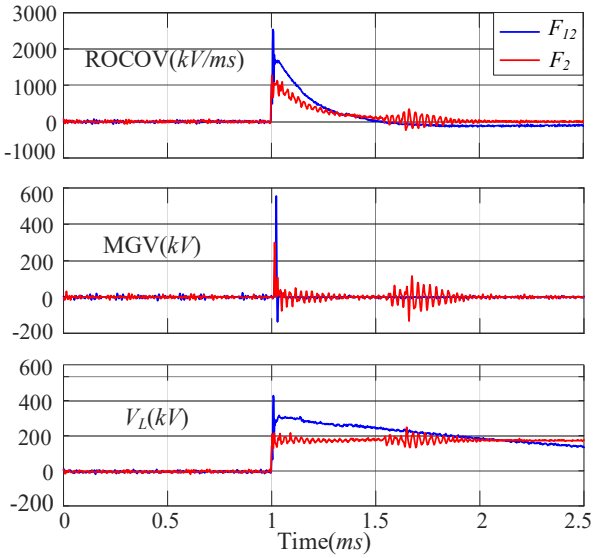


Fig. 25. The comparison results between internal and external faults.

To test the effectiveness of these methods, an external solid fault F_2 is applied at the DC bus of MMC2 to make a comparison between the internal and external faults. The comparison results are shown in Fig. 25.

As can be seen, due to the boundary effects provided by the CLR, the DC line voltage under the internal fault drops rapidly. Thus, the ROCOV and MGV under internal faults are greater than those under external faults. In addition, the fault current rises faster. Thus, the V_L under internal faults is greater than that under external faults. To be concluded, experiment results show that the aforementioned protection schemes can identify the internal faults and external faults selectively and quickly.

VIII. Simulation Comparison of Typical DC Fault Protection Schemes

To further evaluate the performance of the three fault protection schemes against different fault types, fault resistances and noise disturbance, the four-terminal MMC HVDC grid shown in Fig. 2 is built in PSCAD/EMTDC. In the HVDC grid, the MMC1 controls the DC voltage of the DC grid, while the other converters control the active and reactive power. Assuming that the power flowing into the DC grid is the positive direction, the active power transmitted by MMC2~MMC4 is -1.0 *pu*, -1.0 *pu* and 1.0 *pu* respectively. The current-limiting inductor installed on the transmission line is 0.1H and the sampling frequency is 25kHz. The lengths of the lines OHL12, OHL14, OHL32 and OHL43 are 240km, 120km, 100km and 200km respectively. The other system parameters are listed in Table 4 and Table 5.

Table 4. Parameters of the test system

	DC voltage/kV	AC voltage/kV	power/MW
MMC1	±400	380	1500
MMC2	±400	380	1500
MMC3	±400	380	1500
MMC4	±400	380	1500

Table 5. Parameters of each converter

	L_{arm}/mH	C_{arm}/mF	V_{sm}/kV	N
MMC1	40	7.5	4	200
MMC2	40	7.5	4	200
MMC3	40	7.5	4	200
MMC4	4	7.5	4	200

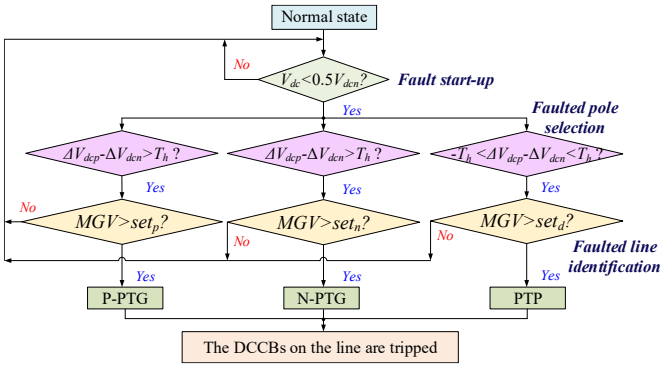


Fig. 26. Flow chart of the protection scheme of MGV.

To make a fair comparison, the differences of the DC voltage change rate between the positive and negative poles (ΔV_{dcp} -ΔV_{dcn}) are adopted to select the faulted pole for the three protection schemes. To improve the sensitivity under different fault types, the internal fault identification criteria are conducted after the faulted pole selection. Taking the *MGV* protection [38] as an example, the flow chart of the protection scheme is presented in Fig. 26. It contains the fault start-up element, the faulted pole selection criterion and the internal fault detection criterion.

A. The Threshold Determination

For the fault start-up element, its purpose is to distinguish the normal and fault states. Thus, the designed threshold can leave a relatively large margin, e.g. 0.5V_{dcn} in Fig. 26. The faulted pole selection criteria are the same for the three aforementioned protection schemes. For the faulted pole selection, the threshold determination can refer to [31]. For the internal fault identification, taking relay CB12 as an example, the threshold determination process is presented as follows.

According to the analysis in Section VI.B, the solid bus fault F_2 is the most severe external fault. Considering the impact of noise disturbance, the solid bus fault F_2 with 20dB noise is regarded as the worst external case to calculate the thresholds.

Applying a solid PTP fault at bus 2 and adding 20dB noise into the measured signals, the values *ROCOV* (F_2, 0.01Ω, 20dB), *MGV* (F_2, 0.01Ω, 20dB), V_L (F_2, 0.01Ω, 20dB) are 1085*kV/ms*, 365 kV and 258 kV respectively.

When the reliability coefficient is selected as 1.3 [105], the thresholds can be calculated as 1410*kV/ms*, 478kV and 335kV respectively, as listed in Table 6.

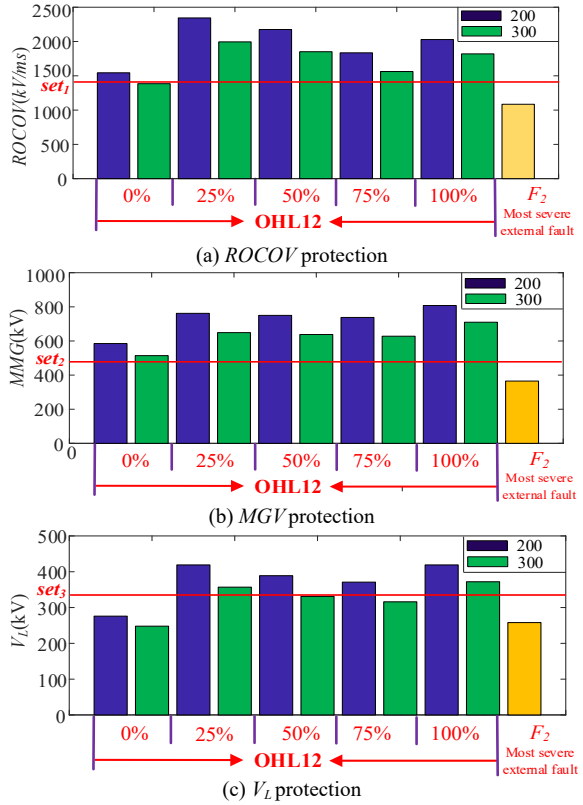
Table 6. Threshold determination of the three protection schemes

Protection	worst external case	reliability coefficient	measured values	thresholds
ROCOV	F_2, 0.01Ω, 20dB	1.3	1085*kV/ms*	Set_1: 1410*kV/ms*
MGV			365 kV	Set_2: 478kV
V_L			258 kV	Set_3: 335kV

B. Response to Fault Resistances

Applying internal PTP faults with different fault resistances (200Ω and 300Ω) at F_{12} and a solid external PTP fault at F_2, the values of *ROCOV*, *MGV* and V_L are measured, as shown in Fig. 27, where "*x*%" means the internal fault F_{12} is applied at the *x*% of the OHL 12.

As can be seen in Fig. 27, with the increase of fault resistance, the amplitudes of the measured *ROCOV*, *MGV* and V_L decrease. When the fault resistance exceeds 200Ω, the V_L based protection cannot identify the internal and external faults correctly. When the fault resistance increases to 300Ω, the *ROCOV* based method cannot work well. The comparison of the fault resistance endurance is presented in Table 7.



(a) *ROCOV* protection

(b) *MGV* protection

(c) V_L protection

Fig. 27. Response to different fault resistances under PTP faults.

Table 7. Comparison of maximum detectable fault resistance

Protection schemes	Maximum detectable fault resistance $R_{f\ max}$
ROCOV	200Ω≤$R_{f\ max}$≤300Ω
MGV	$R_{f\ max}$≥300Ω
V_L	$R_{f\ max}$≤200Ω

Table 7 demonstrates that the *MGV* based method is robust to fault resistance while the V_L based method is easily affected by the fault resistance.

C. Response to Change of Operating Conditions and AC Faults

The operation mode of the MMC HVDC grids is flexible, so it is necessary to investigate the impact of power flow change on the reliability of protection schemes. In addition, the robustness to AC faults should also be evaluated. Table 8 lists the identification results against power reversal and AC faults for the three schemes.

The power reversal does not change the magnitude and polarity of the DC line voltage. The DC voltage has a small fluctuation, which will not trigger the fault start-up element. Thus, it can be seen from Table 8 that the three protection schemes will not be affected by power reversal.

In the case of some severe AC faults, though the amplitude of the DC voltage is smaller than $0.5V_{dcn}$, the DC voltage drops slowly. Thus, the methods based on *ROCOV* and *MGV* will not operate falsely. Meanwhile, the DC line current rises slowly. Thus, the V_L based method will not operate falsely, either. To be concluded, these methods are robust to AC faults.

Table 8. Identification results against power reversal and AC faults.

Protection schemes	Power reversal	AC faults
ROCOV	Not action	Not action
MGV	Not action	Not action
V_L	Not action	Not action

D. Response to Noise Disturbance

According to Section II.B, the signal-to-noise ratio (SNR) represents the noise intensity. Adding disturbance with 20db, 18db, 15db, 13db and 10db noise on the measured signals to evaluate the impact of noise on the three protection schemes. The results are shown in Table 9. As can be seen, Once the noise is stronger than 15dB, the *ROCOV* and *MGV* based protection schemes will output the wrong identification result. In contrast, the V_L based method is robust to noise. For *ROCOV* based protection, to mitigate the impact of noise, the first-order damping element can be adopted, which has been introduced in [106]. For *MGV* based protection, the morphological filter (MF) can be employed to mitigate the impact.

Table 9. The impact of noise disturbance on protection schemes.

Protection schemes	SNR(db)	Identification result
ROCOV	20	Correct
	18	Correct
	15	Correct
	13	False
	10	False
MGV	20	Correct
	18	Correct
	15	Correct
	13	Correct
	10	False
V_L	20	Correct
	18	Correct
	15	Correct
	13	Correct
	10	Correct

E. Detection time

There are two factors determining the detection time. One is the time delay of the fault start-up element. The other is the time-window for the fault characteristic capture. In the case of internal faults, the fault start-up element is activated within one sampling interval. For the fault protection algorithm, once the initial TW arrives, the measured *ROCOV*, *MGV* and V_L will exceed the corresponding thresholds within several sampling intervals. During the design of the faulted pole selection criterion, a time-window with several milliseconds is adopted to capture the differences between the positive and negative poles. Based on equation (22), when the current-limiting inductance is selected as 0.1H, the detection time is $0.3ms+x/v_p$. It demonstrates that the detection time should be no more than 0.3ms when the fault occurs at the terminal of the transmission line. Considering that the sampling step is 0.04ms, the time-window for the faulted pole selection is selected to be 0.24ms (=0.04ms×6), which is smaller than 3ms. Hence, for any fault distance, the detection time for the three protection schemes are:

$$t_d = 0.04ms\ (fault\ start\text{-}up) + 0.24ms\ (time\ window) + x/v_p (TW\ propagation) \quad (26)$$

IX. Future Trends

Based on the aforementioned analysis, regarding the protection scheme design for the MMC based DC grids, the future trends can be summarized as shown in Fig. 29.

(1) Coordination between the control system and the protection system should be considered and designed [107][108]. For low-impedance faults (LIF), the fault characteristics are significant, e.g., the DC voltage drops rapidly and the fault current rises quickly, which can be easily detected. The main purpose of the control system is to limit the fault current to ensure the safe operation of power system. Whereas, under high-impedance faults (HIF), the fault characteristics are less obvious compared with LIF. Thus, the control systems are recommended to actively provide information to improve fault protection reliability.

(2) Coordination between different protection schemes under different fault conditions should be considered and designed. For LIFs, due to the large fault current, a single-end protection with ultra-fast speed is required to guarantee the safe operation of power system. For HIFs, the fault current is smaller, and a longer detection time margin is allowed. Hence, a longer time window can be adopted to improve reliability. Considering these fault conditions, the single-end protection schemes work as the main protection. While the pilot protection, which has a slow speed but high selectivity, can be adopted as the supplementary protection of the main protection. Once the single-end and pilot protection both refuse, the protection of adjacent lines should respond to the faults, which are regarded as back-up protection of the whole line.

(3) Coordination between protection schemes at different stages should be considered and designed [106]. Similar to the three-stage fault protection under AC faults, there is also three-stage protection for the DC grids. The first stage is the transmission line protection, which is adopted to isolate the faulted lines selectively. The second stage is the DCCB device protection. In the case of refusal of the first-stage protection, the DCCB device protection will be activated once the fault current flowing through the DCCB exceeds the threshold. Considering that DCCB protection on the adjacent lines may also be triggered, the second-stage protection is partially selective. When the first and second-stage protection refuse, the MMC protection is triggered to block the converter and acts as the third-stage protection. Since the blocking of MMC will cause the shutdown of the entire grid, the third-stage protection is non-selective [32].

(4) Coordination between the hardware and the protection algorithms, the control systems should be considered. The illustration of the relationship between hardware devices and protection algorithms is shown in Fig. 28. As can be seen, the limitations of hardware devices may constraint the use of some excellent protection algorithms and control methods. For example, the signal processing based protection schemes [84] and the active injection control [109] have outstanding performance in fault identification and fault location. However, they require high sampling frequency, which is a challenge for current hardware devices (10~50kHz in practical engineering). Therefore, those coordination protection schemes maybe not operable at present. Whereas, with the development of hardware devices, the coordination between hardware, protection algorithms and control system will be a feasible approach.

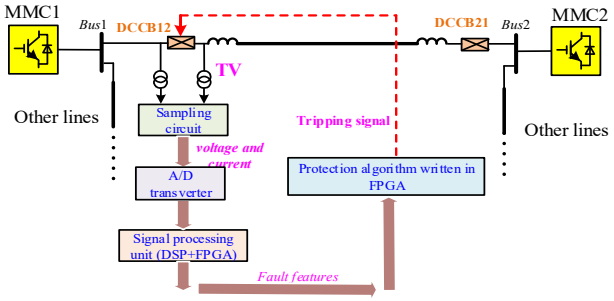


Fig. 28 Illustration of the relationship between hardware devices and protection algorithms.

(5) The impacts of renewable energy integration should be evaluated. Firstly, due to the intermittence and fluctuation characteristics of renewable energy, the power flow will change under normal states, which may result in the false operation of some protection schemes [110]. Also, some protection thresholds should be adjusted correspondingly. To smooth the fluctuations of renewable power, energy storage is adopted. However, the impact of energy storage on fault detection needs to be investigated. Secondly, to guarantee the uninterrupted operation of the integration system, the fault ride-through (FRT) controls are commonly implemented [111]. These FRT controls will affect the transient voltage and current, which will in turn affect the fault protection schemes. Moreover, the coordination between FRT controls and protection systems should be considered. Thirdly, as pointed out in [112], higher penetration of renewable generation will deteriorate the system inertia and cause the frequency instability problem. Thus, it is required to incorporate the DC grid protection and the frequency stability to guarantee system reliability.

(6) The protection thresholds should be determined adaptively and adjusted online. The renewable energy integration, the FRT controls, the active current-limiting controls and flexible loads

will result in the frequent change of system operating states. Thus, the protection thresholds should be adjusted online to respond to these changes. In addition, for LIFs, the thresholds should be larger, thereby avoiding the false protection operation under external faults. Whereas, for HIFs, the thresholds should be smaller to improve the robustness to fault resistances. To be concluded, the protection thresholds should be determined adaptively based on different fault conditions.

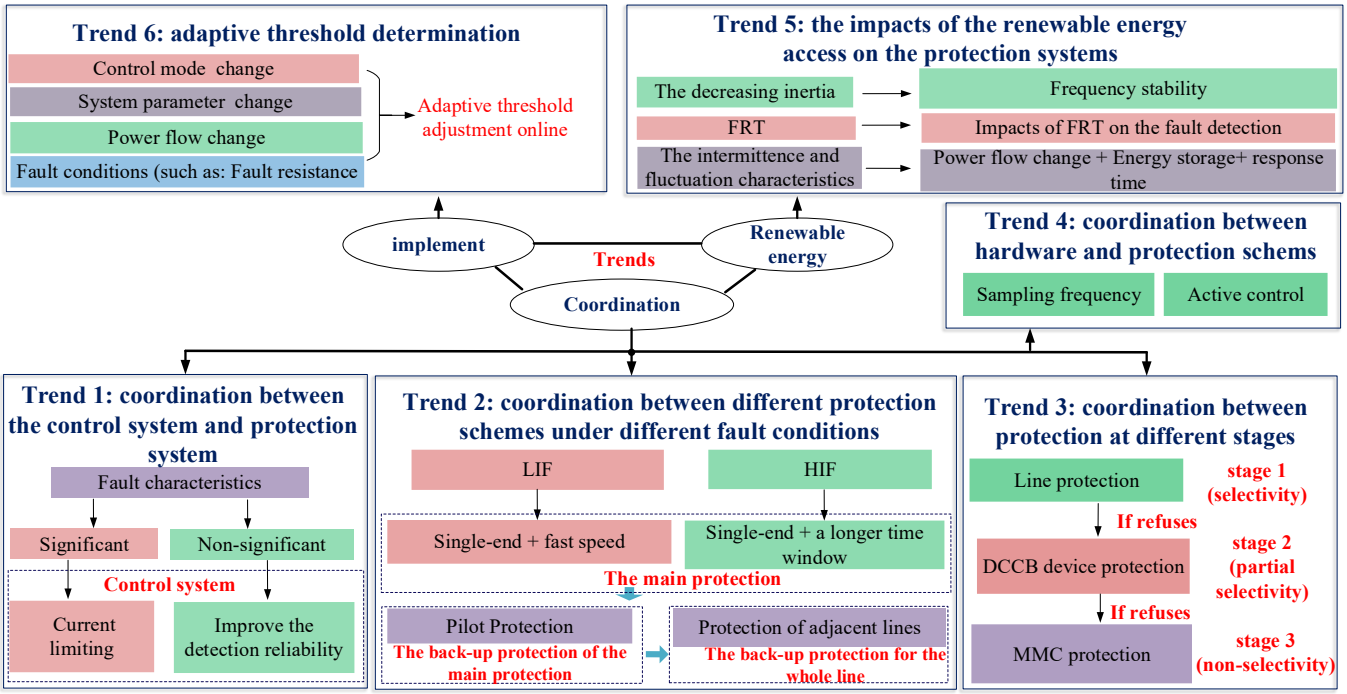


Fig. 29. Future trends of the MMC HVDC grid protection.

X. Conclusion

Focusing on the DC fault protection of MMC HVDC grids, this paper introduces the key technical issues and systematically analyzes the fault behaviors in modal-domain, time-domain and frequency-domain, respectively. Typical protection schemes dedicated to MMC HVDC grids are reviewed and compared. It can be concluded that,

1) Unlike AC power systems and LCC-HVDC systems, speediness is the top concern for MMC HVDC grid protection. Thus, ultra-fast single-end protection schemes are mostly adopted. To overcome the contradiction between speediness and sensitivity, a high sampling frequency is required to improve the single-end protection reliability. And WT or MG are adopted to detect the wave-front of the TW.

2) The modal-domain analysis method can be adopted to decouple the couplings between positive and negative poles, providing a theoretical basis to analyze the asymmetric faults. The zero-mode component is adopted to select the faulted pole while the line-mode component is adopted to identify the internal faults. The time-domain analysis method is mostly used to analyze the TW propagation behaviors, revealing the differences in voltage/ current changes between external and internal faults. The frequency-domain analysis method is used to analyze the difference in high-frequency components of transient current and voltage, thereby adopting the WT and MG to extract the high-frequency components.

3) Most existing single-end protection schemes are boundary protection that relies on large current-limiting inductances to guarantee high selectivity and sensitivity. The boundary protection can be summarized into three categories, the time-domain TW based methods, the signal processing based methods and the current limiting inductor voltage based methods. To improve the performance under weak boundary conditions, single-end protection schemes independent of boundary effects are required, which requires further investigation.

4) Simulations demonstrate that *ROCOV*, *MGV* and V_L protection schemes are fast and not affected by the change of operation mode and AC faults. The V_L method is robust to noise disturbance (>10dB) while vulnerable to fault resistance (≤ 200Ω). The MGV method is robust to fault resistance (>300Ω). The endurance to noise disturbance of the MGV based method (>13dB) is stronger than that of the ROCOV method (<15dB).

5) In future studies, the protection coordination needs to be considered and designed, including the coordination between the hardware, the control systems and the protection algorithms, the coordination between different protection schemes under different fault conditions, and the coordination between protection schemes at different stages. In addition, the impacts of renewable energy integration, energy storage and FRT controls on the protection schemes need to be investigated. To improve the reliability under different fault conditions, the thresholds should be adjusted online and determined adaptively.

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