Study of Power Devices for Use in Phase-Leg at Cryogenic Temperature

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Abstract— As air traffic has been increasing in recent years, the environmental impact of aviation is more obvious, forcing governments to impose stringent regulations on emissions. In order to meet these regulations, and reduce the carbon footprint, research has been directed towards the all-electric and hybrid aircraft, where the use of cryogenic HTS machines and cables has been proposed to reduce the overall size of the aircraft. With the cryogenic system already in place, research has been exploring the use of power electronics at lower temperatures in order to obtain systems with higher power densities and lower losses. In this paper several power semiconductor devices are tested at room and cryogenic temperature in order to evaluate their performance at lower temperature. One of the tested devices, a "CoolMOS" superjunction MOSFET, is used in a single voltage source phase-leg which is experimented with at room and cryogenic temperature to evaluate its efficiency as a primary indication of its usefulness in the All-Electric Aircraft.

Index Terms— All-Electric Aircraft, CoolMOS, cryogenic electronics, gate driver, MOSFET, phase-leg, superjunction.

I. INTRODUCTION

IN order to realize the electric aircraft, research has been focused on increasing the power density of the electric motor propelling the aircraft, and the use of high temperature superconductors (HTS) instead of copper conductors [1]–[3]. With the use of a cryogenic system to cool the HTS down to temperatures in the region of 77 K, it could be beneficial from an engineering point of view to keep all of the electrical system at the same temperature; this in turn would include the power electronic devices that are responsible for driving the motor. The main purpose of this paper is to focus on cryogenic power electronics especially as they have promising benefits when compared to room-temperature converters in terms of reduced size and weight, improved efficiency, and reliability [4], [5]. With the cooling equipment already planned to be in place inside the all-electric aircraft, this would require insulation between cable sections and drives sections if the latter were operated at room temperature. Thus, cryogenic power converters can take up less space and weigh less than their counterparts, as the devices can carry larger currents for the same power loss values, thus avoiding using bigger semiconductor modules. This translates into saving fuel and cost of flights.

This paper focuses on testing the characteristics of a selection of diodes and a superjunction ("CoolMOS") MOSFET at room temperature and cryogenic temperature. Three main

characteristics are tested: 1) The forward voltage of the devices, which has a major contribution to the conduction losses; 2) The breakdown voltage, which affects the ability of the semiconductor devices to withstand reverse voltage; and 3) The reverse recovery charge, which influences the switching losses of the semiconductor devices.

Numerous papers have discussed the effect of low temperature on the characteristics of diodes. The main characteristics that have been widely explored are: a) the forward voltage which generally increases at cryogenic temperature; b) reverse (breakdown) voltage which decreases by around 20%; c) on resistance which decreases [4]-[7]; d) reverse recovery characteristics which generally improve at cryogenic temperature, thereby reducing switching losses by 80% [6], [7], [8].

The literature has shown that the on-state resistance $R_{DS(on)}$ of MOSFETs decreases at cryogenic temperature, thus at cryogenic temperature they have lower conduction losses. The breakdown voltage at cryogenic temperature decreases by 20%, and their overall switching losses have decreased by 60% [4], [5], [8]-[11].

II. CHARACTERIZATION OF SEMICONDUCTOR DEVICES AT CRYOGENIC TEMPERATURE

As the rated voltage and current of the devices in previous literature is different from what is required, in this section a set of semiconductor devices have been chosen to accommodate the requirements of targeted rated voltage and current set by Airbus SAS to be 1200 V and 100 A. These devices shown in Table I have tested at room and cryogenic temperature. The VS-QA250FA20 device is only tested here for completeness. Three main performance tests will be conducted on the devices in Table I. The tests are conducted twice, once at room temperature and a second time at a cryogenic temperature of 77 K. For the cryogenic testing, the device under test (DUT) is placed in a container filled with liquid nitrogen.

A. Forward Voltage Test

This test was carried out with the rig in Fig. 1. A laboratory power supply was used to control the current through the DUT. The anode-cathode (or drain-source) voltage across the device was measured using an NI 9205 Card. The Schottky diodes have shown an increase in the forward voltage. Conversely, the Si ultrafast diodes show reductions. However, the Si superfast

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Device part number	Manufacturer	Technology	Rated voltage (V)	Rated current (V)
GB2X100MPS12-227	GeneSiC	SiC Schottky diode	1200	200
VS-QA250FA20	Vishay	Si Schottky diode	200	250
APT2X101D120J	Microsemi	Si Ultrafast diode	1200	93
VS-HFA220FA120	Vishay	Si Ultrafast diode	1200	110
MUR2X100A12	GeneSiC	Si Superfast diode	1200	200
IPW60R041C6	Infineon	Si CoolMOS	650	50

diode from GenSiC shows little change, and this would lead to further test analysis.

B. Reverse Voltage (Breakdown) Test

The reverse voltage test was carried out with the rig in Fig. 2, where the DUT is connected in reverse polarity to a high-voltage source. The voltage is gradually increased and the reverse current is measured. The gradual increase of the voltage stops as soon as the leakage current reaches the rated leakage current.

C. Reverse Recovery Test

This test was carried out with the double-pulse rig in Fig. 3. Q1 is switched on to charge the inductor L1 with a current I (A). Q1 is then switched off, and I (A) circulates through the diode (DUT). A second pulse is applied to Q1, which commutates the current flowing through the diode. In this manner the switching characteristics of the device can be observed.
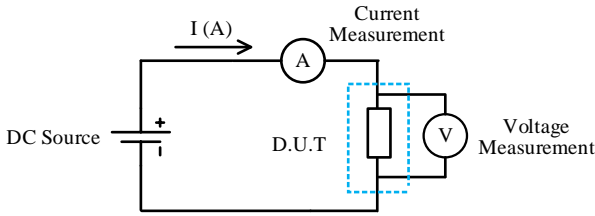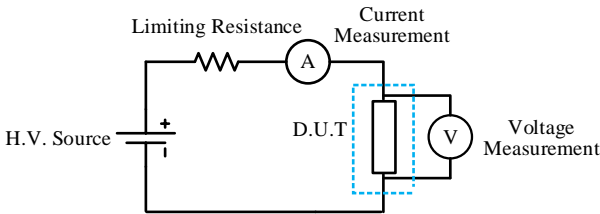

Fig. 1. Forward voltage test circuit.

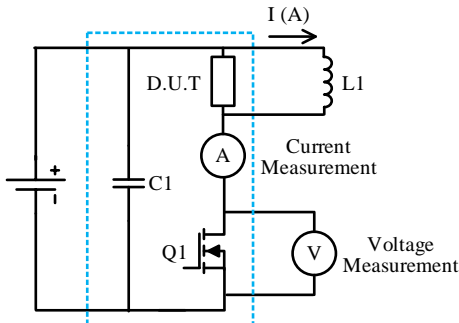Fig. 2. Reverse voltage (breakdown) test circuit.

Fig. 3. Reverse recovery test circuit.

III. EXPERIMENTAL RESULTS

A. Forward Voltage Test Results

The forward voltage for the six devices has been tested at room and cryogenic temperature. The two Schottky diodes, GB2X100MPS12-227 and VS-QA250FA20, have shown an increase in the forward voltage at cryogenic temperature as seen in Figs. 4 (a) and (b) that can be mainly attributed to the increase of resistance and increase of threshold voltage at cryogenic temperature due to the structure of the diode, the same as in the literature [11]. The two Silicon Ultrafast diodes (APT2X101D120J and VS-HFA220FA120) have shown a decrease in the forward voltage, as the resistance had a more dominant effect than the offset voltage [4]. For the Si Superfast diode, the performance showed little change when the temperature was decreased. The superjunction (CoolMOS) MOSFET has seen a significant decrease in its drain-source voltage v_{DS} at a given current which is similar to results in the literature [4], [5].

B. Reverse Voltage (Breakdown) Test Results

The breakdown voltage test has been conducted for the six devices at cryogenic and room temperature as in Figs. 4 (c) and (d). The breakdown voltage for the Si and SiC Schottky diode was not affected by the decrease of temperature, which is similar to [12]. For the Si Ultrafast and Si Superfast diodes, and the superjunction MOSFET, as in [4], there was a decrease in the breakdown voltage of approximately 20%.

C. Reverse Recovery Test Results

The reverse recovery test was conducted for the five diodes, and results are shown in Figs. 4 (e), (f), (g), (h), and (i). For the Schottky diodes, the reverse recovery charge Q_{rr} was not affected by the decrease of temperature. For the Si Ultrafast and Si Superfast diodes there was a decrease in the peak current at reverse recovery at cryogenic temperature, and hence improved performance same results as obtained in [13] and that can be attributed to the increased in mobility of the device increasing the transconductance of the Si device structure.

D. Summary of Test Results

Table II summarizes the results from the tests at room and cryogenic temperature. The forward voltage for the Schottky diodes has increased at cryogenic temperature, whereas the breakdown voltage is almost the same and the reverse recovery characteristic improved for the SiC Schottky diode, and remained the same for the Si Schottky diode.

The Si Ultrafast and Si Superfast diodes both exhibited the same behavior for reduced breakdown voltage and improved reverse recovery characteristics. However, the forward voltage for the Si Ultrafast was lower at cryogenic temperature and the Si Superfast forward voltage remained the same. The superjunction device has exhibited a lower forward voltage and reduced breakdown voltage at cryogenic temperature. For future all-electric and hybrid electric aircraft applications, Si Ultrafast diodes have shown good characteristics at cryogenic temperature and are good candidates to be chosen in converter circuits.
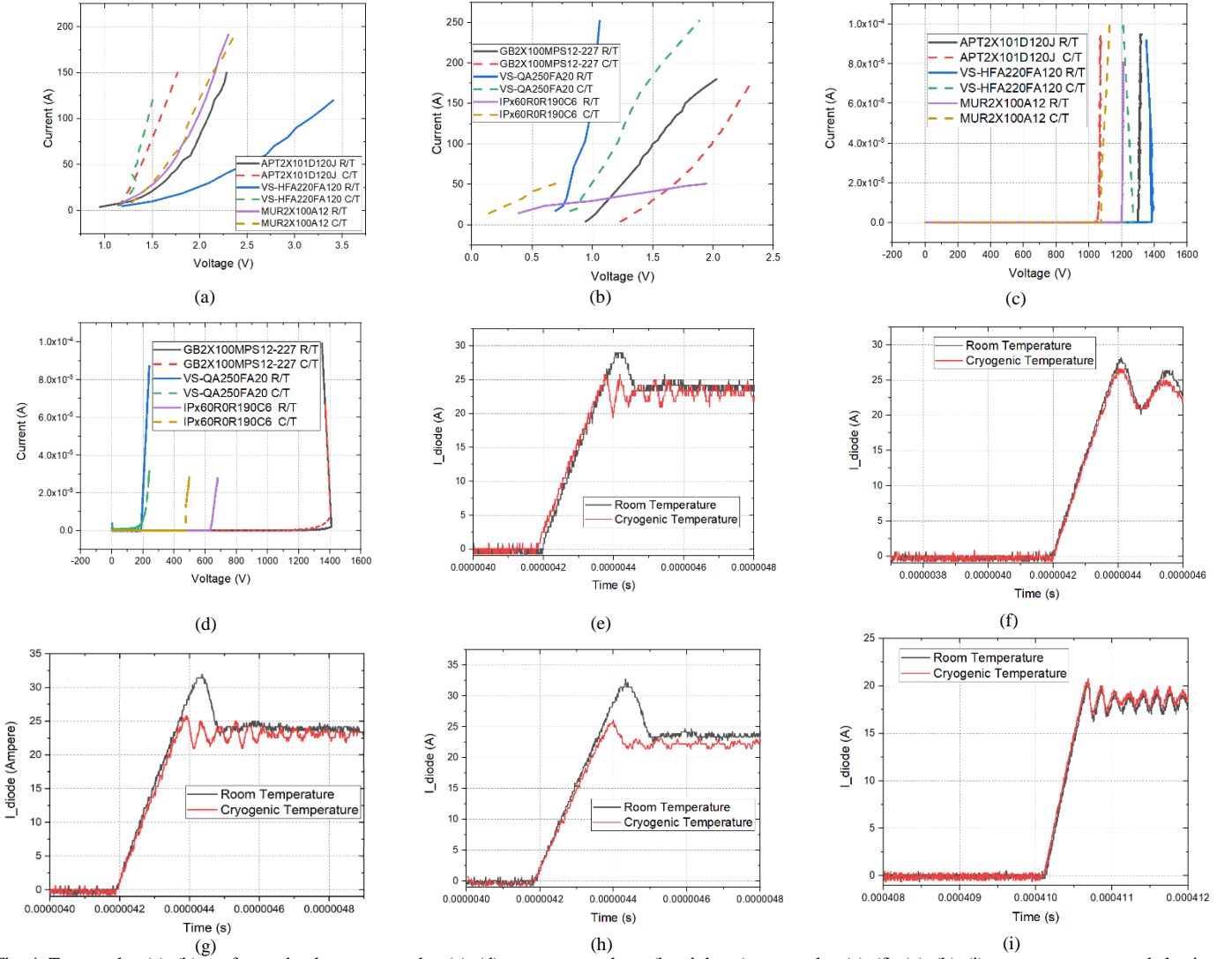
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(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)

Fig. 4. Test results: (a), (b) are forward voltage test results; (c), (d) are reverse voltage (breakdown) test results; (e), (f), (g). (h), (i) are reverse recovery behavior test results, among which (e) is APT2X101D120J, (f) is GB2X100MPS12-227, (g) is MUR2X100A12, (h) is VS-HFA220FA120, (i) is VS-QA250FA20. For the purposes of testing, Q1 in Fig. 3 was switched on relatively slowly.

TABLE II. SUMMARY OF RESULTS

	GB2X100MPS12-227 GeneSiC SiC Schottky		VS-QA250FA20 Vishay Si Schottky		APT2X101D120J Microsemi Si Ultrafast		HFA220FA-120 Vishay Si Ultrafast		MUR2X100A12 GeneSiC Si Superfast		IPX60R190C6 Vishay CoolMOS	
Temperature (CT=77K)	RT	CT	RT	CT	RT	CT	RT	CT	RT	CT	RT	CT
$V_{forward}$ (V)	1.49	1.99	1	3.16	2.08	1.5	3.16	1.46	1.9	1.8	1.0	0.46
% Change	+33%		+60%		-24%		-53%		-5%		-54%	
[Current used for $V_{forward}$ test (A)]	[100]	[100]	[200]	[200]	[100]	[35]	[100]	[100]	[100]	[100]	[35]	[35]
V_{BR} (V)	1400	1400	220	240	1300	1000	1400	1300	1200	1080	650	480
% Change	0%		+9%		-23%		-7%		10%		-26%	
Q_{rr} charge (nC)	168	112	104	128	28	1.62	102	5.43	192	6.56	-	-
% Change	-33%		23%		-94%		-94%		-96%		-	
Peak transient current (A)	28.2	26.6	20.8	32.8	25.8	25.8	32.8	26.1	32.1	25.8	-	-

IV. TESTING OF PHASE-LEG IN DC-DC CONVERTER MODE

As part of the implementation of cryogenic semiconductors for all-electric and hybrid electric aircraft, tests have been conducted for a phase-leg at the same rating requirements by Airbus SAS. Previous papers have tested converters at cryogenic temperature [14], [15] where the converters immersed at cryogenic temperature were found to be more efficient than at room temperature, with cooling losses excluded. In this paper the superjunction MOSFET tested in Section IV was used as the building block for the phase-leg in Fig. 5 (a). Superjunction MOSFETs are known to be superior to standard MOSFETs due to their low on-state resistance [16]. However, their intrinsic diode passes a high reverse recovery charge Q_{rr}. The arrangement in [17] was used to eliminate the large losses attributable to Q_{rr} as seen in Fig. 5 (a). The low-voltage MOSFETs $TS1$ and $TS2$ operate in synchronicity with the main MOSFETs $TR1$ and $TR2$. The low-voltage MOSFETs prevent freewheeling currents from flowing in the main MOSFETs' intrinsic diodes and incurring high losses attributable to their Q_{rr} charges. Instead, current flows through the external diodes D_{ext1} and D_{ext2}. The problem of currents drawn by the MOSFETs' output capacitances is addressed by operating the circuit with the dual-mode control scheme in [18].

Fig. 6 shows the physical circuitry used for testing. The gate driver circuit was located remotely, and was not submerged in the LN2, hence the lengthy gate driver connections. The output inductance (Lchoke) and output capacitance were left at room temperature. Applying a tightly-controlled gate-source voltage is challenging due to the stray inductances introduced with this arrangement. However, the gate-source junction of the Si MOSFET is tolerant of a wider voltage range than is the case with SiC or GaN devices. Furthermore, the gate-source threshold voltage of Si MOSFETs rises [4] when the device is cooled from RT to 77 K, yielding improved noise immunity.

The circuit in Fig. 5 (a) was connected in the buck configuration in Fig. 5 (b), which was run at a duty cycle of 10%. With respect to [18], the circuit is therefore operating in the unipolar mode with a positive output current.
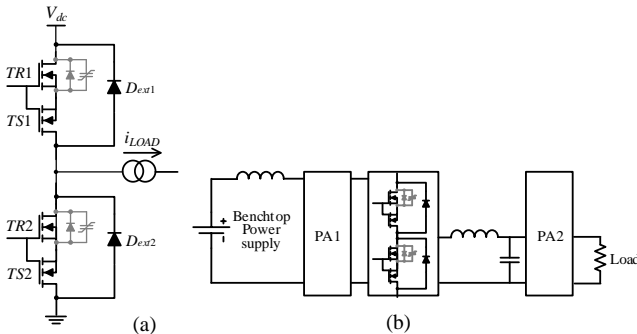

Fig. 5. (a) Phase-leg based around MOSFETs with intrinsic diode deactivation circuitry from [16]. (b) Electrical test connections.
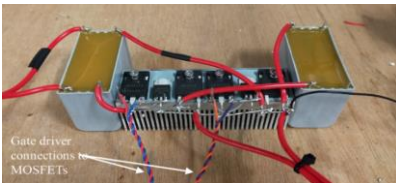

Fig. 6. Experimental phase-leg used for testing.

Two PM100 power analyzers, PA1 and PA2, were used to measure the input power and output power. Using a low duty cycle is advantageous here as the circuit can be run with a low power throughput, but nonetheless with full-load current and full-load switching losses. If the losses are inferred from the difference between the measured input power and output power, this enables more accurate loss measurements to be obtained. The inductor L_{in} was included to reduce the high-frequency ripple current drawn from the supply, and thereby enable a more accurate input power measurement to be obtained from PA1.

Initially, the circuit was run at room temperature before immersing it in LN2 for cryogenic testing. Plots of loss against switching frequency with Vdc = 270 V and i_L = 10 A, at both RT and 77 K are shown in Fig. 7. Losses in the 1-mH output choke (Lchoke) are included here in order to obtain higher accuracy reading from the power analyser. The loss in the choke is assumed constant and thus the losses at room and cryogenic temperature are easily comparable. Fig. 8 shows the efficiency at both room and cryogenic temperature. The efficiency plotted does not include any cooling losses.
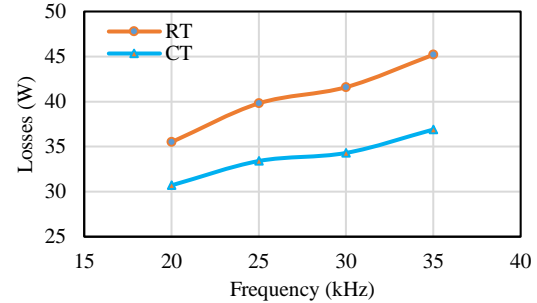

Fig. 7. Losses against switching frequency at both RT and 77 K. The circuitry was intentionally run at a low-efficiency operating point to facilitate accurate loss measurements.
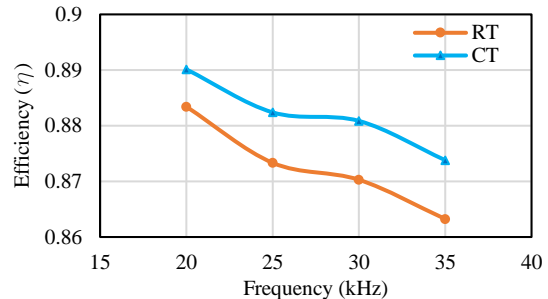

Fig. 8. Efficiency against switching frequency at both RT and 77 K. The circuitry was intentionally run at a low-efficiency operating point to facilitate accurate loss measurements.

V. CONCLUSION

The characteristics of a selection of power semiconductor devices were tested at room and cryogenic temperature to improve the power density of all-electric aircraft. Si Ultrafast diodes and the superjunction MOSFET have shown significant improvements in terms of forward voltage and switching, which will in turn reduce the power dissipation of a converter. The tested MOSFET was then used to build a phase-leg, which has shown a higher efficiency at cryogenic temperature. For future work the phase-leg shall be extended to a full converter to be tested at cryogenic temperature and under AC conditions.

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