Are wave union methods still suitable for 20 nm FPGA-based high-resolution (< 2 ps) time-to-digital converters?

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Abstract: This paper presents several new structures to pursue high-resolution (< 2 ps) time-to-digital converters (TDCs) in Xilinx 20 nm UltraScale field-programmable gate arrays (FPGAs). The proposed TDCs combined the advantages of 1) our newly proposed sub-tapped delay line (sub-TDL) architecture effective in removing bubbles and zero-bins and 2) the wave union (WU) A method to improve the resolution and reduce the impact introduced from ultrawide bins. We also compared the proposed WU/sub-TDL TDC with the TDC combining the dual sampling (DS) structure and the sub-TDL technique. Moreover, we introduced a binning method to improve the linearity and derived a formula of the total measurement uncertainty for a single-stage TDL-TDC to obtain its root-mean-square (RMS) resolution. Results conclude that the proposed designs are cost-effective in logic resources and have the potential for multiple-channel implementations. Different from the conclusions from a previous study, we found that the wave union is still influential in UltraScale devices when combining with our sub-TDL structure. We also compared with other published TDCs to demonstrate where the proposed TDCs stand.

1. Introduction

A time-to-digital converter (TDC) can measure the time interval between two events with a high resolution. Combined with single-photon detectors [1,2], TDCs have been applied widely in clinical positron emission tomography (PET) [3,4], light detection and ranging (LiDAR), robotics and self-driving vehicles [5–8], fluorescence lifetime imaging microscopy [9–12], quantum communications [13,14], time-of-flight (ToF) imaging [15,16], and nuclear/particle physics [17,18]. TDCs can be essential in all-digital phase-locked loops, and digital synthesizers for other applications [19–22].

TDCs can be implemented in analog or digital methods. Boosted by recent advances in CMOS manufacturing technologies, digital TDCs with a sub-nanosecond resolution have become much more prevalent in highly integrated systems. Compared with the digital TDCs implemented with the application-specific integrated circuits (ASIC), field-programmable gate array (FPGA) based TDCs are: 1) fast and easy to prototype, 2) low cost, and 3) reprogrammable.

The resolution (also called the least significant bit, LSB, or the average bin size) of a TDC is the lowest time interval that it can measure. Many applications particularly require high-resolution (<10 ps) TDCs and the demands have been growing strongly significantly for applications in LiDAR [23,24], PET systems [3,4], and time-domain diffuse correlation spectroscopy [25–27].

The tapped delay line (TDL) architecture has been a mainstream approach [28–30] for FPGA-TDCs since carry-chain modules can easily construct TDLs in modern FPGA devices [31–35]. The propagation time of a signal propagating through a TDL can be measured and digitized. The resolution of a TDL-TDC is related to the signal propagation delay in TDLs.

Compare with previous FPGA structures, CARRY8 modules in Xilinx UltraScale FPGAs can double the number of taps of a TDL. With this structure, the resolution of a double sampling (DS) TDL-TDC achieved 2.25 ps [36]. To further improve the resolution of FPGA-TDCs, the Vernier delay line (VDL), the multi-phase design and the multi-chain design have been proposed to overcome process-related limitations [37–47]. These methods can achieve a better resolution than raw TDL architectures. However, these methods consume logic resources significantly, and the systems are complicated. The stochastic method, exploiting the stochastic properties of a set of latches to achieve a higher resolution, is popular in ASIC TDC designs but cannot be easily applied to FPGA designs. In [42], a 2D semi-stochastic Vernier structure was proposed to enhance the performance.

Some researchers used FPGA digital signal processing (DSP) blocks to build a TDL [48,49]. However, the linearity is still low. The linearity of a TDC is also a critical parameter to be ensured; a low-linearity TDC usually causes severe measurement uncertainties, even with a high resolution. The linearity performances of TDCs can be characterized by the differential nonlinearity (DNL) and the integral nonlinearity (INL) [50]. DNL and INL are defined as:

$$DNL[i] = \frac{W[i] - W_{ideal}}{W_{ideal}}, \tag{1}$$

$$INL[i] = \sum_{n=0}^{i} DNL[n], \tag{2}$$

where $W[i]$ is the width of the i-th bin and the W_{ideal} is the ideal bin width. The DNL is the deviation of a quantization step from the ideal value of 1 LSB, and the INL is the accumulation of the DNL. We can obtain DNL and INL from code density tests.

About FPGA-TDCs, the non-uniformity of carry-chains and clock skews are two main reasons for nonlinearity [44]. The clock skew is caused by the dedicated clock distribution tree in FPGAs, and large clock skews usually appear at the boundaries or in the middle of clock regions (CRs). The non-uniformity of carry-chains deteriorates the linearity of entire delay lines and generates ultra-small bins and ultra-wide bins. The ultra-small bins (DNL $\leq$ -0.90 LSB) can be merged, and the zero-width bins (DNL = -1.00 LSB) need to be abandoned (since there are unable to capture any information). However, ultra-wide bins deteriorate the precision of measurements significantly. Wu *et al.* proposed the wave union (WU) method to ease ultra-wide bin problems and improve the precision [51]. A wave union signal, containing several rising edges (0-1 transitions) and falling edges (1-0 transitions), performs multiple measurements with a single TDL. The ultra-wide bins are sub-divided with this method.

To further improve the linearity and precision, calibrations are usually needed in TDCs. Previously published calibration techniques include the bin-by-bin calibration [31,52–54] and bin-width calibration techniques [55,56].

Furthermore, the mismatches between carry-chains in FPGAs lead to bubble problems [38] and cause encoding failures [35]. Traditional de-bubble operations use logic gates to remove bubbles or to recognize real signal transitions [38,54,57]; however, they introduce extra logic resources and clock cycles [38]. Bubble problems become more severe in more advanced UltraScale FPGAs. Moreover, the de-bubble method proposed in [58] performs differently for the 0-1 and 1-0 transitions. Therefore, the bubble problems persist, prompting Wang and Liu to conclude that the wave union method is not suitable for UltraScale FPGAs [36]. Since then, there is no efficient WU TDC implemented in UltraScale FPGAs reported. However, in 2018, the decomposition [35] and our sub-TDL [55] methods were proposed to more efficiently remove bubbles and zero-width bins without consuming extra logic resources.

Chen and Li reported that with sub-TDL structures, bubbles could be removed entirely [55]. It prompted us to ponder: A) whether the WU method still cannot be employed in UltraScale FPGA devices as suggested by [36] if bubble-resistant sub-TDL structures are available; B) whether the

advantages of the sub-TDL design can be applied to DS structures, given the fact that the new CARRY8 modules contain both carry C and sum S output ports for the DS structure [36]; C) whether a combination of the above strategies can be exploited to achieve a resolution (towards 1 ps LSB conversion) with maintained linearity. Although UltraScale FPGAs were first introduced in 2014, there are few efficient TDCs reported in UltraScale FPGAs [32,36,55]. Migrating existing methods to such advanced FPGAs is not trivial at all, as the carry chains are slightly different from earlier generations. Moreover, a detailed uncertainty analysis has not been reported. This study aims to investigate the suitability of the WU method in UltraScale FPGAs and to alleviate related problems.

 With the above rationales, the main innovations of this work include:

 1) We clarified the difference in the propagation speed between the rising edge (0-1 transition) and the falling edge (1-0 transition) of the WU signal with an equation and a figure providing quantitative information. We reached a new conclusion different from a previously published study [36] about the suitability of the WU method in UltraScale devices; our analysis shows that the WU method is still powerful if it integrates our recently proposed sub-TDL structure [55]. We presented the first efficient single-TDL WU TDC in 20 nm UltraScale FPGAs. The outcomes should be able to convince researchers within the community to continue applying the WU method in more advanced FPGAs.

 2) We implemented the first efficient WU TDC in UltraScale FPGA devices by integrating our newly proposed sub-TDL structure [55]. To present its efficiency, we also compared it with three other different TDC structures. Four TDC structures employing sub-TDL designs were proposed, implemented, and tested in the Kintex UltraScale KCU105 Evaluation Kit (UltraScale XCKU040 FPGAs):

  a) WU/Sub-TDL TDC, denoted as WU TDC,
  b) DS/Sub-TDL TDC, denoted as DS TDC,
  c) DS/WU/Sub-TDL TDC, denoted as DSWU TDC,
  d) Binned-DSWU TDC with a proposed binning method to improve the linearity.

The study further demonstrates that the WU method promises an efficient solution.

 3) Detailed analysis of measurement uncertainties and error sources for the four proposed TDCs have been conducted.

2. Design and Architecture

 For the proposed methods, the TDL architecture was used and constructed with cascaded carry chains CARRY8 and implemented in the UltraScale XCKU040 FPGA. Figure 1 shows the block diagrams of the proposed four TDCs. The DSWU and binned DSWU TDCs are derived from the combination of the structures shown in Figures 1(a) and 1(b). The DS TDC is the combination of the designs shown in Figures 1(b) and 1(c), whereas the WU TDC is constructed by the structures shown in Figures 1(a) and 1(d). We employed the newly proposed sub-TDL architectures in all four TDCs. Figure 1(a) shows a WU launcher generating a WU signal (containing a rising edge and a falling edge to provide additional sampling) into a TDL. The delay taps are sampled by the Sub-TDL Rising and Sub-TDL Falling modules. For non-WU designs shown in Figure 1(c), the hit signal is fed to the TDL directly. The launcher and related modules, such as the sub-TDL and the encoder for the falling edge, are removed. From Figures 1(a) and 1(c), the signal width from the CARRY8 depends on whether the DS method is employed. With the DS method, all outputs (both carry C outputs and sum S outputs, 16 bits in total) of the CARRY8 are sampled by a sub-TDL module, as shown in Figure 1(b). However, for the non-DS designs, only C outputs of the CARRY8 (8 bits in total) are considered (see Figure 1(d)). Note that there is still a buffer between S and C ports. In CARRY8, this buffer is a 2-to-1 multiplexer [59]. With the sub-TDL architecture [55], the raw thermometer code generated by a TDL is split into several subsets. These sub-thermometer codes are converted to corresponding one-hot codes (by TM2OH) and then encoded to binary codes (by OH2BIN) in the encoding module. The fine code of the TDC is the sum of these binary codes. From Figure 1, we conclude: 1) The numbers of the sampled taps from a CARRY8 module are $8 \times 2 \times 2 = 32$ (sampled by all outputs of the CARRY8
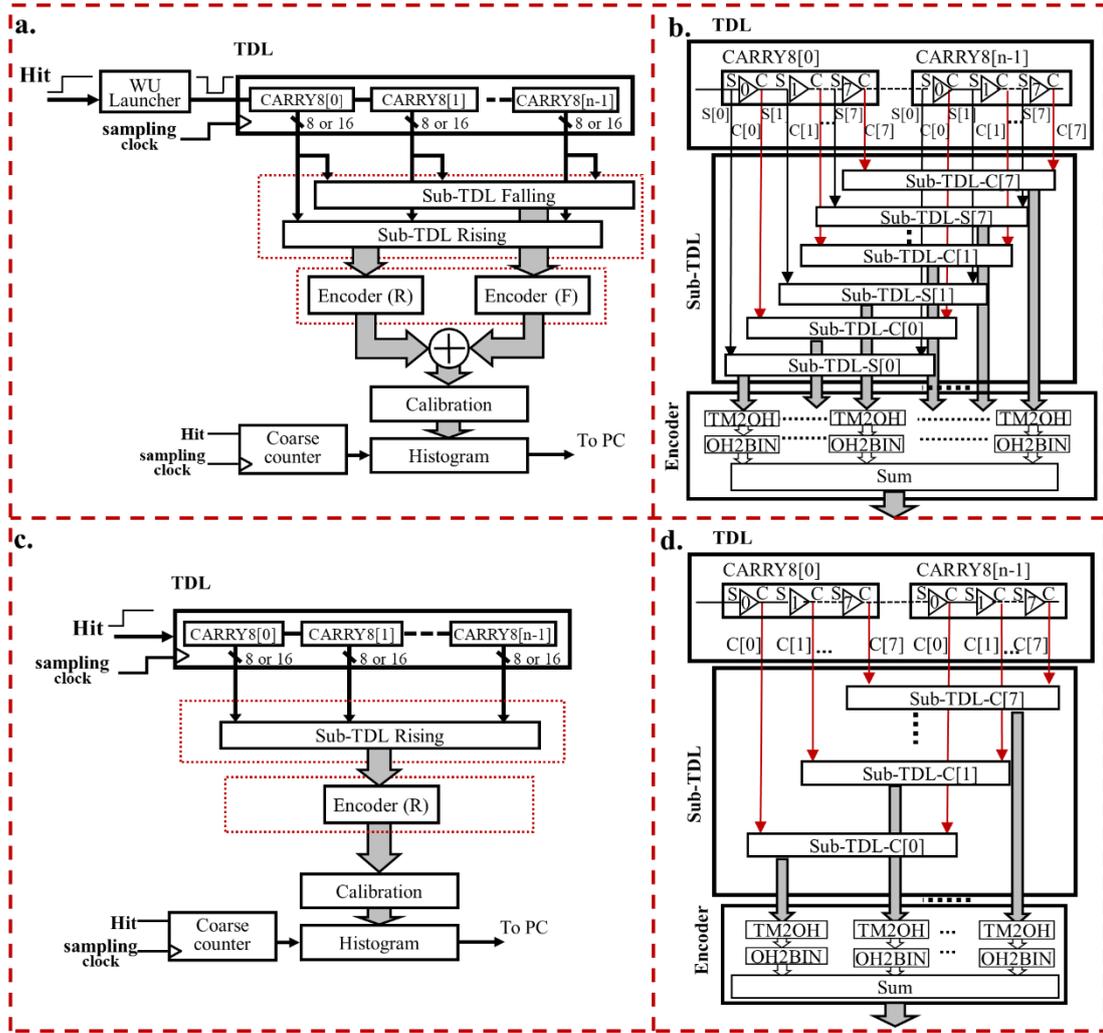
Figure 1. (a) Block diagram for the proposed TDC systems with the WU method. (b) Block diagram for the sub-TDL structure with the DS method and the encoder. (c) Block diagram for the proposed TDC system without the WU method. (d) Block diagram for the sub-TDL structure without the DS method and the encoder.

and then sampled sequentially by the Sub-TDL Rising and Sub-TDL Falling modules) for DSWU or binned DSWU TDCs or $8 \times 2 = 16$ for DS or WU TDCs. A TDC using neither WU nor DS methods only has eight taps sampled from a CARRY8 module, as shown in Figure 1(d). Architectures with more sampled taps offer a higher time resolution. 2) The sub-TDL structure can remove bubbles.

2.1. Dual-sampling Structure with Sub-TDL

The DS TDL structures were proposed in [32,36]. Compared with previous FPGA structures, CARRY8 structures in UltraScale FPGAs double the number of the taps or the equivalent bins of a TDL with the same total propagation delay. Therefore, the theoretical LSB or the average bin size can be reduced. However, the linearity degrades when the resolution is enhanced. A DS TDC with the sub-TDL encoding structure [55] has been proposed in this study. Figure 2 presents the linearity performance for the proposed DS TDC. This TDC achieved 2.53 ps resolution, and the length and the location of the TDL are confined within a central clock region.

In Figure 2, the broader bins around bin 450 cause a distinct step in the INL curve. Similar phenomena can be observed in the proposed DS and DSWU TDCs. The reason for these phenomena is that significant clock skews exist due to the bifurcation of the clock distribution tree in the middle of a clock region. To overcome this problem and to correct the accumulated offset, bin-by-bin remapping or mixed-calibration can be used. The main idea of the bin-by-bin calibration is to calibrate
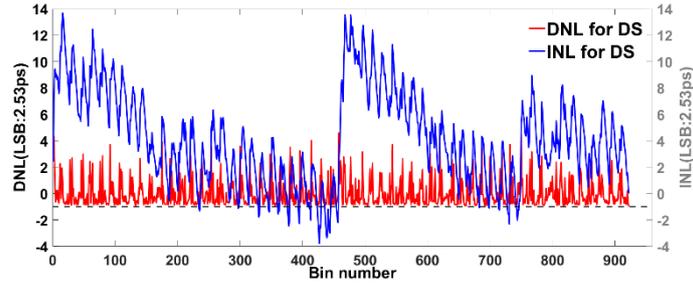
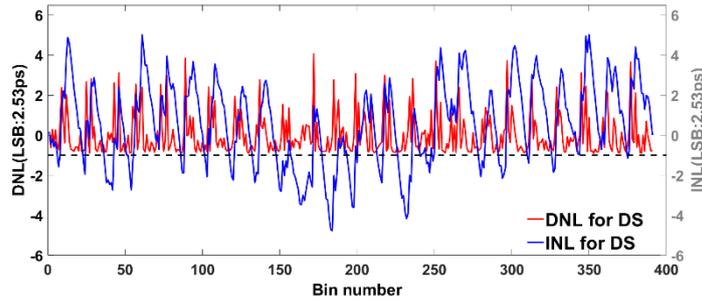**Figure 2.** DNL and INL curves for the DS TDC.

Figure 3. DNL and INL curves for the DS TDC (only using 390 bins).

the times to the centers of the bins to correct the INL. Besides, the double-phase sampling architecture [44] can be used to halve the length of the TDL to avoid the clock skew problem. Figure 3 presents the linearity performance for the DS TDC with a range of 390 bins, and the INL_{pk-pk} (peak-to-peak INL) is improved to 9.80 LSB.

2.2. Wave Union Method

The WU method is another way to improve the resolution and alleviate ultra-wide bin problems. As shown in Figure 4, with the WU signal containing the rising and falling sampling edges, a WU TDC can perform like a TDC with two delay lines, one for the rising edge and another for the falling one. The LSB of the WU TDC is:

$$LSB_{wu} = \frac{MR}{N_{wu}} = \frac{MR}{N_{rising}+N_{falling}} = \frac{LSB_{rising} \times LSB_{falling}}{LSB_{rising}+LSB_{falling}}, \tag{3}$$

where MR is the measurement range of a simple delay line. N_{wu}, N_{rising}, and $N_{falling}$ are the bin numbers of the WU TDC, the plain TDC with the rising edge and the plain TDC with the falling edge, respectively. The WU method can divide the ultra-wide bins in each raw measurement efficiently, and the average of these measurements yields a finer TDC resolution [60].

An effective launcher, capable of producing a stable WU signal, is vital for the whole system. The jitter caused by the WU signal, however, usually feeds to the TDL, and degrades the linearity.

The WU method has been studied by serval groups [52,53,58,61]. However, the propagation speeds of the falling edge and the rising edge are different in Kintex-7 FPGAs [58]. The WU interpolation efficiency on the resolution was revealed in a study, performed in different FPGAs, from 65 nm to 28 nm processes [62]. The results also indicated that the speed of the rising edge is different from that of the falling edge.

We have performed similar tests in UltraScale FPGAs. The results do show the difference in the propagation speed between the falling sampling edge and the rising sampling edge. Figure 5(a) shows the principle of the propagation speed difference between the rising edge and the falling edge; the gap between the rising edge and the falling edge varies when the WU signal propagates along the TDL. Figure 5(b) shows the relationships between the bin number and the measured time for the
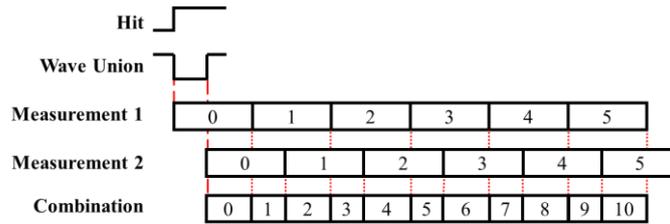
Figure 4. Concept of the WU method. The wave union only contains a pair of 0-to-1 and 1-to-0 transitions
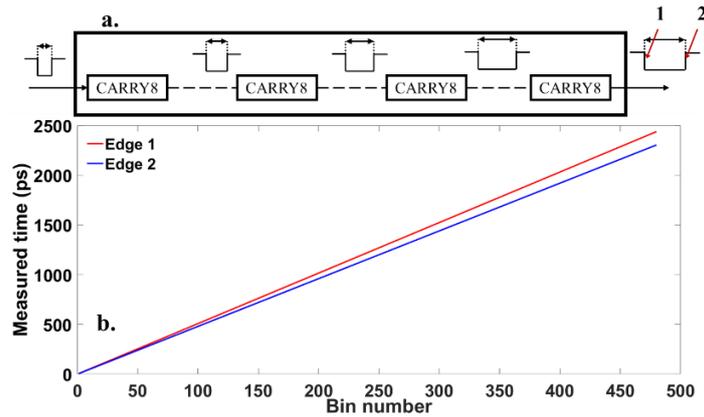

Figure 5. (a). An example of the propagation speed difference between the rising edge and falling edge. (b) The bin number versus the measured time curves for the rising and falling edge signals.
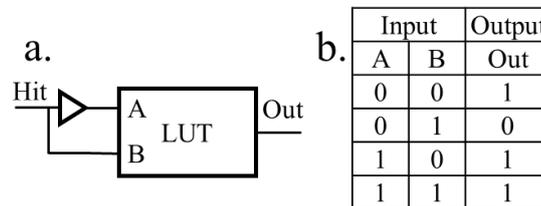

Figure 6. (a) The WU launcher built by a LUT and (b) the truth table for LUT WU launcher.

two edge signals; the edges use a different number of taps to convert a fixed time interval. Although the bin realignment proposed in [58] can remove most bubbles, it performs differently for the 0-1 and 1-0 transitions owing to the speed difference. Therefore, the bubbles cannot be removed easily in traditional WU TDCs [36]. A WU-A launcher constructed by a look-up table (LUT) was applied to our design, as shown in Figure 6(a). Figure 6(b) is the truth table for the LUT WU launcher. It generates a negative pulse when it receives a hit signal.

2.3. Wave Union Method Integrated With sub-TDL Structure

The mismatch [38] in tap timing along the TDL becomes more serious when the tap interval becomes shorter and results in serious bubble problems, especially in 28 nm FPGA and more advanced process technologies [32]. Because of this more severe bubble problem and the speed difference between the rising edge and the falling edge, "The wave union method cannot be used in the UltraScale FPGA for further improving the time precision" [36]. However, we find that it is not the case in our designs.

A bubble-free method called the sub-TDL structure (or the decomposition developed independently at the same time [35]) was proposed in [55]. The main idea is to ignore the mismatch

in the TDL by elongating the tap interval [55]. Song *et al.* also observed that the length of the bubble area is limited. Bubbles can be removed by decomposing the output data from the raw TDL [35].

Figure 1(b) and 1(d) show the sub-TDL structure with and without the DS method, respectively. A TDL can have several subsections with shorter thermometer codes. After encoding, the averaged TDL can be reconstructed by summing up the fine codes of the sub-TDLs. Bubbles can, therefore, be removed, and the WU method can still be applied to UltraScale FPGAs, different from the statement in [36]. The WU signal only contains two edges in this study, and the sub-TDL can be applied directly. In [63], a TDC using an 8-edge WU signal was proposed; however, the encoding process becomes much more challenging. Therefore, the sub-TDL should be modified when using more edges to improve the performance further.

2.4. Compensation Strategies

To improve linearity, a fast calibration approach, called the bin compensation strategy, was demonstrated in [55]. The bin width compensation aims to compensate the bins with a negligible bin width. In this compensation strategy, two factors, the main bin calibration factor (BCF_m, highlighted in black arrow in Figure 7) and the compensation bin calibration factor (BCF_c, highlighted in red arrow in Figure 7), are introduced to reassign the TDC's fine codes to corrected bins. The addresses of corrected bins can be calculated based on code density tests. $T[k]$ can be defined as:

$$T[k] = \sum_{n=0}^{k-1} W[n] = \sum_{n=0}^{k-1} \{LSB \times (DNL[n] + 1)\}, \tag{4}$$

where $W[n]$ is the width of the *n*-th bin. BCF_m and BCF_c are calculated accordingly. For example, the uneven Bin_{actual} *N-2* collects a larger count proportional to its bin width in a code density test, and therefore it is necessary to assign a proportion of the count to Bin_{ideal} *N-1* through BCF_c. This compensation strategy works well if the bin boundaries do not deviate too much from the ideal bin boundaries (highlighted in dash line). As each bin only has at most one BCF_m and one BCF_c, this compensation method makes Bin_{ideal} *N+1* receiving no count allocation (due to the existence of the ultra-wide Bin_{actual} *N+1*, as Bin_{actual} *N+1* has already assigned its contribution to Bin_{ideal} *N+2* and *N+3*) and therefore resulting in a missing code. The compensation process can be simplified as the pseudocode below, according to [55].

```
For k = 1: N
if (Tactual [k] < Tideal [k])
if (Tactual [k+1] < Tideal [k])
      BCFm = k − 1
      BCFc = void
else if (Tactual [k+1] > Tideal [k])
      BCFm = k − 1
      BCFc =k
else
      continue…
```

This method can remap and compensate bins at the same time without changing the resolution. A few missing codes can be ignored with a degraded resolution. Much severer missing code problems, however, degrade the INL and the TDC performance significantly, especially for the two-stage TDCs in [43,64]. A new compensation method still needs to be developed. We will propose a straightforward approach in this study, see Section 2.6.

Table 1 summarizes the linearity performances for the original WU design and the compensated WU design. Figure 8 presents the linearity performances of the original WU TDC and the compensated WU TDC. After compensation, small width bins have been corrected. The DNL is [-0.92, 1.75] LSB, and the INL is [-1.20, 5.97] LSB.
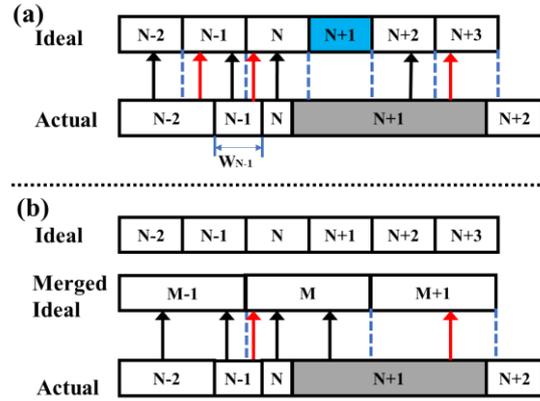
Figure 7. Concepts of (a) the compensation strategy and (b) the binning method.
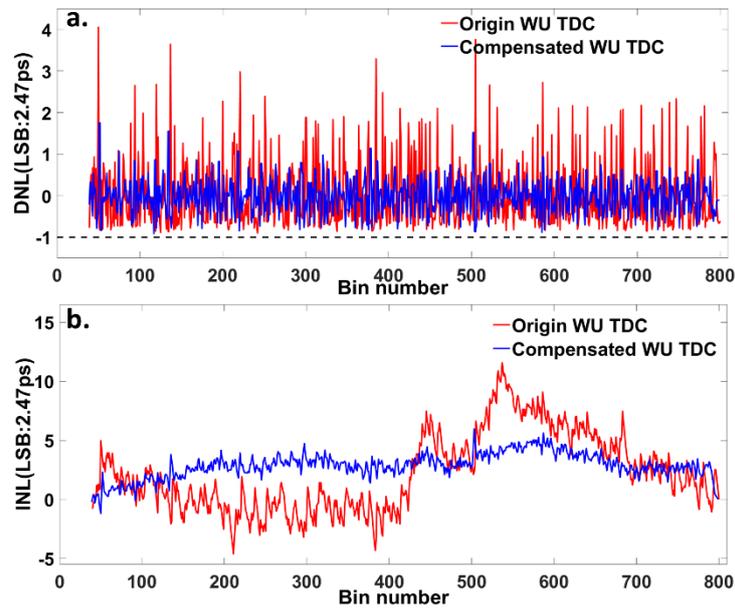
Figure 8. DNL and INL performances. (a) DNL and (b) INL plots of the original WU TDC and the compensated WU TDC in the UltraScale FPGA.

Table 1. Linearity Performance Between Original WU TDC and Compensated WU TDC

	UltraScale (20 nm)	
	Original WU TDC	Compensated WU TDC
LSB	2.47 ps	
DNL	[-0.90, 4.06]	**[-0.92, 1.75]**
DNL_{pk-pk}	4.96	**2.67**
σ_{DNL}	0.82	**0.43**
INL	[-4.62, 11.58]	**[-1.20, 5.97]**
INL_{pk-pk}	16.20	**7.17**
σ_{INL}	3.26	**1.06**

2.5. Dual-sampling Wave Union TDC

As shown in Figure 1 in the DS method, the CARRY8 module doubles the number of sampled taps, compared with traditional FPGA structures. As shown in Figure 4, the WU method samples the

TDL taps twice, equivalently doubling sampled taps. Therefore, to achieve a better resolution, a TDC combining both, denoted as DSWU TDC, was also implemented in this study.

Figure 1(a) also shows the block diagram for this DSWU TDC, and the sub-TDL structure was adopted in this TDC. The DSWU TDC can achieve 1.23 ps resolution. The linearity, however, degrades when the resolution is improved.

2.6. Binned Dual-sampling Wave Union TDC

Considering the linearity performance of the DSWU TDC, a binning method can be applied to improve the linearity. It is inspired by the compensation strategy and the bin decimation method in [32]. As shown in Figure 7(b), a set of merged ideal bins are constructed by merging two consecutive bins into larger bins. Then the compensation strategy can be used to improve the linearity, even when a new bin is still small. The central concept is to reduce the numbers of ultra-wide bins and ultra-small bins, hence improving both the DNL and the INL.

3. Experimental Results

To evaluate the performances of the proposed TDCs, (1) code density tests and (2) time interval tests have been conducted. Two independent on-board low-jitter crystal oscillators were used as the signal sources for code density tests. There is no correlation between these two signal sources ensuring the randomness of the hit signal to the TDC clock [54]. Code density tests aim to assess the linearity performances, whereas time interval tests aim to obtain the measurement errors and the root-mean-square (RMS) resolution.

3.1. Linearity Test Results

Parameters like DNL, INL and standard deviations (σ_{DNL} and σ_{INL}) are used to evaluate the linearity of a TDC. Two equations were derived to assess the equivalent bin width and its standard deviation, summarized in [65]:

$$\sigma_{eq}{}^2 = \sum_{i=1}^{N}\left(\frac{W[i]^2}{12} \times \frac{W[i]}{W_{total}}\right) \text{ where } W_{total} = \sum_{i=1}^{N} W[i], \tag{5}$$

$$w_{eq} = \sigma_{eq}\sqrt{12} = \sqrt{\sum_{i=1}^{N}\left(\frac{W[i]^3}{W_{total}}\right)}, \tag{6}$$

where w_{eq} is the equivalent bin width and σ_{eq} is the equivalent bin width standard deviation, which was named differently by other groups, for example, the quantization error σ_Q [66].

Table 1 summarizes the linearity performances of the WU TDC before and after the compensation. With the compensation strategy, the linearity of the WU TDC has been improved. The DNL_{pk-pk} (peak-to-peak DNL) has been enhanced from 4.96 to 2.67 LSB, whereas INL_{pk-pk} has also been improved significantly after the compensation.

The linearity performances of the four proposed TDCs have been summarized in Table 2. Compared with the original WU TDC and the DS TDC, the WU method is still advantageous in easing ultra-wide bin problems. The DNL_{pk-pk} of the original WU TDC is 4.96 LSB, but that of the DS TDC is 5.60 LSB. The compensation strategy is less suitable to be applied to the DS TDC because of the widespread presence of ultra-wide bins.

Figure 9 shows the DNL and INL curves for the DSWU TDC. The resolution of the DSWU TDC is 1.23 ps. However, the linearity degrades when the resolution is improved. The DNL_{pk-pk} is 8.66 LSB and the INL_{pk-pk} is 35.81 LSB.

The DNL and INL curves for the binned DSWU TDC are shown in Figure 10. With the binning method, the DNL is [-0.93, 1.67] LSB and the INL is [-4.13, 2.01] LSB.

The binning method is still advantageous; even the test results indicate that the compensated WU TDC and the binned DSWU TDC have similar performances in the linearity and the resolution. For the compensated WU TDC, the linearity can be improved by correcting the bins with an ultra-small width. The corrections distort the bin widths. However, the binning method can improve the

linearity with less distortion by merging finer bins (LSB: 1.23 ps) into larger bins (LSB: 2.48 ps). Figure 11 presents the bin width distributions of the compensated WU TDC and the binned DSWU TDC; it shows a more concentrated bin width contribution for the binned DSWU TDC. It means the binned DSWU TDC can deliver more robust results. The standard deviations of DNL (σ_{DNL}) of the compensated WU TDC (0.43 LSB) and the binned DSWU TDC (0.35 LSB) also support this statement.

Table 2. Comparison of The Linearity Performances Between Four Different TDC Designs

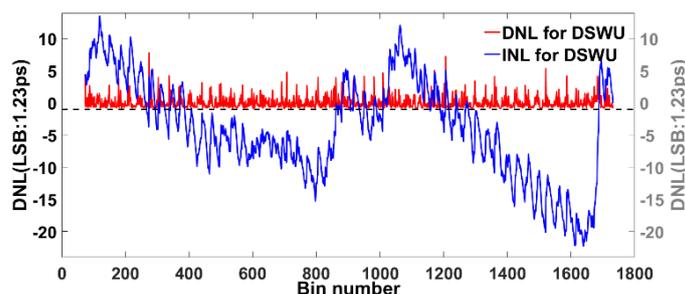|	UltraScale (20 nm)			
	Compensated WU	DS	DSWU	Binned DSWU
LSB (ps)	2.47	2.53	1.23	2.48
DNL	[-0.92, 1.75]	[-0.99, 4.61]	[-0.85, 7.81]	[-0.93, 1.67]
DNL_{pk-pk}	2.67	5.6	8.66	2.60
σ_{DNL}	0.43	1.06	0.92	0.35
INL	[-1.20, 5.97]	[-3.79, 13.69]	[-22.28, 13.53]	[-4.13, 2.01]
INL_{pk-pk}	7.17	17.48	35.81	6.14
σ_{INL}	1.06	3.51	7.65	1.18
w_{eq} (ps)	2.99	6.39	2.92	2.95
σ_{eq} (ps)	0.86	1.84	0.84	0.85

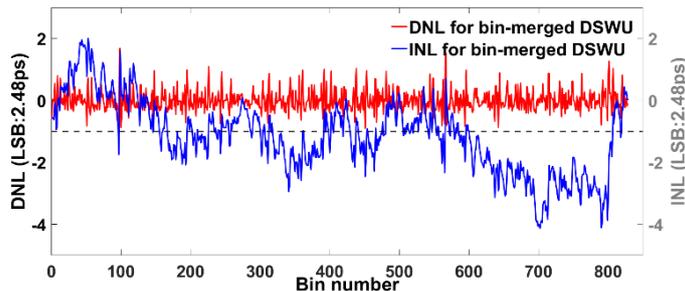**Figure 9.** DNL and INL curves for the DSWU TDC.

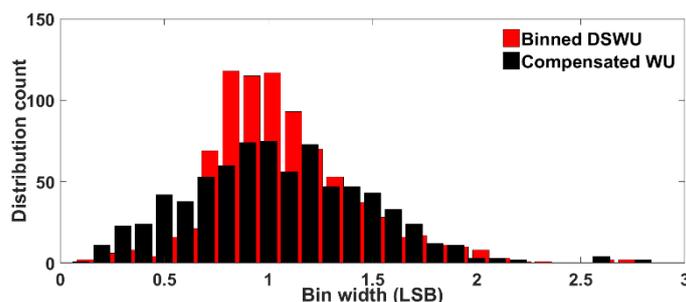**Figure 10.** DNL and INL curves for the binned DSWU TDC.

Figure 11. Bin width distributions for the compensated WU TDC and the binned DSWU TDC.

3.2. Time Interval Measurements

The precision can be estimated by the standard deviation of the distribution of repeated measurements, and it can be affected by clock jitters, jitters of input signals, electronic noise and process, voltage and temperature (PVT) variations [67]. According to [68], the precision of the whole TDC system in our case can be expressed as:

$$\sigma_{system}^2 = \sigma_{start}^2 + \sigma_{INL}^2 + \sigma_{qav}^2 + \sigma_{extra}^2, \tag{7}$$

where σ_{start} is the start signal jitter, σ_{INL} is the integral nonlinearity standard deviation, σ_{qav} is the average quantization error, and σ_{extra} represents internal jitter introduced by the FPGA device.

The delay element, IODELAYE3, was used to generate a delay with a controllable time interval between the delayed signal and the original signal. The time interval was measured by the proposed TDC and an oscilloscope, Teledyne LeCroy WaveRunner 640Z. The temperature of the testing environment was maintained, and an IDELAYCTRL module was introduced to reduce the impact of PVT variations. The step of the controllable time intervals was set to be 9.41 ps. Measurements were repeated 50,000 times for a fixed time interval.

The measurement error (E) is the difference between the measured value and the actual value. The measurement errors for the four TDC systems are shown in Figure 12 and Figure 13. These results were obtained from the time interval tests. The average measurement errors are around 5 ps for the proposed four TDC systems. Figure 14 contains the RMS resolutions for four TDC systems with the jitters from IODELAYE3 also included. The RMS resolution for the DS TDC system is 5.74 ps with $\sigma_{RMS} = 1.09$ ps. The RMS resolution for the WU TDC system is 5.95 ps with $\sigma_{RMS} = 0.77$ ps. The DSWU TDC system achieves an RMS resolution of 5.69 ps with $\sigma_{RMS} = 1.05$ ps. The binned DSWU TDC system reaches an RMS resolution of 5.89 ps with $\sigma_{RMS} = 0.46$ ps.
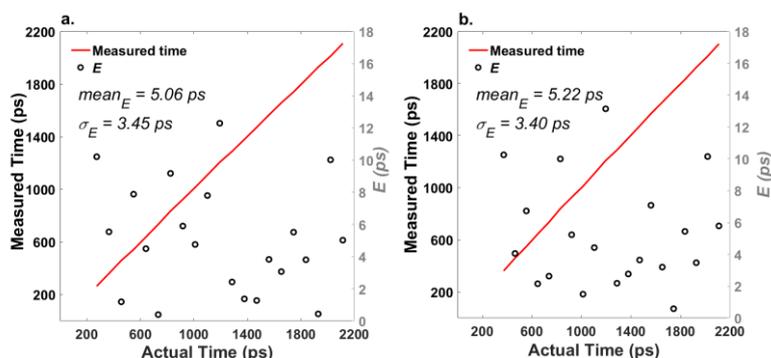

Figure 12. Measurement errors obtained from the time interval tests for (a) the WU TDC system and (b) the DS TDC system.
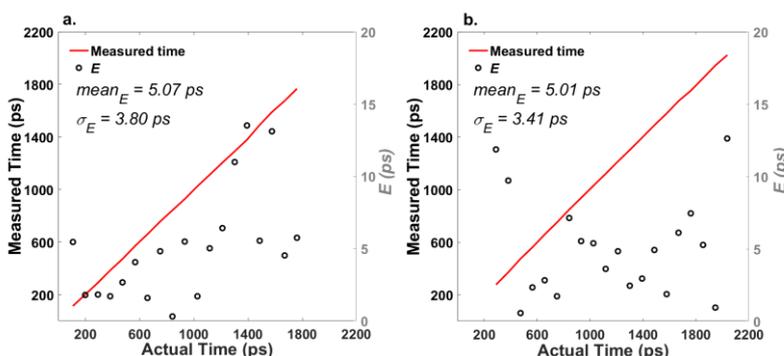

Figure 13. Measurement errors obtained from the time interval tests for (a) the DSWU TDC system and (b) the binned DSWU TDC system.
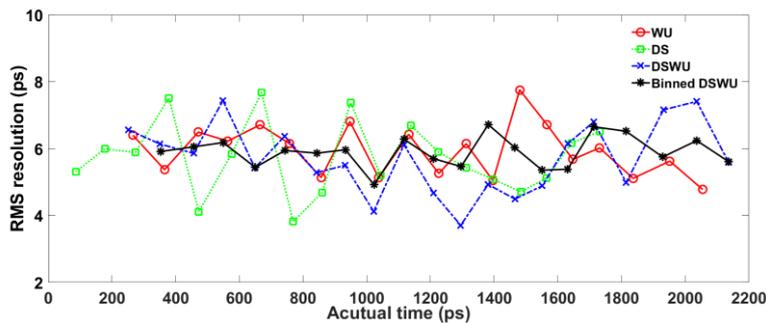
Figure 14. RMS resolutions obtained by the time interval tests for four TDC systems (jitters from IODELAY3 and the clock signal are included).

3.3. Analysis of Measurement Uncertainties

Szplet *et al.* proposed another way to estimate measurement uncertainties by analyzing error sources for two-stage multi-phase TDC [68]. Their analysis approach can be extended for our single-stage TDCs with or without the wave union launcher, and the RMS resolution can be expressed as:

$$\sigma_{system}^2 = \sigma_{sig}^2 + \sigma_{eq}^2 + \sigma_{clk}^2, \tag{8}$$

In Equation (8), σ_{sig} is denoted as the total jitter when a signal transmits through the delay lines and can be calculated as:

$$\sigma_{sig}^2 = \sigma_{wu}^2 + \sigma_{DL}^2, \tag{9}$$

where σ_{wu} is the jitter caused by the wave union launcher and several delay elements in the tapped delay line (σ_{DL}) are involved. For the wave union launcher, it is constructed by a LUT and a CARRY8. And in each CARRY8, there are eight delay elements (σ_{CY}). Therefore, σ_{wu} can be expressed:

$$\sigma_{wu}^2 = 8\sigma_{CY}^2 + \sigma_{LUT}^2, \tag{10}$$

It is difficult to predict how many delay elements of the TDL are involved in measurements. However, according to [68], for a TDL with n delay elements, σ_{DL} can be expressed by its expected value:

$$\begin{aligned} \mathrm{E}[\sigma_{DL}^2] &= \sum_{i=1}^{n} \sigma_{DLi}^2 \cdot p(\sigma_{DLi}^2) = \sum_{i=1}^{n} i \cdot \sigma_{CY}^2 \cdot p(\sigma_{CY}^2) \\ &= \sum_{i=1}^{n} i \cdot \sigma_{CY}^2 / n = (\sigma_{CY}^2/n) \sum_{i=1}^{n} i \\ &= \frac{n+1}{2} \sigma_{CY}^2 \approx \frac{n}{2} \sigma_{CY}^2, \end{aligned} \tag{11}$$

where σ_{DL_i} is the jitter caused by i-th delay element and the i-th delay element has the probability $p(\sigma_{DLi}^2)$ of hitting during a signal measurement. Because the delay element used in our cases is CARRY8, $\sigma_{DL_i}^2 = i\sigma_{CY}^2$ and $p(\sigma_{DLi}^2) = p(\sigma_{CY}^2)$. From Equations (8)–(11), the RMS resolution can be expressed as:

$$\sigma_{system}^2 = \sigma_{clk}^2 + \sigma_{eq}^2 + \sigma_{LUT}^2 + \left(\frac{n}{2} + 8\right)\sigma_{CY}^2, \tag{12}$$

To obtain an estimated value of σ_{LUT} and σ_{CY}, a ring oscillator (RO) has been constructed, as shown in Figure 15. There are m delay elements in this RO, and the jitter in this RO can be expressed as:

$$\sigma_{RO}^2 = \sigma_{LUT}^2 + m\sigma_{CY}^2, \tag{13}$$

The measured results, as shown in Figure 16, show that $\sigma_{CY} = 0.16$ ps and $\sigma_{LUT} = 1.45$ ps. The four proposed TDCs share similar architectures, and there is no wave union launcher in the DS TDC, so $\sigma_{sig} = 2.91$ ps (for WU, DSWU and binned DSWU TDCs) and $\sigma_{sig} = 2.51$ ps (for DS TDC).

The clock signal was generated by a clock generator (Si5335A, Silicon Labs) and an MMCM (Mixed-mode Clock Manager) module. Measured by the oscilloscope, the jitter caused by the clock signal (σ_{clk}) is 4.42 ps. Considering the relatively large clock jitter, we introduced σ_{TDC} to evaluate the RMS resolution of the TDC and it can be expressed as Equation (14). And the measurement uncertainties of four proposed TDCs have been summarized in Table 3. Table 3 also compares our analysis with two previously published works in 45 nm and 20 nm FPGAs with our analysis providing more detailed contributions from the error sources.

$$\sigma_{TDC}^2 = \sigma_{sig}^2 + \sigma_{eq}^2, \tag{14}$$

Table 3. Evaluation of Measurement Uncertainties

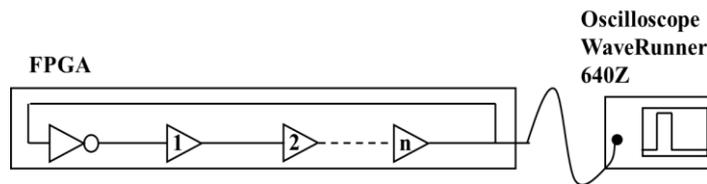|	Spartan-6 (45 nm)	UltraScale (20 nm)				
	[68]-2019	[55]-2019	Compensated WU	DS	DSWU	Binned DSWU
LSB (ps)	-	5.02	2.47	2.53	1.23	2.48
Error Source Analysis						
σ_{clk} (ps)	1.93	-	4.42			
σ_{CY} (ps)	0.153	-	0.16			
σ_{LUT} (ps)	1.33	-	1.45			
σ_{sig} (ps)	-	-	2.91	2.51	2.91	2.91
σ_{eq} (ps)	-	1.45	0.86	1.84	0.84	0.85
$\boldsymbol{\sigma_{TDC}}$ (ps)	-	-	3.03	3.11	3.02	3.03
σ_{system} (ps)	10.19	-	5.36	5.41	5.36	5.36
Time Interval Test						
σ_{system} (ps)	-	7.8	5.95	5.74	5.69	5.89

Figure 15.   Test setup for investigating jitters of LUT and the delay element.
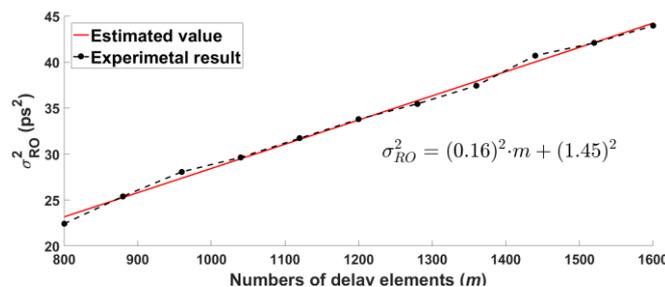

Figure 16.   Test results for investigating jitters of LUT and the delay element.

Table 4. Consumption of Logic Resources

Modules	Total	w/o WU Used	WU Used	DS Used	DSWU/ Binned DSWU Used
CARRY8	30300	80 (0.26%)	85 (0.28%)	76 (0.25%)	88 (0.29%)
LUTs	242400	703 (0.29%)	1349 (0.56%)	1272 (0.52%)	2460 (1.01%)
FFs	484800	1195 (0.24%)	1840 (0.38%)	2190 (0.45%)	3463 (0.71%)
BRAM	600	1.5 (0.25%)	4.5 (0.75%)	3.5 (0.58%)	7.5 (1.25%)
CLB	30300	271(0.89%)	359(1.18%)	283(0.94%)	529(1.75%)
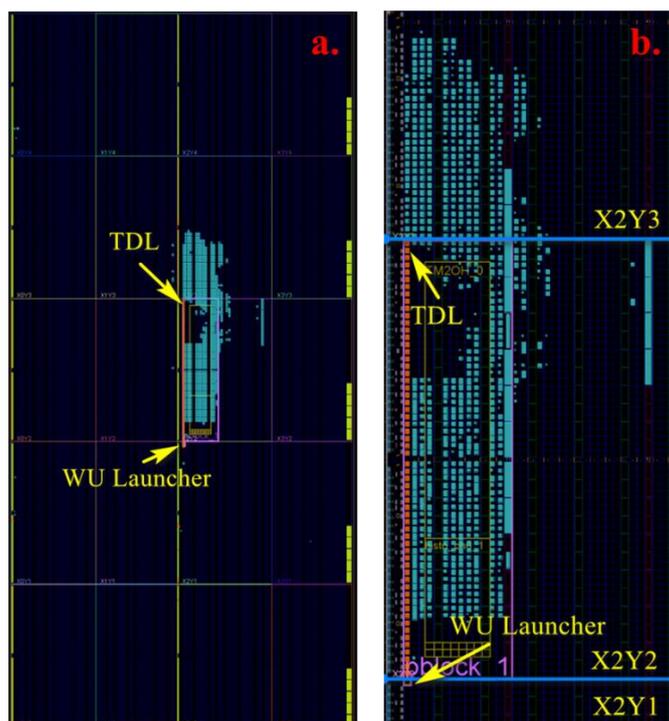
Figure 17. Implementation layouts of the DSWU TDC. a) Overview. b) Clock regions (X2Y1 ~ X2Y3)

3.4. Resource Consumption

The consumptions of logic resources for the proposed TDCs were calculated by the EDA tools and are shown in Table 4. Extra logic resources were used when using the WU method and the DS structure (more block RAM needed to perform the histogram functions). However, the usages of logic resources for proposed TDCs are still low, showing great potential for multiple-channel applications.

The implementation layouts of the DSWU TDC are shown in Figure 17. The overview is shown in Figure 17(a), and the layout of clock regions (X2Y1~X2Y3) is shown in Figure 17(b). The layouts were obtained from the Vivado suite. To reduce the large nonlinearity contributed by the clock tree distribution, the TDL is confined in 60 logic cells within a central clock region (Slice X49Y120~X49Y179). The WU launcher is confined in Slice X49Y119. These constraints are also applicable to the WU TDC and the binned DSWU TDC. For the DS TDC, the constraints for the WU launcher are not required. Figure 17 shows that the layout does not consume much hardware resources, and therefore the proposed TDCs are suitable for multichannel applications. If a longer measurement range is required, coarse counters can be easily included for the proposed TDCs.

Table 5. Comparison of Published FPGA-based TDCs and the Proposed TDCs

Ref - Year	Methods	Device	LSB (ps)	RMS Resol. (ps)	DNL, DNL_{pk-pk} (LSB)	INL, INL_{pk-pk} (LSB)	Power (mW)
[69]-13*	Multichannel, TDL	Virtex-5	30.00	15.00	[-1.00, 3.00], 4.00	[-4.00, 4.00], 8.00	N/S
[70]-13*	Multichannel, TDL	Virtex-6	10.00	18.50	[-1.00, 1.50], 2.50	[-2.25, 1.61], 3.86	N/S
[71]-14*	Multichannel, TDL	Kintex-7	22.70	N/S	N/S, 2.60	N/S, 3.40	N/S
[53]-14*	WU-A, TDL	Cyclone II	20.00	21.00	N/S	N/S	N/S
[58]-15*	WU-A, multichannel, TDL	Kintex-7	N/S	< 10.00	N/S	N/S	N/S
[39]-15*	Multichain averaging, TDL	Virtex-6	1.50 M=16	4.20 M=16	[-0.70, 0.80], 1.50 (M=8, LSB=24ps)	[-1.00, 0.70], 1.70 (M=8, LSB=24ps)	N/S
[44]-16*	Dual-phase, TDL	Virtex-6	10.00	12.80	[-1.00, 1.91], 2.91	[-2.20, 3.93], 6.13	N/S
[72]-16*	WU-A, multichain, 2-stage interpolation, TDL	Spartan-6	0.90	< 6.00	[-1.00, 6.25] [1]	[-26.20, 11.50], 37.70	N/S
[34]-16*	Tuning-TDL, heterogenous sampling	Kintex-7 Virtex-6 Spartan-6	10.6 10.1 16.7	N/S N/S N/S	[-1.00, 1.45], 2.45 [-1.00, 1.18], 2.18 [-1.00, 1.22], 2.22	[-1.23, 4.30], 5.53 [-3.03, 2.46], 5.49 [-0.70, 2.56], 3.26	N/S
[36]-16*	Dual sampling	Ultra-Scale	2.25	3.90	[-1.00, 4.78] [1]	N/S	N/S
[73]-17*	Tuned-TDL	Virtex-7	10.5	N/S	[-0.38, 0.87], 1.25	[-1.23, 1.02], 2.25	N/S
[74]-17*	Multichain, TDL	Virtex-7	1.15	3.50	[-0.98, 3.50], 4.48	[-5.90, 3.10], 9.00	N/S
[45]-18*	Multi-phase	Cyclone V	1.56	2.30	[-1.00, 5.60] [1]	[-8.00. 35.00] [1]	N/S
[55]-19*	Multichannel, sub-TDL	Ultra-Scale	5.02	7.80	[-0.12, 0.11], 0.27	[-0.18, 0.46], 0.59	N/S
[75]-19*	Super-WU, multichannel	Artix-7	2.00	< 12.50	N/S	N/S, 2.10	< 10
[63]-19*	WU-A, TDL	Kintex-7	1.77	3.00	[-1.00, 4.50] [1]	[-37.70, 12.00] [1]	< 1.02

Table 5. (*Continued.*) Comparison of Published FPGA-based TDCs and the Proposed TDCs

This Work [▲]	**1) Sub-TDL, compensation, WU-A**		2.47	5.95 [2], 3.03 [3]	[-0.92, 1.75], 2.67	[-1.20, 5.97], 7.17	0.92
	2) Sub-TDL, dual sampling		2.53	5.74 [2], 3.11 [3]	[-0.99, 4.61], 5.60	[-3.79, 13.69], 17.48	0.88
	3) Sub-TDL, dual sampling, WU-A	Ultra-Scale	1.23	5.69 [2], 3.02 [3]	[-0.85, 7.81], 8.66	[-22.28, 13.53], 35.81	1.03
	4) Sub-TDL, dual sampling, WU-A, binning		2.48	5.89 [2], 3.03 [3]	[-0.93, 1.67], 2.60	[-4.13, 2.01], 6.14	1.03

[1] Approximate values from the figures; [2] Data obtained from time interval tests; [3] Data obtained from the analysis of measurement uncertainties; * Modelling method unknown; ▲ Modelled with Verilog HDL.

3.5. Discussions

We used Verilog hardware description language to model the proposed TDCs. VHDL can also be used to build a TDC. However, most TDCs are built with cell primitives provided by FPGA manufactures [30]. The cell primitives are intrinsic to the target architecture and cannot be changed by the modelling methods and EDA tools [76,77]. With cell primitives, redundant logic resource consumption can be avoided.

Table 5 summarizes the key parameters of the proposed TDCs against other recently proposed advanced TDCs. The power consumptions of the proposed TDCs were estimated by Vivado Design Suite, and the results show that the proposed TDCs have comparable performances in power consumption, compared with some earlier TDCs [63,75]. Thanks to recent advances in CMOS manufacturing technologies and research in TDC architectures, the resolution (LSB) has been significantly improved from 30.00 ps to 0.90 ps. However, there are trade-offs between the resolution and the linearity. The improvements in the linearity are not usually at the same pace as those in the resolution.

Compared with previously published works (the 16-chain TDC design in [39]), the LSB of the DSWU TDC has been significantly improved with acceptable consumption of logic resources. The DSWU TDC also performs better in the linearity and the logic consumption than other previously published TDCs [45,72,74] with a close or similar LSB. In [45,72,74] multi-phase or multi-TDL channels were used, whereas, in our methods, only a single TDL channel was used. Compared with the previously published DS TDC in [36], the sub-TDL structure can remove zero-width bins (see [36] and this work in Table 5) and this feature can be further exploited to improve the TDC performance. Zero-width bins can be ignored when processing the TDC outputs in the TDC in [36], but this degrades the resolution of TDC.

The combination of the WU method with the sub-TDL structure also shows promising results, suitable for multichannel applications.

Experimental results show that the binning method seems an applicable method to improve the linearity and in our study the DNL_{pk-pk} has been enhanced to 2.60 LSB and the INL_{pk-pk} has been improved to 6.14 LSB. If the merged bins are wide enough, a long TDL can be constructed regardless of the large clock skews. Note that the binning method shows great potential for some LiDAR systems that require an acceptable resolution (~50 ps) with high linearity [78].

The estimation of precision becomes a challenging issue when the resolution is close to 1 ps. The experimental RMS resolution can be affected by the experimental devices, such as the clock generator and the oscilloscope. The precision can also be obtained by analyzing the error sources. For a TDC design, once the general architecture (σ_{sig}) has been fixed, the equivalent standard deviation of the bin widths (σ_{eq} or the quantization error σ_Q defined in [66]) will be the only factor that varies when different methods are implemented. From Table 3, both the WU TDC and DSWU TDC can reduce σ_{eq} by improving the resolution. For the binned DSWU TDC, σ_{eq} is still low, because its linearity has been improved significantly with a loss in the resolution (LSB: from 1.23 ps to 2.48 ps). Therefore, these TDCs achieve similar precision. In our study, the measurement uncertainties of the four proposed TDCs (σ_{TDC}: ~3 ps) are mainly contributed by architecture-dependent jitters σ_{sig} (σ_{sig} = 2.51 ps for the DS without the wave union launcher and σ_{sig} = 2.91 ps for the WU, DSWU and binned DSWU TDCs). By analyzing the error sources, we can conclude that the precisions of the proposed WU-related TDCs (σ_{eq} ~ 0.85 ps) reach the upper limit of their architectures, and the precision of DS TDC, however, can still be further improved with σ_{eq} = 1.84 ps.

From Table 3, σ_{system} obtained from time interval tests is slightly larger than that obtained through the detailed analysis of measurement uncertainties. It indicates that the IODELAY module could introduce extra jitter to the tested systems.

The potential for a multichannel TDC design is essential for broader applications. Compared with recently published works, the proposed TDCs are efficient in the consumption of logic resources. A 7.4 ps TDC was proposed in [79] claiming to consume low logic resources. Their solution, however, was not without a price, as the routing resources were used as the delay elements. Even the consumption of logic elements was low; it still needed to use a large logic area to constraint the

routing paths: 1024 configurable logic blocks (CLBs) [79]. In comparison with this design, the proposed TDCs use a smaller logic area (shown in Table 4). Therefore, as high-performance TDCs in UltraScale devices, the proposed TDCs show great potential for multichannel applications due to the low logic resource consumption.

4. Conclusion

In this paper, we proposed and evaluated:
1) Four TDC architectures by integrating the WU method and the DS structure with the sub-TDL topology;
2) The first efficient WU TDC in UltraScale FPGA (Different from the previously reported study [36], we concluded that the WU method is still useful in UltraScale FPGAs when it integrates sub-TDL structures.);
3) A binning method to improve the linearity;
4) Detailed analysis of measurement uncertainties and error sources for the four proposed TDCs.

With the sub-TDL architecture, bubble problems have been significantly alleviated. Meanwhile, the WU method can still be applied to improve the resolution in UltraScale FPGA devices. The compensated method has been used to correct the conversion bias and the deviation of the bin width directly with acceptable logic resources. The DS structure is another way to improve the resolution, although it does not perform better in comparison with the WU method.

By integrating these methods, a TDC with 1.23 ps resolution was also implemented and evaluated. A binning method was implemented to the proposed DSWU TDC to improve the linearity. The binning method can also be implemented with multi-chain design strategies to improve the linearity with an acceptable resolution and be preferable to some LiDAR systems. Latest TDC architectures show limited precision due to device mismatch problems prevailed in advanced manufacturing technologies. For our proposed TDCs, when the tapped delay line method is fixed, the precision can be improved by using a better clock source and by reducing σ_{eq}. However, the accumulated jitters caused by delay elements will mainly contribute to the precision of a TDC.

Our solutions demonstrate comparable improvements in the resolution compared with previously published works, listed in Table 5. Moreover, compared with other published TDCs with high resolution (~1 ps) in [45,72,74], the proposed 1.23 ps resolution TDC requires less hardware. In [45,72,74], the multi-phase or multi-TDL channel was used, whereas in this report, only a single TDL channel was used. With low consumptions of logic resources, the proposed TDCs also show great potential for multichannel applications.

Conflicts of Interest: The authors declare no conflict of interest.

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