DC Fault Management Strategy for Continuous Operation of HVDC Grids based on Customized Hybrid MMC

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***Abstract*—Successful deployment of High-Voltage Direct Current (HVDC) grids necessitates effective DC fault handling strategies, which can minimize the severe consequences caused by DC faults on the AC and DC side of the HVDC grids. Therefore, this paper investigates the enhanced DC fault performance of the Customized Hybrid Modular Multilevel Converter (CH-MMC), in which a limited number of full-bridge sub-modules (FB-SMs) is added into the arms of the conventional MMC in an effort to significantly extend the timespan between fault inception and fault clearance, thus allowing the use of relatively slow and cheaper DC circuit breakers. Based on this converter, a dedicated DC fault handling strategy for CH-MMC based HVDC grids is proposed, which aims to improve the fault resiliency and security of HVDC grids for pole-to-pole faults. Moreover, the proposed DC fault management strategy guarantees the continuous operation of the grid during pole-to-ground DC faults, including full reactive power provision from the converter stations. The performance of the strategy is demonstrated using comprehensive electromagnetic transient (EMT) simulation studies conducted on an illustrative four-terminal meshed HVDC grid, which consider a range of scenarios with different fault current limiting inductors and DC circuit breaker operation times.**

***Index Terms*—DC fault ride-through, DC grid protection, HVDC grids, modular multilevel converter (MMC).**

I. Introduction

HIGH Voltage DC transmission is widely used for integrating offshore wind farms to mainland AC grids and for interconnecting asynchronous AC zones due to its ability for bulk power transmission over very long distances. HVDC grids are considered as the natural evolution of existing point-to-point transmission links that enable the integration and better utilization of massive amounts of offshore energy. Moreover, they offer a plethora of attractive features such as: enhanced controllability, flexibility and redundancy, improved reliability and security, lower investment costs, etc [1].

As with any developing technology, the HVDC grid concept has its challenges, with the requirement for sufficient DC fault ride-through capability being the most prominent. When a DC short-circuit fault occurs in a HVDC grid, distributed cell capacitors of the commonly used Half-Bridge MMC (HB-MMC) tend to contribute currents to the DC fault prior converter blocking, while further current stresses are induced on the converter semiconductor devices by the additional distributed capacitors of the DC lines [2]. Moreover, pole-to-ground DC faults can cause severe voltage stress on insulation of the non-faulted DC pole of a symmetrical monopole transmission line, and expose converter transformers to significant DC offsets.

Fault management strategies for HVDC grids primarily rely on the use of AC circuit breakers (ACCBs), DC circuit breakers (DCCBs) or fault blocking converters. The use of ACCBs for fault clearance in HVDC grids is an economic and simple approach, which has been discussed in [3], [4], where the AC grid fault current contributions are eliminated using ACCBs. Subsequently, when DC fault currents drop to zero, fast disconnectors are used to isolate the faulty DC line/cable. Nevertheless, these approaches lead to de-energization of the DC grid and the post-fault recovery process may take several hundreds of milliseconds, which is not suitable for critical power corridors.

The second option is to incorporate fast acting DCCBs at all line ends of the HVDC grid. Several hybrid DCCBs have been developed, which can interrupt fault currents within 2-3 ms [5], [6]. Moreover, the use of sizeable DC inductors has been proposed as one of the viable measures for slowing the rate of rise of DC fault currents and to facilitate fault interruption before the fault current exceeds the DCCB breaking capacity [7], [8]. The use of hybrid DCCBs in conjunction with DC fault detection and discrimination methods has been extensively investigated for fast and selective isolation of the faulted line [9]–[12]. In addition, coordination of the HB-MMC with hybrid DCBBs has been proposed in [13], [14], where the Half-Bridge Sub-modules (HB-SMs) are immediately bypassed after DC fault detection in an effort to suppress the DC fault current and support the DCCBs. The main shortcoming of the above solutions is that hybrid DCCBs require designs with large footprint and high capital cost. Alternatively, mechanical DC circuit breakers can be used for fault isolation in HVDC grids at the expense of increased breaking speed but larger DC inductors are required [15], [16].

An alternative method for addressing HVDC grid vulnerability to DC faults is to use converters with fault current blocking capabilities, such as the Full-Bridge MMC (FB-MMC) [17], [18]. Unlike the HB-SMs, Full-Bridge Sub-modules (FB-SMs) can recreate any DC voltage the DC fault may present at its DC terminal if the bipolar capability of the FB-SM is fully exploited; thus, providing greater controllability during DC faults.

Fault management strategies for multi-terminal HVDC grids

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based on FB-MMCs have been developed using mechanical DCCBs [18], [19], or fast disconnectors [20]. Both strategies can control fault currents and facilitate continuous operation with limited periods of power interruption.

Moreover, the conventional Hybrid MMC (H-MMC) that employs equal number of HB-SMs and FB-SMs in each arm, has been proposed to offer improved DC fault ride-through capability at reduced semiconductor losses than the FB-MMC [21]. Other hybrid topologies with similar functionality, which combine HB-SMs with FB-SMs or other SM types have also been proposed [22]–[24]. A fault management strategy based on the H-MMC for HVDC grids has been proposed in [25], which explores the capability to control either the converter current or the line current to clear the DC fault with limited power interruption. Despite the fault current limitation capability, the increased investment and operational costs, and the higher conduction losses cannot justify the additional functionalities offered by the FB-MMC and H-MMC.

To achieve an adequate and cost-effective solution for improved security of supply in hybrid AC/DC grids, an alternative approach that relies on converters with partial DC fault tolerant capability and less expensive DCCBs is required [26]. Therefore, this paper proposes a fault management strategy for handling DC faults in HVDC grids using the bespoke design of the Customized H-MMC (CH-MMC), in which the number of FB-SMs represents 25% of the total converter SMs, a ratio which is selected for the desired level of resiliency against pole-to-pole DC faults and for relaxed operational speed and current breaking capacity of mechanical DC circuit breakers. The CH-MMC uses its FB chain-links to present opposing and increasing counter-voltages, which tend to suppress the AC side, arm and DC side currents at the expense of increased SM capacitor voltages. It has been found that the 25% ratio is sufficient to block half of the nominal DC voltage thus, enabling the strategy to achieve continuous HVDC grid operation during pole-to-ground (P2G) faults, in which full controllability of the converters is maintained. For pole-to-pole (P2P) faults, the proposed strategy can significantly improve the DC fault survival of HVDC grids. The main contributions of this paper are the following:

- Development of a DC fault management strategy (FMS) for HVDC grids that employ CH-MMCs with partial fault tolerant capability in order to extend the time frame for DC fault clearance to levels compatible with mechanical DCCB operation times. This is achieved through the substantial suppression of the arm, AC and DC side fault currents, leading to further reduction in the maximum current breaking capacity of the DCCBs. The relaxation of DCCB requirements indicates that less expensive DCCBs can be utilized as a result of the proposed strategy.
- Through quantitative studies and qualitative discussions, it has been shown that the CH-MMC leads to enhanced station and system wide performance. The CH-MMC with 25% ratio provides practical trade-offs that prioritize extension of fault clearance and high converter efficiency. At the same time the over-currents and over-voltages exerted on the semiconductor switches and SM capacitors as a result of P2P DC faults remain within tolerable levels.
- Rigorous simulation studies on an illustrative meshed HVDC grid, with detailed converter control and protection systems included, confirm the suitability of the proposed FMS in handling P2G and P2P DC faults.

The rest of the paper is organized as follows: Fundamentals of the CH-MMC under investigation and its associated control systems are described in section II. Section III presents the HVDC grid that is used in Section IV to explore the fault management strategy for CH-MMC based HVDC grids and to conduct extensive simulation studies in Section V. Section VI provides further insight into the results and finally, conclusions are drawn in section VII.

II. Customized Hybrid Modular Multilevel Converter

A. Fundamentals and Circuit Topology

Fig. 1 shows a generic diagram of the CH-MMC topology with asymmetrical ratio of FB-SMs and HB-SMs, in which N_{HB} and N_{FB} is the number of HB-SMs and FB-SMs per arm, respectively. The ratio of N_{FB} to the total number of SMs per arm, N, is denoted as R and is defined as

$$R = \frac{N_{FB}}{N} = \frac{N_{FB}}{N_{FB} + N_{HB}} \tag{1}$$

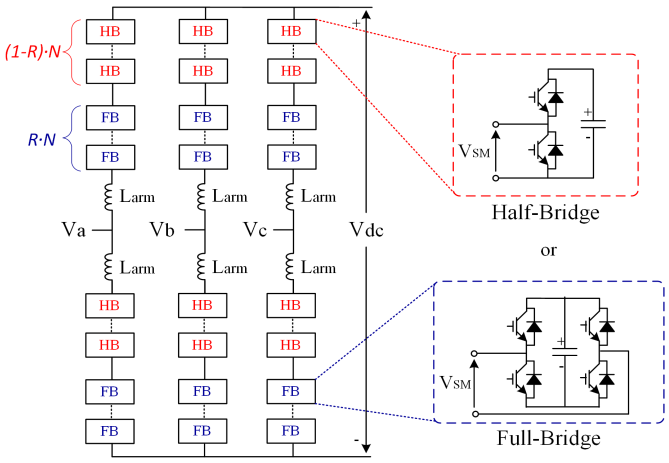


Fig. 1. Structure of the CH-MMC topology.

Theoretically, in the CH-MMC, the ratio R could be set anywhere between 0 and 1. Nevertheless, the proposed bespoke design of the CH-MMC uses limited number of FB-SMs incorporated in its arms to extend the controllable range of DC voltage, benefiting from the combined negative voltage capabilities of the FB chain-links beyond that of the the conventional HB-MMC. In this paper, R=0.25 which is equivalent to 25%, is found to be beneficial for reasons that will be elaborated later. The HB and FB-SM capacitors are designed to have the same rated voltage V_{SM} as shown by

$$V_{SM} = \frac{V_{DC}}{N} = \frac{V_{HB}}{N_{HB}} = \frac{V_{FB}}{N_{FB}} \tag{2}$$

where V_{DC} is the rated pole-to-pole DC voltage and V_{HB}, V_{FB} are the blocking voltages of HB and FB chainlinks, respectively. For ease of explanation in the rest of the section, subscript j is the phase index (i.e. $j = a, b, c$) and k refers to

upper and lower arm (i.e. $k = u$ for the upper arm and $k = l$ for the lower arm). Taking the upper arm as an example, the arm voltage for any phase j of the CH-MMC is given by

$$V_{j,u}(t) = \frac{1}{2} V_{DC} \cdot (M_{AC} cos(\omega t + \delta_j) + m_{DC}) \tag{3}$$

where M_{AC} and m_{DC} are the AC and DC modulation index, respectively. The component M_{AC} is related to the magnitude of fundamental AC voltage and it varies in the range $0 < M_{AC} < 1$. The m_{DC} component reflects the extent at which the customized hybrid MMC can achieve operation over a wide range of DC voltages, exploiting the bipolar output voltages of the FB-SMs. The minimum value of the DC modulation index depends on R and is given by

$$m_{DC-min} = 1 - 2 \cdot R \tag{4}$$

The DC voltage range for which the CH-MMC retains controllability is

$$1 \geq V_{DC}^{pu} \geq 1 - 2 \cdot R \tag{5}$$

B. Converter Control

Fig. 2 shows the control system of the CH-MMC with asymmetrical blocking voltages of the HB and FB chainlinks. The control system consists of DC voltage or active power, and AC voltage or reactive power controllers in the outer loops along the d and q axes. The standard vector control is employed in the inner current loops that regulate positive and negative sequence currents, and define the AC components of the modulation functions of the arms. Nearest level modulation is used to generate the IGBT firing signals [27].

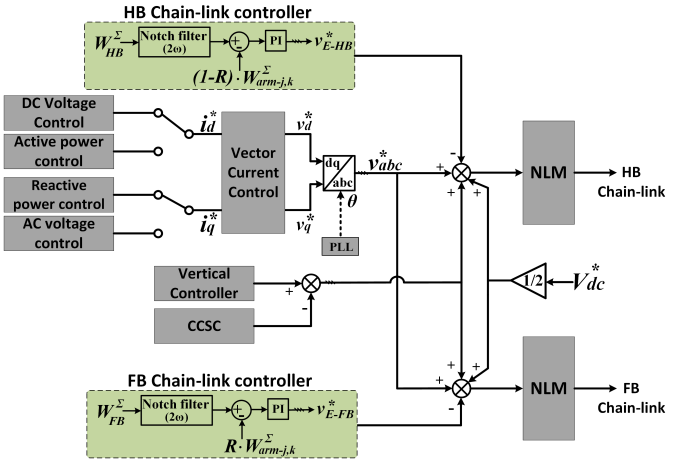


Fig. 2. Control system of the CH-MMC.

The employed per phase circulating current suppression controllers (CCSC) modify the modulation index in an effort to suppress the second-order current harmonics from the converter arms [27], [28]. These controllers dominantly inject small second-order harmonic components into the modulation functions of the phase-legs to suppress the circulating currents, which largely contain second-order harmonic currents.

The horizontal and vertical energy balancing controllers modify the DC and AC components of the modulation functions for the HB and FB chain-links. The conventional implementation of vertical energy controller that ensures the upper and lower arms of each phase-leg have the same total average capacitor voltage is adopted [28]. The per phase horizontal energy controllers ensure that all three phase-legs have the same mean DC voltage to prevent DC circulating currents between the phase-legs.

In CH-MMC with asymmetrical ratio of HBs and FBs (e.g. 75% HB-SMs and 25% FB-SMs), explicit horizontal energy controllers are required to ensure correct voltage or energy sharing between the FB and HB chain-link of each arm. These controllers primarily introduce a small DC component into the modulation function of the HB and FB chain-link of each arm. Typically, the set-point for the per phase horizontal controller defines the total arm blocking voltage or energy. Fundamentally, the necessary condition for SM capacitor voltage balancing is that the energy exchange between the SM capacitors of the HB and FB chain-links, and both chain-links with the AC side, must be zero as described in (6) and (7).

$$E_{HB_{j,k}} = \int_0^T \left(m_{HB} \cdot i_{arm_{j,k}}(t) \right) dt = 0 \tag{6}$$

$$E_{FB_{j,k}} = \int_0^T \left(m_{FB} \cdot i_{arm_{j,k}}(t) \right) dt = 0 \tag{7}$$

The DC offset of the modulating signal m_{HB} and m_{FB} of the HB and FB chain-link is manipulated in order to ensure that the HB and FB chain-links exchange zero net energy or active power with the AC side. Modulation index m_{HB} and m_{FB} are adjusted according to the SM energy as shown in (8) and (9).

$$W_{HB_{j,k}} = \frac{1}{N_{HB}} \sum_{n=1}^{N_{HB}} \frac{C_{SM-HB} \cdot u_{SM_{HB_{j,k}}}^2}{2} \tag{8}$$

$$W_{FB_{j,k}} = \frac{1}{N_{FB}} \sum_{n=1}^{N_{FB}} \frac{C_{SM-FB} \cdot u_{SM_{FB_{j,k}}}^2}{2} \tag{9}$$

III. HVDC Grid Topology

The meshed HVDC grid illustrated in Fig. 3 will be used to assess the performance of the proposed fault management strategy when CH-MMCs are used. The test system is modelled with the PSCAD/EMTDC simulation tool. All converters are modelled as CH-MMCs with asymmetrical ratio of FB-SMs to total number of sub-modules, which can be set to an arbitrary value (between 0% and 100%). All converters are modelled based on extensively validated average value modelling, in which appropriate measures are taken to accurately represent the converter behavior during blocking state [29]. All converters have 350 sub-modules and the capacitance is calculated assuming the same minimum inertia constant of 30ms (or 30kJ/MVA) as suggested in [30].

All transmission media are assumed to be DC cables, which are represented based on the frequency-dependent cable model available in PSCAD library, and the parameters are adopted from [31]. The network is operating at ±320kV in

a symmetric mono-pole configuration, in which converters C1 and C2 are configured to control the active power, while converters C3 and C4 employ DC voltage droop control to regulate the DC system voltage. Moreover, all converters are configured to control reactive power. AC grids are modelled by a voltage source and their equivalent short-circuit impedance that comprises of a series resistance and inductance. Strong AC networks are assumed at all terminals to demonstrate the performance of the fault management strategy for high fault current levels. The main parameters of the HVDC grid and CH-MCCs with 25% ratio are summarized in Table I. The converters' operating conditions are also shown in the table.

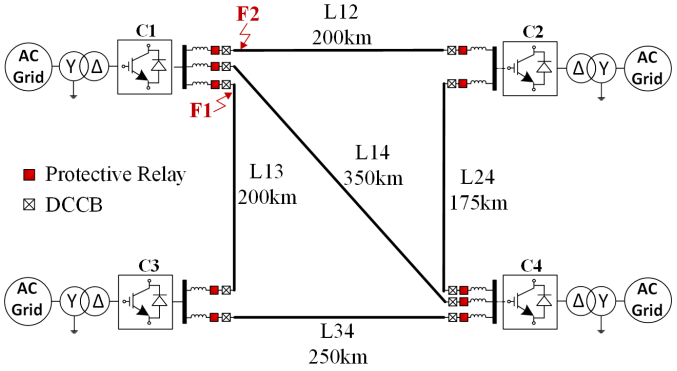


Fig. 3. HVDC grid test system.

TABLE I. System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated AC (line-to-line) voltage	400 kV
Short circuit ratio of AC grids	15
X/R of AC grids	10
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,−100,−100 MVAr
Total number of SMs	350
Arm inductance	42 mH
Arm resistance	0.08 Ω
Total FB-SMs capacitance	125.68 μF
Total HB-SMs capacitance	41.89 μF

IV. DC Fault Management Strategy

A. Converter Behaviour during pole-to-pole Faults

Pole-to-pole faults have severe consequences on the safety and operation of HVDC grid and consequently, they must be isolated as quickly as possible. It is worth reiterating that the bespoke design of CH-MMC being perused in this paper aims to extend the time frame for fault detection and isolation so as effective protection coordination with slow mechanical DCCBs in the order of 5 ms to 15 ms becomes technically feasible [15], [16], [32]. The fault behaviour of the CH-MMC in this time frame can be divided into two stages.

1) Fault current prior converter blocking: This stage initiates when travelling waves induced by the fault reach the converter after a short propagation period through the transmission medium, resulting in the discharge of sub-module capacitors into the fault and causing a rapid increase of the fault current. As the converter retains controllability in this stage due to the active capacitor voltage balancing algorithm, equal discharge of the SM capacitors of the arms will be observed. The rate at which the SM capacitors discharge is largely limited by the arm inductance and the effective DC side inductance (current limiting inductor and DC cable inductance). In the worst-case of a DC fault at converter DC terminals, the fault network can be considered as an equivalent RLC circuit as follows

$$R = \frac{2R_{arm}}{3} + R_f, \quad L = \frac{2L_{arm}}{3} + L_{DC}, \quad C = 6 \cdot C_{arm} \tag{10}$$

where R_f is the fault resistance, L_{DC} is the DC current limiting inductor, R_{arm}, L_{arm} and C_{arm} are the converter's arm resistance, inductance and capacitance, respectively. The fault current flowing to the DC fault can be derived as

$$I_f(t) = e^{-\sigma t}\left(2V_{DC}\sqrt{\frac{C}{L}}sin(\omega t) + I_0 cos(\omega t)\right) \tag{11}$$

where $\sigma = \frac{R}{2L}$, $\omega = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2} \approx \sqrt{\frac{1}{LC}}$ and I_0 is the pre-fault current. This stage lasts until the worst-case converter arm current hits the pre-set over-current threshold, or until the DC link voltage has fallen below a specified threshold. Alternatively, the converter can block upon DC fault detection, if required.

2) Fault Current after converter blocking: This stage starts once the converter blocks, which subsequently triggers blocking (switching off) of the IGBTs of the HB and FB chain-links. The latter contribute to a build-up of reverse voltage, which helps to reduce the DC fault current.

During normal operation, approximately 50% of the SMs are inserted, hence N SMs (equivalent to one arm) contribute to the fault. The contribution of each phase to the fault current is determined by

$$I_{fault_j} = \frac{c_{SM}}{N}(2N_{FB} - 1)\left(\frac{d(u_{j,u} - u_{j,l})}{dt}\right) \tag{12}$$

From (12) it is observed that the fault current can be controlled according to the number of FB-SMs in each arm. However, in case where N_{FB} is less than approximately 50% of N, the total reverse blocking voltage capability is less than the peak AC line-to-line voltage, V_{AC}^{max}. This results in the over-voltage of FB-SM capacitors, until the total phase FB chainlink voltage matches V_{AC}^{max}. The voltage rise in the FB-SMs is determined by the magnitude of the DC fault current in each phase i_{fault_j}, and the total capacitance of the FB-SMs C_{FB} and is described by

$$V_{FB_j}(t) = \frac{1}{C_{FB}}\int_0^T i_{fault_j} dt + V_{FB_j}^0 \tag{13}$$

where $V_{FB_j}^0$ is the initial voltage of the FB chainlink of phase j the moment the second stage initiates. To enable the fault-ride through functionality of the converter, the capacitors should be designed to withstand overcharging for a short period of time, and for their protection, a maximum allowable limit on

FB-SM over-voltage should be set, beyond which the FB-SM capacitors are bypassed (using similar techniques as in HB-SMs, e.g. dedicated thyristors [14]). In this work, this limit is set to 1.6 p.u., which has been found to be adequate even when slow mechanical DCCBs are employed. Moreover, equation (13) indicates that the higher the value of C_{FB} and hence, the higher the individual FB-SM capacitance C_{SM-FB}, the slower the rate of voltage increase in the FB chainlink. Consequently, another method to limit the over-voltage rate until fault clearance is to utilize capacitors of greater size. Once the fault current is cleared, all sub-module voltages will converge to their pre-fault level due to the separate employed capacitor voltage balancing control.

As shown from equation (12), a higher ratio of FB-SMs to total number of sub-modules results in lower current in each arm, which in turn leads to a reduction in total fault current. To illustrate this effect, a solid P2P DC fault is applied at location F1 (shown in Fig. 3) on cable 13, 1 km away from converter C1 and the cable current of the faulted pole is shown in Fig. 4a for different ratios R of the CH-MMC, without enforcing the capacitor over-voltage limit. The current limiting inductance, L_{DC}, is set to 50mH and the circuit breaker operation time is assumed to be t_{br}=15ms. The fault is applied at time t=0.1s.

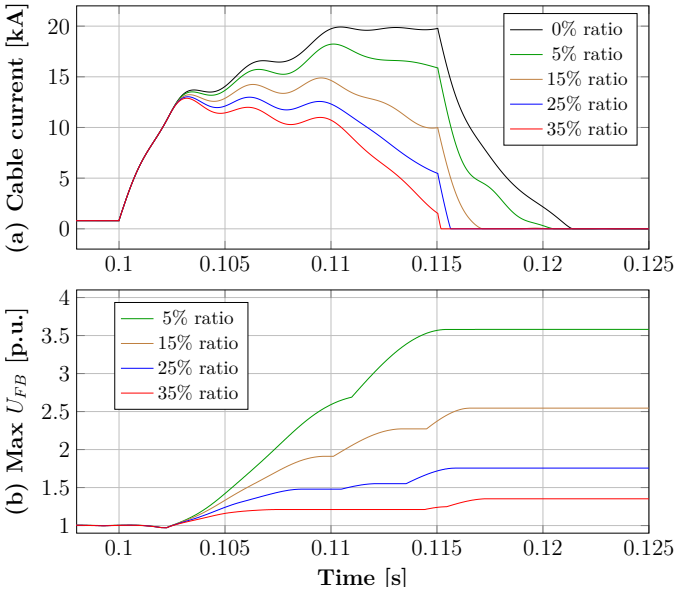


Fig. 4. Effect of R on (a) Cable fault current and (b) Maximum value of FB-SM voltages.

In the initial stage of the fault, the cable current is composed of the SMs capacitor discharge current and the current contribution from the adjacent cables. The effect of ratio R during this period is minimal and the rise of fault current is mainly determined by the DC inductor size. Around t=1.025ms, the converter blocks, and the fault current is regulated. It is evident that in comparison with lower ratios, R=25% and R=35% lead to a more profound reduction in the fault current, which is controlled within a reasonable range until the DCCB operates.

Moreover, the maximum value of the FB-SM capacitor voltages for all arms for the entire fault duration is depicted in Fig. 4b for all ratios. As the fault current flows through the FB-SMs, the capacitors continue to charge, leading to voltage increase. It is evident that ratios lower or equal to 15% lead to rapid increase of FB-SM capacitors voltage. For R=25%, even for a fault at very short distance, an extended time window of reverse DC voltage is provided and the maximum voltage reaches 1.76 p.u. approximately 15 ms after the fault. The charging of the FB-SM capacitors is further restrained in the case of R=35%, where the voltage rises to 1.35 p.u.

It can be argued that the significant fault current limitation bestowed by the use of at least 25% ratio implies that the current stresses on system components are decreased and that the time provided for protection system response and fault isolation can be significantly extended; therefore, slower but less expensive DCCBs can be utilized. As a consequence of the blocking action of the converter, power transfer capability during and after fault clearance is lost, as well as the ability for ancillary services provision to the connected AC grids. Nevertheless, since the converter remains blocked only for a short period of time (10-20 ms) only to allow for slow mechanical DCCBs to operate, the influence on the connected AC grid can be minimized.

B. Converter Behaviour During pole-to-ground Faults

When a pole-to-ground fault occurs, the voltage of the faulted pole collapses to zero. On the other hand, the healthy pole can experience a significant over-voltage up to twice the nominal voltage. To mitigate the impact of the fault on the HVDC grid and to ensure continuous operation of the converters, when a P2G fault is detected, the voltage reference is set to 0.5 p.u.

To accomplish 50% reduced DC voltage operation during P2G DC faults, the DC components of the upper and lower arm voltage being contributed by the FB chain-links are adjusted. In this way, the required number of FB-SMs to allow controlled operation at $0.5V_{dc}$ during P2G faults is 25%, as described by (4). Thus, the modulation functions for the upper and lower arms become

$$m_{j,u} = M_{AC} \cdot cos(\omega t) + 0.25 \tag{14}$$

$$m_{j,l} = -M_{AC} \cdot cos(\omega t) + 0.25 \tag{15}$$

The issues that are overcome in the event of P2G faults and the benefits of using the CH-MMC converter with R=25% are:

- **Healthy pole over-voltage avoidance:** The P2G voltage of the healthy pole can be maintained at nominal; hence, the risk of DC cable insulation failure is prevented.
- **Fault current elimination.** The controlled operation at 50% of the rated DC voltage retains the ability of the converter to synthesize the full AC grid voltage and control active and reactive power, while also the uncontrolled flow of AC current from the AC grid is eliminated. Also, the DC currents associated with the rise of healthy DC pole across the DC grid can be dramatically reduced. In cases where DCCBs of the HVDC grid are designed for interrupting fault currents originating only from P2G faults rather than P2P faults, the DCCBs current breaking

and energy absorption capabilities can be greatly reduced, or even instead of DCCBs, high-speed DC switches with reduced cost and footprint can be employed.

- **Mitigation of DC offset in converter transformer voltage.** In HB-MMCs, converter transformers are exposed to severe DC voltage stresses during P2G DC faults. In contrast, with the utilization of the CH-MMC, the DC voltage stress on transformer can be reduced to $\frac{1}{4}V_{DC}$. The DC offset can be further reduced when using a higher ratio R.
- **Continuous HVDC grid operation.** During P2G DC faults, the proposed converter retains full control of active and reactive power exchange with the connected AC grids. Since the DC grids operate at $\frac{1}{2}V_{DC}$, they retain at least half of the rated power capability, which can lead to faster post-fault power flow restoration.

C. Proposed DC Fault Management Strategy for HVDC Grids

Based on the aforementioned discussions, the CH-MMC with at least R=25% is promoted for the proposed DC Fault Management Strategy (FMS) for CH-MMC based HVDC grids, which requires coordination with local protection relays. Taking converter C1 of Fig. 3 as an example, the basic flowchart of the FMS along with the coordination scheme with the protection relays are shown in Fig. 5. Since P2G and P2P faults require different fault handling techniques, the FMS receives information from the protection relays about whether a P2G or P2P DC fault is detected, and then activates the corresponding measures for the converter. This process takes place at each converter station individually.

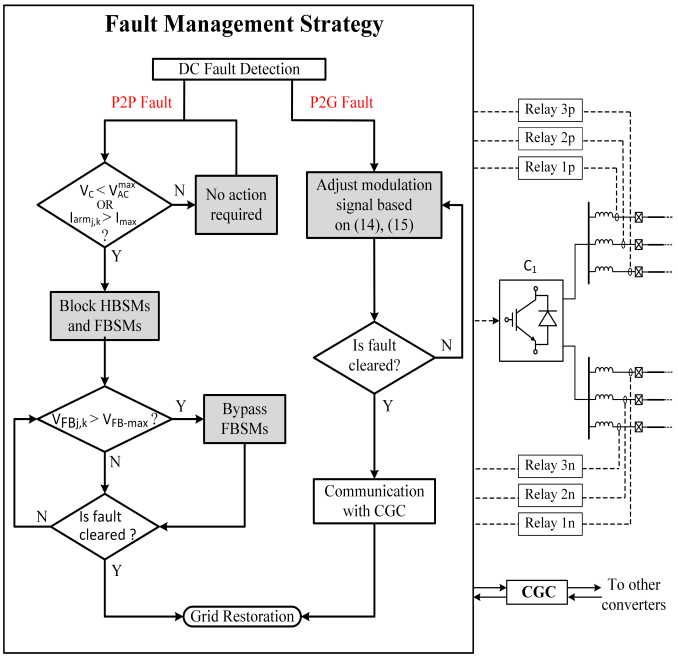
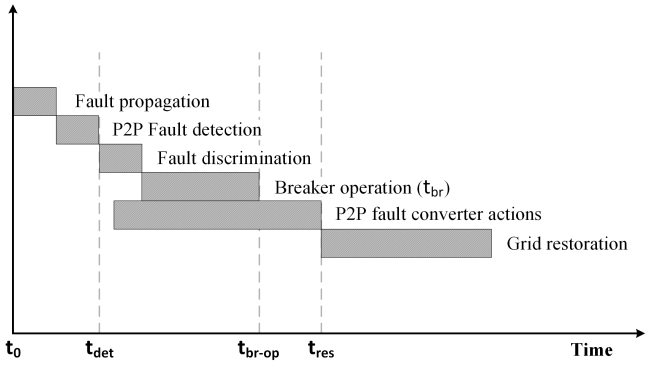


Fig. 5. Flowchart of the proposed FMS.

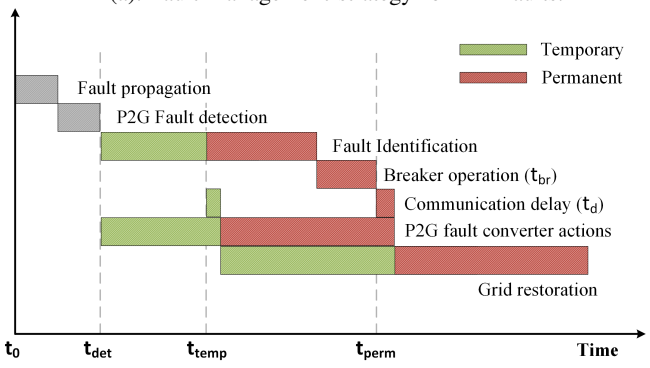
To detect every probable fault on any cable of the HVDC grid, protection relays are placed at both poles of each cable end. Owing to the fact that DC faults have distinctive impact on DC voltages, under-voltage is used for fault detection. If both poles are affected a P2P fault is detected, otherwise a P2G fault is detected.

Moreover, DC cable faults are cleared selectively to ensure continued operation of the remaining HVDC grid. Towards this aim, fault discrimination is performed by protection relays to identify the faulted cable and issue a trip command to the corresponding DCCBs. Recent proposed DC protection solutions offer discriminative protection at very high speeds (less than 100μs signal processing time) [9]–[12]. Nevertheless, a simplified non-unit protection method based on du/dt is employed, in which pole voltage measurements are used with a sampling frequency of 20 kHz. It is worth noting that du/dt is selected in this paper for illustration only, and the proposed FMS is applicable for any fault discrimination method that is employed, including unit protection techniques.

Also, a Central Grid Controller (CGC) is introduced for exchanging information between converters, if required. Due to the severity of P2P DC faults and the requirement for fast fault clearance, the fault management strategy for P2P faults precludes the use of the CGC. On the contrary, in case of a P2G fault, the CGC is employed to coordinate converter actions before commencing grid restoration process after fault clearance. More details on the fault management strategy and the sequence of events during P2P and P2G faults are subsequently provided.



(a). Fault management strategy for P2P faults.



(b). Fault management strategy for P2G faults.

Fig. 6. Sequence of events during the fault management strategy.

1) Sequence of events for pole-to-pole faults: Fig. 6a shows the sequence of events when the FMS is activated for a P2P fault that occurs at t_0 and starts to propagate in the HVDC grid. The fault is detected by the corresponding protection

relays at instance t_{det}. Provided a P2P fault is detected, the FMS initiates when any converter arm current $I_{arm_{jk}}$ exceeds the maximum overcurrent limit, I_{max}=1.8 p.u., or when the DC link voltage V_c falls below the peak AC line-to-line voltage, V_{AC}^{max}. In this way, unnecessary blocking of the CH-MMC in the event of non-critical faults with limited impact (e.g. highly resistive faults) is avoided.

Following activation of the FMS for a P2P fault, the converter HB-SMs and FB-SMs will be blocked, prompting the FB chain-links to gradually recreate the reverse DC voltage as explained in Section III-A. During this process, the voltages of all FB chain-links are continuously monitored. If any of the FB chain-link voltages exceeds the maximum allowable limit V_{FB-max}=1.6 p.u., all FB-SMs of the converter are bypassed to protect the SM capacitors. When the fault is discriminated by the protective relays of the faulted cable, a trip signal is generated for the corresponding DCCBs, which trip after the operation time, t_{br}, has elapsed. The converter exits the strategy when information is received by the corresponding relays that the fault is successfully is cleared. Once the DCCBs are opened and the converter exits the strategy, grid restoration process will start, at time t_{res}. To ensure security of the FMS during P2P faults, a dead time dt=5 ms is introduced between circuit breaker operation, at t_{br-op}, and the grid restoration starting time, t_{res}. For converters in which the FMS has been activated but are not connected to the faulted medium, the DC fault is deemed to be cleared when time ($t_{br} + dt$) has passed after fault discrimination stage.

It is worth noting that fault discrimination is realized by the protection relays independently from the converter actions. Therefore, the converter may block during or after the fault discrimination stage, depending on the impact of the DC fault on converter voltage and arm currents. Moreover, the strategy can be activated for all converters of the HVDC grid or at least for the local converters (i.e. connected to the faulted medium). If blocking of only local converters is required, appropriate measures should be taken, (e.g. use of high line inductor value), for ensuring that arm over-current or under-voltage limits of the remote converters are not violated. It is worth noting that for P2P faults, the FMS is applicable for any ratio R of the CH-MMC, while for the effective operation of the strategy during P2G faults, a ratio of R≥25% is required.

2) Sequence of events for pole-to-ground faults: Fig. 6b shows the corresponding sequence of events when the FMS is activated for both temporary and permanent P2G faults. When the P2G fault is detected by the local protection relays, activation of the FMS is triggered at each converter terminal individually, and the modulation signals for the upper and lower arms of all grid converters are modified based on equations (14) and (15). Voltage controlling converters set DC voltage reference to 0.5 p.u., while converters that regulate active power also reduce their active power orders in proportion to the DC voltage to avoid overloading of the DC cables. As the proposed CH-MMC design is able to retain controllability during P2G faults, the FMS remains active until the protection systems perform fault identification, (i.e. to identify whether the fault is temporary or permanent). Since all converters participate in the fault management process in an effort to achieve controlled operation of the HVDC grid, knowledge of fault nature, i.e., temporary or permanent, is not required instantaneously. Therefore, this paper assumes that if the fault is not deemed temporary within 180ms ($t_{perm} - t_{det}$), then a trip command is sent to the DCCBs of the faulted cable.

For P2G faults, the central grid controller is utilized to ensure that all grid converters exit the strategy and resume normal operation almost simultaneously. When the CGC receives information that either a temporary or a permanent P2G fault has been cleared, it distributes a grid restoration start signal to all converters. To account for the communication delay between the grid controller and the converters, a conservative fixed time delay t_d=30ms is assumed.

V. Performance of DC Fault Management Strategy

The enhanced DC fault ride-through performance of the CH-MMC and the performance of FMS during P2P and P2G faults are assessed in this section using the illustrative meshed HVDC grid of Fig. 3. Various values of ratio R, current limiting inductances L_{DC}, and operating speeds of DCCBs t_{br}, are tested to evaluate the performance of the DC fault management strategy over a wide range of scenarios and to provide an operating envelope for the proposed strategy.

Initially, a sensitivity analysis for the size of the current limiting inductance is performed and its impact on pole-to-pole fault current is investigated. Subsequently, the FMS is evaluated and the fault response of the CH-MMC based HVDC grid in terms of voltage and power recovery times is assessed. Finally, exemplary P2P and P2G fault cases are selected and discussed to further demonstrate the effectiveness of FMS for handling DC faults.

A. Impact of series inductor

The size of current limiting DC inductors is one of the dominant factors that determine the rate of rise of fault current, and directly affects the available time margin for protection response. To investigate this effect, 50, 100 and 200 mH DC current limiting inductors are selected for further analysis. The maximum fault currents observed in DC cable current values are depicted in Fig. 7, for different values of R of the CH-MMC, when a solid P2P fault is applied at location F1. This fault location has been selected due to its direct proximity with converter C1 and because three cables are connected to the same terminal. This study aims to reveal potential trade-offs between the R ratio of the CH-MMC, magnitude of L_{DC} and DC circuit breaker operating times. In other words, the study aims to identify potential savings in the size of minimum current limiting inductance required to enable the use of a range of existing mechanical circuit breakers, with operating times ranging from 5 ms to 15 ms [15], [16].

The observations drawn from the results in Fig. 7 are summarized as follows:

- For R≥25%, a significant decrease in fault current is achieved when compared to R<0.25%.
- In comparison to R=0% (i.e. typical HB-MMC), the proposed R=25% achieves a reduction in peak DC fault

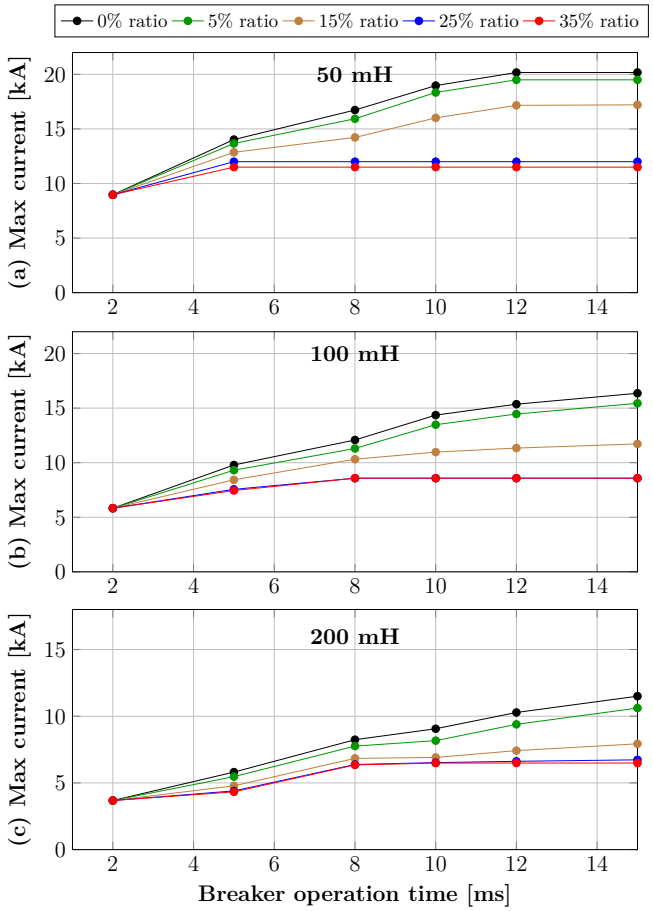


Fig. 7. Maximum cable fault current for different R, when (a) L_{DC}=50mH, (b) L_{DC}=100mH and (c) L_{DC}=200mH

current of 40.5%, 47.5% and 41.5% for L_{DC}=50, 100, 200 mH, respectively, when t_{br}=15ms.

- It is worth noting, that the differences between R=35% and R=25% are marginal in all scenarios, and the observed current magnitudes for both ratios are almost identical for all DC circuit breaker operating times. Similar to the case shown in Fig. 4a, the maximum current values are observed in the early stage of the fault, i.e. within 5ms in Fig. 7a and within 8ms for Fig. 7b and 7c. Afterwards, both ratios achieve successful regulation of the fault current at lower levels for an extended period of time as long as the FB-SM capacitor voltages remain below the designated limit (1.6 p.u.).

In summary, the above discussion shows that the customized current suppression capability exhibited by FB chain-links of the CH-MMC for various R values can replace or minimize the required current-limiting role of series inductors when the proposed FMS is adopted. The reduction observed in the fault currents with the increase of R is practically meaningful as it leads to reduction in DCCB current breaking capacity.

B. Fault Management Strategy Evaluation for pole-to-pole Faults

As P2P DC faults provoke serious disruption of power flows across HVDC grids and the surrounding AC networks, the priority is to minimize the power flow interruption by quick isolation of the faulted section; however, the cost of fast acting hybrid DCCBs to realize such an approach can be prohibitive. An alternative approach as proposed in this paper, is to create a shielding state in which the converter terminals must contribute to minimization of magnitude and duration of system wide power flow interruption, and facilitation of rapid resumption of power flows to pre-fault or new post-fault states. The indicators used to assess DC grid recovery from a P2P DC fault are the DC voltage and power flow recovery times. The former and the latter represent the times that DC voltage and power recover within ±5% of the nominal voltage and ±10% of the post-fault steady state power flow, respectively.

This subsection assesses the extent of improvement in HVDC grid performance when FMS and CH-MMC are employed, considering the cases listed in Table II, which are denoted by A, B and C. In cases A and B, converters C1 through C4 of the four-terminal HVDC grid of Fig. 3 are simulated as CH-MMCs with R=0% and 25%, respectively, when also the minimum DC side current limiting inductance that is required to prevent blocking of remote converters is used (calculated using the approach presented in [7]). Recall that R=0% resembles conventional HB-MMC. Based on the findings of the previous subsection, Case C uses R=25% and L_{DC}=50 mH (significantly smaller than that in cases A and B) to demonstrate the broader benefits of FMS, when temporary blocking of the FB chain-links of all CH-MMCs is permitted based on DC under-voltage or arm over-currents thresholds.

TABLE II. Case studies for FMS evaluation for P2P faults.

Case Study	Description	Comment
A	HB-MMC (R=0%) with high L_{DC}	Local converters are allowed to block
B	CH-MMC (R=25%) with high L_{DC}	Local converters are allowed to block
C	CH-MMC (R=25%) with L_{DC}=50mH	All converters are allowed to block

Fig. 8a, 8c and 8e, and 8b, 8d and 8f present the DC voltages of converter terminals C1 through C4 and their respective active powers for each case, when the DC grid in Fig. 3 is subjected to a solid P2P fault at location F1 and the DCCB operating speed (t_{br}) is set to 10ms. At this operating speed, the calculated minimum DC side current limiting series inductance to prevent blocking of remote converters (C2 and C4) is 320 mH. The main observations drawn from Fig. 8 are:

- The continuous operation of the remote converters is maintained in cases A and B, in which DC voltage collapse is observed only at DC terminals of converters C1 and C3 (the nearest to the fault point).
- The use of CH-MMCs with R=25% in case B instead of conventional HB-MMCs leads to a reduction in voltage and power recovery time by 30% and 19%, respectively.
- Despite the temporary blocking of all converters, it is evident that case C leads to much faster power and voltage recovery times when compared to the base-case A, i.e., 35% and 50.3% reduction in DC voltage and power recovery times, respectively.

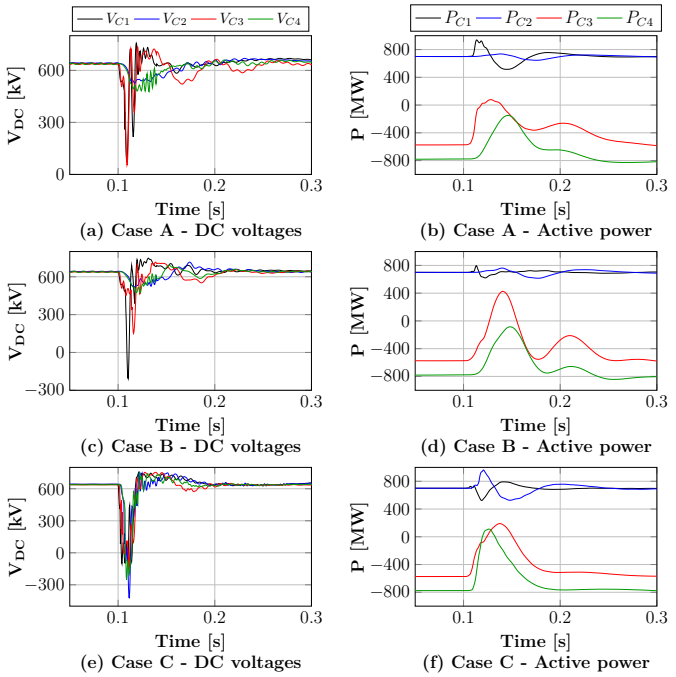


Fig. 8. System transients for fault F1 for all case studies (t_{br}=10ms).

Furthermore, Fig. 9 displays the most affected arm current, the upper arm of phase A of converter C1, which is the nearest to F1. It can be seen that the use of CH-MMC leads to reduced peak arm currents during the fault. In detail, the arm current reaches 3.31 p.u. for case A, while the maximum observable current in case B is limited to 2 p.u. The peak arm current is further reduced to 1.8 p.u. in case C, even though a significantly smaller current limiting inductance is used.

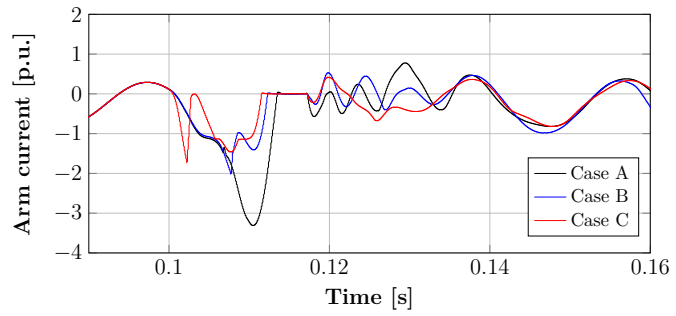


Fig. 9. Comparison of arm currents for all case studies. The arm current shown is the upper arm of phase A.

The same P2P fault is repeated for different DCCB operating times and the observed voltage and power recovery times are summarized in Fig. 10. For cases A and B, the derived series inductor values for t_{br}=5, 8, 10, 12, 15ms are L_{DC}=110, 230, 320, 425 and 590 mH, respectively, while in case C, L_{DC}=50 mH. For cases A and B, as the circuit breaker operating speed increases, a higher inductor value is required to ensure continuous operation of the remote converters, while also system recovery times increase. Case C exhibits much faster recovery times than the other cases, a trend which remains consistent for all DCCB operating times. The results suggest that temporary blocking of all CH-MMCs leads to improved converter and system response during DC faults. In addition, incorporation of sizeable series inductors is not required, thus reducing DCCB cost and footprint, and avoiding their interference with the upper level converter controls that may lead to erratic behaviour during post-fault recovery.

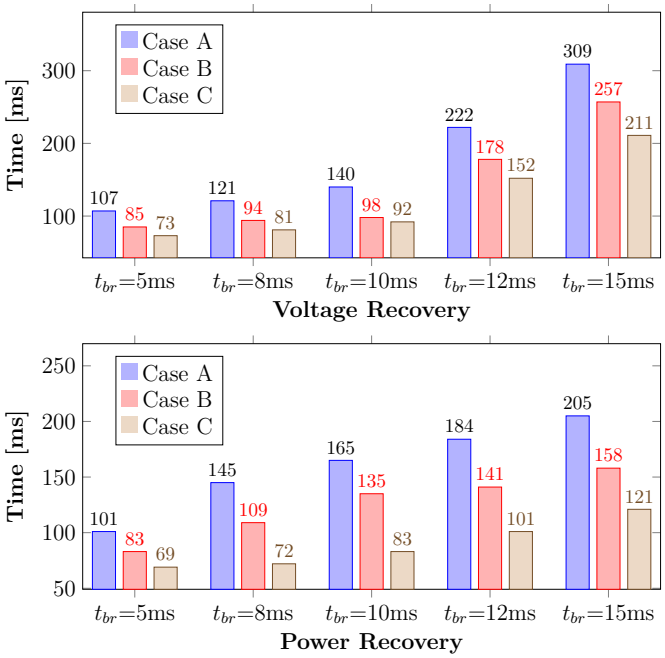


Fig. 10. Voltage and power recovery times for all cases.

For a more rigorous performance assessment of the FMS under P2P DC faults, several fault locations are simulated, in which all converters are permitted to participate in the proposed FMS (as performed in Case C). In the assessment, solid P2P DC faults are applied in the beginning, middle, and end of each cable of the HVDC grid. Table III summarizes the average voltage and power recovery times for different t_{br} and R, with L_{DC} fixed at 50mH.

TABLE III. Average voltage and power recovery times for P2P faults.

FB-SM Ratio [%]	**Voltage Recovery [ms]** DCCB speed, t_{br} [ms]					**Power Recovery [ms]** DCCB speed, t_{br} [ms]				
	5	8	10	12	15	5	8	10	12	15
0	105	125	147	235	343	100	139	162	183	209
15	92	99	124	188	266	78	126	142	151	163
25	69	77	91	149	205	65	71	81	95	116
35	67	73	86	129	188	61	68	77	86	107

The main conclusions of this study are the following:

- In comparison with HB-MMC (R=0%), it is evidently clear that the DC voltage and power recovery times reduce consistently as the ratio R increases.
- Ratio R=25% reduces power recovery times to less than 4-5 fundamental cycles for DCCB operating times up to 12 ms. This reinforces the benefits of the CH-MMC and the proposed DC fault management strategy, i.e. reduced protection requirements in terms of DC fault detection speed, series inductor size and breaking operation speed,

without significantly compromising DC grid security during DC faults, and the speed of power system restoration.
- Moreover, use of R=35% for the CH-MMC further improves system recovery time for DCCB with a slower operating time than 12 ms.

C. Exemplary pole-to-pole Fault

For a detailed demonstration of the DC fault behaviour of a HVDC grid that employs CH-MMCs (R=25%) and operates under the fault management strategy for P2P faults, an exemplary fault scenario is selected, in which a solid fault is applied at location F1 at time t=0.1s, when L_{DC}=50mH and t_{br}=8ms. Selected simulation results are shown in Fig. 11. Within a short time from fault inception, the FMS is initiated at all converters, at different time instances depending on the moment the converter blocking criteria are satisfied. Meanwhile, protection relays of cable L13 discriminate the DC fault and send a trip command to the cable DCCBs. The main observations are summarized as follows:

- Fig. 11a shows that the activation of the FMS has led to brief collapse of DC voltages at all converter stations and to relatively fast recoveries, approximately 100ms after fault inception.
- Fig. 11b shows that the proposed FMS significantly reduces the converter DC currents and thus, the DCCBs let-through current and breaking capacity.
- The temporary loss of controllability over the active and reactive powers exchange with the surrounding AC grids has led to brief interruption of power flows across the DC grid, which are re-established in less than 80ms as shown in Fig. 11c and 11d.
- Fig. 11e and 11f display the DC voltages across the HB and FB chain-links of all arms for the most affected (nearest) converters (C1 and C3). It is evident that in the moment the fault management strategy starts, HB-SMs are blocked, while the FB-SMs that provide counter voltages are charged by the fault current. In this way, higher counter voltages are generated in the arms of the CH-MMC, which aid to suppress the AC-side fault current contribution as well as the DC fault currents. It is worth mentioning that the capacitor over-voltage limit (1.6 p.u.) is not reached in any of the converters' arms.
- Following fault clearance, all HB and FB chain-links briefly exhibit disturbances and eventually converge to the nominal set-points as designated by the horizontal controllers.
- Fig. 11g and 11h show the upper arm currents for the same converters. It is observed that converter arm currents remain within normal operating range.

D. Exemplary pole-to-ground Fault

This subsection illustrates the performance of the proposed FMS when the HVDC grid is subjected to a permanent P2G fault at location F2 (shown in Fig. 3) on cable L12, 1 km away from converter C1. R, L_{DC} and t_{br} are fixed at 25%, 50mH and 8ms, respectively. The fault is applied at 0.1s and the

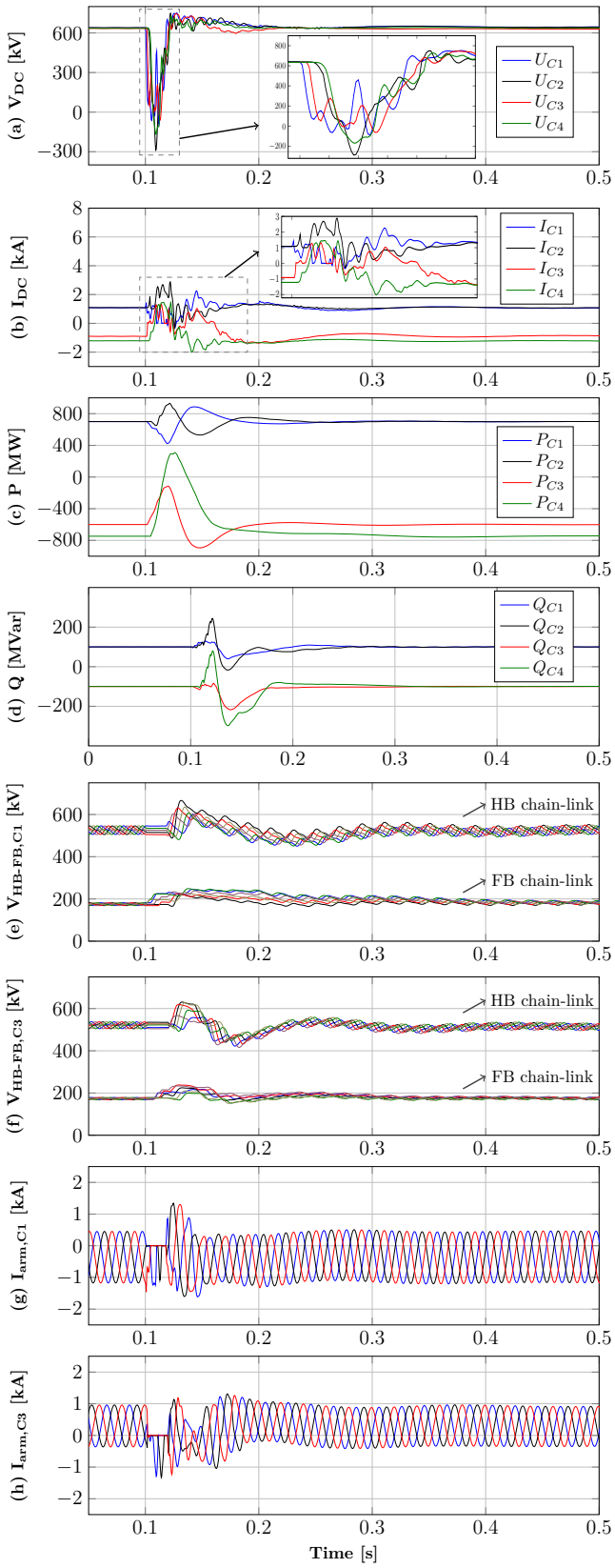


Fig. 11. Exemplary P2P fault waveforms: (a) converter voltages, (b) converter currents, (c) active power of CH-MMCs, (d) reactive power of CH-MMCs, (e) C1 chain-link voltages, (f) C3 chain-link voltages, (g) C1 arm currents, and (h) C3 arm currents.

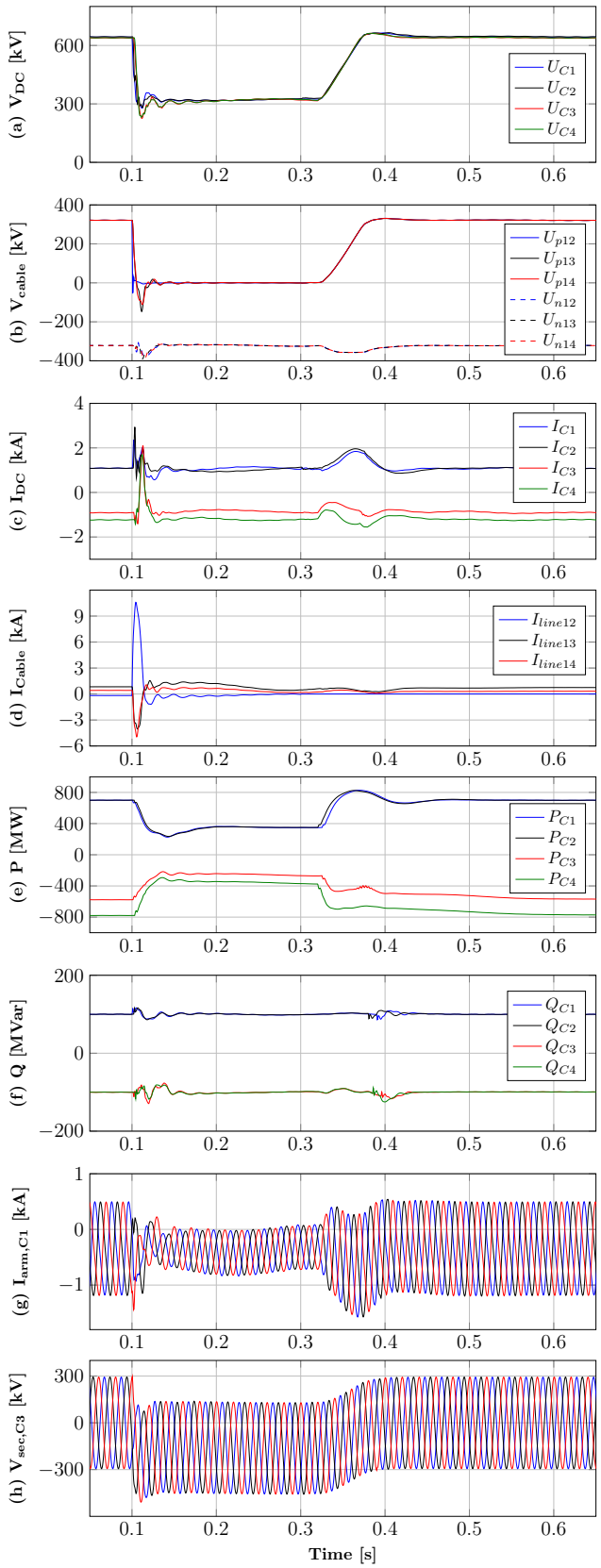


Fig. 12. Exemplary P2G fault waveforms: (a) converter voltages, (b) cable voltages at bus B1 (c) converter currents, (d) cable currents at bus B1, (e) active power of CH-MMCs, (f) reactive power of CH-MMCs, (g) C1 arm currents, and (h) converter C3 transformer secondary voltage.

simulation results are presented in Fig. 12. When protection relays in the proximity of each converter detect a P2G fault, the FMS for pole-to-ground faults is activated. Followingly, protective relays of cable L12 discriminate the DC fault as internal. Since the fault is not identified as temporary within 180ms from FMS activation, a trip command is sent to the DCCBs of cable L12. For the entire fault duration, all converters participate in the fault management process and controlled continuous HVDC grid operation is retained with partial loss of power transfer capability. Following isolation of cable L12, the CGC is notified that the fault has been cleared and a grid restoration start signal is distributed to all converters (assuming 30ms delay). The main observations are summarized as follows:

- Fig. 12a shows that all converter DC voltages are halved in a controllable manner, and after fault clearance they are simultaneously restored to nominal value as a result of the actions of the CGC.
- Fig. 12b shows the positive and negative pole-to-ground voltages at the cables connected to bus B1 (DC bus of converter C1). It is evident that the DC voltages of the faulty poles are collapsed to zero, while those of the healthy poles are maintained at nominal level.
- Moreover, it can be noticed from Fig. 12c that shortly after fault detection, the converter currents are controlled at the pre-fault set-points. With the employed FMS, the current of the faulted cable (I_{12}) decays rapidly towards zero as shown in Fig. 12d.
- After P2G fault detection, converters operate at almost half of the prefault power setpoints, as demonstrated in Fig. 12e. Once the fault is cleared, power flows are quickly re-established. Owing to the continuous operation of the HVDC grid, reactive power flows are marginally affected (Fig. 12f). It is evident that the proposed FMS allows the converters to retain controllability for the entire fault duration and thus, the capability to provide ancillary services to the connected AC networks.
- Fig. 12g shows that the nearest converter to the fault is not experiencing current stresses in any of each arms throughout the fault period.
- The converter transformer is experiencing a DC offset equal to 1/4 of total V_{DC} (Fig. 12h). In comparison with a converter transformer connected to a HB-MMC, the DC offset is decreased by 50%.

VI. Discussion

The proposed fault management strategy that is developed particularly for HVDC grids that employ the CH-MMC offers a plethora of functionalities achieved at reduced capital and operational costs. Table IV summarizes the findings of the comprehensive quantitative studies presented in this paper, in the form of high-level qualitative comparison, in which the ratio R of the CH-MMC is varied, with emphasis given to the following aspects: fault current contribution, breaking speed, system recovery times in P2P DC faults, and continued operation in the event of P2G DC fault. For completeness, a qualitative loss indicator, which assumes that the converter

total semiconductor loss varies proportionally with ratio R, is provided in Table IV.

It is evident that the CH-MMC with 25% ratio represents an attractive option for the practical realization of the of the proposed fault management strategy, in which the HVDC grid P2P and P2G fault performances can be achieved at reasonable overall costs (capital and running costs). At granular level, the sensitivity analysis has shown that the CH-MMC with R =25% offers practical compromises in terms of the magnitude of the fault currents that the mechanical DCCBs can interrupt, and the system recovery times following DC faults clearance. Furthermore, it has been demonstrated that the CH-MMC with R =35% can lower fault current during P2P faults and further extend the time window for the protection systems. However, the enhanced fault performance of the CH-MMC with $R \geq 35\%$ is achieved at the expense of increased cost of semiconductor losses over project lifetime. It is worth stating that the overall performance improvement in the latter case, with R =35% is marginal compared to that with R =25%.

TABLE IV. Comparison between different ratios of the CH-MMC.

Performance indicator	R = 15%	R = 25%	R = 35%
Converter fault current contribution (P2P faults)	medium	low	very low
Breaking speed requirements	high	low	very low
System recovery time (P2P faults)	low	very low	very low
Continuous operation (P2G faults)	no	yes	yes
Converter transfomer DC offset (P2G faults)	high	low	very low
Converter losses	low	medium	high

Even though the R=25% has been put forward as a minimum requirement for achieving all the desired functionalities for technically sound and cost-effective HVDC grids, the final design in a particular project may differ, depending on the required balance between practical design considerations and broader system operational objectives and priorities, which are beyond those accounted for in this paper. For example, in certain scenarios where the extended downtime is allowed, the P2P DC fault-ride-through may not be a stringent requirement. In such cases, CH-MMC with lower R ratios might be adopted, and the proposed FMS can still be used to coordinate protection actions, reduce fault currents and for the effective use of DCCBs with reduced requirements. However, continued operation during P2G DC faults cannot be achieved. In conclusion, the proposed FMS may be tailored according to the given requirements in order to mitigate the capital and operation costs, and ensure the desired degree of full or partial controllability during DC faults.

VII. Conclusion

This paper has proposed a DC fault management strategy for HVDC grids that employ CH-MMCs, in an effort to align the security of supply requirements of HVDC grids with those of the conventional HVAC grids, while at the same time maintaining the affordability of total system cost at reasonable levels. Initial parametric studies have revealed that the 25% ratio, the number of FB-SMs with respect to the total number of sub-modules per arm of the CH-MMCs, is critical for the proper operation of the proposed FMS and its effective coordination with DCCBs. Furthermore, simulation results from a representative 4-terminal meshed HVDC grid have demonstrated that the proposed FMS enables continuous operation during pole-to-ground faults, and fault-tolerant operation with minimum power flow interruption during pole-to-pole DC faults. It has been shown that the current limiting modes of the CH-MMCs enable the extension of fault clearance times to levels compatible with the mechanical DCCB operation times, and significantly reduce the magnitudes of fault and arm currents during pole-to-pole DC faults. In this way, DCCBs' current breaking capacities are reduced using significantly smaller current limiting series inductances. Also, it has been demonstrated that the proposed FMS results in improved DC voltage and power recovery times with respect to conventional HB-MMC based HVDC grids. The above-mentioned features collectively, lead to a satisfactory trade-off between cost, efficiency and DC fault-ride through capability, which constitutes the proposed strategy an attractive option for the technical and economical feasibility of future HVDC grids.

VIII. Acknowledgments

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References

[1] G. P. Adam, T. K. Vrana, R. Li, P. Li, G. Burt, and S. Finney, "Review of technologies for dc grids – power conversion, flow control and protection," *IET Power Electronics*, vol. 12, no. 8, pp. 1851–1867, 2019.

[2] O. Cwikowski, H. R. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, "Modular multilevel converter dc fault protection," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 291–300, Feb. 2018.

[3] L. Tang and B. Ooi, "Locating and isolating dc faults in multi-terminal dc systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1877–1884, July 2007.

[4] R. Dantas, J. Liang, C. E. Ugalde-Loo, A. Adamczyk, C. Barker, and R. Whitehouse, "Progressive fault isolation and grid restoration strategy for mtdc networks," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 909–918, April 2018.

[5] C. C. Davidson, R. S. Whitehouse, C. D. Barker, J. . Dupraz, and W. Grieshaber, "A new ultra-fast hvdc circuit breaker for meshed dc networks," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1–7.

[6] B. J. J. Hafner, "Proactive hybrid hvdc breakers-a key innovation for reliable hvdc grids," in *Proc. CIGRE Bologna Symposium*, 2011, pp. 1–8.

[7] M. Abedrabbo, W. Leterme, and D. Van Hertem, "Systematic approach to hvdc circuit breaker sizing," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 288–300, Feb. 2020.

[8] Y. Wang, W. Wen, C. Zhang, Z. Chen, and C. Wang, "Reactor sizing criterion for the continuous operation of meshed hb-mmc-based mtdc system under dc faults," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5408–5416, Oct. 2018.

[9] W. Leterme, J. Beerten, and D. Van Hertem, "Nonunit protection of hvdc grids with inductive dc cable termination," *IEEE Trans. on Power Delivery*, vol. 31, no. 2, pp. 820–828, April 2016.

[10] D. Tzelepis, A. Dyśko, S. M. Blair, A. O. Rousis, S. Mirsaeidi, C. Booth, and X. Dong, "Centralised busbar differential and wavelet-based line protection system for multi-terminal direct current grids, with practical iec-61869-compliant measurements," *IET Generation, Transmission Distribution*, vol. 12, no. 14, pp. 3578–3586, 2018.

[11] W. Xiang, S. Yang, L. Xu, J. Zhang, W. Lin, and J. Wen, "A transient voltage-based dc fault line protection scheme for mmc-based dc grid embedding dc breakers," *IEEE Trans. on Power Delivery*, vol. 34, no. 1, pp. 334–345, Feb. 2019.

[12] R. Li, L. Xu, and L. Yao, "Dc fault detection and location in meshed multiterminal hvdc systems based on dc reactor voltage change rate," *IEEE Trans. on Power Delivery*, vol. 32, no. 3, pp. 1516–1526, June 2017.

[13] O. Cwikowski, H. R. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, "Modular multilevel converter dc fault protection," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 291–300, Feb. 2018.

[14] S. Wang, C. Li, O. D. Adeuyi, G. Li, C. E. Ugalde-Loo, and J. Liang, "Coordination of mmcs with hybrid dc circuit breakers for hvdc grid protection," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 11–22, Feb. 2019.

[15] K. Tahata, S. E. Oukaili, K. Kamei, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "Hvdc circuit breakers for hvdc grid applications," in *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1–9.

[16] T. Eriksson, M. Backman, and S. Halen, "A low loss mechanical hvdc breaker for hvdc grid applications," in *in Proc.Cigré Session, Paris, France*, 2014, pp. 1–8.

[17] D. Vozikis, P. Rault, D. Holliday, and S. Finney, "Fault blocking converters for hvdc transmission: a transient behaviour comparison," *The Journal of Engineering*, vol. 2019, no. 17, pp. 3825–3830, 2019.

[18] D. Jovcic, W. Lin, S. Nguefeu, and H. Saad, "Low-energy protection system for dc grids based on full-bridge mmc converters," *IEEE Transactions on Power Delivery*, vol. 33, no. 4, pp. 1934–1943, Aug. 2018.

[19] W. Lin, D. Jovcic, S. Nguefeu, and H. Saad, "Protection of full bridge mmc dc grid employing mechanical dc circuit breakers," in *2017 IEEE Power & Energy Society General Meeting*, 2017, pp. 1–5.

[20] P. Ruffing, N. Collath, C. Brantl, and A. Schnettler, "Dc fault control and high-speed switch design for an hvdc network protection based on fault-blocking converters," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 397–406, Feb. 2019.

[21] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, March 2015.

[22] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[23] X. Yu, Y. Wei, Q. Jiang, X. Xie, Y. Liu, and K. Wang, "A novel hybrid-arm bipolar mmc topology with dc fault ride-through capability," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1404–1413, June 2017.

[24] R. Li, L. Xu, L. Yu, and L. Yao, "A hybrid modular multilevel converter with reduced full-bridge submodules," *IEEE Transactions on Power Delivery*, vol. 35, no. 4, pp. 1876–1885, Aug. 2020.

[25] J. Xu, X. Zhao, H. Jing, J. Liang, and C. Zhao, "Dc fault current clearance at the source side of hvdc grid using hybrid mmc," *IEEE Transactions on Power Delivery*, vol. 35, no. 1, pp. 140–149, Feb. 2020.

[26] D. Vozikis, "Modern voltage source converter topologies for future dc grids," Ph.D. dissertation, University of Strathclyde, 2018.

[27] D. Vozikis, G. Adam, P. Rault, O. Despouys, and D. Holliday, "Enhanced modular multilevel converter for hvdc applications: Assessments of dynamic and transient responses to ac and dc faults," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.

[28] J. Freytes, S. Akkari, P. Rault, M. M. Belhaouane, F. Gruson, F. Colas, and X. Guillaud, "Dynamic analysis of mmc-based mtdc grids: use of mmc energy to improve voltage behavior," *IEEE transactions on power delivery*, vol. 34, no. 1, pp. 137–148, Feb. 2018.

[29] D. Guo, M. Rahman, G. Adam, L. Xu, A. Emhemed, G. Burt, and Y. Audichya, "Detailed quantitative comparison of half-bridge modular multilevel converter modelling methods," in *14th IET International Conf. on AC and DC Power Transmission*, 2018, pp. 1–8.

[30] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "Vsc-hvdc transmission with cascaded two-level converters," in *Cigré session*, 2010, pp. B4–B110.

[31] W. Leterme, N. Ahmed, J. Beerten, L. Ängquist, D. Van Hertem, and S. Norrga, "A new hvdc grid test system for hvdc grid dynamics and protection studies in emt-type software," in *11th IET International Conf. on AC and DC Power Transmission*, 2015, pp. 1–7.

[32] Z. Shi, Y. Zhang, S. Jia, X. Song, L. Wang, and M. Chen, "Design and numerical investigation of a hvdc vacuum switch based on artificial current zero," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 22, no. 1, pp. 135–141, Feb. 2015.