



# Suspension and transfer printing of ZnCdMgSe membranes from an InP substrate

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**Abstract:** Wide bandgap II-VI semiconductors, lattice-matched to InP substrates, show promise for use in novel, visible wavelength photonic devices; however, release layers for substrate removal are still under development. An under-etch method is reported which uses an InP substrate as an effective release layer for the epitaxial lift-off of lattice-matched ZnCdMgSe membranes. An array of 100- $\mu\text{m}$ -square membranes is defined on a ZnCdMgSe surface using dry etching and suspended from the InP substrate using a three-step wet etch. The ZnCdMgSe membranes are transfer-printed onto a diamond heatspreader and have an RMS surface roughness  $< 2$  nm over 400  $\mu\text{m}^2$ , similar to the epitaxial surface. Membranes on diamond show a photoluminescence peak at  $\sim 520$  nm and a thermal redshift of 4 nm with  $\sim 3.6$   $\text{MWm}^{-2}$  continuous optical pumping at 447 nm. Effective strain management during the process is demonstrated by the absence of cracks or visible membrane bowing and the high brightness photoluminescence indicates a minimal non-radiative defect introduction. The methodology presented will enable the heterogeneous integration and miniaturization of II-VI membrane devices.

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## 1. Introduction

Wide bandgap II-VI semiconductors can be engineered to target almost any wavelength across the entire visible spectrum, offering the opportunity to develop ‘green-gap’ photonic systems such as light-emitting diodes (LEDs) [1], lasers [2–4], and color converters [5]; and their capacity for very large conduction band offsets is of interest for quantum cascade lasers and photodetectors in the infrared [3,6]. II-VI semiconductors are grown on GaAs, GaP, and InP substrates [7], with appropriate buffer layers, and therefore, to fully incorporate these II-VI epitaxial layers into devices, epitaxial lift-off (ELO) is essential due to the poor thermal and optical properties (at visible wavelengths) of the substrates. A variety of methods have been devised to accomplish this, ranging from chemical or mechanical thinning of InP substrates and a subsequent selective wet etch of the InGaAs buffer layer [8,9], to making use of metastable sacrificial layers for growths on GaAs [10,11]. The large bandgap range of II-VI semiconductors that may be grown lattice-matched to InP in particular enables the fabrication of unstrained quantum wells (QWs) suitable for emission from blue to orange without the requirement for strain compensation [4]. InP is already a common substrate for the growth of infrared structures based on III-V semiconductors and so the optimization of epitaxial lift-off of epitaxial layers from these substrates is important for a broad range of novel devices beyond the current work.

There has been extensive work on the wet etching behavior of InP, due to the highly direction-dependent wet etch rates of different faces of the InP zincblende crystal structure and its differing etch behaviors with various etchants [12–15]. Previous work has shown how InP etches when

it is masked by square and rectangular masks tilted to align with specific crystallographic orientations and has highlighted the dominance of  $\langle 1\ 0\ 0 \rangle$  directions in the under-etch of masks on InP [12,13], which dictates the alignment of device masks for successful, efficient fabrication. Microfabrication on InP has been successful over multiple geometries, from microscale wedges and stripes to the under-etching of photonic crystal lasing membranes [14,16,17]; however we make use of these microfabrication techniques to use an InP substrate itself as an effective release layer. For complex or thick II-VI structures, such as multi-QWs, it is often impractical to include a specific epitaxial release layer, such as MgS [10], due to the inclusion of strain or defects which can occur and the difficulty of growing such a layer on InP.

We have previously released II-VI epitaxial membranes via substrate and buffer layer removal [5]; however, we have found that mechanically polishing InP substrates and wet etching any remaining InP with hydrochloric acid (HCl) based etchants often introduces significant defects into the epitaxial layer, particularly with strained structures. The usage of the InGaAs buffer layer as an etch stop proved ineffective over large scale substrate wet etching. The InP forms very deep etch pits, when bulk etched, which results in a non-uniform removal of the InP. The InP remnants micromask the InGaAs during the InGaAs buffer layer wet etch and this roughens the II-VI epitaxial layer underside.

The suspension method involves the definition of a device pattern into an epitaxial layer and the subsequent under-etching, usually with wet etchants, of this patterned layer to liberate it from the growth substrate. This method has been successfully demonstrated in the production of InGaN micro-LEDs on diamond and AlInGaN LEDs on flexible substrates [18,19]. For this method to be successful with II-VI semiconductors on InP, and indeed any material grown on InP, the key challenge is the difficulty of wet-etching InP to a specifically masked shape. Further, in this work we have the additional challenge of under-etching II-VI epitaxial layers without a very high selectivity wet etchant.

Handling epitaxial membranes in liquid suspension (see [9]) is challenging, non-deterministic and impractical for commercial scaling of ELO technologies. In contrast, transfer printing using viscoelastic stamps of polydimethylsiloxane (PDMS) has shown that the deterministic transfer of micro-LEDs and vertical-cavity surface-emitting lasers (VCSELs) can be realized [18,20,21], and in doing so demonstrates its use as a powerful tool for the development of advanced heterostructures and devices from the nanoscale to the microscale. Micro-molding PDMS stamps enables their optimization for the transfer of discrete objects with specific geometries, including the detachment of suspended semiconductor films (membranes) from anchors. The mechanical relaxation of PDMS is used to provide a varying adhesion, allowing the transfer process, and the constant contact with the membranes maintains the strain. Once free of the anchors, a membrane on PDMS can be transferred onto any suitable substrate and, in the case of many devices with strict thermal management requirements, this is ideally a transparent single crystal diamond or silicon carbide heatspreader, which is used to extract heat from an active region. The continuity of contact of membranes, and hence the heat flow into a heatspreader, depends strongly on the surface roughness of the material transferred and the acceptor substrate; and is further improved in this case by not using adhesion layers, which add thermal impedance [18]. For optimum device performance the surface roughness of any processed semiconductor heterostructure is therefore a key metric for improvement.

A methodology is presented here which can be applied to all materials grown on an InP substrate, through minor adjustments to the etch chemistry. Through careful optimization of the suspension method, high quality membranes of ZnCdMgSe have been obtained, demonstrating the strain-maintained suspension of II-VI semiconductors, for the first time, and the suspension of samples from an InP substrate. This proof-of-principle work represents an important step in the development of an ideal ELO system for use in the heterogeneous integration of semiconductors grown on InP. The customizable design of the membranes that are released means that this

methodology offers a highly controllable and high yield method of miniaturizing wafer-scale grown devices. Here we characterize the high surface quality, and measure some optical and thermal properties of suspended ZnCdMgSe membranes transfer-printed onto a diamond heatspreader.

## 2. Experimental

### 2.1. ZnCdMgSe growth

Molecular beam epitaxy (MBE) was used to produce a 500-nm-thick II-VI,  $\text{Zn}_{0.37}\text{Cd}_{0.49}\text{Mg}_{0.14}\text{Se}$  layer using a dual Riber 2300P chamber with ultra-high vacuum transfer modules, which is capable of growing III-V and II-VI semiconductors [22]. Reflection high energy electron diffraction (RHEED) allowed a continuous assessment of the crystal quality during the growth and the oscillatory amplitude of the RHEED signals gave an indication of the number of monolayers grown. All samples were grown lattice matched to the (0 0 1) face of an InP substrate with a 110 nm-thick  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  buffer layer.

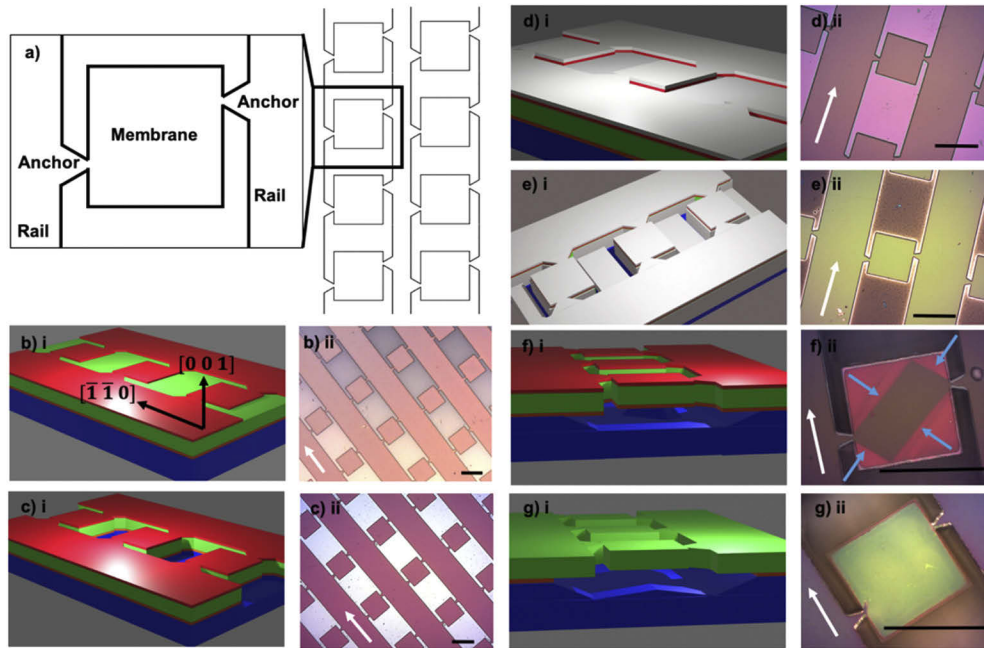
### 2.2. The suspension method

The II-VI on InP samples are cleaned thoroughly and an Oxford Instruments Plasmalab 80 Plus is used to deposit a 1.2  $\mu\text{m}$  protective layer of silica onto ZnCdMgSe using plasma enhanced chemical vapor deposition (PECVD; see Table 1 for conditions). Silica was chosen due to its high growth quality by PECVD, easy dry etching, and chemical resistance to the acids used in the wet under-etching step. Photoresist (PR) is then spin coated onto the samples and patterned with a mask, which consists of a grid of evenly spaced 100- $\mu\text{m}$ -sided square membranes held to rails through a pair of off-centered anchors (see Fig. 1(a)). This mask allows the formation of channels for the wet etching step and the anchors hold the membrane in place during the suspension and maintain the strain on the sample during substrate removal. The rails of the mask were aligned to run parallel to the  $[\bar{1} \bar{1} 0]$  direction (white arrows in Fig. 1), to prevent the under-etch of the rails (see section 2.3).

**Table 1. Summary of the dry process conditions.**

Process	Process gases (flow rate [sccm])	Substrate temperature [°C]	Pressure [mTorr]	Input power [W]	Total input power density [ $\text{kW m}^{-2}$ ]
PECVD	$\text{SiH}_4$ 5% v/v in $\text{N}_2$ carrier gas (170), $\text{N}_2\text{O}$ (710)	300	1000	70	2.23
RIE	Ar (15), $\text{CHF}_3$ (5)	20	30	120	3.82
ICP	Ar (4), $\text{BCl}_3$ (16)	20	6	200 (platen), 500 (coil)	89.1

The patterned PR is developed and used as a mask to transfer the pattern onto the silica using reactive ion etching (RIE) with an Oxford Instruments Plasmalab 80 Plus (see Fig. 1(bi) and (bii)). RIE of 1.2  $\mu\text{m}$  of silica is performed (see Table 1 for conditions), and the remaining PR mask is removed in a plasma asher (Matrix 105, see supplementary information) and a solvent clean. Note that the silica protects the II-VI during these steps. Inductively coupled plasma (ICP), from an SPTS Multiplex tool, is used to etch through the ZnCdMgSe, InGaAs and InP (see Table 1 for conditions). The ICP etches trenches through the II-VI material exposed by the silica mask until the trenches reach a depth of around 3  $\mu\text{m}$ , hence into the InP substrate (see Fig. 1(c) and (cii)). The silica mask etches at 80 nm/min in the ICP recipe and so it is important that a sufficient thickness is deposited initially so that the remainder provides protection during the wet under-etching step. The mask geometry used ensures a very high aspect ratio between



**Fig. 1.** a) A schematic of the mask format with an inset showing an enlarged view of the repeating unit of the mask, b) silica hardmask formation with the RIE of the pattern of membranes held by anchors to rails along  $[\bar{1} \bar{1} 0]$ , c) ICP etching of the hardmask into the InP substrate, d) conformal silica deposition to coat the sidewalls, e) RIE to open wet etch holes, f) wet etch to suspend the membranes (the first etch step of  $\text{HCl}:\text{H}_3\text{PO}_4$  is shown and sidewall protection is omitted for clarity) and g) the InGaAs etch step followed by the sidewall protection removal by RIE. i show 3D schematics of each step and ii show images of each step under white light illumination. The black scale bars represent  $100 \mu\text{m}$ . The white arrows mark the  $[\bar{1} \bar{1} 0]$  direction and the blue arrows in e) ii show the  $\langle 1 0 0 \rangle$ -like under-etch directions. Key for schematic layers: blue is the InP, orange is the InGaAs, green is the II-VI, red is the first silica deposition, white is the sidewall silica deposition.

the feature distances and the trench depths etched during the ICP stage (around 100:3) and this ensures that the ICP etched sidewalls are near-vertical.

Wet etching to suspend the II-VI layer is non-trivial; we are not aware of relevant work published on the development of wet etchants with a high selectivity between InP and ZnCdMgSe. Therefore, to protect the membrane and the rails during the wet etch, a sidewall protection scheme is used. A conformal deposition of silica into the trenches is completed, using PECVD, to coat all the sidewalls (see Fig. 1(di) and (dii)). RIE is then used to create etch holes at the base of the silica. We propose that the mechanism for this is microtrenching [23], which results in a thin layer of silica remaining on the sidewalls and trench base whilst creating small imperfections at the corner regions where the sidewalls meet the trench base (see Fig. 1(ei) and (eii)). Further, at these corner regions the silica film is under strain and therefore is susceptible to fractures that expose the InP, which allows the wet etchants to under-etch below the epitaxial layer of interest (see Supporting Information).

The wet etch is completed as a three step process at a room temperature of  $21.0 \pm 0.5 \text{ }^\circ\text{C}$ . A mixture of HCl and phosphoric acid ( $\text{H}_3\text{PO}_4$ ) (3:1 by volume) is used to selectively etch InP over InGaAs to begin the under-etch [8,9]. The under-etch (see Fig. 1(fi)) is allowed to progress for 20 minutes; Fig. 1(fii) shows the recession of InP after 15 minutes of etching. The ZnCdMgSe is

grown on the (0 0 1) face of InP, which is rapidly etched. The under-etch of the effective mask of silica/ZnCdMgSe can be seen as a recession of a dark shaded parallelogram, as the anchors impose a two-fold rotational symmetry masking on the InP under-etch directional progress. The rails are not under-etched due to their alignment with the  $[\bar{1} \bar{1} 0]$  crystallographic direction (see section 2.3), which instead etches to sloped sidewalls, of the very slow etching, (1 1 1) A faces [13]. The silica sidewall protection prevents the etchants from attacking the ZnCdMgSe, but also covers some InP under the membrane, preventing initial etching directly in the  $[1 \ 1 \ 0]$ ,  $[\bar{1} \ 1 \ 0]$ ,  $[1 \ \bar{1} \ 0]$  and  $[\bar{1} \ \bar{1} \ 0]$  directions. The etch of the membranes proceeds via etching down into the substrate along the  $[0 \ 0 \ \bar{1}]$  direction through the microtrenches, whilst simultaneously etching the InP under the membranes in the  $[1 \ 0 \ 0]$ ,  $[\bar{1} \ 0 \ 0]$ ,  $[0 \ 1 \ 0]$  and  $[0 \ \bar{1} \ 0]$  directions and upwards from the underside of the membranes towards the InGaAs etch-stop in the  $[0 \ 0 \ 1]$  direction (once the sidewall protection is under-etched). Underneath the membranes, etching proceeds along the  $[1 \ 1 \ 0]$ ,  $[\bar{1} \ 1 \ 0]$ ,  $[1 \ \bar{1} \ 0]$  and  $[\bar{1} \ \bar{1} \ 0]$  directions at a rate much slower than the  $[1 \ 0 \ 0]$ -like direction, which results in the dark parallelogram shape of the under-etch seen in Fig. 1(fii), which has faces aligned to the  $[1 \ 0 \ 0]$ ,  $[\bar{1} \ 0 \ 0]$ ,  $[0 \ 1 \ 0]$  and  $[0 \ \bar{1} \ 0]$  like directions. Here we assume that the InP etch planes are near parallel with respect to the (0 0 1) as sloped facets such as  $\{2 \ 1 \ 1\}$ , which can arise at mask edges perpendicular to  $1 \ 1 \ 0$ , have been reported to be eliminated by faster etch planes [12].

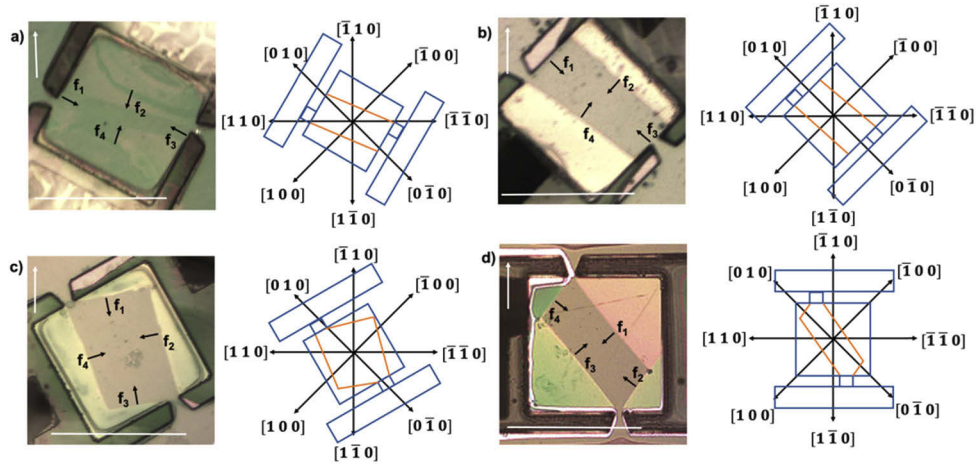
After the first etch the membrane is still held by a slow-etching InP pillar, which likely arises due to the formation of other, slower etching, crystallographic faces seeded by the anchors during the under-etch [12]. A second under-etching step is completed with HCl, which has been reported to aggressively etch  $\{1 \ 0 \ 0\}$  faces of InP [15], for 1 minute. The InP pillar is etched by the HCl whilst the InGaAs buffer layer acts as an etch stop, to prevent further vertical etching, which protects the II-VI material. Following this etch a wide v-groove can be seen in the substrate, formed by  $\{1 \ 1 \ 1\}$  faces, which completes the suspension of the membranes [17]. The added aggression of the HCl results in some damage to the II-VI at the edge of the membrane, which can be seen by the recession, in Fig. 1(fii), of the ZnCdMgSe (pink in this image) and the appearance of the InGaAs (white due to light scattering). It should be noted that the color of the membranes in the images of Fig. 1 arises from interference effects of the white light source and will depend on the illumination source used, as well as the thickness and refractive index of the layers grown.

The third step is the careful removal of the InGaAs buffer layer with minimal damage to the ZnCdMgSe. This is achieved using a 10 s hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) based etch of  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  (1:1:6 by volume) [8], which, when complete, results in the membranes changing color to green. At the end of the three-step under-etch process, the membranes are now composed of ZnCdMgSe with a protective silica layer, suspended on anchors of the original growth structure. The final step is to remove the protective silica using RIE to reveal the epitaxial growth side of the membrane. An example of a fully suspended membrane is shown in Fig. 1(gii).

### 2.3. Optimization of the suspension method

The membrane, anchors and rails each mask the InP during the wet etch and so the process is optimized to ensure that the membranes are under-etched and that the rails are minimally under-etched. Figure 2 shows etch tests of our mask structure when rotated through  $30 \pm 1^\circ$ ,  $45 \pm 1^\circ$ ,  $60 \pm 1^\circ$  and  $90 \pm 1^\circ$  from the  $[\bar{1} \ 1 \ 0]$  direction towards  $[\bar{1} \ \bar{1} \ 0]$  and shows how the geometry of the full mask influences the etching of a square membrane. The anchors mask the edges of the membrane and prevent inward etching of the membrane, which pins the under-etch to specific sites.

The optimum mask alignment gives maximum exposure to  $\langle 1 \ 0 \ 0 \rangle$  etch faces, to ensure a complete under-etch [12,24]. Table 2 summarizes the findings displayed in Fig. 2. For the under-etching InP we have defined recession faces,  $f_n$ , shown in Fig. 2 with an angle from  $[\bar{1} \ 1 \ 0]$



**Fig. 2.** The response of the InP under-etch as a function of mask orientation. The orientation angles from  $[\bar{1} 1 0]$  towards  $[\bar{1} \bar{1} 0]$  and processing stages shown are a)  $30 \pm 1^\circ$  during InP etching, b)  $45 \pm 1^\circ$  during InP etching, c)  $60 \pm 1^\circ$  during InP etching, and d)  $90 \pm 1^\circ$  after an InGaAs etch. The process stages in the images were chosen for each angle according to their clarity. (Note that a) and b) were taken with slightly lower image quality.) The white arrow shows the  $[\bar{1} 1 0]$  direction and the white scale bar represents  $100 \mu\text{m}$ . To the right of each image is a schematic clarifying the crystallographic evolution of the angular dependent wet etch progress. The blue and orange lines represent the mask outline and the InP recession faces respectively. The recession face directions,  $f_n$ , are marked on each image.

shown in Table 2. From the recession angles of the InP faces with respect to  $[\bar{1} 1 0]$  it is possible to calculate the crystallographic direction of the receding faces, also shown in Table 2.

**Table 2. Directions of the recession faces of InP during the wet under-etch of the square membranes with varied mask orientation. Directions are given as an angular magnitude from  $[\bar{1} 1 0]$  and a corresponding crystallographic direction.**

Rail orientation from $[\bar{1} 1 0]$ to $[\bar{1} \bar{1} 0]$ [°]	Magnitude of the recession face angles from $[\bar{1} 1 0]$ and recession direction <sup>b</sup> , $f_n$ [°]			
	$f_1$	$f_2$	$f_3$	$f_4$
30	$60^a$	18	$60^a$	18
	N/A	$[2 \bar{1} 0]$	N/A	$[\bar{2} 1 0]$
45	$45^a$	41	$45^a$	37
	N/A	$[1 0 0]$ -like	N/A	$[\bar{1} 0 0]$ -like
60	13	77	9	69
	$[2 \bar{3} 0]$	$[3 2 0]$	$[\bar{3} 4 0]$	$[\bar{7} \bar{3} 0]$
90	47	53	52	54
	$[1 0 0]$ -like	$[0 1 0]$ -like	$[\bar{1} 0 0]$ -like	$[0 \bar{1} 0]$ -like

<sup>a</sup>Denotes a static (non-etching) direction.

<sup>b</sup>The crystallographic directions given take into account a  $\pm 1^\circ$  uncertainty in the mask orientation.

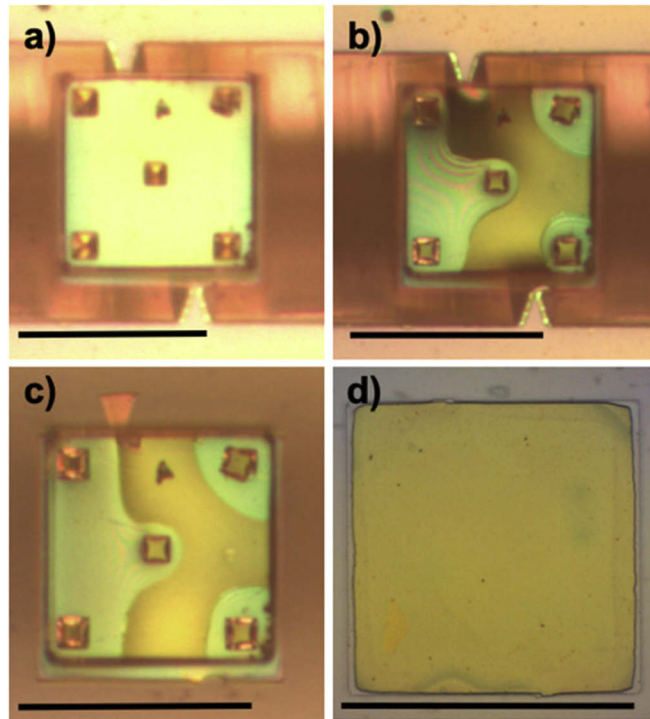
For a perfect  $\langle 1 0 0 \rangle$  under-etch, all recession faces should have a recession angle magnitude of  $45 \pm 1^\circ$  from  $[\bar{1} 1 0]$ . Previous work has shown that the ideal alignment for the under-etch of the square membranes alone would be to set the square edges perpendicular to the  $\langle 1 0 0 \rangle$  directions [12], however the inclusion of anchors and rails complicates this by adding extra mask features. From Table 2 the  $30^\circ$  (Fig. 2(a)) and  $60^\circ$  (Fig. 2(c)) alignments from  $[\bar{1} 1 0]$  towards

$[\bar{1} \bar{1} 0]$  only etch along high-order crystallographic directions and the  $30^\circ$  alignment also exhibits very little etch activity along the  $f_1$  and  $f_2$  etch directions due to the sidewall protection silica blocking the relatively small gap between the membrane and the rails in the mask design.

The alignments of  $45^\circ$  (Fig. 2(b)) and  $90^\circ$  (Fig. 2(d)) from  $[\bar{1} 1 0]$  towards  $[\bar{1} \bar{1} 0]$  allow InP etching along wholly  $\langle 1 0 0 \rangle$  (or  $\langle 1 0 0 \rangle$ -like) directions, but with important differences:  $45^\circ$  alignment positions the rails for under-etching along the  $[0 1 0]$  and  $[0 \bar{1} 0]$  directions, which would be highly disadvantageous for strain maintenance on the membrane as we require the anchors and rails to be as robust as possible. In contrast,  $90^\circ$  alignment (Fig. 2(d)) sets the rails perpendicular to the slow etching  $[\bar{1} 1 0]$  and  $[1 \bar{1} 0]$  directions, which greatly slows any under-etching. Interestingly,  $45^\circ$  (Fig. 2(b)) alignment prevents any under-etching along the  $[0 1 0]$  and  $[0 \bar{1} 0]$  directions, which is due to the sidewall protection silica blocking the etch gap, as described for the  $30^\circ$  orientation (Fig. 2(a)). This etching along only two directions of the possible  $\langle 1 0 0 \rangle$  set is disadvantageous for reducing etch time. It would be possible to increase the anchor length in the mask design to allow the full RIE etching of the sidewall protection between the membrane and the rails, however this would increase the mechanical moment on the anchor, which could compromise its strength during the under-etch or could allow for unwanted membrane bowing which would encourage strain changes. The  $90^\circ$  alignment (Fig. 2(d)) has no blocked etch directions, but it exhibits under-etching along faces which are not purely  $\langle 1 0 0 \rangle$ . The small angular difference (taking into account the uncertainty) between these  $\langle 1 0 0 \rangle$ -like and a pure  $\langle 1 0 0 \rangle$  face means that these higher order faces are comprised mostly of  $\langle 1 0 0 \rangle$ , which gives them similar under-etch properties to  $\langle 1 0 0 \rangle$ . The  $90^\circ$  alignment (Fig. 2(d)) provides the closest results to the ideal case and is selected for the under-etch process. We note that previous work by Cich *et al.* found that for InGaP etched in HCl the maximum under-etch rate has a twofold symmetry about  $[1 0 0]$  along  $55^\circ$  and  $125^\circ$  from  $[0 1 1]$  towards  $[0 \bar{1} 1]$ , only  $10^\circ$  off  $\langle 1 0 0 \rangle$  directions [25], similar to our observations for the binary InP. The InP recedes along the directions of maximum undercut when the rail orientation is set to  $90^\circ$  and we observe the  $f_4$  and  $f_3$  face angles at  $55 \pm 1^\circ$  and  $128 \pm 1^\circ$  degrees from  $[\bar{1} 1 0]$  to  $[1 1 0]$  respectively, and similarly for  $f_1$  and  $f_2$  face angles at  $54 \pm 1^\circ$  and  $124 \pm 1^\circ$  degrees from  $[\bar{1} 1 0]$  to  $[\bar{1} \bar{1} 0]$  respectively.

#### 2.4. Membrane detachment via transfer printing

A desktop nanolithography platform (NanoInk NLP 2000) adapted into a home-built transfer print machine is used to transfer print suspended ZnCdMgSe membranes onto a diamond heatspreader. Diamond was chosen because of its excellent thermal transport properties and previous successful demonstration as a heatspreader [18]. Both flat,  $100\text{-}\mu\text{m}$ -sided, square tip stamps and pyramidal style  $100\text{-}\mu\text{m}$ -stamps, used in previous investigations [19], were found to be effective for the transfer print. The shaped stamp was pressed onto the membrane and, owing to its viscoelasticity, adhered to the membrane. The pressing breaks the anchors, freeing the membrane from the growth wafer so that it can be transferred. Figure 3(a) shows the stamp as the pressing begins and Fig. 3(b) shows the stamp adhesion taking place. After pressing to liberate the membrane from the anchors (see Fig. 3(c)), it is free to be moved to a new acceptor substrate. The flatness and surface roughness of the diamond used as a substrate in this work does not always favor direct Van der Waals bonding and therefore a solvent wetting layer is often used to conform the membrane into a strong contact with the diamond as it evaporates [26]. A layer of isopropanol is carefully deposited onto the accepting surface of the diamond and left to evaporate so that a thin layer of the solvent remains [18]. The membrane is then pressed onto the diamond and the PDMS stamp slowly withdrawn. A transfer-printed membrane of ZnCdMgSe on diamond is shown in Fig. 3(d). The transparent edge visible on the side of the membrane is the remains of the sidewall protection of protective silica.



**Fig. 3.** Transfer printing with a PDMS stamp, patterned with a 100- $\mu\text{m}$ -sided square tip with pyramid features [19]. a) A suspended membrane of ZnCdMgSe, imaged through the PDMS stamp before contact. b) The PDMS stamp is pressed into contact with the membrane. The brown surface seen through the stamp shows the progression of the increased stamp contact during the fast pressing. c) The membrane adheres to the stamp and the supporting anchors are broken, liberating the membrane. The quaternary membrane is translated to a diamond heatspreader, following isopropanol wetting, and pressed into surface contact. The quaternary membrane preferentially capillary bonds to the diamond surface. d) A 500-nm-thick ZnCdMgSe membrane transfer-printed onto a diamond. The black scale bars represent 100  $\mu\text{m}$ .

### 3. Membrane characterization

From Fig. 1(gii) and Fig. 3(d) it can be seen that during the under-etch and the release from the growth wafer the membrane does not fracture or curl. During the growth of the II-VI a very small compressive strain is inherent but, as the strain is maintained by the anchors and PDMS during the processing, there is no visible sign of deformations or cracking related to strain release.

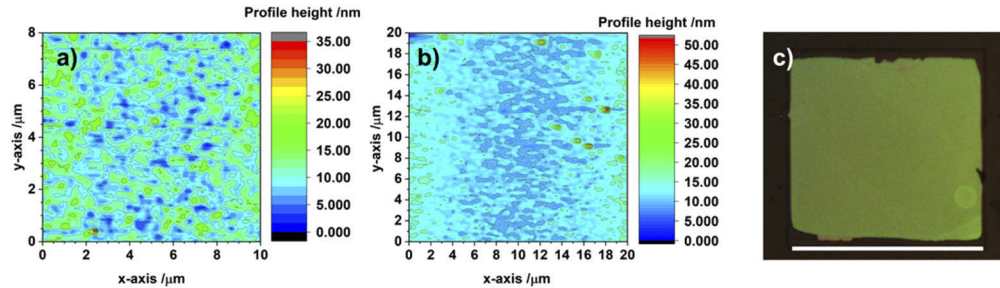
#### 3.1. Atomic force microscope measurements

Low surface roughness in processed films is essential for optimal device performance, forming the strongest capillary bonds and maximizing heat flow from active components. Atomic force microscope (AFM) measurements of the wet etch and epitaxial surfaces of the membranes were performed on an XE-100 Park Systems AFM. The AFM tip used was n-type silicon with an aluminum backside coating (NSC15). The full angle of the tip was  $40^\circ$  and the resonant frequency of the tip was 325 kHz. A “true non-contact tapping mode” was used for the AFM measurements. The epitaxial side of the membrane was measured following the transfer print onto diamond, whereas the etch side was measured by detaching membranes post wet etch (pre-RIE of the



topside silica) using an un-patterned piece of PDMS and then measuring the surface profile of the membrane while adhered to the PDMS.

The surface roughness of the epi-side membrane face was found to have a root mean square (RMS) value of  $\sim 1$  nm over a relatively large  $80 \mu\text{m}^2$  test area, and the etch side RMS roughness was  $\sim 2$  nm, over a much larger  $400 \mu\text{m}^2$  test area. The AFM profiles are shown in Fig. 4(a) and Fig. 4(b), along with an image of the etch side surface of a detached membrane in Fig. 4(c).



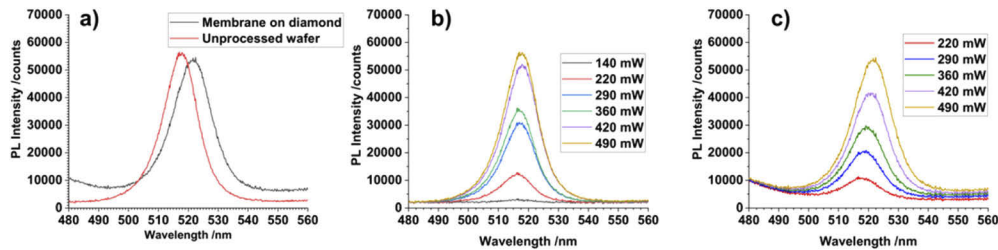
**Fig. 4.** An AFM surface profile of a) the epitaxial growth side of the ZnCdMgSe which has been transfer-printed onto diamond and b) the etch side of the membrane, shown etch side up in c). c) An image of the wet etch (under-etch) surface of the ZnCdMgSe sample, which still has a protective silica layer on its epitaxial side, that has been flipped etch-side-up and is held on PDMS. The white scale bar represents  $100 \mu\text{m}$ .

To the best of our knowledge, there are no previous reports of epitaxial lift-off methods for II-VI semiconductors producing films with an RMS surface roughness of  $< 2$  nm. We propose that the high surface quality originates primarily from the geometry used in this method: ELO of smaller, as opposed to large, scale membranes. Reducing the etch time with smaller membranes decreases the likelihood of epitaxial layer etch damage due to sidewall protection breach and means that less aggressive etchants can be used within a realistic etch time window. In this work the total wet etch time was around 20 minutes. Unlike previously reported II-VI ELO methodologies [5,8,27], the etching of InP is not on the same scale or depth, so uncontrollable etch pits do not form and cause InGaAs micromasking. This means that the subsequent high selectivity etch of InGaAs from ZnCdMgSe yields a very flat surface and enables the fabrication of ZnCdMgSe membranes suitable for transfer printing.

### 3.2. Photoluminescence measurements

The unprocessed sample had no heatspreader and was clamped in a brass mount maintained at  $10^\circ\text{C}$ , with indium foil on the substrate side of the wafer to ensure a good thermal contact with the mount. The membrane on diamond was mounted in identical conditions, with the indium foil on the opposite face of the diamond to the membrane; the membrane was only in contact with the diamond. Each sample was pumped with up to 500 mW optical power at 447 nm (Laserglow LRD-0447 laser-diode) in a  $238 \times 182 \mu\text{m}$  focus spot ( $3.6 \text{ MWm}^{-2}$ ). PL measurements, shown in Fig. 5, were collected at normal incidence to the sample surface using a 15 mm focal length lens and a pump blocking filter to couple light into a 600 micron core fiber connected to a spectrometer (Ocean Optics USB 4000) with an integration time of 500 ms.

A series of basic photoluminescence (PL) measurements were completed to further assess a processed membrane printed on diamond in comparison with an equivalent sample from the unprocessed wafer. Firstly, we note that a quantitative comparison in peak PL signal between the two samples, shown in Fig. 5(a), should be treated with caution due to changes in the measurement conditions, such as the absence of back reflections from the InGaAs layer in the case of the membrane PL. Nevertheless the strong PL signal after processing is indicative of the absence of



**Fig. 5.** a) A comparison of the PL spectra of the growth wafer (red) and the membrane on diamond (black), both cooled with a heatsink temperature of 10 °C and pumped at an intensity of around  $3.6 \text{ MWm}^{-2}$ . Intensity dependent photoluminescence measurements of b) the as-grown ZnCdMgSe on InP and c) the ZnCdMgSe membrane on diamond, both cooled with a heatsink temperature of 10 °C.

significant additional non-radiative defect states being introduced during the processing. We can, however, determine a significant red-shift in central peak position for the transferred membrane compared with the unprocessed wafer. By measuring the intensity dependent photoluminescence (IDPL) of the unprocessed sample and membrane, shown in Fig. 5(b) and (c) respectively, we attribute this shift to greater pump-induced heating in the membrane, due to imperfect contact with the diamond. Increasing the pump power linearly increases the heat load on the membrane (assuming a constant quantum defect and temperature independent absorption coefficient) and the heating of the ZnCdMgSe shifts the bandgap in a Varshni relation [28,29].

The as-grown wafer experienced a small  $\sim 1$  nm redshift for an increase in pump intensity from  $1.0 \text{ MWm}^{-2}$  to  $3.6 \text{ MWm}^{-2}$ , whereas Fig. 5(c) shows the approximately 4-nm redshift measured during an increase of the pump intensity from  $1.6 \text{ MWm}^{-2}$  to  $3.6 \text{ MWm}^{-2}$  for the membrane on diamond. For the unprocessed sample the substrate acts as a large heatsink, however, the bond between the diamond and the ZnCdMgSe membrane has an unknown thermal impedance that is a function of the bond quality. An imperfect bond would therefore limit heat transfer from the pumped region and is likely the majority source of the membrane PL redshift [9]. Previous work with GaN LEDs has shown that good thermal contact can be achieved via transfer-printing to diamond for the same sample area as that used in our work [18]. Future work will focus on improving the transfer print technique to optimize the bond between the II-VI and diamond, e.g. using different patterned PDMS stamps, to assist release from the carrier, and thermal annealing techniques.

#### 4. Discussion

Previous transfer print methodologies have reported the release and transfer print of devices from InP substrates using a layer of InGaAs as a laterally-etched release layer and by exploiting the high etch selectivity between  $\sim 1 \mu\text{m}$  of doped InGaAs and InP-based device layers [30,31]. For an ELO method to be truly applicable to release any device from an InP substrate this high etch selectivity assumption cannot be made and is especially invalid with II-VI materials which have an etch selectivity in peroxide based etchants which is at least 1–2 orders of magnitude lower than InGaAs/InP [8,31]. For lateral etching of an InGaAs release layer an extremely high etch selectivity is required otherwise chemical damage will likely occur to the epitaxial layers of interest. The benefit of our technique is that vertical etching of an InGaAs layer requires a much shorter etch time, several seconds rather than tens of minutes, and the InGaAs is removed as a uniform front, which reduces the likelihood of etching a curvature into the epitaxial layers. Even for materials with a low etch selectivity to InGaAs, the well-known etch rate, with  $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2$  based etches, and short vertical etch time will keep the etch damage roughness to a minimum.

We propose that the membrane size could be increased to a size dictated by the anchor strength without any deterioration, as long as the sidewall protection and the InGaAs buffer layer protect the ZnCdMgSe. The buffer layer thickness could also be increased to afford extra protection for larger membranes. This will be a subject of future investigations.

The use of the substrate as an effective release layer has advantages over other release layers, such as MgTe [11], which have a large lattice mismatch with ZnCdMgSe, leading to a high level of defects in the target epitaxial layers [32]. The growth of telluride binaries on the III-V interface of an InGaAs buffer layer on InP introduces strain in the base of the structures, which can lead to more complex device designs and epitaxial layer strain changes during ELO. The methodology presented removes any requirement for intentionally grown release layers.

The II-VI material system contains magnesium which, when in high concentrations in the quaternary, can yield a very slow yet total oxidation of the device in atmospheric conditions. Silica sidewall protection can be removed using oxygen-free plasmas, unlike thick photoresist which is often used for sidewall passivation. Photoresist stripping requires oxygen-based plasmas that could quickly oxidize the II-VI, and even a thorough solvent-based removal may leave residues or cause premature and unintended device release. The silica sidewall protection removal using Ar:CHF<sub>3</sub> plasmas avoids any oxidation risk at the expense of a small risk of physical sputtering damage to the surface of the epitaxial layers. Physical etch damage can be negated by using a silica on silicon reference sample and white light reflectance spectroscopy to carefully monitor the progress of the silica removal. Our AFM measurement of the epitaxial surface in Fig. 4(a) shows that there is minimal surface roughness and that any physical sputter damage does not increase the RMS surface roughness far above 1 nm. A downside to the silica sidewall protection is that it may be damaged by etch materials that produce much gas, such as the significant phosphine production during the HCl etch of InP. Future work will be carried out on the development of an alternative method of silica-based sidewall protection that is more robust.

The suspension of ZnCdMgSe provides an opportunity to study the physical properties of this novel material in a highly controlled environment. Suspending membranes from the growth substrate (whilst maintaining the strain) and depositing gold contacts onto the anchors could allow for novel measurements of the thermal and electrical conductivity and the Hall Effect in II-VI or III-V materials without influence from the growth substrate [33,34]. Suspended membranes could also prove ideal for testing the mechanical strength of epitaxial layers using AFM cantilever deflection, such as measuring the Young's Modulus [24,35].

Future work will involve the processing of more complex II-VI structures, such as multi-quantum-well (ZnCdSe/ZnCdMgSe) gain films, and the incorporation of these components in novel 'green gap' photonic devices. For devices which currently operate as single released membranes, such as DBR-free VECSELs or solar cells [36,37], this technique has the potential for controllable miniaturization and easy integration of these technologies.

## 5. Conclusion

We present a method for the suspension and transfer printing of II-VI on InP (ZnCdMgSe) membranes that requires no specifically engineered epitaxial release layer, no organic based sidewall protection, and is relatively independent of the etch selectivity of the III-V buffer layer (InGaAs). Our optimization of the suspension method with respect to InP makes use of aligning the rails, which hold the membranes, along the  $[\bar{1} \bar{1} 0]$  direction to ensure a full membrane under-etch whilst preventing the under-etch of the rails. We demonstrate the first transfer print of high quality II-VI membranes onto non-native substrates, showing that nanometer scale surface roughness is achieved on both sides of the membranes. 500-nm-thick, 100 × 100 μm<sup>2</sup> square membranes of ZnCdMgSe were transferred to transparent diamond heatspreaders, achieving optical contact with no observable flexing or fractures occurring during transfer. Photoluminescence measurements revealed an intense peak at ~520 nm under optical pumping

at 447 nm, with a 4 nm redshift induced over  $3.6 \text{ MWm}^{-2}$  incident pump intensity. The high quality membranes show the potential for this method to be a powerful tool for miniaturizing and carefully positioning membranes of any device grown on InP with an InGaAs buffer layer. Further development of this technique will be carried out with a target of processing high quality ZnCdSe/ZnCdMgSe multi-QW membranes for use in novel ‘green-gap’ photonic devices, such as color conversion of LEDs.

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Data related to this publication have been made available at the University of Strathclyde data repository [38].

## Disclosures

The authors declare no conflicts of interest.

See [Supplement 1](#) for supporting content.

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