A Single-end Protection Scheme for Hybrid MMC HVDC Grids Considering the Impacts of the Active Fault Current-limiting Control

Saizhao Yang, Wang Xiang, *Member, IEEE*, Meng Zhou, Wenping Zuo, Jinyu Wen, *Member, IEEE*

***Abstract*- In the hybrid modular multilevel converter (MMC) based high voltage direct current (HVDC) systems, the fault current can be actively suppressed by the converter itself, which endows a smaller requirement for current-limiting reactors (CLR) and a larger time margin for fault detection algorithms, comparing with the half-bridge MMC. But the robustness to fault resistance and noise disturbance of existing boundary protection schemes will be deteriorated with small CLRs. Moreover, the fast response of the fault current-limiting control will change the output DC voltage of hybrid MMC, which affects the fault characteristics and may cause mal-operation of existing protection algorithms. Thus, a single-end protection scheme considering the impacts of the active current-limiting control is proposed for the hybrid MMC based DC grids. The traveling-wave characteristics under different fault stages are analyzed to evaluate the impacts of the fault current-limiting control. In addition, a coordination protection strategy versus different fault conditions is adopted to improve reliability. Various cases in PSCAD/EMTDC are simulated to verify that the proposed method is robust to fault resistance, fault distance, power reversal, AC faults, and immune to noise.**

***Index Terms*— Hybrid MMC, DC line protection, the active current-limiting control, the forward traveling-wave, fault characteristic analysis.**

I. Introduction

With the merits of flexibility and reliability, the modular multilevel converter (MMC) based DC grid using overhead lines transmission is promising to integrate large-scale wind power and solar energy over long-distance [1][2]. There are two main approaches to construct the DC grid topology: 1) The half-bridge (HB) MMC with large-capacity fast-speed DC circuit breakers (DCCB). 2) The fault-tolerant MMC with low-capacity DCCBs or mechanical disconnectors. For the first approach, the speed of the selective protection scheme should be ultra-fast (less than 3ms) since the HB-MMC is vulnerable to DC faults, which is a great challenge for the protection scheme. On the other hand, the large-capacity DCCBs will increase the cost. Hence, the reliability of the DC fault protection scheme and the cost of DCCBs hamper the development of HB-MMC based DC grids [3][4].

Various fault-tolerant MMCs have been proposed to handle the DC faults by taking advantage of converter topologies, such as the self-blocking sub-modules (SM) in [5], the clamping-double SM in [6] and the hybrid MMC in [7]. The hybrid MMC consisting of HB SMs and full-bridge (FB) SMs in series connection can reduce the output DC voltage by negatively inserting the full-bridge FB SMs, thereby suppressing the DC fault current. This approach achieves DC fault ride-through without blocking the SMs and provides reactive power support during DC faults. As a preferred solution to deal with DC faults, the hybrid MMC technology is being applied to China's first three-terminal hybrid HVDC *Kunliulong* project.

Currently, most of the research is focusing on the fault control design of hybrid MMC, such as the enhanced independent pole control in [8], the additional phase angle control in [9], and the active fault current limiting control (ACLC) in [10]. During DC faults, the fault current rises to a large amplitude within several milliseconds, which imposes great stress on the safe operation of semiconductors. To avoid damage from overcurrent, all hybrid MMCs of DC grids will suppress the fault current by their fault current limiting control. Considering that the short-circuit fault still exists, a selective DC fault detection method is required to isolate the faulty lines, thereby avoiding a shutdown of the entire DC grid. But suitable protection schemes are rarely reported in existing publications. A current differential protection scheme is employed in [11] to achieve selective fault protection. However, the proposed method is easily affected by the line distributed capacitor current and the reliability will be decreased under pole-to-ground (PTG) faults with high fault resistances. Additionally, these pilot protection schemes are highly dependent on the communication between stations, which is vulnerable to the data code and synchronization errors [12].

For hybrid MMC HVDC systems, existing single-end protection algorithms are originated from the protection schemes of HB-MMC HVDC systems. These protection algorithms rely on large current-limiting reactors (CLR) to provide the boundary effect. As pointed out in [11], for existing protection schemes, large CLRs (over 100mH) are adopted to enable high selectivity and reliability. Various simulation results also demonstrate that 200mH or larger CLRs are required to guarantee the robustness to large fault resistance and noise disturbance [13]-[16]. However, since the fault current can be suppressed by the ACLC, smaller CLRs are adopted in hybrid MMC HVDC systems, which weaken the boundary effect. On the other hand, for HB-MMC HVDC systems, the speediness of fault protection algorithm is the top

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concern. Due to the fast detection speed, there lacks coordinated protection against different fault conditions. For hybrid MMC HVDC systems, a larger time margin is allowed for fault detection, which provides a potential solution to improve the reliability by the protection coordination. However, there still exist some challenges to be addressed. For example, the protection roles versus different fault conditions need to be well defined. Besides, the operation time and threshold determination of different fault protection criteria need to be coordinated.

Moreover, the impacts of fault current limiting on protection algorithms remain an unsolved problem. During DC fault analysis, the HB MMC is often simplified as a constant voltage source [17][18] at DC side. The fault traveling wave is the main indicator to design the protection algorithm [19]. However, for hybrid MMC based DC grids, the ACLC will quickly decrease the MMC output voltage to respond to the rapid drop of the DC line voltage. Thus, the hybrid MMC is equivalent to an adjustable voltage source at DC side. And the impacts of the ACLC should be considered to design the protection scheme.

To address these challenges, a two-stage coordinated protection strategy is proposed to improve the robustness under different fault conditions and a detailed fault characteristic analysis with ACLC is carried out in this paper. According to different fault stages, the impacts of the ACLC on fault traveling-wave (TW) characteristics are evaluated. Then, the forward TWs under different fault locations are analyzed to design the criterion for fault detection.

The remainder of this paper is structured as follows. Section II introduces the principle of the hybrid MMC and the ACLC. The TW characteristics under different fault stages and locations are analyzed in Section III. Then, the two-stage protection scheme that considers the impacts of the ACLC is proposed in Section IV. Finally, the effectiveness and robustness of the proposed method are verified under extensive cases in Section V and VI.

II. Operating Principle of the Hybrid MMC and the Active Current-limiting Control

A. Operating Principle of the Hybrid MMC

Fig. 1 shows the equivalent circuit of the hybrid MMC in single phase view. Each arm contains N_F FBSMs and N_H HBSMs in series connection. For FBSMs, they can output negative voltages when they are negatively inserted.

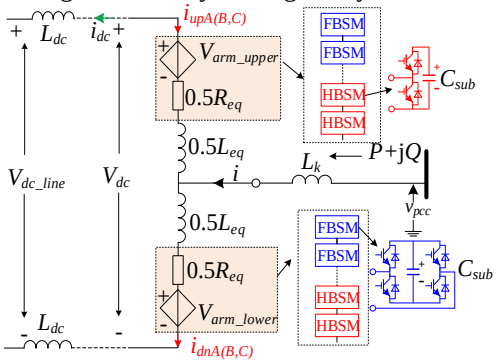


Fig. 1 The single-phase view of hybrid MMC.

Assuming the rated DC voltage is V_{dcn} and the AC modulation ratio is M_{ac}, the output AC voltage v_{pcc} is [8]:

$$v_{pcc}=M_{ac}\frac{V_{dcn}}{2}\cos(\omega t+\varphi_{ac}) \tag{1}$$

Supposing the DC modulation ratio to be M_{dc}, the MMC output DC voltage V_{dc} yields:

$$V_{dc}=M_{dc}V_{dcn} \tag{2}$$

where N_F is equal to N_H and M_{ac} is selected to be 0.9. According to [8], M_{dc} is ranging from -0.1 to 1. Thus, the MMC output DC voltage V_{dc} satisfies:

$$-0.1V_{dcn}\le V_{dc}\le V_{dcn} \tag{3}$$

As can be seen from equations (1)-(3), the hybrid MMC can operate normally with lower output DC voltages and the controls between AC side and DC side are independent.

B. The Principle of the Active Current-limiting Control

The diagram of a typical active current-limiting control (ACLC) for the hybrid MMC is depicted in Fig. 2 [10]. In Fig. 2, per-unit values are adopted to design the ACLC so that the system parameters have no impacts on the controller. For example, V_{dcref} is the DC voltage reference of the constant DC voltage control and it is a per-unit value. V_{dcpu} (V_{dcpu}=V_{dc}/V_{dcn}) is the per-unit value of measured DC voltage.

Compared with the HB MMCs, the hybrid MMCs have more control freedoms. To guarantee the sub-module capacitor voltage balance during DC faults, the *d*-axis (M_d) AC control loop adopts the average capacitor voltage control. For *q*-axis (M_q), the reactive power control is employed.

Under normal operation, the DC control loop (M_{dc}) adopts the constant DC voltage control (mode I) or the active power control (mode III). In the event of DC faults, to suppress the fault current and reduce the breaking capacity of DCCBs, the DC current control (mode II) is adopted. I_{dcref} is selected to be 0. The criterion to select mode II selection is:

$$\frac{dV_{dc}}{dt}<DV_{set} \tag{4}$$

where V_{dc} is the MMC output DC voltage and DV_{set} is the threshold for the mode II selection.

As shown in Fig. 2, to achieve fast fault isolation and post-fault recovery, the voltage feed-forward control K_{FF}*V_{dcpu} is adopted to quickly respond to the rapid drop of the DC voltage [10]. The voltage feed-forward control will adjust the DC component of the arm voltage, thereby decreasing the DC fault current.

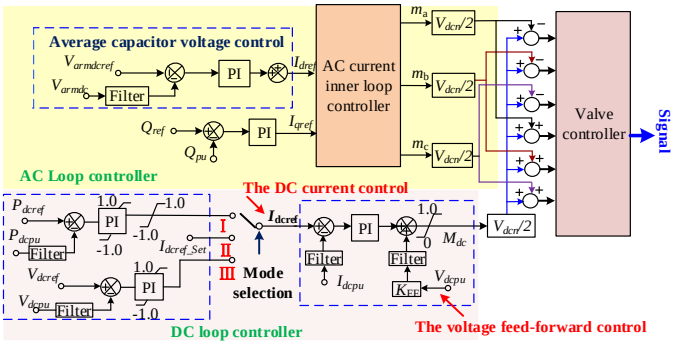


Fig. 2 The active fault current-limiting control diagram of the hybrid MMC.

III. Analysis of TW Characteristics under Different Fault Stages and Locations

A. The TW Characteristic Analysis under Different Fault Stages

Under DC faults, a negative voltage source $-V_0$ is superimposed on the fault point [20]. The voltage $-V_0$ propagates toward the transmission line (OHL) terminal and is reflected at the current-limiting reactor, as shown in Fig. 3.

The change of the DC line voltage V_{dc_line} (ΔV_{dc_line}) can be expressed as:

$$\Delta V_{dc\_line}=V_f\left(t-\frac{x}{v}\right)+V_b\left(t+\frac{x}{v}\right) \tag{5}$$

where V_f and V_b represent the forward TW in the positive direction and the backward TW in the negative direction of x-axis respectively. The specific TW analysis under different fault stages will be conducted as follows.

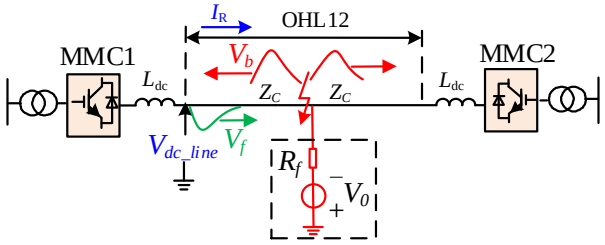


Fig. 3. The diagram of the reflection and refraction of the fault TW.

1) *First stage: the initial TW propagation*

Denote the first negative backward TW from the fault point as V_b^1. The initial backward TW V_b^1 will be reflected at the terminal of OHL. The reflected TW is forward and denoted as V_f^1. The initial TWs V_b^1 and V_f^1 can be calculated as [21]:

$$\begin{cases} V_f^1=\left[\dfrac{2Z_C}{Z_C+Z_{eq}}\times e^{\frac{-t}{T_L}}+\dfrac{Z_{eq}-Z_C}{Z_C+Z_{eq}}\right]\times V_b^1 \\ V_b^1=\dfrac{Z_C\times(-V_0)}{Z_C+2R_f}e^{-\gamma x} \end{cases} \tag{6}$$

where R_f and Z_C represent the fault resistance and the wave-impedance of the OHL, respectively. x is the fault distance. γ is the propagation coefficient, which represents the attenuation characteristics of OHL. For two-terminal systems, Z_{eq} represents the equivalent impedance of MMC. For meshed DC grids, considering multiple parallel lines connected to the same DC busbar, the equivalent impedance of parallel lines connected to the same DC busbar should also be accounted into Z_{eq}. T_L is the time constant, which can be expressed as:

$$T_L=\frac{L_{dc}}{Z_C+Z_{eq}} \tag{7}$$

Based on equations (5)-(7), the change of the DC line voltage (ΔV_{dc_line}) can be obtained as:

$$\Delta V_{dc\_line}=V_f^1+V_b^1=\left[\frac{Z_C}{Z_C+Z_{eq}}\times e^{\frac{-t}{T_L}}+\frac{Z_{eq}}{Z_C+Z_{eq}}\right]\times 2V_b^1 \tag{8}$$

As can be seen from equation (8), the DC line voltage V_{dc_line} drops rapidly once TW V_b^1 arrives at the terminal of the OHL.

Denote the time when the initial backward TW V_b^1 arrives at the terminal of OHL as t_1. With the delay for the voltage derivative measurement, the reference of the DC current I_{dcref} shifts to zero. Meanwhile, the voltage feed-forward control perceives the rapid drop of DC voltage. At t_2, the ACLC consisting of the DC current control and the feed-forward control starts to respond to the change of the DC voltage. After the response delay of the pole controller, M_{dc} is adjusted quickly so as to reduce the DC component of the arm bridge voltage V_{armdc} at t_3. Subsequently, the valve controller acts to insert some FBSMs negatively, thereby decreasing the MMC output voltage at t_4. The overall response process of the ACLC is depicted in Fig. 4.

The total response delay for the ACLC (t_4-t_1) is ranging from 0.5ms to 1ms [10], where the total response means the interval from ACLC activation to the reduction of M_{dc}. The PI parameters of the controllers have an impact on the response delay (t_4-t_1). Due to plenty of energy-storage elements (the line inductances and capacitors) and the current-limiting reactors (CLRs), the voltage V_{dc_line} will not be affected by the ACLC immediately. After a short delay, the ACLC affects the DC line voltage V_{dc_line} at t_5, leading to the further drop of the voltage V_{dc_line}. The time interval between t_1 and t_5 is ranging from 1ms to 2ms and it is defined as the initial TW stage.

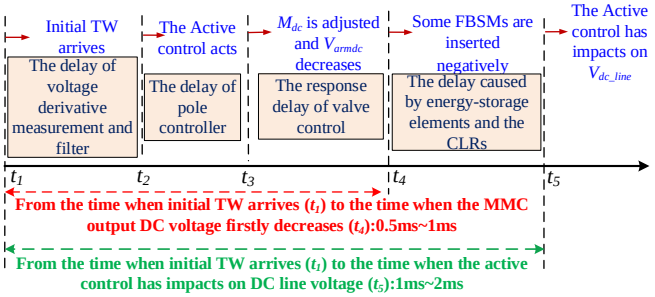


Fig. 4. The overall response process of the active current-limiting control.

During the initial TW stage (t_1~t_5), due to the response delay, the influence of ACLC is negligible. The fault characteristics are predominantly determined by the reflection and refraction of the TWs. As shown in Fig. 5, the initial forward TW V_f^1 propagates towards MMC2 and is reflected again at the fault point. The reflected wave will travel back to the terminal of OHL while the refracted wave will continue to propagate towards MMC2. Thus, there exist multiple TW reflections and refractions during the initial TW stage.

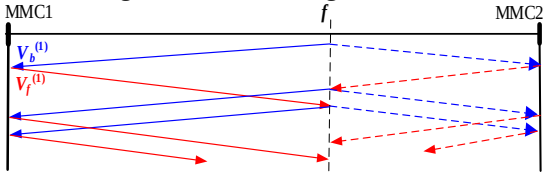


Fig. 5. The diagram of multiple traveling-wave reflections and refractions.

Considering that the dispersion effect of OHL on TWs and the amplitude of the reflection coefficient is smaller than 1, the initial TWs (V_f^1 and V_b^1) are dominant.

2) *Second stage: the impact of ACLC*

During the second stage, the ACLC will affect the fault characteristics.

During DC faults, the upper and lower arms of hybrid MMC can be equivalent as a controllable voltage resource, as shown in Fig. 6. Where I_{dc} is the DC current and I_{dcn} is the rated DC current. V_{dc_line} is the DC line voltage at the terminal of the OHL. L_{eq} and R_{eq} are the equivalent inductance and resistance of the MMC respectively. R_0 and L_0 are the arm bridge resistance and arm inductance of MMC, respectively.

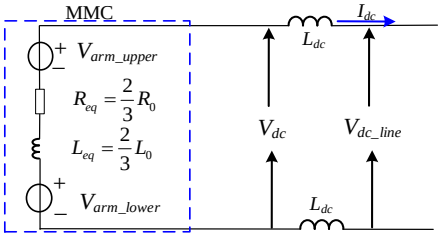


Fig. 6 The equivalent circuit of the hybrid MMC under DC faults.

The MMC output DC voltage V_{dc} can be calculated as:

$$V_{dc}(s)=2sL_{dc}I_{dc}(s)+V_{dc\_line}(s) \tag{9}$$

Based on the equivalent circuit in Fig. 6, it yields,

$$V_{arm\_upper}(s)+V_{arm\_lower}(s)=(sL_{eq}+R_{eq})I_{dc}(s)+V_{dc}(s) \tag{10}$$

where V_{arm_upper} and V_{arm_lower} are the DC components of the upper and lower arm voltages respectively. They can be calculated as:

$$V_{arm\_upper}(s)+V_{arm\_lower}(s)=M_{dc}(s)V_{dcn} \tag{11}$$

Thus, the DC current I_{dc} can be expressed as:

$$I_{dc}(s)=\frac{M_{dc}(s)V_{dcn}-V_{dc}(s)}{sL_{eq}+R_{eq}} \tag{12}$$

According to Fig. 2, the block diagram of the ACLC can be obtained, as shown in Fig. 7. We have,

$$(I_{dcref}-\frac{I_{dc}}{I_{dcn}})(k_{pi}+\frac{k_{ii}}{s})+\frac{K_{FF}V_{dc}}{V_{dcn}}=M_{dc}(s) \tag{13}$$

where k_{pi} and k_{ii} are the PI parameters of the DC current control in Fig.2. I_{dcref} is adopted to be 0. Substituting equation (12) into (13) yields,

$$-\frac{M_{dc}(s)V_{dcn}-V_{dc}}{(sL_{eq}+R_{eq})I_{dcn}}(k_{pi}+\frac{k_{ii}}{s})+\frac{K_{FF}V_{dc}}{V_{dcn}}=M_{dc}(s) \tag{14}$$

Let $(k_{pi}+\frac{k_{ii}}{s})V_{dcn}\Big/\left[(sL_{eq}+R_{eq})I_{dcn}\right]$ be $k_1(s)$, then (14) can be obtained as:

$$M_{dc}(s)=\frac{K_{FF}+k_1(s)}{1+k_1(s)}V_{dcpu} \tag{15}$$

$$I_{dc}(s)=\frac{(K_{FF}-1)V_{dcpu}}{(1+k_1(s))(sL_{eq}+R_{eq})} \tag{16}$$

Substituting equation (16) into (9), we have,

$$V_{dc}(s)=\frac{sL_{dc}(K_{FF}-1)V_{dc}(s)}{(sL_{eq}+R_{eq})(1+k_1(s))}+V_{dc\_line}(s) \tag{17}$$

Let $sL_{dc}(1-K_{FF})/[(sL_{eq}+R_{eq})(1+k_1(s))]$ be $k_2(s)$, then it can be obtained as,

$$V_{dc}(s)=\frac{V_{dc\_line}(s)}{1+k_2(s)} \tag{18}$$

where K_{FF}<1. Thus, $k_2(s)$>0.

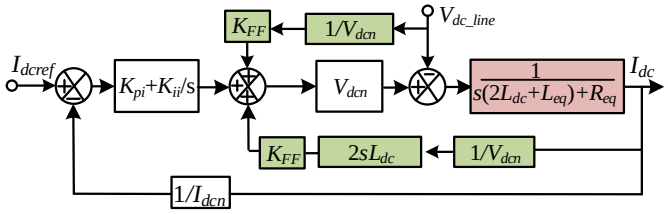


Fig. 7 The block diagram of the ACLC.

Based on the aforementioned analysis, it can be concluded:

1) Equation (16) indicates that the ACLC can be adopted to decrease the amplitude of the fault current.

2) As can be seen in equations (15)(18), there exist deep interactions among the DC modulation ratio M_{dc}, the MMC output DC voltage V_{dc} and the DC line voltage V_{dc_line}. To respond to the rapid drop of the DC line voltage V_{dc_line} under DC faults, the ACLC will act to reduce the voltage V_{armdc} quickly by decreasing the DC modulation ratio M_{dc}, thereby decreasing the MMC output voltage V_{dc}. The reduction of V_{dc} causes a further decrease of the voltage V_{dc_line}.

The voltage feed-forward control perceives the DC voltage drop and acts to accelerate the attenuation of the voltages V_{dc} and V_{dc_line}. The positive feedback process results in the continuous drop of the DC voltage until the fault steady stage reaches. Thus, the aforementioned DC voltage regulation process is equivalent to injecting a negative voltage forward TW into the OHL, as shown in Fig. 8.

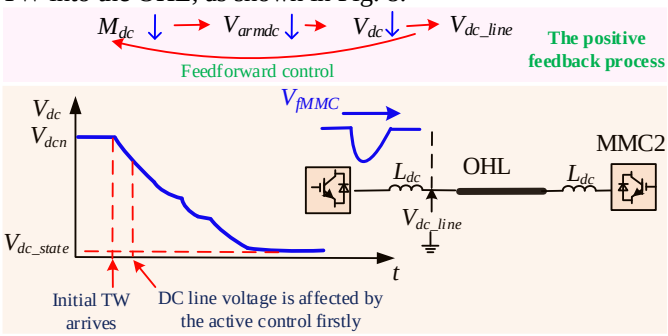


Fig. 8. The diagram of impacts of the ACLC on fault protection.

Thus, considering the impacts of the ACLC, the detected forward TW V_f can be expressed as:

$$V_f=V_f^{(0)}+(-V_{fMMC}) \tag{19}$$

where $V_f^{(0)}$ is the forward TW without regard to the impacts of the ACLC. The voltage $-V_{fMMC}$ represents the injected negative equivalent voltage forward TW from the hybrid MMC.

3) As shown in equations (15)(18), in the case of a larger K_{FF}, the response of ACLC to DC faults is faster, resulting in the voltages V_{dc} and V_{dc_line} decreasing more greatly. Therefore, the amplitude of the fault current is smaller. Especially, when K_{FF} is selected to be 1, M_{dc}, V_{dc} and V_{dc_line} have the same attenuation characteristics under DC faults. To be concluded, a larger K_{FF} will bring about larger impacts of ACLC on the fault characteristics.

To verify the impacts of the ACLC on fault characteristics, a positive PTG fault with 100Ω fault resistance is tested in the hybrid MMC-HVDC and half-bridge MMC-HVDC systems respectively. The system parameters are shown in Section V. The fault is applied in the middle of OHL12 at 2.5s. The detected forward TW waveforms are shown in Fig. 9.

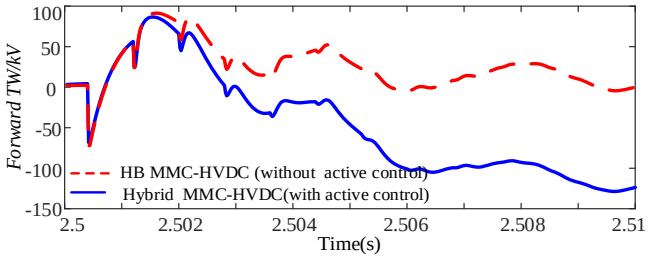


Fig. 9. The forward TW waveforms under different systems.

As can be seen in Fig. 9, for hybrid MMC-HVDC systems, the ACLC will decrease the magnitude of the forward TW. Besides, the response delay of the ACLC is no more than 2ms, which demonstrates the ACLC has a fast response speed.

In the case of low-impedance faults, the DC line voltage V_{dc_line} drops rapidly even no active control is employed. In contrast, under high-impedance faults, the voltage drop of DC line voltage is not severe without the ACLC control. Thus, the ACLC affects the TW characteristics under high-impedance faults rather than those under low-impedance faults.

B. The TW Analysis under Different Fault Locations

Fig. 10 shows the diagram of TW reflection and refraction under different fault locations, where F_{12} is an internal fault while F_1 and F_2 are external faults for the relay CB12. Assuming that the direction from MMC to OHL is positive, F_{12} and F_2 are forward faults while F_1 is a backward fault.

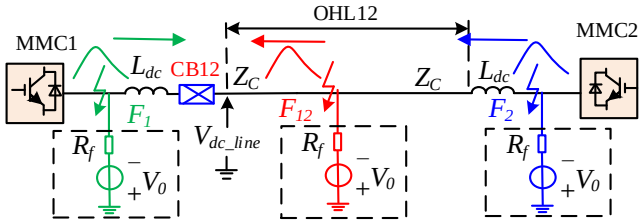


Fig. 10. The diagram of TW characteristics under different fault locations.

1) *The TW analysis under backward and forward faults*

For forward faults (F_{12} and F_2), equation (6) points out that the magnitude of the voltage derivative of the initial backward TW V_b^1 (dV_b^1/dt, it is negative) is larger than that of the initial forward TW V_f^1 (dV_f^1/dt, it is negative). Thus, for forward faults, it can be obtained:

$$\frac{min(dV_b^1/dt)}{min(dV_f^1/dt)}>1 \tag{20}$$

where *min* () represents the function that obtains the minimum value.

As shown in Fig. 11, for backward faults (F_1), the forward TW from the fault point propagates towards the measured point V_{dc_line}. The initial forward TW V_f^1 is reflected at the OHL terminal close to MMC2. After a delay of $2l/v$ (l is the length of OHL12 and v is the TW propagation speed), the reflected wave V_b^1 arrives at the measured point. The initial backward TW V_b^1 can be expressed as:

$$\begin{cases} V_b^1 = \Gamma(t)\times V_f^1 \times (e^{-\gamma l})^2 \\ \Gamma(t) = \left[\dfrac{2Z_C}{Z_C+Z_{eq}}\times e^{\frac{-t}{T_L}} + \dfrac{Z_{eq}-Z_C}{Z_C+Z_{eq}}\right] \end{cases} \tag{21}$$

Thus, for backward faults, it can be obtained:

$$\frac{min(dV_b^1/dt)}{min(dV_f^1/dt)} \ll 1 \tag{22}$$

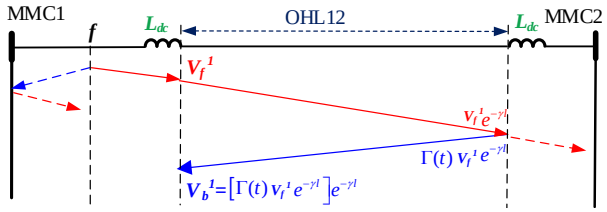


Fig. 11. The diagram of the reflection and refraction under backward faults.

To be concluded, the ratio between *min* (dV_b^1/dt) and *min*(dV_f^1/dt) can be adopted to identify backward faults.

2) *TW analysis under forward external and internal faults*

In the case of a solid fault at F_2, the detected initial TW at the relay CB12 is [20],

$$V_b^1 = \frac{Z_C\times(-V_0)}{Z_C+sL_{dc}}e^{-\gamma x} \tag{23}$$

As can be seen from equations (6)(23), under the forward external fault, due to the smooth effects provided by the current-limiting reactors, the DC line voltage drops slowly.

Based on equations (15)(18) and the criterion (4), it can be obtained that:

(1) Due to the slow drop of the DC voltage, the DC current control (mode II selection) is activated at a slower speed under the external faults.

(2) The slower drop of the DC line voltage results in the minor reduction of the DC modulation ration M_{dc} and the DC voltage V_{dc}, which weakens the impact of the ACLC.

Thus, under a forward external fault (F_2), a negative TW with a smaller amplitude is injected into the OHL. The forward TW V_f falls slightly.

However, for a forward internal fault (F_{12}), due to the rapid drop of the DC line voltage, the DC current control is activated faster. The voltage feed-forward control perceives the rapid drop of the DC line voltage and the M_{dc} is reduced drastically. A negative TW with a larger amplitude is injected into the OHL. Thus, the forward TW drops more greatly. The injected negative equivalent voltage forward TW ($-V_{fMMC}$) under different faults can be expressed as:

$$-V_{fMMC}(F_{12}) < -V_{fMMC}(F_2) \tag{24}$$

The detailed comparison of impacts of the ACLC on forward TWs can be concluded, as shown in Table 1.

Table 1 Impacts of the ACLC on forward TWs under different faults

Fault	The impacts of ACLC on the forward TWs V_f				
	V_{dc_line}	V_{dc}	M_{dc}	$-V_{fMMC}$ (negative)	V_f
Forward internal faults	↓ greatly	↓ greatly	↓ greatly	A larger amplitude	Smaller
Forward external faults	↓ slowly	↓ slowly	↓ slowly	A smaller amplitude	Larger

As can be seen in Table 1, considering the impacts of the ACLC, the forward TW V_f is smaller under internal faults. Thus, the under-voltage criterion of the forward TW can be employed to differentiate external faults and internal faults.

IV. A Two-Stage Fault Protection Scheme Considering The Impacts of the ACLC

The ACLC of the hybrid MMC allows a longer time window to detect DC faults. To improve the reliability of fault detection, a two-stage coordinated protection strategy is proposed. For the severe internal DC faults with low resistances, the *Stage I* protection can identify them with ultra-high-speed. For the internal DC faults with higher resistances, the *Stage II* protection considering the impacts of ACLC is designed to detect the faults.

A. The Design of Stage I Protection: ROCOV with Fast Speed

With the merits of low computation burden, low sampling frequency, fast detection speed and simple implementation, the rate of change of DC line voltage (ROCOV) is preferred to serve as the main protection [22]. The criterion of ROCOV is as:

$$\frac{dV_{dc\_line}}{dt} < \Delta \tag{25}$$

where V_{dc_line} is the DC line voltage. Δ is the threshold for ROCOV and it is negative.

To avoid noise disturbance under external faults, the threshold with higher reliability coefficient k_{rel1} is selected to design the criterion of the *Stage I* protection, which can be expressed as:

$$\frac{dV_{dc\_line}}{dt} < \Delta_I \tag{26}$$

where Δ_I is the threshold for the *Stage I* protection.

The *Stage I* protection is fast and not affected by noise disturbance. However, equation (8) points out that ROCOV is less endurable to fault resistance. Thus, the *Stage II* protection is required to improve the endurance to fault resistance.

To detect the arrival of the initial fault TW and avoid the noise disturbance under normal state, the threshold with a smaller reliability coefficient k_{rel2} is adopted as the fault start-up element to activate the *Stage II* protection.

$$\frac{dV_{dc\_line}}{dt} < \Delta_{II} \tag{27}$$

where Δ_{II} is the threshold for the start-up element of *Stage II* protection and Δ_I (negative) $<\Delta_{II}$ (negative).

B. The Design of Stage II Protection: The Impacts of the Active Control Has Been Considered

Based on the aforementioned analysis, the forward TWs are smaller under internal faults. Thus, the low-voltage criterion using the forward TW has been adopted to detect internal and external faults. To mitigate the impacts of the noise disturbance, the integral process is employed to optimize the low-voltage criterion [23], which can be expressed as:

$$\Delta V_f = \int_{t}^{t+T_w} V_f < \Delta V_{set} \tag{28}$$

where ΔV_{set} is the threshold for the low-voltage criterion and T_w is selected as 1ms.

Considering the response delay of the ACLC, a delay Δt_1 is required to calculate the ΔV_f. Namely, after the activation of the fault start-up element, wait a delay Δt_1. Then, the forward TW low-voltage criterion calculation is conducted for further detection. To avoid the disturbance of backward faults, the directional element based on criterion (20) is adopted.

From the aforementioned analysis, the overall protection scheme that considers the impacts of the ACLC can be obtained, as depicted in Fig. 12.

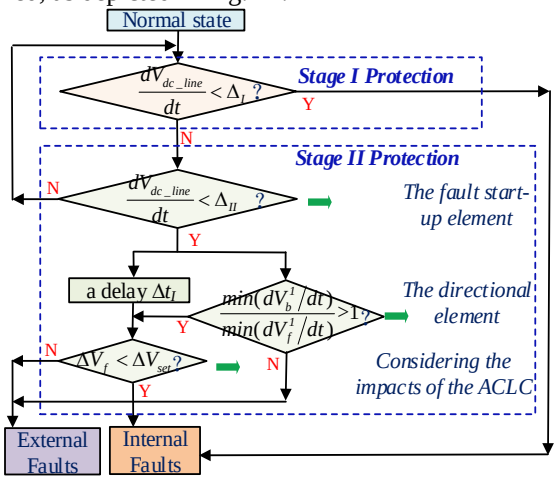


Fig. 12. The overall protection scheme that considers impacts of the ACLC

V. Simulation and Verification

In order to verify the feasibility and effectiveness of the proposed method, a ±500kV four-terminal hybrid MMC based DC grid is built in PSCAD/EMTDC, as shown in Fig. 13. The overhead line adopts the frequency-dependent model. and the system is a symmetric monopole structure and the other converter parameters are listed in Table 2. MMC3 controls the DC link voltage while other converters control the transmitted power. With the great likelihood of the occurrence, pole-to-ground faults are the main concern in the simulation. D_{Vset} for the *Mode II selection* is adopted to be -75*kV/ms*. Besides, Δt_1 is adopted as 5ms. DCCB adopts the hybrid DCCB topology proposed by ABB [24].

Table 2 Parameters of each converter station

Converter	MMC1	MMC2	MMC3	MMC4
arm inductance / mH	50	50	50	50
sub-module capacitor / mF	4	4	8	8
sub-module number / *N*	200	200	200	200
rated power / MW	750	750	1500	1500

Based on the methodology to determine the CLRs in [25], the lower limit of CLR (L_{dc}^{lower}) for unblocking HB-MMC systems can be calculated as 269mH. Due to the current-limiting capacity, the CLRs for hybrid MMC will be smaller. Thus, L_{dc}^{lower} can be adopted as the upper limit for hybrid MMC based DC systems. Combing the simulation results, 0.1H CLR is adopted to guarantee the safety of converter under DC faults. And this value is sufficient to distinguish a low impedance fault using travelling wave or fast transient based algorithms.

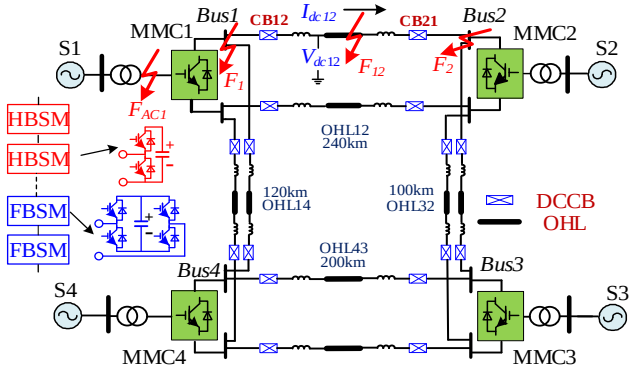


Fig. 13. The topology of a four-terminal hybrid MMC based DC grid.

A. Determination of Thresholds

Taking the relay CB12 as an example, the threshold setting calculation will be conducted as follows. Regarding the selection of reliability coefficients, for increment protection algorithms, such as ground instantaneous overcurrent protection, the reliability coefficient is ranging from 1.25 to 1.5 [26]. For decrement protection algorithms, such as the protection *zone I* of distance protection, the reliability coefficient is ranging from 0.8 to 0.9 [26]. To improve the reliability to avoid mal-operation, the reliability coefficients are selected to be 1.5 for increment protection criterion while 0.8 for decrement protection criterion.

1) *Threshold setting Δ_I for Stage I protection*

The ROCOV with a lower threshold Δ_I is employed to detect low-impedance faults as *Stage I* protection. Thus, the threshold Δ_I should be much smaller than the measured ROCOV under the most severe external fault that happens at the DC terminal of MMC2 (F_2).

Generally, the noise disturbance will increase the amplitude of the ROCOV. To avoid false-operation under external faults, an external fault F_2 with 20dB noise disturbance has been considered to determine the threshold Δ_I. The specific process of the threshold determination is presented as follows:

1) The ROCOV under the most severe external fault case (F_2, 0.01Ω) is measured: ROCOV=-1093*kV/ms*.

2) A high reliability coefficient (k_{rel1}=1.5) is adopted to make sure that the protection scheme will not be falsely triggered under the most severe external faults with noise disturbance: Δ_I =1.5×(-1093) =-1640 *kV/ms*.

2) *Threshold setting Δ_{II} for the start-up element*

The ROCOV with a higher threshold Δ_{II} is employed to trigger the following *Stage II* protection. Thus, the threshold Δ_{II} (negative) should be larger than the measured ROCOV under all internal faults. To avoid false activation caused by noise disturbance under the normal state, the threshold Δ_{II} should be smaller than the measured ROCOV under normal state. Based on the aforementioned principle, scan different positive pole-to-ground (P-PTG) DC faults with 500Ω fault resistance along OHL12 to obtain the measured ROCOV, as shown in Table 3.

Table 3 Measured ROCOVs under different internal P-PTG faults with 500Ω resistance (*kV/ms*)

Fault locations	0% of OHL12	25% of OHL12	50% of OHL12	75% of OHL12	100% of OHL12
ROCOV	-1038	-1067	-920	-780	-912

As shown in Table 3, the maximum value of *ROCOV* is -780*kV/ms*. In the simulations, the dV_{dc_line}/dt (negative) caused by 20dB noise disturbance under normal state is larger than -400*kV/ms*. To avoid noise disturbance under the normal state, the reliability coefficient k_{rel2} is selected as 0.8. The threshold Δ_{II} can be obtained: Δ_{II} =0.8×(-780) =-625*kV/ms*.

3) *Threshold setting ΔV_{set} for Stage II protection*

Applying P-PTG faults at F_2 with different fault resistances, the measured ROCOV and ΔV_f are shown in Fig. 14.

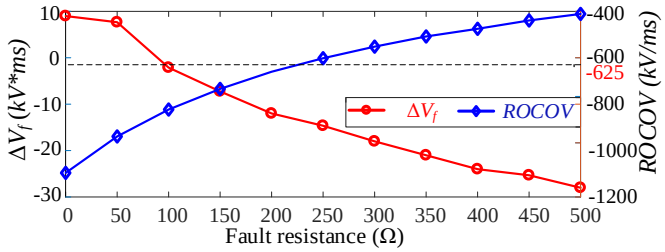


Fig. 14. The measured ROCOV and ΔV_f under DC faults at F_2 with different resistances.

In Fig. 14, with the increase of fault resistance, ROCOV increases while ΔV_f decreases. When the fault resistance exceeds 250Ω, ROCOV is larger than the threshold Δ_{II}, which will not activate *Stage II* protection. Thus, the measured ΔV_f under DC fault with 500Ω resistance at F_2 is employed to calculate the threshold ΔV_{set}. When the reliability coefficient k_{rel3} is selected as 1.5 and the threshold ΔV_{set} can be obtained: ΔV_{set} =1.5×(-28)≈ -45*kV*ms*.

4) *The selection of the forward-feedback control coefficient K_{FF}*

Regarding the selection of the forward-feedback coefficient K_{FF}, the response of ACLC to DC fault and the stability of the current-limiting controller should be considered. A larger coefficient K_{FF} will bring about a faster response of ACLC to DC faults. However, the coefficient K_{FF} is restricted by the stability of the current-limiting controller. With the increase of the coefficient K_{FF}, the phase margin (PM) decreases, which weakens the stability.

Based on the Bode diagram analysis of DC current control loop, the phase margins (PM) under different coefficients K_{FF} can be calculated, as shown in Table 4.

Table 4 The measured *PMs under different* coefficients K_{FF}

K_{FF}	0.1	0.3	0.5	0.7
PM	53.9 °	49 °	46.3 °	44.1 °

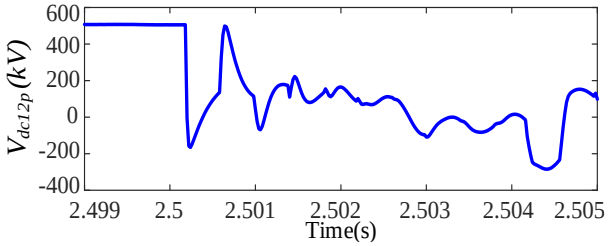
To obtain good dynamic performances, the phase margin is suggested to range from 45° to 60°. Thus, the coefficient K_{FF} is suggested to range from 0 to 0.5. To be conservative, the coefficient K_{FF} is selected to be 0.3.

B. Simulation Analysis under Internal Faults

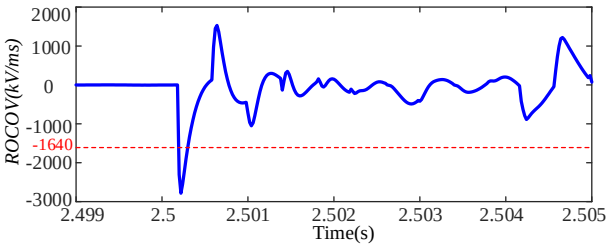
1) *Response to a metallic P-PTG fault*

At 2.0s, a solid positive pole-to-ground fault is applied at 25% of OHL12 and the simulation waveforms are shown in Fig. 15.

As shown in Fig. 15(a), the initial backward TW V_b^I arrives at 2.0002s, resulting in the rapid drop of the DC line voltage V_{dc12p}. The measured ROCOV is smaller than the threshold Δ_I (-1640*kV/ms*), as shown in Fig. 15(b). Thus, it is deemed to be an internal fault and the detection time is no more than 0.3ms.



(a) The positive pole-to-ground DC line voltage V_{dc12p}



(b) ROCOV

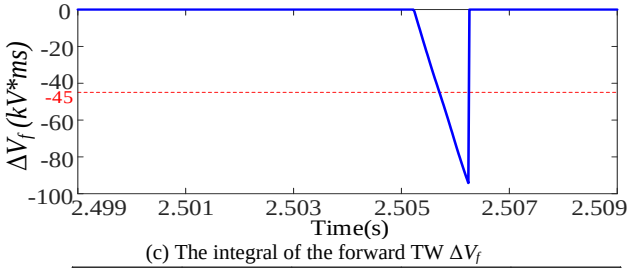
Fig. 15. Simulation waveforms under a metallic internal P-PTG fault.

2) *Response to a P-PTG fault with 400Ω fault resistance*

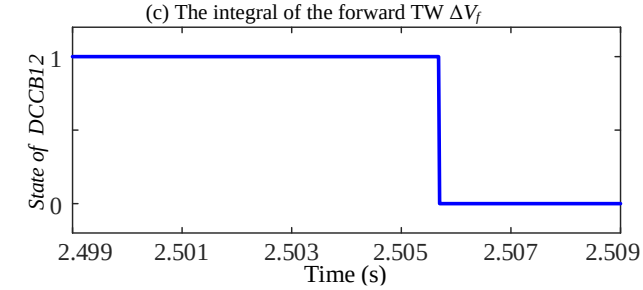
At 2.0s, a P-PTG fault with 400Ω fault resistance is applied at 25% of OHL12 and the simulation waveforms are shown in Fig. 16.

As can be seen in Fig. 16 (a), the DC line voltage drops rapidly at 2.002s. In Fig. 16(b), the measured ROCOV is larger than the threshold Δ_I (-1640*kV/ms*) while smaller than threshold Δ_{II} (-625*kV/ms*), leading to the activation of the fault start-up element. The minimum values of the measured dV_b^1/dt and dV_f^1/dt are -318.62*kV/ms* and -286.42*kV/ms* respectively. $min\ (dV_b^1/dt)/min(dV_f^1/dt)$=1.11>1, which demonstrates that it is an internal forward fault. In Fig. 16 (c), the measured ΔV_f is smaller than the threshold ΔV_{set} (-45*kV*ms*), satisfying the criterion of the *Stage II* protection. Thus, it is identified to be an internal fault and the DCCB12 is tripped at 2.5057s, as shown in Fig. 16 (d).

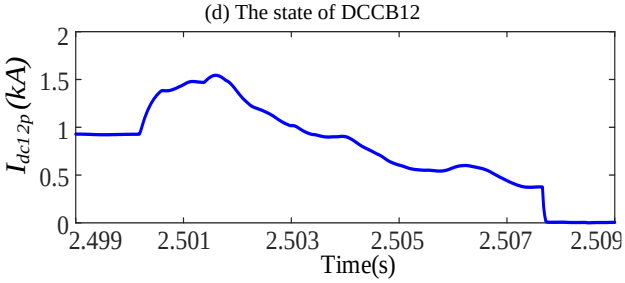
In Fig. 16 (e), the maximum of the line current I_{dc12p} is no more than 1.8kA (twice of the rated line current), indicating that there is no overcurrent. In addition, the ACLC can decrease the fault current before the DCCB12 is tripped. Thus, the breaking capacity of the DCCBs is decreased.



(c) The integral of the forward TW ΔV_f



(d) The state of DCCB12



(e) The DC line current I_{dc12p}

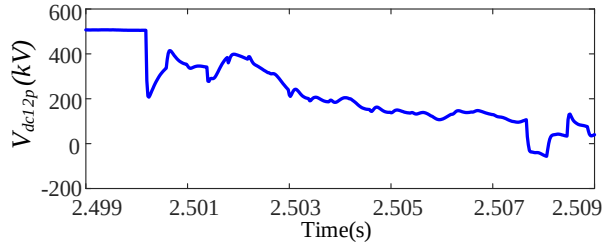
Fig. 16. Simulation waveforms under a P-PTG fault with 400Ω resistance.

C. Simulation Analysis under External Faults

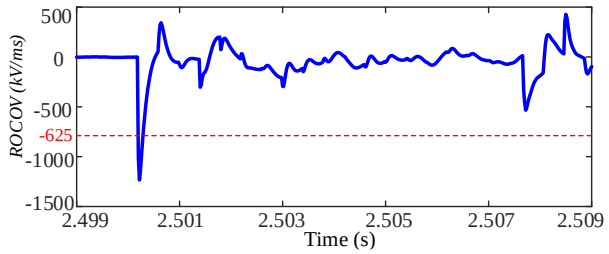
1) *Response to a bus fault*

At 2.0s, a solid P-PTG fault is applied at the Bus2 (F_2) and the simulation waveforms are shown in Fig. 17.

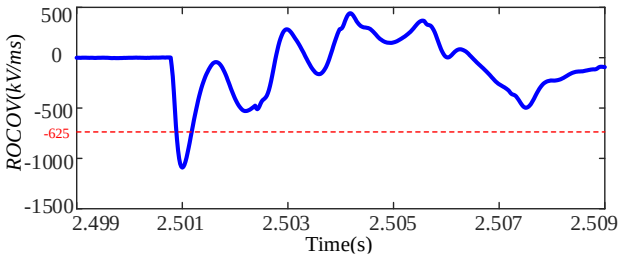
As can be seen in Fig. 17 (a), the measured ROCOV is smaller than the threshold Δ_{II} (-625*kV/ms*), triggering the fault start-up element. In Fig. 17 (b), the measured ΔV_f is larger than the threshold ΔV_{set} (-45*kV*ms*), which does not satisfy the criterion of the *Stage II* protection. Thus, the fault is deemed to be external. Fig. 17 demonstrates that the proposed method can identify internal and external faults correctly.



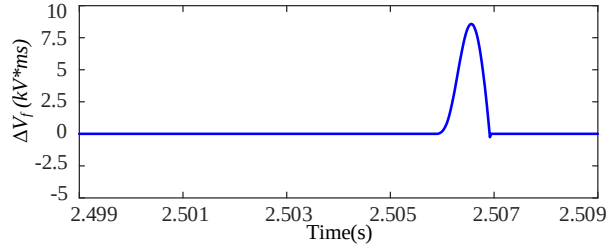
(a) The positive pole-to-ground DC line voltage V_{dc12p}



(b) ROCOV



(a) ROCOV



(b) The integral of the forward TW ΔV_f

Fig. 17. Simulation waveforms under an external P-PTG fault.

2) *Response to external faults on the OHL14 and OHL23*

More solid P-PTG faults are applied in the middle of the OHL14 and OHL23 respectively to test the effectiveness under external faults. The simulation waveforms are shown in Fig. 18 and Fig. 19.

As can be seen in Fig. 18, the measured ROCOV is larger than threshold Δ_{II} (-625*kV/ms*), which will not trigger the fault start-up element. Thus, the fault on the OHL14 is identified to be external.

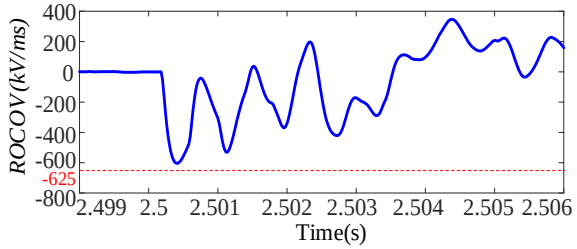
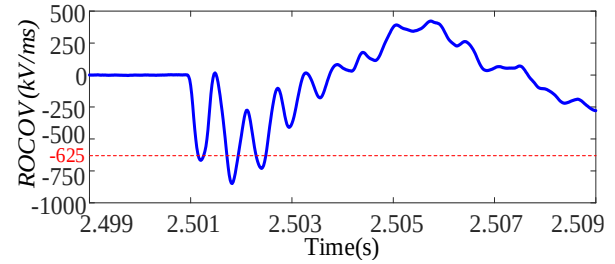


Fig. 18. Simulation waveform in the case of a fault in the middle of OHL14.

In Fig. 19(a), the measured ROCOV is smaller than threshold Δ_{II} (-625*kV/ms*), activating the fault start-up element. In Fig. 19(b), ΔV_f is larger than the threshold ΔV_{set} (-45*kV*ms*), which does not satisfy the criterion of the *Stage II* protection. Hence, the fault on the OHL23 is deemed to be external.



(b) The integral of the forward TW ΔV_f

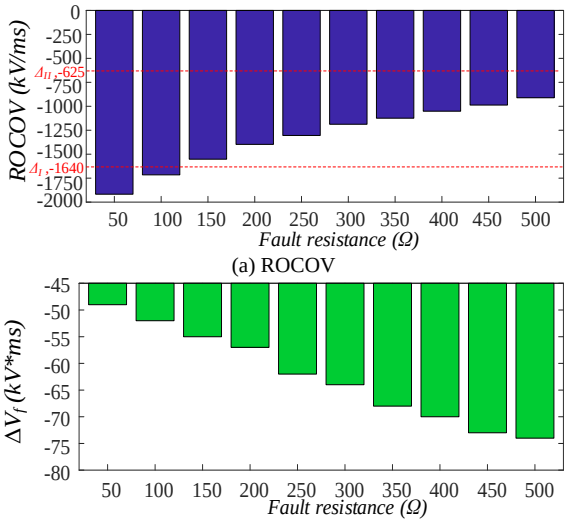
Fig. 19. Simulation waveforms in the case of a fault in the middle of OHL32.

In the case of external line faults, such as the faults on the OHL32 and OHL14, the sharp negative voltage TW induced from the fault point will be smoothed by multiple current-limiting reactors. Thus, for relay CB12, the amplitude of the measured ROCOV is smaller, Hence, the *Stage I* protection will not be activated, neither the fault start-up element, as shown in Fig. 18 and Fig. 19. To be concluded, the external line faults can be identified correctly.

VI. Robustness Analysis

A. Impacts of Fault Resistance

At 2.0s, various P-PTG faults with different resistances varying from 50Ω to 500Ω are applied at the end of OHL12 (close to MMC2) to test the impacts of fault resistances. The simulation waveforms are shown in Fig. 20.



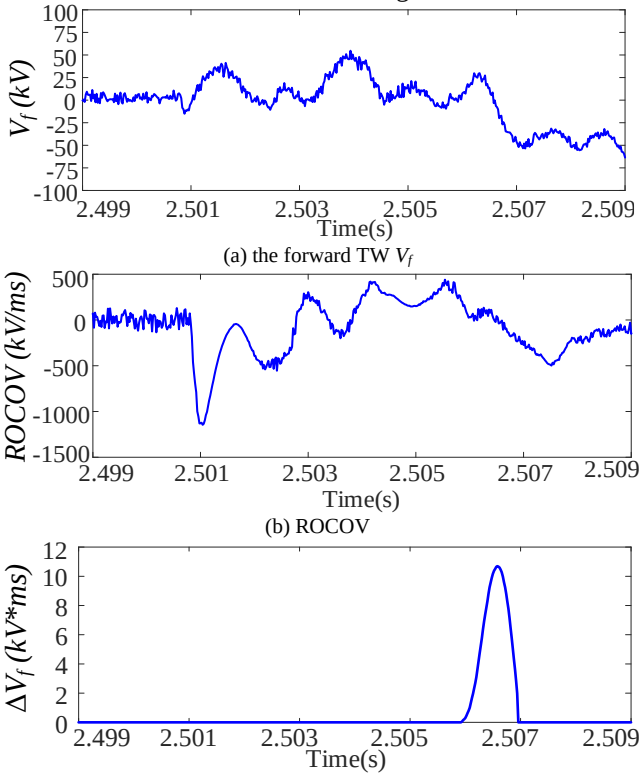
(b) The integral of the forward TW ΔV_f

Fig. 20. The measured ROCOVs and ΔV_f under various fault resistances

As can be seen in Fig. 20(a), when the fault resistance increases to 100Ω, the ROCOV will be larger than the threshold Δ_I. However, the measured ΔV_f is still smaller than the threshold ΔV_{set} (-45*kV*ms*), which demonstrates that the proposed method is endurable to large fault resistances. The maximum fault resistance that the proposed method can identify is up to 500Ω.

B. Influence of Noise

To test the robustness of the noise disturbance, a 20dB white noise is added into the measured voltages V_{dc12p} and V_f. Then, at 2.5s, a solid P-PTG fault is applied at the DC bus (F_2). The simulation waveforms are shown in Fig. 21.



(c) The integral of the forward TW ΔV_f

Fig. 21. Simulation waveforms under an internal fault with 20db noise.

During the determination of threshold Δ_I, a large reliability coefficient k_{rel1} is adopted to guarantee high selectivity. Thus,

the measured ROCOV with 20dB noise is larger than the threshold Δ_I, which will not lead to the false operation of the *Stage I* protection. However, the measured ROCOV is smaller than the threshold Δ_{II}, triggering the fault start-up element, as shown in Fig. 21 (a).

The average value of the noise signal is equal to zero. Thus, the integral method is employed to mitigate the impacts of the noise. As can be seen in Fig. 21(b), the measured ΔV_f is larger than the threshold ΔV_{set}. Thus, it is identified to be external. To be concluded, the proposed method is robust to noise.

C. The Applicability of the Pole-to-pole Faults.

Based on the aforementioned principle of the threshold determination, the threshold ΔV_{set} for PTP faults is adopted as $184kV*ms$. Various PTP faults are applied to test the applicability of the proposed method for the PTP faults, as shown in Table 5.

As can be been in Table 5, the proposed method can be employed to detect PTP faults correctly. Compared with PTG faults, the amplitude of the dV_{dc_line}/dt is larger than that under PTP faults. Thus, the *Stage I* protection is activated faster under internal PTP faults.

D. Discussions and Comparisons

1) *The impacts of the change of the operation mode*

As pointed out in [27], in the case of the operation mode changes, such as the power reversal, the DC line voltage has a small fluctuation, which will not trigger the fault start-up element. Thus, the change of the operation mode has no impacts on the proposed method

2) *The Response to AC faults*

In the event of the most severe AC fault, the DC line voltage has a small fluctuation, due to the independent control between the AC side and DC side. The fault start-up element will not be activated. To be concluded, the proposed method will not be affected by AC faults.

Table 5 Simulation results under different PTP faults

Fault Location	Fault resistance (Ω)	dV_{dc12p}/dt	ΔV_f	Fault identification
0% of OHL12 (close to MMC1)	0.01	2297<Δ_I	/	*Stage I* protection is activated and it is deemed to be an internal fault
	200	1771<Δ_I		
	300	Δ_I <1590<Δ_{II}	153<ΔV_{set}	*Stage II* protection is activated and it is deemed to be an internal fault
	500	Δ_I <1319<Δ_{II}	59<ΔV_{set}	
50% of OHL12	0.01	-3828<Δ_I	/	*Stage I* protection is activated and it is deemed to be an internal fault
	200	-2487<Δ_I		
	300	-2116<Δ_I		
	500	Δ_I <-1627<Δ_{II}	53<ΔV_{set}	*Stage II* protection is activated and it is deemed to be an internal fault
100% of OHL12 (close to MMC2)	0.01	-3473<Δ_I	/	*Stage I* protection is activated and it is deemed to be an internal fault
	200	-2645<Δ_I		
	300	-2363<Δ_I		
	500	-1947<Δ_I		
The Bus2 (F_2)	0.01	Δ_I <-1004<Δ_{II}	503>ΔV_{set}	Neither *Stage I* nor *Stage II* Protection is activated and it is deemed to be an external fault
	50	Δ_I <-834<Δ_{II}	379>ΔV_{set}	
	150	Δ_I <-641<Δ_{II}	300>ΔV_{set}	
	200	-577>Δ_{II}	/	

Table 6 Comparison between the proposed method and some typical methods without the impacts of ACLC

Protection schemes		Endurance to fault resistance/Ω	Resistance to noise/dB	Sampling frequency/kHz	Other drawbacks
without considering the impacts of ACLC	[21]	weak	×	100	/
	[22]			/	
	[27]	√	weak	200	Close-in faults are difficult to be detected
	[14]		×	100	
	[28]		weak	√	WT mother function and sampling frequency are difficult to be selected
	[25]				
	[19]		√	1000	More voltage transformers are required
	[16]			200	
	[17]	200		√	
The proposed method		√			/

3) *Comparison with other protections*

A comprehensive comparison between the proposed method and other protection schemes without considering the impacts of ACLC has been conducted, as shown in Table 6. Where "√" means that the maximum resistance that can be identified is ≥300Ω, the sampling frequency is ≤50kHz, and the noise that can be endured is stronger than 20dB. Otherwise, the relevant technology is noted as "×".

As can be seen in Table 6, the proposed method has significant advantages on the robustness against fault resistance and noise disturbance. In addition, a lower sampling frequency is adopted. Among these protections without the impacts of ACLC, for WT based methods, the cascaded filtering and multi-scale decomposition will lead to a higher sampling-frequency and a heavier computation burden. For reactor voltage-based methods, they are vulnerable to resistance or noise.

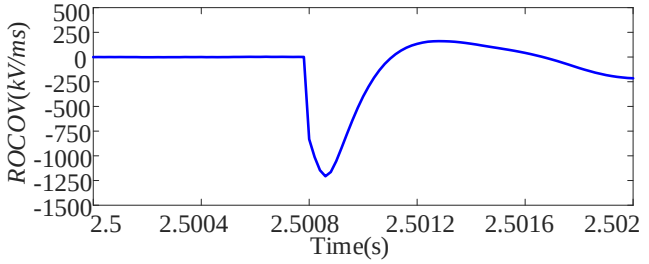
Moreover, a detailed simulation is conducted to test the performances of the proposed method in [21]. The criterion for the discrimination of internal and external faults in [21] is:

$$\begin{cases} \dfrac{dV_{dc}}{dt} < Th1 \ \ and \ \dfrac{dI_{dc}}{dt} > Th2 \\ V_{dc}(t_{det} + \Delta t_{discr}) < Th3 \end{cases} \tag{29}$$

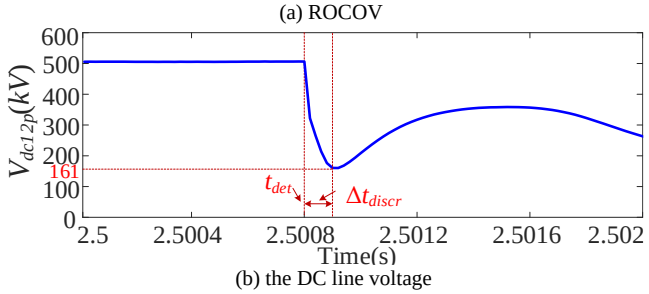
where the under-voltage criterion is achieved by monitoring the voltage with a defined period of time Δt_{discr} (100μs) after the start-up element is activated. The time when the start-up element is activated is defined as t_{det}.

A solid PTG fault with 20dB noise is applied at the Bus2 (F_2) and a PTG fault with 300Ω resistance is applied at the end of OHL12 (F_{12}).

The measured ROCOVs are respectively -1140 *kV/ms* for the fault F_2 and -1206 *kV/ms* for the fault F_{12}, as shown in Fig. 21 (b) and Fig. 22 (a). The DC line voltages at the time $t_{det}+\Delta t_{discr}$ are respectively 161 *kV* for the fault F_{12} and 133 *kV* for the fault F_2, as shown in Fig. 22 (b) and Fig. 23. The low-voltage criterion in (29) does not hold true, which demonstrates that the proposed method in [21] is vulnerable to fault resistance and noise disturbance.



(a) ROCOV



(b) the DC line voltage

Fig. 22. Simulations under the internal fault with 300Ω resistance (F_{12}).

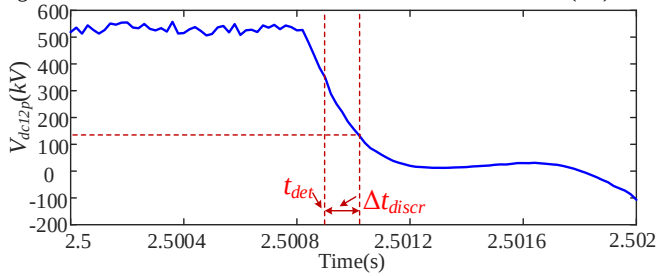


Fig. 23. DC line voltage under the solid external fault with 20dB noise (F_2).

VII. Conclusion

For the hybrid MMC based DC grids, a single-end protection scheme that considers the impacts of the ACLC is proposed to achieve selective fault detection. The impacts of the ACLC on TW characteristics under different stages are evaluated and the differences of forward TWs under different fault locations are analyzed. Based on the analysis, it can be concluded:

1) The ACLC will actively reduce the MMC output DC voltage, which is equivalent to injecting a negative forward TW into the transmission lines. The impacts of the ACLC on forward TWs under internal faults are greater than those under external faults. Thus, the low-voltage criterion of the forward TW is employed to design the criterion.

2) The proposed method can identify faults with fault resistance as high as 500Ω and it is immune to noise with 20dB. In addition, the method is not affected by the changes of the operation mode, fault distances and AC faults.

3) In comparison with schemes of HB MMC based DC grids, such as ROCOV, WT based methods and so on, the proposed method has advantages on the capability of the robustness to high-resistance and noise disturbance. Besides, a lower sampling frequency and computation burden is adopted.

The proposed method provides a systematical approach for the protection design of fault-tolerant MMCs with fault current-limiting capability.

APPENDIX

The overhead transmission lines are modeled based on the frequency-dependent (phase) model of the PSCAD/EMTDC. Fig. 24 illustrates the configuration of the DC overhead transmission line.

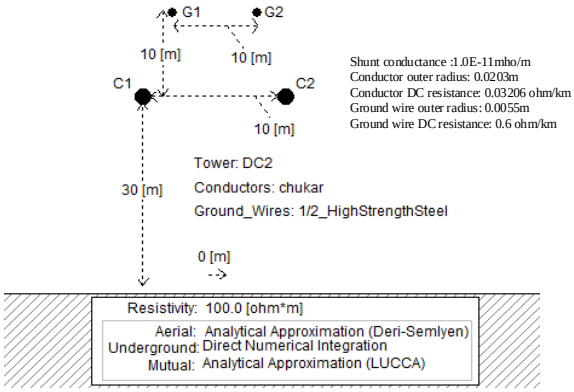


Fig. 24. Configuration of the overhead lines.

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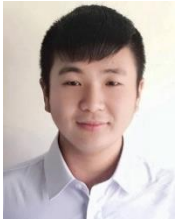
BIOGRAPHIES



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