Analysis of Controller Bandwidth Interactions for Vector-Controlled VSC Connected to Very Weak AC Grids

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***Abstract*—Stability assessment of conventional vector current control (VCC) of voltage-source converters (VSCs) in weak grids has not been standardized. In this paper, a small signal model is derived to quantify the maximum active power transfer in a very weak grid across a much wider range of controller bandwidths than has previously been investigated. A novel investigation of the VCC-VSC controller bandwidth interactions between inner and outer control loops, including the phase-locked loop (PLL) dynamics, is demonstrated and a stability bubble of safe operating points is established. Robustness of the stability bubble under different SCRs is investigated and dynamic performance considerations are introduced to form a reduced operating region with good transient performance. The controller gains within this region allow rated power transfer in inverting mode and good dynamic performance with no modifications to the conventional VCC structure. For very weak grids, it is recommended that PLL bandwidths between 5 and 30 Hz are avoided. If a slow PLL bandwidth is chosen, the outer loop *q*-axis should have a fast bandwidth; with a fast PLL, the outer loop *q*-axis control bandwidth should be reduced. In all cases, the outer loop *d*-axis should be slowed down to reach the power transfer limit.**

***Index Terms*—vector current control, VSC, weak AC grids, stability, small signal analysis**

I. Introduction

Power systems worldwide are under increasing pressure to facilitate the integration of renewable energy generation, and energy storage [1], [2]. Voltage-source converters (VSCs) are the favored technology for grid interfacing due to their flexible control performance. Recently, VSCs have been shown to offer improved performance in weak grids [3], [4]. Nevertheless, the connection of VSCs to very weak AC grids still poses many challenges and continues to attract significant research attention e.g. [5]–[22]. The two most significant challenges yet to be resolved are 1) to maximise bidirectional active power transfer; 2) to be sufficiently robust (stable) under parameter uncertainty or changes in short circuit ratio (SCR). Many efforts have been made to improve very weak grid connected VSC performance in these respects. However, evaluation of such control strategies has not been standardized. The main causes of instability for VSCs in very weak grids are classified into two main factors. The first key factor is the phase-locked loop (PLL), as highlighted in [5]–[11]. At high PLL bandwidth, fast changes in the controller phase angle cause rapid changes in current injections, which in turn perturb the AC busbar voltage such that the PLL cannot lock on to the correct phase angle [5]. The second factor that contributes to instability is the other controller elements, as investigated in [6], [8], [12]–[14]. All aspects of the controller structure are critical for overall stability of very weak grid-tied VSCs. However, in all literature works, analysis is focused on only one aspect of the controller at a time, such that potential interactions between these components are overlooked. This single-variable analysis is often based on the assumption that the inner and outer control loops are decoupled by their different time scales and thus can be considered separately [8]. However, stability analysis which varies the parameters of the cascaded control loops simultaneously is not performed to verify this assumption.

To mitigate the destabilizing effects of the PLL, control methods have been proposed to enhance or modify conventional vector current control. In [6] and [15], an artificial bus has been used to add impedance compensation to the PLL while [10] and [12] focus on re-tuning the PLL. This invariably requires slowing down the PLL, which leads to a slower controller response and poor transient performance [5], [6], [16]. In [17]–[19], the authors proposed VSC control methods which dispense with the PLL completely. Power-synchronization control (PSC) eliminates the PLL and instead emulates the synchronization behaviors of synchronous machines. PSC can increase the maximum active power transfer of very weak grid connected VSC, but this control has no intrinsic current-limiting capability [18]. The frequency-synchronization approach in [19] also eliminates the PLL but has similar limitations under fault conditions. Direct power control (DPC) requires no PLL or Park transformations and so removes the PLL interactions, whilst maintaining the conventional VCC structure [17]. DPC improves dynamic performance compared to conventional VCC with a very slow PLL, however there is limited work on very weak grid performance at this stage. All of these proposed control methods offer improved power transfer and stability compared to conventional VCC. However, controller performance is evaluated at only a single controller operating point (or at an 'ideal' and a deliberately poorly-tuned point). No comprehensive evaluation was performed to determine if the optimum controller tuning has indeed been achieved or whether improved transient or power transfer performance can be achieved at an alternative operating point. These proposed controllers are also developed under the assumption that the PLL is the most significant cause of instability, which overlooks the contribution of other control loops. To address the limitations imposed by the outer loops, feed-forward terms have been added to the reactive power control (in order to speed up this outer loop) [12], [15], [20]. To improve the

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system damping, [13] introduces current-error based compensators to the VSC voltage reference, while gain-scheduling and cross-coupling terms in the outer loop were proposed in [21] to decouple the *d*- and *q*-axis control. Each of these strategies performs better than conventional VCC but, as with the PLL-focused controllers, these works do not consider multiple controller operating points. This limited analysis does not accurately evaluate the complete stability boundary of any given strategy and prevents the fair comparison of the various enhanced VCC methods.

Each of the modified VSC control strategies targets the PLL- or controller-induced instability with precise controller tuning that assumes accurate system quantification and, in some cases, requires gain scheduling based on the grid impedance and real-time power transfer (e.g. [21]). Impedance estimation methods are either intrusive or slow and cannot be implemented in all weak grid systems. Sensitivity analysis is therefore important in weak grids and sensitivity of individual controller tunings was examined in several works e.g. [5], [8], [14]. The sensitivity of the active and reactive power loops was studied in [8], but this work ignores the inner current loop, assuming that the different time-scales of the cascaded loops prevent any interaction. Conversely, [14], considered only current time-scale stability effects and demonstrated the positive damping effect of the current controller on terminal voltage as the current control bandwidth increases. These studies do not consider the sensitivity of more than two variables simultaneously i.e. at best, the tuning of two control loops is examined at a fixed power level or one control loop tuning is examined at varying power level. The coupled impact of more than one control loop on the maximum power transfer is not assessed. In addition, the controller bandwidth ranges covered are often small (less than one order of magnitude) and so the full extent of each effect may not be covered.

In this paper, a new stability study methodology is developed in order to determine the stability limit as a function of three variables (two controller tunings and the active power). For each unique set of controller parameters, small signal models are constructed at power steps using initial conditions calibrated from the time-domain simulation. Stable operating regions for these bandwidths are established and discussed, and an overall stability bubble for VCC in very weak AC grids is presented. The robustness of VCC-VSC in weak grids is also presented. High stability regions are demonstrated across a range of controller operating points and dynamic transient performance is considered to form a smaller stability bubble in which both absolute stability and acceptable dynamic transient performance are achieved. This region offers operators a range of controller gains at which conventional VCC can achieve rated power transfer in inverting mode and good dynamic performance without any modifications to the control structure. VCC therefore comes much closer to addressing the challenges of VSC control in very weak grids than has previously been assumed.

The contributions of the paper are as follows: 1) to establish power transfer limits of conventional VCC-VSC connected to a very weak grid across a broad range of controller operating points, 2) to quantify the impact of all VCC control loops, including the PLL, on overall stability and describe the controller stabilizing or destabilizing effects, 3) to quantify the interactions between any two control loops and the impact of three-way interactions on stability, and 4) to extract all controller operating points that can provide both stable operation and acceptable dynamic performance at a fixed power transfer level.

The rest of this paper is organized as follows. Section II introduces the study system and conventional VCC structure. The small signal model is derived and validated in Section III. The developed model is used to perform controller operating point sweeps in Section IV.A. An impedance model to corroborate the small signal modelling results is presented in Section IV.B. Section V discusses the small signal results, establishes stable and dynamic performance operating regions for VCC and assesses the controller robustness.

II. Study System

The schematic diagram of the grid-connected VSC system under investigation is presented in Fig. 1. U_g is the grid voltage, U_f is the voltage at the point of common coupling (PCC) and U_c is the converter voltage. A very weak AC grid with SCR = 1 is used for all analyses in this paper. The AC system parameters are based on the study system in [20] and are given in Table I. The AC grid is represented by a Thevenin equivalent impedance $Z_g = R_n + j\omega_g L_n$, where ω_g is the grid frequency and R_n and L_n are the Thevenin-equivalent grid resistance and inductance. The VSC is connected via a coupling impedance $Z_c = R_c + j\omega_g L_c$ where R_c and L_c are the resistance and inductance of the inductive filter between the converter and the grid. In order to avoid low frequency passive resonances on the AC side, the filter capacitance, C_f , is zero. All reactive power will instead be provided by the VSC and it is therefore overrated to approximately 1.58 p.u. apparent power. The VSC voltage rating is 1.22 p.u. The control system for classical VCC-VSC is also shown in Fig. 1including an inner current loop (ICL), outer active power loop (APL), outer AC voltage loop (AVL) and PLL. Control is performed in the *dq*-frame, which is synchronized to the PCC grid voltage via the reference phase angle produced by the PLL. All inputs to the PLL and controller are measured at the PCC through a first-order low-pass filter.

TABLE I
STUDY SYSTEM PARAMETERS

Parameters	Value
AC system rated voltage, RMS line (kV)	195
AC system rated power (MW)	350
AC system frequency (Hz)	50
SCR	1
X/R ratio	10
AC system inductance, L_n(H)	0.3441
AC system resistance, R_n (Ω)	10.864
Coupling inductance, L_c (mH)	69.2
Coupling resistance, R_c (Ω)	1.0864
Filter capacitance, C_f (μF)	0

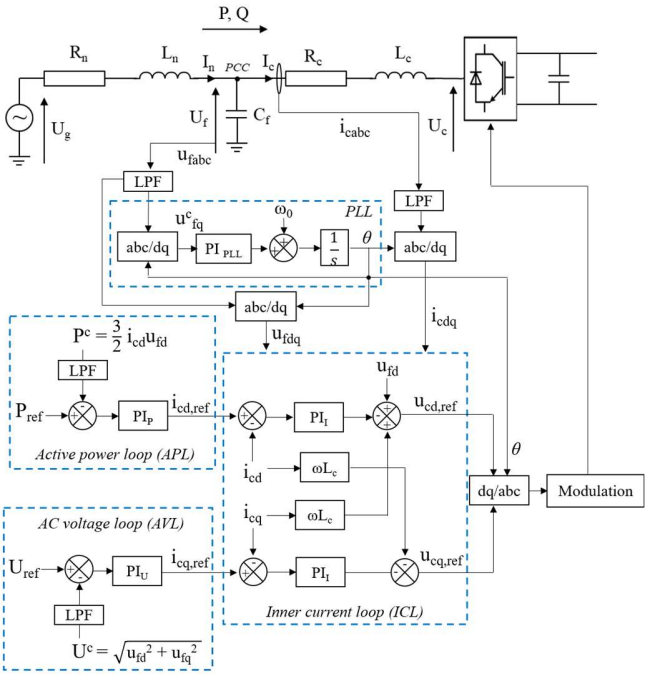

Fig. 1 - Schematic diagram of VSC and AC grid test system with classical VCC.

III. Small Signal Modelling and Validation

A linearized model using full state-space representations of each component of the AC grid, VSC and controller is used to quantify the small signal stability limits. In the following sections, the superscript '*c*' denotes the converter frame and the superscript '*f*' denotes a low-pass filtered variable. The subscript '$_0$' denotes a steady-state linearization point.

A. Small Signal Modelling

The grid-connected VSC system in Fig. 1 is non-linear. Small signal stability analysis therefore requires linearization of the AC system dynamic differential equations, the PLL and the grid-converter *dq*-frame transformations.

1) AC system linearization

The linearized equations for the AC system are:

$$sL_c\Delta i_{cd}=\Delta u_{fd}-R_c\Delta i_{cd}-\Delta u_{cd}+\omega L_c\Delta i_{cq} \quad (1)$$

$$sL_c\Delta i_{cq}=\Delta u_{fq}-R_c\Delta i_{cd}-\Delta u_{cq}-\omega L_c\Delta i_{cd} \quad (2)$$

$$sC_f\Delta u_{fd}=\Delta i_{nd}-\Delta i_{cd}+\omega C_f\Delta u_{fq} \quad (3)$$

$$sC_f\Delta u_{fq}=\Delta i_{nq}-\Delta i_{cq}-\omega C_f\Delta u_{fd} \quad (4)$$

$$sL_g\Delta i_{nd}=-\Delta u_{fd}-\Delta i_{nd}+\Delta u_{gd}+\omega L_g\Delta i_{nq} \quad (5)$$

$$sL_g\Delta i_{nq}=-\Delta u_{fq}-R_g\Delta i_{nq}+\Delta u_{gq}-\omega L_g\Delta i_{nd} \quad (6)$$

Where u_f is the voltage at the PCC, u_c is the converter voltage, u_g is the grid voltage, i_c is the current flowing into the converter and i_n is the current flowing from the grid. The corresponding state-space matrices are presented in [21].

2) PLL and Reference Frame Linearization

A classical PLL based on feedback of the *q*-axis PCC voltage is employed and this control law is shown in Fig. 1 and (7).

$$\theta_{PLL}=\left(\underbrace{\left(k_{ppll}+\frac{k_{ipll}}{s}\right)}_{F_{PLL}(s)}u_{fq}^{c}+\omega_0\right)\cdot\frac{1}{s} \quad (7)$$

where θ_{PLL} is the reference phase produced by the PLL, k_{ppll} is the PLL proportional gain, k_{ipll} is the PLL integral gain and ω_0 is the reference grid frequency. The transformation from the grid *dq*-frame to the converter *dq*-frame is given by,

$$\mathbf{u_f^c}=\mathbf{u_f}e^{-j\theta_{PLL}},\ \mathbf{i_c^c}=\mathbf{i_c}e^{-j\theta_{PLL}} \quad (8)$$

In the steady state, the PLL phase is 0. Therefore, with $\theta_0 = 0$ and substituting the component form of (8) into (7),

$$\Delta\theta_{PLL}=\underbrace{\frac{F_{PLL}(s)}{s+u_{fd0}F_{PLL}(s)}}_{G_{PLL}(s)}\Delta u_{fq} \quad (9)$$

The PLL gains can be calculated using,

$$\tau_{pll}=\frac{2\xi}{\omega_{pll}},k_{p\text{-}pll}=\frac{2\xi\omega_{pll}}{u_{fd0}},k_{i\text{-}pll}=\frac{k_{p\text{-}pll}}{\tau_{pll}} \quad (10)$$

Where ξ is the PLL damping factor, ω_{pll} is the PLL bandwidth (in rad/s) and τ_{pll} is the PLL time constant [23].

3) Inner control loop

The inner control loop uses a proportional-integral (PI) controller to adjust the converter current. Decoupling terms on each axis are used for independent *d*- and *q*-axis current control. The ICL control laws are,

$$\Delta u_{cdref}=\Delta u_{fd}-F_{CL}(s)\left(\Delta i_{cdref}-\Delta i_{cd}\right)+\omega L_c\Delta i_{cq} \quad (11)$$

$$\Delta u_{cqref}=-F_{CL}(s)\left(\Delta i_{cqref}-\Delta i_{cq}\right)-\omega L_c\Delta i_{cd} \quad (12)$$

Where $F_{CL}(s) = k_{p\text{-}I} + k_{i\text{-}I}/s$ and $k_{p\text{-}I}$ and $k_{i\text{-}I}$ are the ICL proportional and integral gains, respectively. The controller gains are tuned using $k_{p\text{-}I} = L_c/\alpha$ and $k_{i\text{-}I} = R_c/\alpha$ where α is the current loop time constant, such that $\alpha = 1/\omega_{ICL}$. The full state-space representation of the ICL is given in [21].

4) Outer control loops

The *d*- and *q*-axis current references for the inner current loop are produced from PI control of the active power and AC voltage magnitude errors, respectively,

$$\Delta i_{cdref}^{c}=F_P(s)\left(\Delta P_{ref}^{c}-\Delta P^{cf}\right) \quad (13)$$

$$\Delta i_{cqref}^{c}=F_U(s)\left(\Delta U_{ref}^{c}-\Delta U^{cf}\right) \quad (14)$$

Where ΔP^{cf} is the filtered active power at the PCC, ΔU^{cf} is the filtered AC voltage magnitude at the PCC, $F_P(s) = k_{p\text{-}P} + k_{i\text{-}P}/s$ (where $k_{p\text{-}P}$ and $k_{i\text{-}P}$ are the APL proportional and integral gains, respectively) and $F_U(s) = k_{p\text{-}U} + k_{i\text{-}U}/s$ (where $k_{p\text{-}U}$ and $k_{i\text{-}U}$ are the AVL proportional and integral gains, respectively). The full state-space representations of the APL and AVL are derived in [21].

5) Low-pass filters

ΔP^c and ΔU^c, u_f and i_c are filtered through a first-order low-pass filter before being used as inputs to the controller. In the *dq*-frame the u_f and i_c low pass filters take account of the axis cross-coupling. The final structure of the state-space small signal model is shown in Fig. 2.

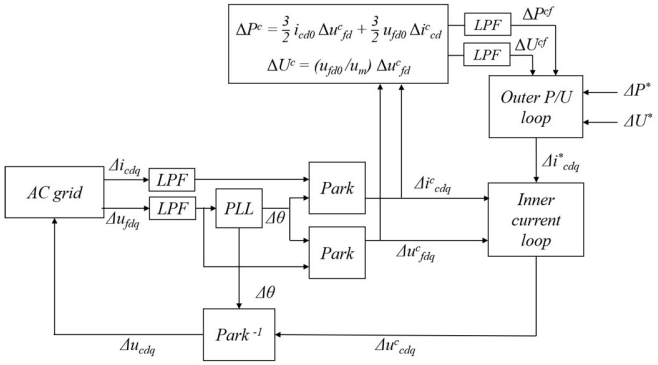

Fig. 2 - Schematic diagram of the linearized small signal model of the VSC and AC grid.

B. *Small Signal Validation*

The small signal model is validated by comparison with a non-linear MATLAB/Simulink time-domain simulation of the full system. Fig. 3 shows the results of 0.1 p.u. voltage and power steps in the small signal and time domain models. The small signal model shows very good transient agreement with the time-domain model and is therefore valid for small signal stability analysis.

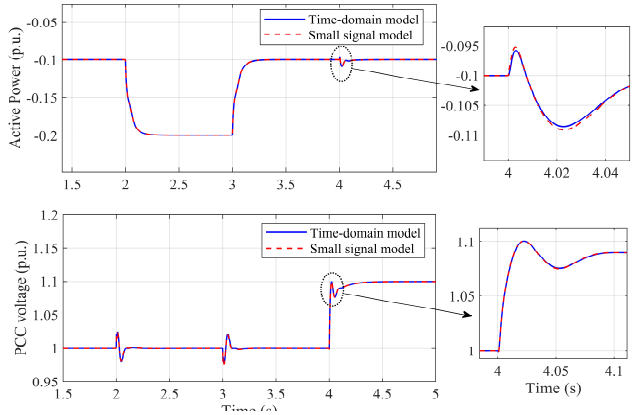

Fig. 3 - Small signal model validation with active power and PCC voltage response to 0.1 p.u. power and voltage step changes.

IV. VCC Stability Limits and Controller Interactions

Comprehensive active power limits for VCC-VSC are determined by performing sweeps across of a wide range of controller bandwidths. At each operating point, the maximum active power (measured at the PCC) that can be exchanged between the grid and the VSC whilst maintaining stability is calculated in both inverting and rectifying modes. For the ICL and PLL, the bandwidths can be varied directly by controlling α and τ_{pll} and are therefore defined by these quantities as in Section III.A. For the APL and AVL, no single parameter in the small signal model can exactly define the bandwidth due to the system cross-coupling. However, the integral gains $k_{i\text{-}P}$ and $k_{i\text{-}U}$ can be used as proxies for the APL and AVL bandwidths respectively while the proportional gains are kept constant. An approximate value of the +/- 3 dB bandwidth can then be extracted from the respective channel of the small signal model. The methodology to determine this power transfer limit for any given set of controller parameters is based on conventional eigenvalue analysis of the state space model. However, existing eigenvalue analysis methods examine the influence of only one variable (either active power transfer level or the tuning of one controller parameter). Therefore, a novel methodology has been developed to determine the stability limit as a function of three variables (two controller tunings and the active power). For each set of controller parameters, small signal models are constructed at power steps of 0.005 p.u. in the interval -1.0 to 1.0 p.u. using initial conditions calibrated from the time-domain simulation. Eigenvalue analysis is then used to determine if each of these systems is stable. The boundaries between stability and instability are determined by linear bisection, giving the inverting and rectifying active power transfer limits for that controller configuration. This process is repeated with the gains of two control loops fixed while the gains of the other two control loops are varied simultaneously. Values for the controller gains when a given loop is fixed are based on [20] and given in Table II. The gain and bandwidth ranges covered when varying a given loop are given in Table III. These ranges were chosen to provide at least one order of magnitude variation in ICL bandwidth and at least two orders of magnitude variation in APL, AVL and PLL bandwidths about the 'default' settings.

TABLE II
DEFAULT CONTROLLER TUNING PARAMETERS

Control loop	Parameters	Value
ICL	$\alpha = 1/\omega_{ICL}$ (s)	0.0015
	$k_{p\text{-}I}$	13.8
	$k_{i\text{-}I}$	217.3
PLL	$\tau_{pll} = k_{p\text{-}pll} / k_{i\text{-}pll}$(s/rad)	0.159
	$k_{p\text{-}pll}$	1.315×10^{-5}
	$k_{i\text{-}pll}$	8.263×10^{-5}
APL	$k_{p\text{-}P}$	1×10^{-6}
	$k_{i\text{-}P}$	1×10^{-3}
AVL	$k_{p\text{-}U}$	2×10^{-2}
	$k_{i\text{-}U}$	0.3

TABLE III
OPERATING POINT RANGES

Control loop	Parameter	Parameter range	Equivalent bandwidth range
ICL	α (s)	$10^{-4} - 10^{-3}$	$\omega_{ICL} = 100 - 1000$ Hz
PLL	τ_{pll} (s/rad)	0.0045 – 0.45	$\omega_{PLL} = 0.5 - 50$ Hz
APL	$k_{i\text{-}P}$	$10^{-4} - 10^{-2}$	$\omega_{APL} \approx 2.5 - 480$ Hz
AVL	$k_{i\text{-}U}$	0.03 – 30	$\omega_{AVL} \approx 0.5 - 230$ Hz

A. *Small Signal Model Results*

The operating point sweeps performed with the small signal model for maximum power transfer are shown in Fig. 4 to Fig. 9. Fig. 4 shows the active power transfer limits for varying ICL and PLL bandwidths, demonstrating two distinct high-stability regions at low and high PLL bandwidth in the

inverting mode, and an overall increase in stability with increasing ICL bandwidth. A low PLL bandwidth is proposed in e.g. [10], [22] to stabilize very weak grid AC systems. However, this proposed wider range analysis reveals an additional stable region at higher PLL bandwidths – this observation is discussed further in Section V.B. As discussed in [24], a slower ICL with respect to the PLL is destabilizing in both power directions due to the impact on the negative-real-part of the input-admittance.

Fig. 5 shows the active power transfer limits for varying APL and PLL bandwidths. Fig 5(a) shows a very similar pattern for the PLL bandwidth impact, but this effect is less exaggerated for the APL-to-PLL interaction than the ICL-to-PLL interaction. A slow APL improves stability in both power directions at all PLL bandwidths. The APL is shown in [8] to impact the PLL-related dominant oscillation mode. A fast APL increases the negative damping of this mode and thus destabilizes the system.

Fig. 6 shows the active power transfer limits for varying AVL and PLL bandwidths. In this case, two regions of stability at low and high PLL bandwidths are again visible in the inverting mode. However, a high AVL bandwidth increases stability at low PLL bandwidth, but the reverse holds at high PLL bandwidth. This is due to the competing influences of the non-minimum phase behavior of the power response and the negative damping off the PLL mode on the system stability. A step increase in the active power reference will increase i_{cd}, but in very weak grids this will cause a decrease in the PCC voltage. The AVL produces reactive power to support the voltage, but there is a delay in the control which leads to an initial decrease in the power [20]. As such, speeding up the AVL to decrease this non-minimum phase behavior will stabilize the system. However, as discussed in [8], the negative damping of the PLL-related dominant oscillation mode first increases and then reduces as the AVL bandwidth is increased. These competing mechanisms lead to complicated trends in the stability limits when the AVL is considered. In rectifying mode, stability decreases with increasing AVL and PLL bandwidths as the negative damping effects of the PLL mode dominate.

Fig. 7 shows the active power transfer limits for varying APL and ICL bandwidths. In inverting mode (Fig. 7(a)), stability is almost independent of APL bandwidth, but in rectifying mode a fast APL causes significant instability, particularly when the ICL is slow. This echoes the pattern seen in Fig. 5. If the APL bandwidth is too fast, the inner and outer loops are no longer decoupled by their different time scales and this destabilizes the system.

Fig.8 shows the active power transfer limits for varying AVL and ICL bandwidths. In inverting mode, a fast AVL is stabilizing. In this case the PLL bandwidth is fixed at 1 Hz (as per the 'default' values in Table II) and so the non-minimum phase effect of the power response dominates over the negative damping of the PLL mode. However, the AVL-to-ICL interaction is more complex in rectifying mode. When the ICL is fast, a slower AVL is stabilizing. As the ICL bandwidth decreases below approx. 680 Hz, the optimum AVL bandwidth increases. In rectifying operation, the negative damping of the PLL-mode competes more strongly with the non-minimum phase behavior of the power response, leading to a complex stability pattern.

Fig. 9 shows the active power transfer limits with varying APL and AVL bandwidths. Increasing the APL bandwidth decreases stability as seen in Fig. 5 and Fig. 7. There is an optimum, intermediate value of AVL bandwidth as different system modes dominant stability, as discussed in Fig. 6. For clarity, $k_{i\text{-}U}$ is plotted as the proxy for AVL bandwidth in Fig. 9 due to the impracticalities, discussed in Section IV, of directly specifying the bandwidth in the small signal model. The *dq*-frame cross-coupling means that the AVL bandwidth at a given value of $k_{i\text{-}U}$ varies slightly as the APL bandwidth is varied (via $k_{i\text{-}P}$) so each curve would require a unique axis in order to directly plot the bandwidth. However, an additional scale showing the approximate AVL bandwidth is included within Fig. 9.

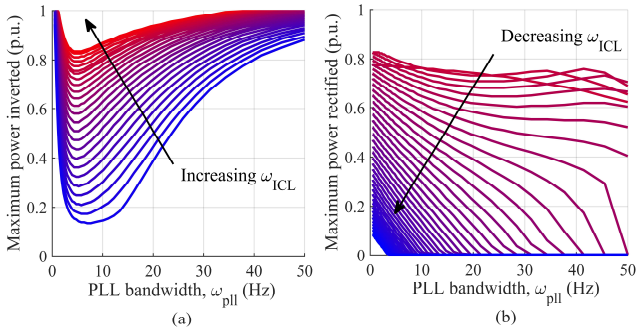

Fig. 4 - Maximum active power transfer as a function of ICL and PLL bandwidths (low ICL bandwidths shown in blue and high ICL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

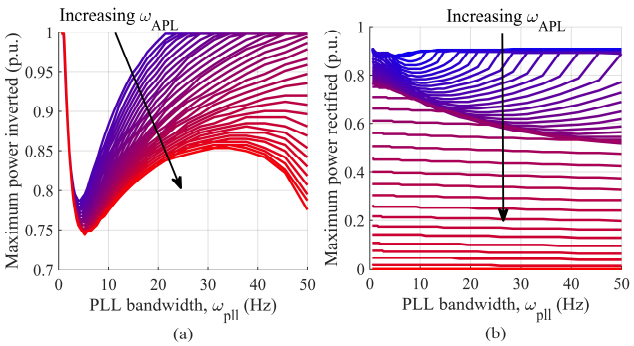

Fig. 5 - Maximum active power transfer as a function of APL and PLL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

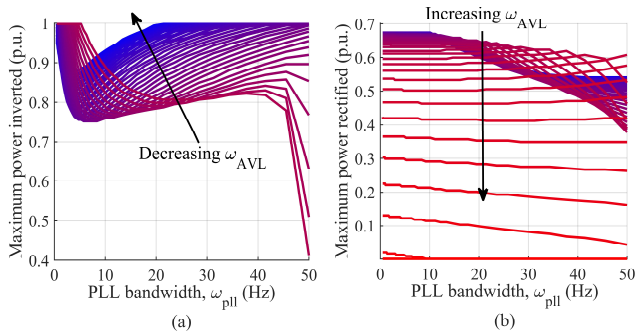

Fig. 6 - Maximum active power transfer as a function of AVL and PLL bandwidths (low AVL bandwidths shown in blue and high AVL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

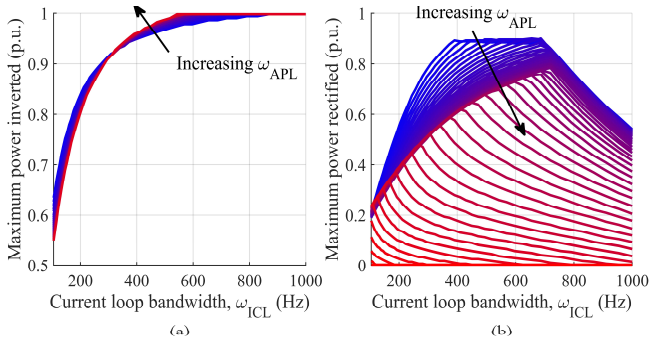

Fig. 7 - Maximum active power transfer as a function of APL and ICL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

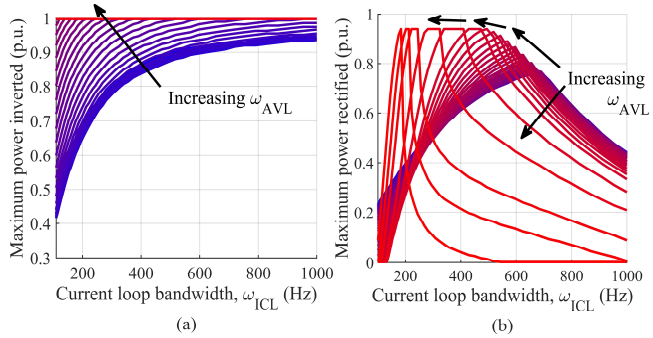

Fig. 8 - Maximum active power transfer as a function of AVL and ICL bandwidths (low AVL bandwidths shown in blue and high AVL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

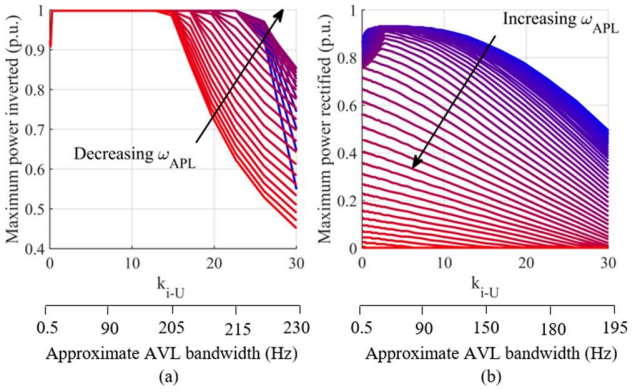

Fig. 9 - Maximum active power transfer as a function of APL and AVL bandwidths (low APL bandwidths shown in blue and high APL bandwidths in red): (a) inverting mode, and (b) rectifying mode.

B. Impedance Model Analysis

To validate the novel stability methodology presented in Section IV.A, a secondary analysis (impedance modelling) method is used to corroborate the state space model results. Impedance modelling can fully substitute state space small signal modelling [25], [26] and so can be used to independently reproduce the results of Section IV.A and thus give confidence to the presented methodology. In this section, an impedance model for a grid-connected VSC is derived and shown to successfully reproduce the same bandwidth sweep results in Section IV.A. The converter-grid system is represented by a Norton-Thevenin equivalent model; the VSC converter is represented by a current source with an output admittance $\mathbf{Y}(s)$, while the AC grid is modelled by a voltage source in series with an impedance, $\mathbf{Z_g}(\omega_g,s)$, as shown in Fig. 10 [25], [27]. This leads to equation (15) for the converter output current.

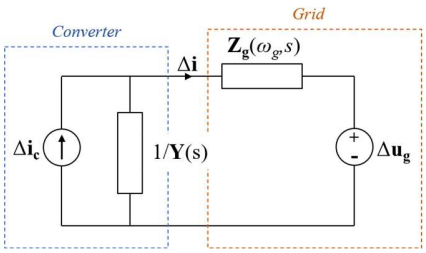

Fig. 10 - Equivalent circuit impedance model of a grid-connected VSC.

$$\Delta\mathbf{i} = \left[\Delta\mathbf{i_c} - \mathbf{Y}(s)\Delta\mathbf{u_g}\right]\cdot\frac{1}{\left[\mathbf{I}+\mathbf{Y}(s)\mathbf{Z_g}(\omega_g,s)\right]} \tag{15}$$

Where,

$$\mathbf{Z_g}(\omega_g,s) = \begin{bmatrix} R_n + sL_n & -\omega_g L_n \\ \omega_g L_n & R_n + sL_n \end{bmatrix} \tag{16}$$

As established in [27], the stability of the system can be determined by applying the Nyquist stability criterion to the open-loop gain $\mathbf{Y}(s)\mathbf{Z_g}(\omega_g,s)$or by examining the poles of the closed loop, $[\mathbf{I} + \mathbf{Y}(s)\mathbf{Z_g}(\omega_g,s)]^{-1}$. For this analysis, the impedance model is deemed to be stable if all closed-loop poles exist in the left-hand plane. The converter admittance is derived in the grid frame and described in equations (17) to (19) and Fig. 11. For simplicity, this impedance model retains only the ΔP, ΔU and Δu_{fd} filters shown in Fig. 2. Further details of the impedance model derivation are given in Appendix B.

$$\Delta\mathbf{i_c}=\mathbf{Y}(s)\Delta\mathbf{u_f} \tag{17}$$

$$\Delta\mathbf{i_c}=\mathbf{G_c}(s)\Delta\mathbf{i_{cref}}+\mathbf{Y_i}(s)\Delta\mathbf{u_f} \tag{18}$$

$$\Delta\mathbf{i_c}=\mathbf{G_c}(s)[\mathbf{G_0}(s)\Delta\mathbf{u_f}]+\mathbf{Y_i}(s)\Delta\mathbf{u_f} \tag{19}$$

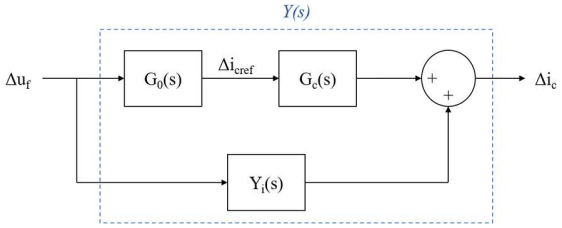

Fig. 11– Block diagram of VSC admittance.

Where the components of Fig. 11 are given by,

$$\mathbf{G_c}(s) = \begin{bmatrix} \frac{1}{1+s\alpha} & 0 \\ 0 & \frac{1}{1+s\alpha} \end{bmatrix} = \begin{bmatrix} g_c(s) & 0 \\ 0 & g_c(s) \end{bmatrix} \tag{20}$$

$$\mathbf{Y_i}(s) = \begin{bmatrix} \frac{1 - H_{u\text{-}dd}(s)}{F_{CL}(s)+R_c+sL_c} & \frac{aG_{pll}(s) - H_{u\text{-}qd}(s)}{F_{CL}(s)+R_c+sL_c} \\ 0 & \frac{1+bG_{pll}(s)}{F_{CL}(s)+R_c+sL_c} \end{bmatrix} \tag{21}$$

$$\mathbf{G_0}(s)=\begin{bmatrix} -G_{pd}(s) & -G_{pq}(s) \\ -H(s)F_U(s)\dfrac{u_{fd0}}{u_m} & -H(s)F_U(s)\dfrac{u_{fq0}}{u_m} \end{bmatrix} \quad (22)$$

$$\begin{cases} G_{pd}(s) = \dfrac{1.5H(s)F_P(s)\left(i_{cd0}+u_{fd0}\,y_{dd}(s)\right)}{1+1.5u_{fd0}\,g_c(s)H(s)F_p(s)} \\ G_{pq}(s) = \dfrac{1.5H(s)F_P(s)\left(i_{cq0}+u_{fd0}\,y_{qd}(s)\right)}{1+1.5u_{fd0}\,g_c(s)H(s)F_p(s)} \end{cases} \quad (23)$$

$$\begin{cases} a=u_{cq0}+\omega L_c i_{cd0}-F_{CL}(s)i_{cq0} \\ b=u_{cd0}-\omega L_c i_{cq0}-F_{CL}(s)i_{cd0} \end{cases} \quad (24)$$

$F_{CL}(s)$, $F_P(s)$ and $F_U(s)$ are defined in Section III.A.3) and further expressions within (20) to (24) to are described in Appendix B. All the bandwidth sweeps shown in Fig. 4 to Fig. 9 can be reproduced using this impedance model. For small signal modeling results validation, only active power transfer limits with varying ICL and PLL bandwidths (including inverting and rectifying modes) are shown in Fig. 12. The impedance model stability limits match those of the small signal model. Note that, for fair comparison, the state-space small signal model is amended here to contain the same low-pass filters as the impedance model. This therefore validates the active power transfer and controller bandwidth interaction results that were produced with the state-space small signal model and shows that the impedance model is equally valid for stability analysis.

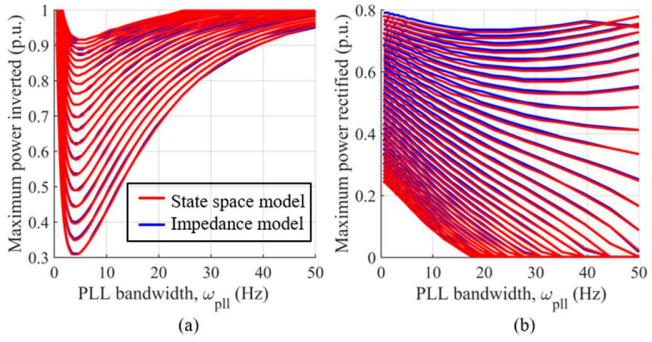

Fig. 12 - Maximum active power transfer as a function ICL bandwidth and PLL bandwidth, as predicted by the impedance model (blue) and the small signal model (red): (a) inverting mode, and (b) rectifying mode.

V. Discussion

A. General Observations

In inverting mode, rated active power can be transferred if appropriate controller parameters are chosen. However, in rectifying mode, rated active power cannot be achieved at any operating point. Small signal stability is more sensitive to controller tuning and control loop interactions in rectifying mode than in inverting mode. This makes intuitive sense given the asymmetry between active power exchanged and converter voltage angle in the steady-state [29]. A fast ICL with respect to the outer loops is required for maximum stability. In general, slowing down the APL, AVL and PLL (i.e. decreasing the bandwidths) improves the system stability. The exception to this is the AVL at some operating points and the multiple stable regions of PLL bandwidth in inverting mode. With a slow ICL or fast PLL, increasing the AVL bandwidth can increase the maximum active power transfer (e.g. Fig. 6(a) and Fig. 8). The impact of grid strength on stability can be more easily examined using the impedance model derived in Section IV.B. Fig. 13 shows the bode diagram of the closed-loop impedance model, $[\mathbf{I}+\mathbf{Y}(s)\mathbf{Z_g}(\omega_g,s)]^{-1}$ at SCR = 1, 2, 3 and 5. In Fig. 13, part (a) shows the bode diagram from Δu_{fd} to Δi_{cd}, part (b) shows the bode diagram from Δu_{fq} to Δi_{cd}, part (c) shows the bode diagram from Δu_{fd} to Δi_{cq} and part (d) shows the bode diagram from Δu_{fq} to Δi_{cq}. For SCR = 1, all of the responses in Fig. 13 show very strong resonances at the PLL bandwidth (1 Hz) but these resonances are almost non-existent when the grid is strengthened. A large grid impedance amplifies the coupling between the grid and the controller via the PLL and thus decreases the stable operating region of vector control. The effect of the PLL is examined more closely in the following section.

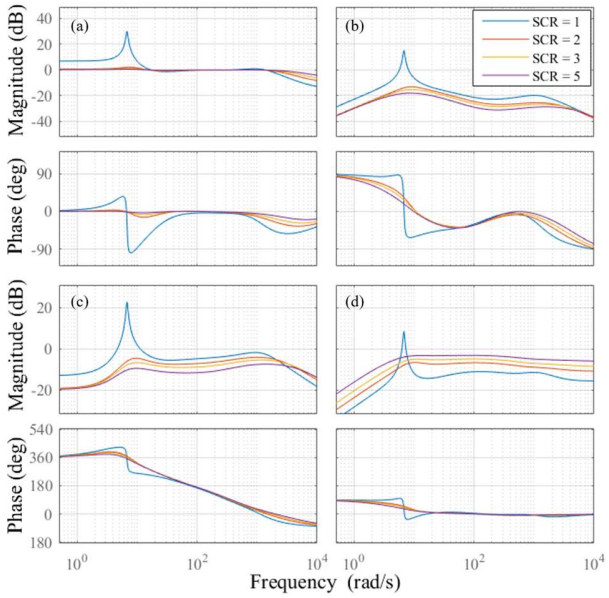

Fig. 13 - Bode diagram of the closed-loop impedance model at varying SCR: (a) Δu_{fd} to Δi_{cd}, (b) Δu_{fq} to Δi_{cd}, (c) Δu_{fd} to Δi_{cq}, and (d) Δu_{fq} to Δi_{cq}.

B. PLL Operating Regions

Fig. 4(a), Fig. 5(a) and Fig. 6(a) show two distinct regions of high system stability for inverting operation. Optimum performance (i.e. maximum active power injection to the AC grid) is achieved at both very low PLL bandwidth ($\omega_{PLL} < 5$ Hz) and some higher PLL bandwidths ($\omega_{PLL} > 30$ Hz). This stability variation is again easier to analyze using the impedance model developed in Section IV.B. As discussed, stability is determined by the impedance ratio $\mathbf{Y}(s)\mathbf{Z_g}(\omega_g,s)$; specifically, it is the *dq* component of each impedance which is limiting in very weak grids i.e. i_{cd} to u_{fq}. Fig. 14 shows the bode diagrams of $[\mathrm{Y}(s)]^{-1}_{dq}$ and $Z_{g\text{-}dq}(\omega_g,s)$ for PLL bandwidth from 0.5 Hz to 50 Hz. A magnitude of $[\mathrm{Y}(s)]^{-1}_{dq}$ below the $Z_{g\text{-}dq}(\omega_g,s)$ grid impedance magnitude is one indicator of system

instability. It can be seen that this occurs only at intermediate values of PLL bandwidth. At high ω_{PLL}, the VSC behaves as a grid-following converter i.e. the controller reference frame is synchronized to transient changes in the PCC voltage phase via the PLL. However, at very low ω_{PLL}, the PLL effectively provides a fixed reference angle, which depends only on the steady-state value of the PCC voltage phase. This leads to an interesting phenomenon at low ω_{PLL} in which the controller appears to mimic some of the behaviors of grid-forming operation. Between these regions, active power transfer performance is significantly reduced as the PLL is too slow to synchronize effectively with the grid, but too fast to provide a fixed reference angle. Depending on the power transfer and transient performance requirements, VSCs in weak grids could therefore be deployed in a conventional grid-following mode or in this quasi-fixed-angle mode by simply changing the PLL bandwidth. Regardless of the mode selection, the operating point must be comfortably within one of these stable regions.

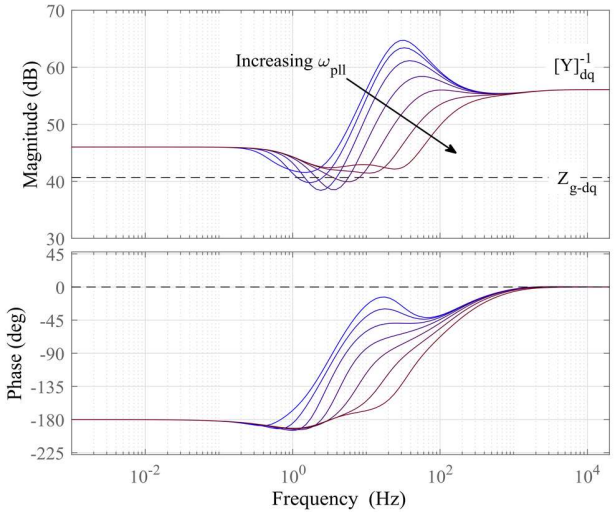

Fig. 14 - Bode diagram of the *dq* VSC and grid impedances with varying PLL bandwidth.

These distinct regions of high stability are not present in rectifying operation, but there is an overall decrease in stability as PLL bandwidth increases. It would therefore be recommended that operation with a slow PLL bandwidth is chosen in systems where bi-directional power flow is required. However, for rectifying operation alone there is no requirement to avoid intermediate PLL bandwidth values.

C. Stability Assessment and Safe Operating Region

The operating point sweeps described in Section IV can be applied, with appropriate modifications, to all VCC-based VSC control strategies. This gives a much more detailed view of system stability and controller interactions than the single operating point analyses that are commonly performed. Insights are also provided into the robustness of conventional VCC to tuning variations. Present analysis at a single operating point gives no indication of performance away from the design point, and so could be vulnerable to inaccuracies in system quantification. However, the output of this more comprehensive evaluation is a stability bubble of operating points as which stable operation is ensured. A suggested definition for this region is:

> All operating points at which the system remains stable for ≤ **1.0 p.u.** active power transfer into the AC grid (i.e. inverting) and for ≤ **0.70 p.u**. active power transfer into the DC link (i.e. rectifying).

A rectifying power level of 0.7 p.u. is chosen to ensure a large enough operating region for meaningful analysis. Evidently, this is difficult define in four-dimensional space if considering all controller components. However, as discussed in [14], [30] and Section V.A, a fast ICL is considered a basic requirement for vector control. Therefore, this region is defined only as a function of the PLL, APL and AVL bandwidths. This stability bubble definition is technology agnostic, so any stability analysis method (e.g. impedance modelling, eigenvalue analysis, bode diagrams) can be used to determine the controller parameters which satisfy these criteria. For this work, stability is assessed using eigenvalue analysis of the state space small signal model. The eigenvalues of this MIMO system, λ_{PU}, are a function of ω_{APL}, ω_{AVL}, ω_{PLL}, ω_{ICL}, P^{ref} and U^{ref}. By setting the ICL bandwidth at the 'default' value given in Table II and ΔU^{ref} = 1.0 p.u., minimum power transfer levels can then be chosen so that the eigenvalues now depend only on the APL, AVL and PLL bandwidths. The small signal model is reproduced at every combination of these bandwidths for the ranges in Table III and the system eigenvalues are checked for stability. This criterion produces a stability bubble of PLL, APL and AVL controller tunings, shown in Fig. 15. This region represents all combinations of PLL, APL and AVL parameters which can achieve between -1.0 p.u. and 0.7 p.u. power transfer.

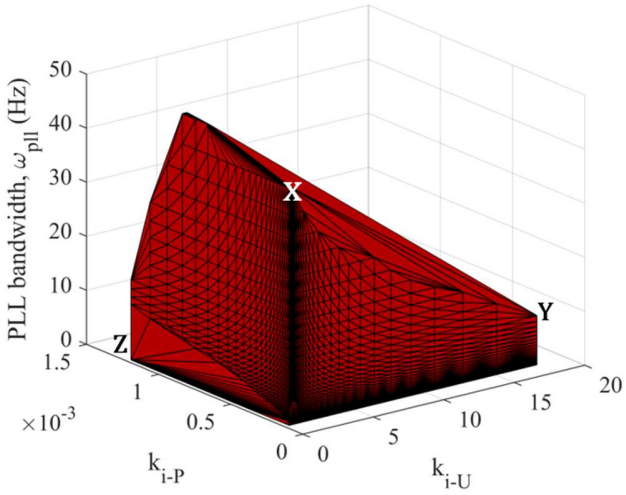

Fig. 15 – Stable operating region for -1.0 p.u. < *P* < 0.7 p.u.

Time-domain simulations at the 'corners' of this stability region (X, Y, Z) are shown in Fig. 16 to validate the stability boundary. These points were selected in order to cover a broad range of operating points within the stability bubble and a different controller parameter is used to induce instability in each case. Fig. 16(a) corresponds to point X marked on Fig. 15and instability is caused by perturbing the PLL bandwidth. Fig. 16(b) corresponds to point Y and instability is caused by perturbing the AVL bandwidth. Fig. 16(c) corresponds to

point Z and instability is caused by perturbing the APL bandwidth. At X and Y, the inverting mode is the limiting case (at -1.0 p.u.), and at Z the rectifying mode is limiting (at 0.7 p.u.). The controller parameters at these points are given in Table IV.

TABLE IV
CONTROLLER PARAMETERS AT SMALL SIGNAL STABILITY BOUNDARY

Corner point	Parameters within boundary (stable)	Parameters outside boundary (unstable)
X	ω_{pll} = 44 Hz $k_{i\text{-}P}$ = 1 x 10^{-4} $k_{i\text{-}U}$ = 0.1	ω_{pll} = 45 Hz $k_{i\text{-}P}$ = 1 x 10^{-4} $k_{i\text{-}U}$ = 0.1
Y	ω_{pll} = 9.5 Hz $k_{i\text{-}P}$ = 1 x 10^{-4} $k_{i\text{-}U}$ = 18.0	ω_{pll} = 9.5 Hz $k_{i\text{-}P}$ = 1 x 10^{-4} $k_{i\text{-}U}$ = 18.3
Z	ω_{pll} = 0.5 Hz $k_{i\text{-}P}$ = 1.2 x 10^{-3} $k_{i\text{-}U}$ = 0.3	ω_{pll} = 0.5 Hz $k_{i\text{-}P}$ = 1.3 x 10^{-3} $k_{i\text{-}U}$ = 0.3

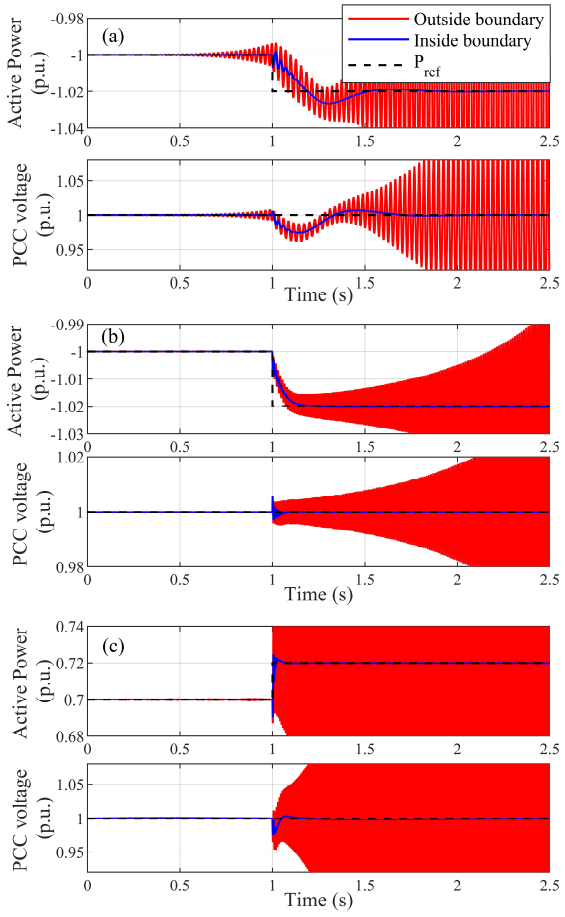

Fig. 16 – Active power and PCC voltage responses to a 0.02 p.u. step in active power inside (blue) and outside (red) the stability boundary at (a) point X, (b) point Y and (c) point Z in Fig. 15.

The definition of this stability region can be adapted as required. Fig. 17 shows an equivalent stability bubble for active power transfer of up to 0.9 p.u. in inverting mode and up to 0.6 p.u. in rectifying mode. This region represents all combinations of PLL, APL and AVL parameters which can achieve between -0.9 p.u. and 0.6 p.u. power transfer.

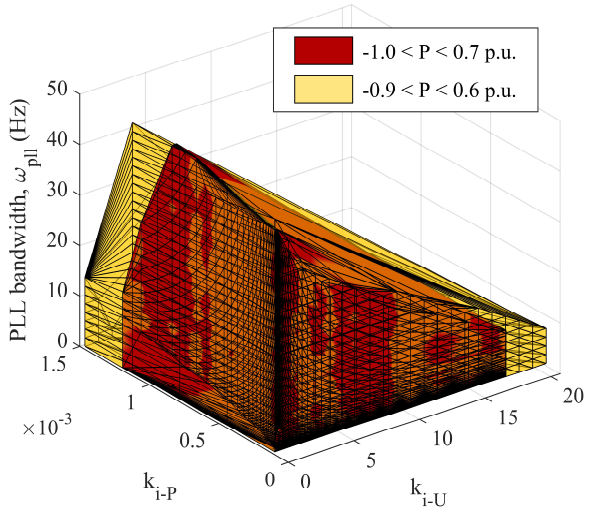

Fig. 17 - Stable operating region for -1.0 p.u. < P < 0.7 p.u. (red) and -0.9 p.u. < P < 0.6 p.u. (yellow).

D. Robustness

The stability region presented in Section V.C should be robust enough under different SCR or errors in grid impedance uncertainty. This can be tested by reproducing the stability bubble at different SCR. Fig. 18 shows the same stability bubble in Fig. 15 (at SCR = 1) and the equivalent stable operating regions for SCR = 2 and SCR = 3. The stability bubbles at SCR = 3 and SCR = 2 include all the stable operating points for SCR = 1. The SCR = 1 condition is therefore the limiting state for stability and so analysis at this point is sufficient to ensure stable operation at higher SCR.

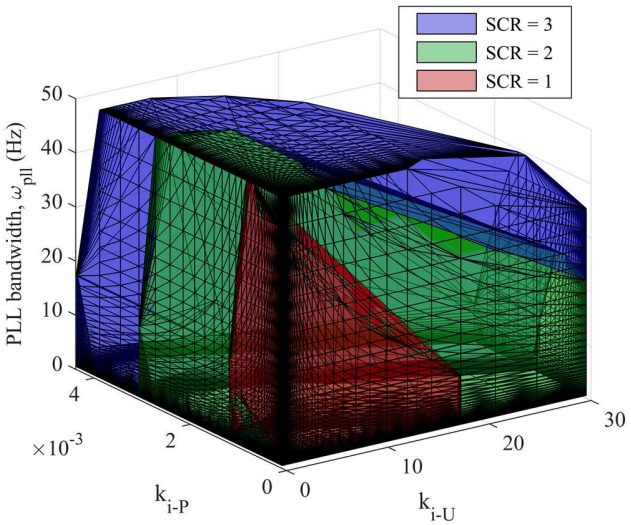

Fig. 18 - Stable operating region for -1.0 p.u. < P < 0.7 p.u. at SCR = 1, 2 and 3.

E. Dynamic Performance Considerations

The results in Section IV.A suggest that the VCC-VSC can operate stably across a wide range of controller tunings.

Indeed, there appear to be regions where large parameter changes have a negligible impact on the system stability limit e.g. Fig. 8(a) shows that, at high AVL bandwidth, the ICL bandwidth has minimal impact on the power transfer limit. However, the dynamic performance at these points is very different. The above stability bubble analysis should therefore be extended to consider the operating region where both stability and acceptable transient performance are achieved. Operating regions are defined for which the stability condition in Section V.C is met, and where the system step response meets the following requirements:

1. Overshoot < 20%
2. Settling time (within 2% of steady-state value) < 0.75 s

For a unit step in active power demand at the specified power transfer levels (-1.0 p.u. and 0.7 p.u.), Fig. 19 shows the outer stability bubble from Fig. 15 and an inner dynamic performance bubble. This dynamic performance bubble represents all combinations of PLL, APL and AVL parameters which can achieve between -1.0 and 0.7 p.u. power transfer and at which a unit power step meets the transient performance requirements above; as expected, the operating region for acceptable transient performance is smaller than that for absolute stability.

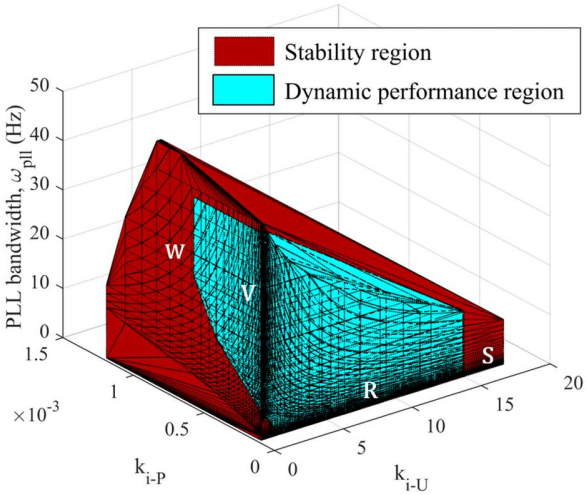

Fig. 19 - Stable operating region for -1.0 p.u. < P < 0.7 p.u. (red) and acceptable transient performance region (cyan) (a unit step for active power demand).

TABLE V
CONTROLLER PARAMETERS AT DYNAMIC PERFORMANCE POINTS

Operating point (Fig. 19)	Controller parameters	Stable	Good dynamic performance
V	ω_{pll} = 30 Hz, $k_{i\text{-}P}$ = 1 x 10^{-4}, $k_{i\text{-}U}$ = 3	Yes	Yes
W	ω_{pll} = 30 Hz, $k_{i\text{-}P}$ = 6 x 10^{-4}, $k_{i\text{-}U}$ = 3	Yes	No
R	ω_{pll} = 0.5 Hz, $k_{i\text{-}P}$ = 1.3 x 10^{-4}, $k_{i\text{-}U}$ = 7	Yes	Yes
S	ω_{pll} = 0.5 Hz, $k_{i\text{-}P}$ = 1.3 x 10^{-4}, $k_{i\text{-}U}$ = 17	Yes	No

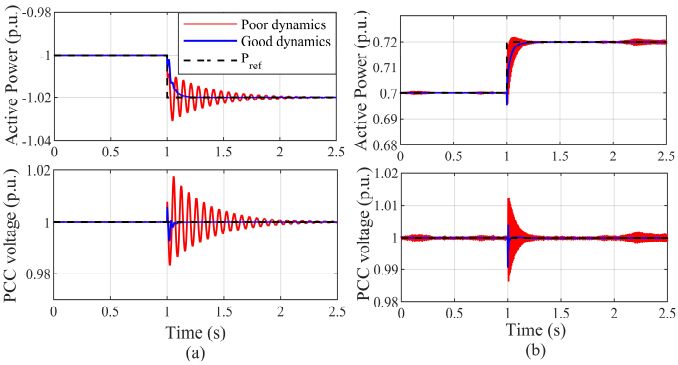

Fig. 20 - Active power and PCC voltage responses to a 0.02 p.u. power step inside and outside the dynamic performance bubble at (a) points V and W, Fig. 19 and at (b) points R and S, Fig. 19.

Fig. 20 shows examples of time-domain simulations within this dynamic stability region and within the intermediate region of absolute stability with unacceptable transient performance. The controller parameters at these points are given in Table V and are marked on Fig. 19. This analysis can therefore be used to investigate dynamic performance, and the sensitivity of transient performance to controller tuning, without the requirement for protracted time-domain simulations.

F. Design process recommendations

This method for development of the stability bubble and dynamic performance region can also be used as a valuable tool for controller design and tuning. The power transfer requirements and dynamic performance constraints for a given application can be used to amend the stability definition in Section V.C and the acceptable dynamic performance definition in Section V.D. Following the developed methodology with these alternative conditions will thus provide the operator with all combinations of controller parameters that meet their specific design requirements. Crucially, this reveals those controller operating points which are not only stable but are also surrounded by sufficient stable parameter space that they are robust to parameter uncertainty or tuning deviations.

VI. CONCLUSIONS

This paper has established bidirectional active power transfer limits for classical vector control of VSCs across a broad range of controller operating points. All interactions between inner and outer control loops and the PLL have been shown to produce a significant impact on system stability and therefore must not be neglected in favor of a focus on the PLL alone. The controller parameter sweeps performed in this analysis provide an objective evaluation of VCC-based VSC control strategies. The study has considered the performance at a wide range of controller bandwidths to inform transient performance and stability insights, rather than studying a single operating point as is considered in existing literature. Observing the effect of controller bandwidth has also revealed distinct stable operating regions for the PLL, showing that multiple modes of operation can be achieved with intelligent tuning of a single VSC control structure. This allows for more

widespread implementation of established VCC-VSC technologies in AC grids with fluctuating impedance and variable control requirements. A stability bubble is established for VCC-VSC within which stability can be guaranteed at a given active power transfer level. The consideration of wider operating points is also shown to be significant for achieving acceptable dynamic performance. The operational envelope for good dynamic performance is smaller than that for absolute stability but still covers a range of controller operating points. Operating at controller gains within this region can achieve rated power transfer in inverting mode and good dynamic performance with no changes to the conventional VCC control structure. Controller interactions and dynamic performance considerations are overlooked by conventional controller analysis at a single operating point, and so this method offers considerably higher objectivity and robustness for evaluation of vector control based VSC. Practical recommendations arising from this research include the avoidance of intermediate PLL bandwidths (approx. 5 – 30 Hz), which offer poor stability, and the implementation of customized control tunings for inverting and rectifying operation. Care should also be taken to ensure that the PLL and ICL bandwidths are considered when tuning the *q*-axis outer loop bandwidth. If these interactions are taken into account, conventional VCC is shown to perform much better than is currently assumed and can inject nominal active power to a very weak AC grid with no modifications to the controller structure.

APPENDIX - IMPEDANCE MODEL

Substituting (8) and the current loop law (11) into the linearized grid equations (1)-(6) gives,

$$\begin{aligned}\Delta i_{cd} &= \frac{F_{CL}(s)}{(F_{CL}(s)+R_c+sL_c)}\Delta i_{cdref} \\ &+ \frac{1-H_{u\text{-}dd}(s)}{(F_{CL}(s)+R_c+sL_c)}\Delta u_{fd} \\ &+ \frac{G_{pll}(s)\left(\omega L_c i_{cd0} - F_{CL}(s) i_{cq0}+u_{cq0}\right) - H_{u\text{-}qd}(s)}{(F_{CL}(s)+R_c+sL_c)}\Delta u_{fq}\end{aligned} \tag{25}$$

$$\begin{aligned}\Delta i_{cq} &= \frac{F_{CL}(s)}{(F_{CL}(s)+R_c+sL_c)}\Delta i_{cqref} \\ &+ \frac{1+G_{pll}(s)\left(u_{cd0} - \omega L_c i_{cq0} - F_{CL}(s) i_{cd0}\right)}{(F_{CL}(s)+R_c+sL_c)}\Delta u_{fq}\end{aligned} \tag{26}$$

Where

$$H_{u\text{-}dd}(s) = \frac{s\tau_f+1}{(s\tau_f+1)^2+(\omega\tau_f)^2} \tag{27}$$

$$H_{u\text{-}qd}(s) = \frac{\omega\tau_f}{(s\tau_f+1)^2+(\omega\tau_f)^2} \tag{28}$$

However,

$$\begin{aligned}F_{CL}(s) &= k_{p\text{-}I}+\frac{k_{i\text{-}I}}{s} = \frac{sL_c+R_c}{s\alpha} \\ \Rightarrow \frac{F_{CL}(s)}{(F_{CL}(s)+R_c+sL_c)} &= \frac{1}{s\alpha+1}\end{aligned} \tag{30}$$

Equations (25) and (26) in matrix form give $\mathbf{G_c}(s)$ and $\mathbf{Y_i}(s)$ in (20) and (21). $\mathbf{G_0}(s)$ is derived from consideration of the outer loop control laws. For the *d*-axis,

$$\Delta i_{cdref} = -1.5H(s)F_P(s)\begin{pmatrix} i_{cd0}\Delta u_{fd} \\ +i_{cq0}\Delta u_{fq}+u_{fd0}\Delta i_{cd}\end{pmatrix} \tag{31}$$

Substituting (20) and (21) into(30),

$$\begin{aligned}&\Delta i_{cdref}\left(1+1.5H(s)F_P(s)u_{fd0}g_c(s)\right) = \\ &-1.5H(s)F_P(s)\begin{pmatrix}\left(i_{cd0}+u_{fd0}y_{dd}(s)\right)\Delta u_{fd} \\ +\left(i_{cq0}+u_{fq0}y_{qd}(s)\right)\Delta u_{fq}\end{pmatrix}\end{aligned} \tag{32}$$

$$\therefore \Delta i_{cdref} = -G_{pd}(s)\Delta u_{fd} - G_{pq}(s)\Delta u_{fq} \tag{33}$$

Where $G_{pd}(s)$ and $G_{pq}(s)$ are given in (23) and

$$H(s) = \frac{1}{s\tau_f+1} \tag{36}$$

For the *q*-axis,

$$\Delta i_{cqref} = -H(s)F_U(s)\left(\frac{u_{fd0}}{u_m}\Delta u_{fd} + \frac{u_{fq0}}{u_m}\Delta u_{fq}\right) \tag{37}$$

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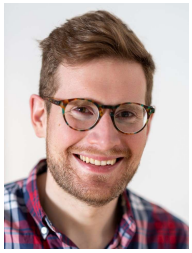

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