Real Time Evaluation of Wavelet Transform for Fast and Efficient HVDC Grid Non-Unit Protection

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***Abstract*—This paper presents a real-time evaluation of a Wavelet Transform (WT) for HVDC grid non-unit protection. Due to its time and frequency localisation capability, WT can successfully extract the necessary information present in the voltage transients following a DC fault. This capability is exploited to achieve fast and selective HVDC grid protection. A Digital Signal Processor (DSP) is employed to execute real-time Stationary Wavelet Transform (SWT) on voltage signals using discrete convolution to efficiently compute the WT coefficients. Hardware-in-the loop (HIL) simulation is performed to test a WT-based hardware module using a Digital Real-Time Simulator (DRTS), in which a meshed HVDC grid is modelled. The closed-loop interaction enables the hardware device to emulate a protection relay that can generate trip commands for the HVDC breakers integrated within the HVDC grid model. The real-time simulations demonstrate the technical feasibility, speed and robust performance of the SWT implementation.**

***Index Terms*—HVDC grids, HVDC grid protection, Real-time implementation, Wavelet Transform (WT).**

I. Introduction

HVDC grids constitute an attractive option for bulk power transfer over long distances and facilitate the integration of large offshore wind farms dispersed over wide geographical areas with the onshore AC grids. One of the key-enabling technologies towards the realisation of the HVDC grid concept is the development of well performing and cost-effective DC protection systems [1]. Without adequate protection solutions, converter stations will block their operation, resulting in the undesirable loss of power transfer between the HVDC grid and the adjacent AC networks. Owing to the very high rate of rise of fault currents and under-voltages during DC faults, DC protection systems are characterised by more stringent requirements than AC systems in terms of speed, selectivity, sensitivity and reliability.

Wavelet analysis is a powerful signal processing tool that has the ability to detect singularities and abrupt, local changes in a signal such as voltage transients after a fault. Therefore, WT can be employed and applied on terminal voltage measurements for HVDC fault detection. The series reactors that are commonly placed at the ends of HVDC transmission media do not only limit the fault current, but they also behave as natural boundaries for a range of frequencies [2]. Based on this, the voltage signatures of DC faults outside the protected line or cable are influenced due to the inductive termination. Consequently, series reactors impact the frequency characteristic of the measured voltage and hence the resulting WT outputs (coefficients), thus providing the capability for discriminating DC line/cable faults from external faults based exclusively on local measurements (nonunit protection).

Wavelet transform has been widely used in the literature [3]–[5], thus verifying the strength of the technique for HVDC grid protection but limited practical implementations has been reported. In particular, real-time implementation of WT has been reported for AC power system protection based on a Digital Signal Processor (DSP) [6], and a Programmable Field Gate Array (FPGA) [7], while hardware platforms have been employed for the practical implementation of WT-based HVDC protection [8], [9]. In all these applications, Discrete Wavelet Transform (DWT) has been utilised due to its reduced complexity. Nevertheless, the downsampling stages involved in DWT lead to loss of high frequency information which may compromise the performance in detecting and discriminating DC faults.

To eliminate the downsampling stages of the analysed signal, Stationary Wavelet Transform (SWT) can be used instead at the cost of additional computational burden. Therefore, this paper introduces an approach for designing an efficient real-time SWT implementation for HVDC grid protection based on DSP technology and validates its technical feasibility through hardware-in-the-loop simulations using DRTS. The rest of the paper is organised as follows. Section II introduces the principles of WT that are then used in Setion III for developing an approach for implementing SWT on a DSP platform. Moreover, the test model developed within DRTS is described and the simulation results that demonstrate the suitability of SWT for fast-transient HVDC protection are presented in IV. Finally, conclusions are drawn in Section V.

II. Wavelet Transform Theory

Wavelet analysis is a powerful signal processing tool that can achieve adequate resolution in both the time and frequency domains. One of the main strengths of wavelet transform (WT) is its ability to detect singularities and abrupt, local changes in a signal such as voltage and current transients after a fault. Therefore, WT can be employed and applied on voltage measurements captured by protection relays for

protecting DC lines from DC faults. The difference between an internal fault on the line protected by a relay from an external fault that occurs beyond the series inductor (on an adjacent line or a bus fault) is that the frequency characteristic of the measured voltage for an external fault is influenced due to the presence of DC reactors at line ends. In turn, the series reactor influences the resulting WT outputs (coefficients).

WT is characterised by a dilation or scale parameter (α) and a translation or position parameter (β). The scale parameter determines the size of the window in which the transform is performed. Translation corresponds to the action of shifting the wavelet forward in time while analysing the entire signal. By manipulating the scale and position parameters, the time-frequency properties of the original signal can be identified. The continuous wavelet transform (CWT) of a signal *u(t)* with scale α at time *t* is calculated through the following formula

$$WT_{(\alpha,\beta)}u(t) = \int_{-\infty}^{+\infty} u(t)\frac{1}{\sqrt{\alpha}}\psi^*(\frac{t-\beta}{\alpha})dt \qquad (1)$$

where ψ^* is the daughter wavelet that is a scaled and shifted version of the mother wavelet function ψ. This equation implies that WT works in a similar manner as Fourier Transform, where the correlation between the signal to be analysed (*u(t)*) and the analysing function (i.e. the wavelet) is computed for different sets of α, β parameters.

The calculation of wavelet coefficients through CWT at every possible scale involves intensive computational work and results in a large number of coefficients. Therefore, for the application of WT in real-time applications, such as DC fault detection, faster processing algorithms are required. Discrete Wavelet Transform (DWT) can be employed to provide a more efficient solution while maintaining high levels of accuracy. The main difference between CWT and DWT lies in the way scale and translation parameters are defined. In DWT these parameters are discretised and can only take values based on the powers of two. This results in dyadic scales and positions that are expressed as follows:

$$\begin{gathered}\alpha = 2^j \quad (j = 0, 1, 2...) \\ \beta = k \cdot \alpha\end{gathered} \qquad (2)$$

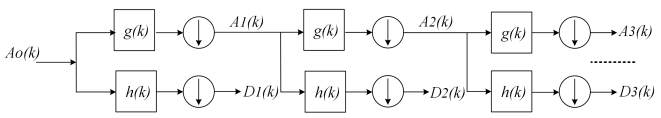

Fig. 1: Multiresolution Analysis.

This scheme can be realised with the use of filters, as proposed by Mallat. The proposed algorithm is in fact, a two-channel subband coder, in which the filters that are typically used are the Quadrature Mirror Filters (QMF), where one filter is a mirror image of the other filter around $\pi/2$. This practical filtering technique is called fast wavelet transform. The principles of fast wavelet transform are based on multiresolution analysis, according to which, the signal is passed through successive layers of low-pass and high-pass filters and each layer (or level *j*) produces low frequency approximation (A_j) and high frequency detailed (D_j) coefficients, respectively. DWT based on multiresolution analysis is represented graphically in Fig. 1, where *g(k)* is the low-pass filter (LPF) and *h(k)* is the high-pass filter (HPF).

One significant drawback of DWT for HVDC grid protection purposes is that the resulting detailed coefficients differ depending on the moment the DC fault occurs. This is caused by the downsampling process involved at each decomposition level leading to loss of information present in the high frequency content. In particular, when analysing a fault signal with DWT up to level *j*, the number of different sets of coefficients that can be extracted is 2^j. To overcome this issue, DWT could be applied 2^j times while moving the data window by one sample. However, as the decomposition level increases, this solution necessitates extensive calculations.

Another potential solution to tackle this problem is to use stationary WT. SWT avoids the use of downsampling and provides the same number of coefficients as the analysed signal at each decomposition level. SWT is less efficient than DWT and requires additional time to extract the detailed coefficients. Nevertheless, when compared to the option of performing DWT 2^j times on the fault signal, the total execution time of SWT becomes equal or smaller, especially as *j* increases. Therefore, the SWT algorithm is considered in this paper.

III. Real-time SWT Implementation

A. SWT Algorithm

The SWT algorithm can be efficiently implemented with the use of discrete convolution based on Finite Impulse Response (FIR) filters. In particular, the approximation and detailed coefficients at each decomposition level *j* are calculated as the sum of the product of the *N* most recent input values with the *N* low-pass and high-pass filter coefficients respectively. At each level *j* the wavelet filter coefficients are upsampled and discrete convolution is re-excecuted. This process is illustrated graphically in Fig. 2.

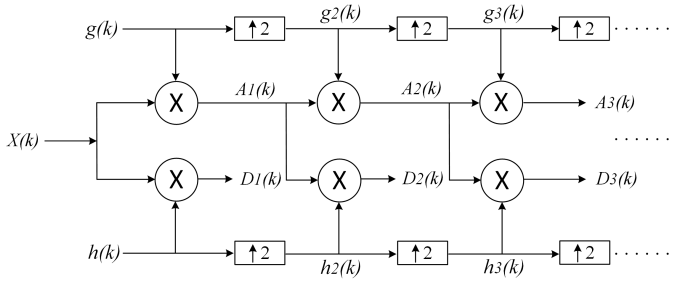

Fig. 2: SWT algorithm.

This implementation of SWT algorithm can be extended for an arbitrary number of levels. However, due to the intrinsic computational complexity of SWT, the maximum decomposition level should not be too high because the computational delay accumulates as the level increases. Nevertheless, this is not a limiting factor for HVDC grid protection purposes since the

most significant information of the transient phase of DC faults lies in the high frequency region (lower decomposition levels) of DC voltage. Hence, the first three levels are considered in this study. By setting a threshold on the magnitude of detailed coefficients (that contain the high frequency information), an SWT-based HVDC grid protection solution can be designed.

B. Hardware

For the hardware implementation of SWT, the Texas Instruments C2000 MCU F28379D Digital Signal Processor (DSP) has been used [10]. The device constitutes a low-cost solution for implementing efficiently, and with high accuracy, the SWT algorithm. The main features of the incorporated microcontroller are:

- 200 MHz dual C28xCPUs
- Dual 200 MHz Programmable Control Law Accelerators
- 1 MB Flash and 204KB RAM
- Four ADCs with selectable 16-bit/12-bit operation
- Three 12-bit DAC modules

The DSP was programmed in MATLAB-Simulink using an embedded coder support package available from TI. The first core of the hardware is assigned to calculate the SWT approximation and detailed coefficients for the first two levels, while the second core is responsible for the calculation of the third level coefficients. To realise this operation, the calculated approximation coefficients for level 2 are sent from one core of the DSP to the other using inter-processor communication blocks available through the simulink TI library. This configuration has proven to be effective for sampling frequencies up to 100 kHz and for wavelets with up to 20 filter coefficients.

C. Digital Real-Time Simulator

Digital Real-Time Simulator can perform electromagnetic power system simulation in real-time and it can interact with external hardware via analogue and digital signals through hardware-in-the-loop simulation [11]. Hence, it provides a realistic environment for the physical testing of the HVDC grid protection technique running on the DSP. The HVDC grid model used for the simulation studies is shown in Fig. 3 and it has been developed in RSCAD software and simulated using a digital real-time simulator from RTDS technologies.

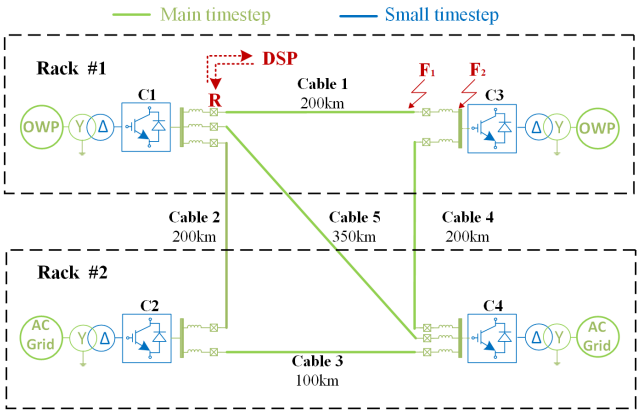

Fig. 3: HVDC grid modelled in RTDS.

The HVDC grid comprises of two offshore wind power plants (OWP) that feed two onshore terminals connected to the main AC grid. The network is operating at ±320kV DC in a symmetric monopolar configuration. All converters in the HVDC grid are Half-Bridge Modular Multilevel Converters (HB-MMCs) and are represented by their averaged models adapted from [12]. The AC networks and the OWPs have been modelled as 400 kV voltage sources behind an impedance. The cables are represented by frequency dependent (phase) models and the cable parameters are adapted from [13]. DC reactors in series with DC circuit breakers (DCCBs) are included at the end of each cable and the breaker opening time is set to 5ms. The system parameters are cited in Table I.

TABLE I: System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated AC voltage (line-to-line)	360 kV
Rated power (C1∼C4)	1000,900,1000,1200 MVA
Active power setpoint (C1∼C4)	700,-800,700,-600 MW
Reactive power setpoint (C1∼C4)	100,-100,100,-100 MVar
DC Inductors	50 mH
Arm inductance	42 mH
Arm Resistance	0.08 Ω
Arm capacitance	31.42 μF

The concept of multi-rate real-time simulation is employed to achieve greater accuracy and efficiency and consequently, two separate time steps are used. The large scale network simulations run on the main timestep of 50 μs. The AC networks and the DC cables along with the converter control systems operate at the main timestep. For greater accuracy, the MMCs are solved in a small timestep of 2500 ns. Each MMC is modelled inside a separate small timestep subnetwork and requires a single core of a processor card (GPC). The whole grid is split between two hardware racks that include two PB5 cards and five GPC cards. The PB5 cards are assigned for the total network solution and the control systems, while the AC and DC power system components are assigned to the GPC cards.

Special interfaces are used to migrate from the small timestep to the main timestep and vice versa. In particular, interfacing transformers are employed to interconnect the AC networks and the Offshore Wind Plants (OWP) to the main converters, while short travelling wave line models are used to interface the converters to the main DC network. To compensate for the presence of the travelling wave interface line models, the length of the DC cables is reduced accordingly. Finally, Cables 2, 4 and 5 interface the two subsystems that run on a separate rack (see Fig. 3).

D. Experimental Arrangement

The practical performance of the SWT hardware implementation is assessed in a controller hardware-in-the-loop configuration, in which the DSP that runs the protection algorithm emulates the operation of a protection relay by exchanging information with the HVDC grid model within the RTDS. The experimental arrangement is shown in Fig. 4.

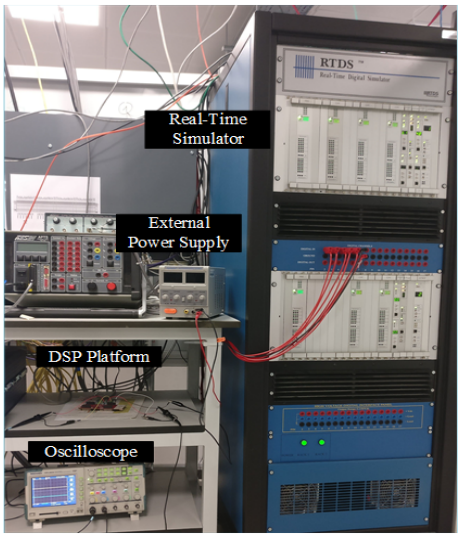

Fig. 4: Test system.

The DSP receives analog DC voltage measurements at the relay point (shown as R in Fig. 3) from an output channel provided by the analog output card of the DRTS. The single-ended input signals are scaled down to fit the DSP operating range (0-3.3 V) and are sampled by the ADC module with 12-bit resolution. When an internal DC fault is detected, a digital trip signal is generated from a DSP DAC module and is sent to a digital input port of the DRTS. The signal is used to trigger the operation of the HVDC breaker next to relay R. The minimum duration of the trip signal is set to four timestemps. The hardware module receives the measurements at 20 kHz (50 μs main step) and is powered by an external power supply (3.3 V). Moreover, the calculated SWT coefficients are sent to a analog output channel of the DSP to enable real-time monitoring of the protection scheme output.

IV. Simulation Results

A. Validation of SWT Implementation

In this study, an internal pole-to-pole (PTP) fault is applied at the end of the protection zone of relay R, i.e. location F1 in the HVDC grid of Fig. 3. The fault resistance R_f is equal to 30 Ω. Fig. 5 a) shows the voltage measurements (U_R) provided to the DSP during the early duration of the DC fault and Fig. 5b) and 5c) illustrate the detailed and approximation coefficients for all three decomposition levels, respectively. The results validate the proper operation of the DSP module. The wavelet coefficients were obtained using *sym4* as the mother wavelet.

Moreover, it is evident that all *D1*, *D2* and *D3* coefficients respond to the internal fault due to the high frequency components that are present in the transient fault voltage. This is the reason behind the use of the magnitude of detailed coefficients for detecting DC faults. Fig. 5 also highlights that as the level increases, the response of the algorithm becomes slower due to the greater length of the filters. Due to the critical requirement for high-speed operation of the HVDC grid protection systems, lower decomposition levels are preferred. On that basis, fault detection within a few ms (see Fig. 5) is possible.

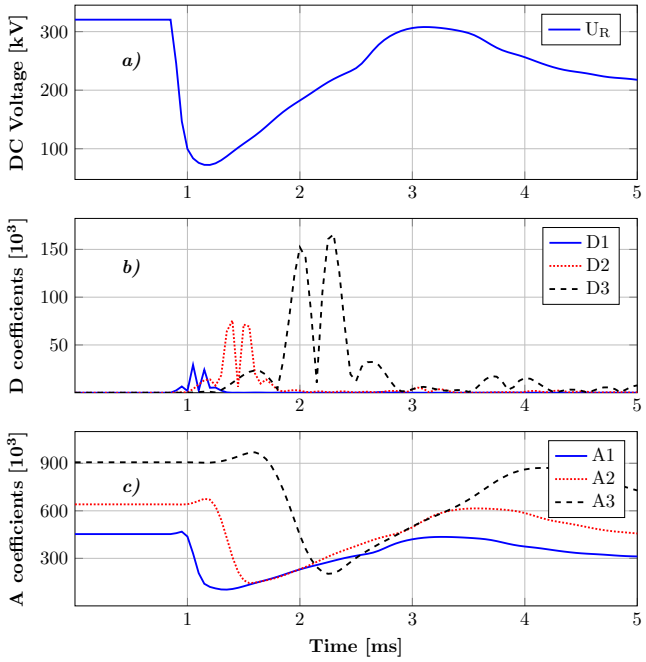

Fig. 5: Calculated detail and approximation coefficients for an internal fault at location F1 with R_f=30 Ω.

B. SWT-based HVDC Grid non-unit Protection

In this subsection, the performance of the real-time implementation of SWT in discriminating internal DC faults from external faults in HVDC grids is investigated. Towards this aim, a high resistive PTP internal fault (100 Ω) is applied at location F1 and a solid PTP external fault is applied at location F2 behind the DC reactor as shown in Fig. 3. The second decomposition level is selected as a compromise between computational delay and the impact of high-frequency noise. *Sym4* wavelet was again used in this scenario. Finally, a conservative threshold was selected based on off-line analysis of voltage waveforms using matlab. Fig. 6 illustrates the fault voltage profile, the *D2* detailed coefficients and the trip signal in each case, as captured by an oscilloscope in real-time.

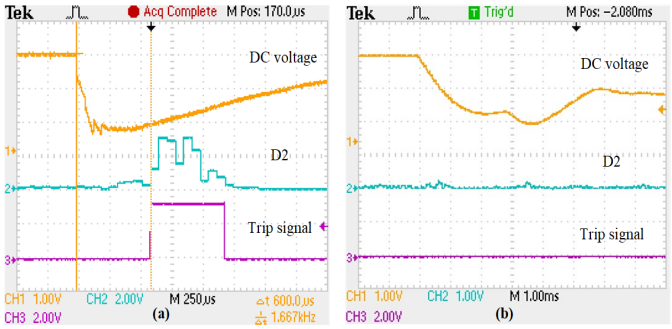

Fig. 6: Hardware module response to a) an internal fault at location F1 with R_f=100 Ω and b) a solid external fault at location F2.

For fault F1, *D2* coefficients rise significantly above the threshold and hence, a DC fault is successfully discriminated

and a trip signal is generated. It is evident that the method operates at very high speed, producing the trip signal 600 μs after the DC voltage is influenced by the fault. In the case of fault F2, the DC reactor damps the high frequency components of DC voltage. As a result, there is no significant rise in *D2* coefficients and the external fault is not detected. Consequently, the protection solution can successfully discriminate between high resistive internal and solid external faults.

C. Impact of Mother Wavelet and Decomposition Level

The selected wavelet decomposition level and mother wavelet have a significant impact on the real-time implementation of SWT both in terms of computational workload and DC fault detection speed. To investigate this impact and the capability of the hardware module to perform the SWT algorithm for longer wavelets, the internal fault study is applied repeatedly for different wavelets. Table II shows the DC fault detection time in terms of the required number of main timesteps (50 μs in this case) for different wavelets with filter length ranging from 6 to 18 coefficients. The fault detection time is expressed in timesteps, since this representation is valid for any sampling frequency and is defined as the number of timesteps it takes for the detailed coefficient to reach 30% of its maximum value.

TABLE II: Detection time for different mother wavelets.

Mother Wavelet	Filter Coefficients	Detection Time [Δt] Level 2	Level 3
db3	6	5	14
db5	10	11	29
db7	14	15	39
db9	18	19	50
sym3	6	5	14
sym5	10	14	31
sym7	14	17	41
sym9	18	24	52
coif2	12	14	35
coif3	18	23	55
bior2.2	6	7	15
bior2.4	10	13	29
bior2.6	14	19	43
bior2.8	18	25	67

The results demonstrate that the hardware module can successfully perform the calculations associated with SWT algorithm within a single timestep without loosing synchronisation even when longer high-pass and low-pass filters are used. Generally, as the filter length increases, the fault detection time rises. Nevertheless, this analysis does not consider practical aspects of WT, such as the capability of each mother wavelet in localising a disturbance in the frequency or time domain and therefore it serves only as an indication of the performance of each wavelet in detecting fault transients in DC voltage measurements. This complex task will be the focus of future research in SWT-based HVDC grid protection.

V. Conclusion

This paper presents a real-time implementation of an HVDC grid nonunit protection method based on stationary wavelet transform applied on transient voltage measurements for detecting DC faults. The SWT algorithm was implemented based on discrete convolution and the practical feasibility of the approach has been validated by using a DSP to execute the algorithm and emulate the operation of an HVDC protection relay. The hardware module provides a high level of confidence that the proposed method is practical and cost-effective, while considering data acquisition issues and the communication and computational aspects of the technique. Moreover, real-time simulations in a hardware-in-the-loop configuration using DRTS have demonstrated the reliable operation of the implementation for different mother wavelets and decomposition levels, and the suitability of SWT to rapidly detect DC faults in HVDC grids in a discriminative manner. The methods for determining the appropriate mother wavelet, decomposition level and protection threshold will be refined in the next stage of this work.

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