The Journal of Engineering

The 9th International Conference on Power Electronics, Machines and Drives (PEMD 2018)

eISSN 2051-3305
Received on 21st June 2018
Accepted on 27th July 2018
E-First on 16th April 2019
doi: 10.1049/joe.2018.8054
www.ietdl.org

High-voltage pulse generator using sequentially charged full-bridge modular multilevel converter Sub-modules, for water treatment applications

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Abstract: This paper proposes a new high-voltage pulse generator (PG) fed from a low-voltage DC supply V_s, which charges one arm of N series-connected full-bridge (FB) modular multilevel converter (MMC) sub-module (SM) capacitors sequentially, through a resistive-inductive branch. By utilising FB-SMs, the proposed PG is able to generate bipolar rectangular pulses of peak NV_s and unipolar rectangular pulses of either polarity, at high repetition rates. Asymmetrical pulses are also possible. The proposed topology is assessed via simulation and scaled-down experimentation, which establish the viability of the topology for water treatment applications.

1 Introduction

Applying lethal electroporation is required for the disinfection process in water treatment applications. Harmful microorganisms are subjected to an electric field E such that $E > E_{cr}$ where E_{cr} is the critical electric field beyond which the cell-membrane cannot reseal its pores [1]. The created pores lead to biological cell death, and disinfection results. In order to create such an electric field across the treatment chamber, a high-voltage (HV) for sufficient time should be applied. Recent research confirms the effectiveness of applying HV-pulses of a few kV with a duration of micro-seconds [2]. Hence, both energy efficiency and the lethal electroporation criteria are met. Thus, a low-power long duration input is used to provide high-power short-duration pulses for the electroporation as illustrated in Fig. 1 [3]. Thus, a controllable, high efficiency power electronics-based converter can be utilised.

Utilising modular multilevel converter (MMC) sub-modules (SMs) in the power conversion stage is viable. Both full-bridge (FB) and half-bridge (HB) SMs, illustrated in Fig. 2, can be employed in pulsed power applications [4–13].

Since SMs have capacitors, these can facilitate flexible pulse waveforms generation and flexible individual SM control [8, 9].

This paper exploits individual FB-SM control to charge capacitors sequentially as proposed in [13]. Efficient SM-capacitor charging is achieved through an rL branch, which allows fast individual SM-capacitor charging. The proposed topology utilised one arm of series-connected FB-SMs with the ability of generating bipolar and unipolar rectangular HV pulses. The generated pulses can be tailored to meet the application requirement by controlling the pulse polarity magnitude and/or the pulse duration.

This paper is structured as follows: next the proposed converter is introduced in Section 2, highlighting its operational principle. Simulation and experimental results are presented in Sections 3 and 4, respectively. Conclusions are drawn in Section 5.

2 Proposed pulse generator topology

The proposed PG topology is shown in Fig. 3. The PG is formed of N series-connected FB-MMC SMs, which are charged sequentially from a low-voltage DC (LVDC) supply V_s through an rL branch via the reverse blocking switch S. As illustrated in Fig. 2, the individual FB-SM is formed of four insulated gate bipolar transistors (IGBTs) connected with a capacitor. The FB-SM terminals, A and B, are short-circuited (bypassed $V_{AB} = 0$) in two

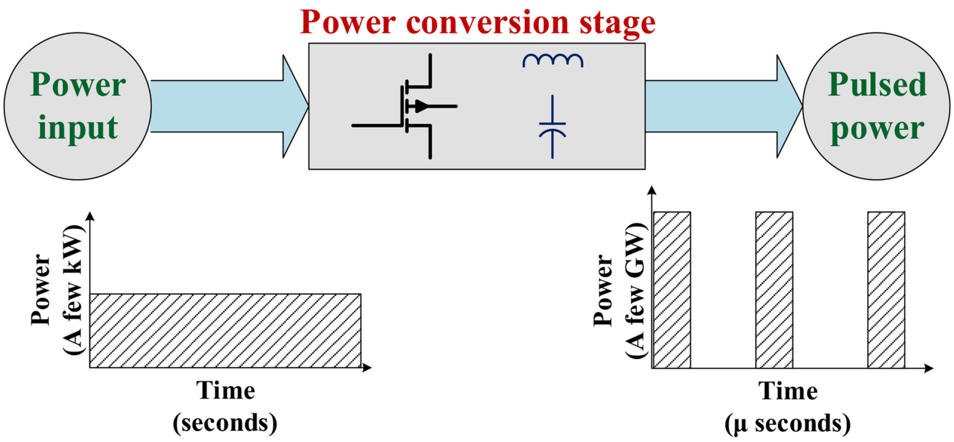
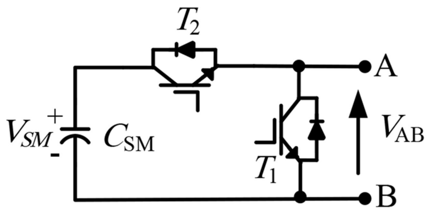
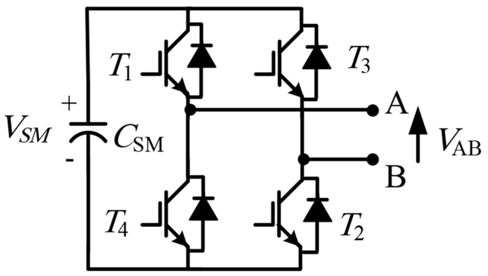


Fig. 1 *Pulsed power energy concept*



HB-SM Switching States

T_1	T_2	V_{AB}
ON	OFF	0
OFF	ON	$+V_{SM}$



FB-SM Switching States

T_1	T_2	T_3	T_4	V_{AB}
ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	0
ON	ON	OFF	OFF	$+V_{SM}$
OFF	OFF	ON	ON	$-V_{SM}$

Fig. 2 *Modular multilevel converter sub-modules*

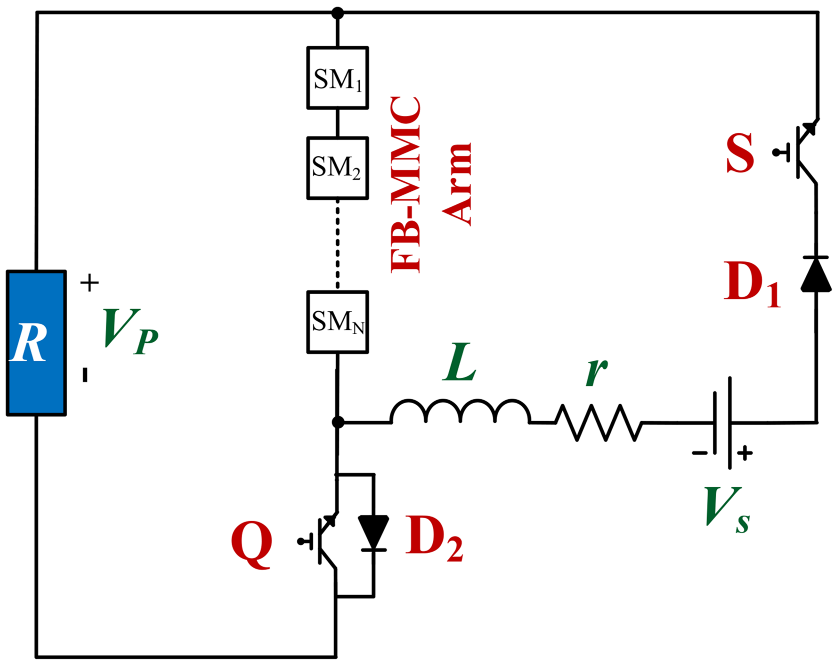


Fig. 3 *Proposed PG topology*

cases when (T_1 and T_3) or (T_2 and T_4) are switched ON with the other two switches OFF. A positive capacitor voltage is applied, $V_{AB} = +V_{SM}$, across terminals A and B when (T_1 and T_2) are ON and (T_3 and T_4) are OFF. When (T_1 and T_2) are OFF and (T_3 and T_4) are ON, a reverse polarity capacitor voltage appears across terminals A and B, $V_{AB} = -V_{SM}$. Thus, with appropriate control of individual SM zero voltage, positive and negative voltages can be applied across the load. The topology incorporates two additional switches, switch S and switch Q. Switch S provides a closed current path during sequential charging the SM capacitors, while switch Q provides a closed current path for SM capacitors to discharge across the load, R, and forming the required pulse waveform. When S is ON, Q is OFF and vice versa. The switch S must have a high reverse blocking capability, formed of series-connected IGBTs and diodes [14–19]. The IGBTs are rated at $(N+1)V_s$ and the diodes are rated at $(N-1)V_s$. This series connected S and D_1 only support a high voltage, and switch current at low-voltage V_s. Switch Q is rated at the LVDC supply $V_s$and is formed of an IGBT Q with anti-parallel diode D_2 to allow bidirectional current flow.

Fig. 4 shows a typical rectangular pulse waveform generated by the proposed PG. The circuit during each stage of generating bipolar rectangular pulses is illustrated in Fig. 5. Fig. 5*a* shows the circuit during positive pulse generation (stage 1 in Fig. 4) where individual SM capacitors are inserted in series (by turning ON T_1 and T_2 SM switches with T_3 and T_4 switches OFF) and switch Q ON with its antiparallel diode reverse biased. Fig. 5*b* shows the charging current path for individual SM-capacitors (stages 2 and 4 in Fig. 4). The load is isolated and has zero-voltage during the SM charging process. Finally, in stage 3, a negative voltage can be formed across the load, with SM switches T_1 and T_2 OFF and T_3 and T_4 switches ON. Switch Q is OFF and its antiparallel diode conducts, allowing a discharging current to flow.

A wide range of bipolar rectangular pulses can be generated by the proposed PG. Both symmetrical and asymmetrical pulses can be generated. The zero-time load voltage period can be combined by activating stages 1 and 3 successively and delaying the charging process. Bypassing the generation of a specific pulse polarity

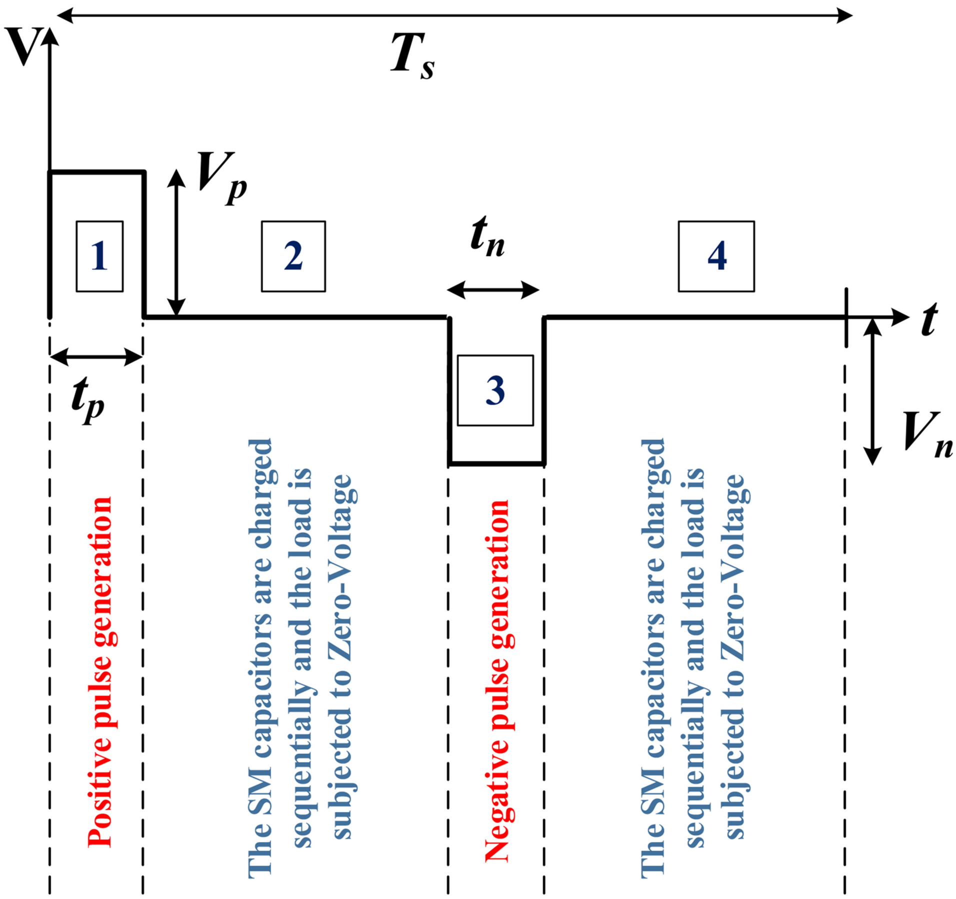


Fig. 4 *Stages for generating bipolar rectangular pulses*

(stage 1 for a positive pulse and stage 3 for a negative pulse) leads to unipolar pulse generation.

3 Simulation results

The proposed PG is simulated using Matlab/Simulink, with five FB-SMs and a 2 kV input supply voltage, the complete simulation specifications are given in Table 1. The selection of SM capacitance and the input charging *rL* branch is similar to that in [13].

With a 2 kV supply, all SM capacitors are charged to 2 kV sequentially. Then if all the SMs are inserted simultaneously, a peak voltage of 10 kV is generated across the load. Fig. 6*a* shows bipolar pulses of 10 kV peak voltage with $t_p = t_n = 10$ µs and a repetition time of $T_s = 120$ µs. The five SM capacitor voltages are shown in Fig. 6*b*, while the charging input current is in Fig. 6*c*.

Several bipolar pulse variations are simulated in Fig. 7. In Fig. 7*a*, symmetric bipolar pulses of 10 kV peak voltage with $t_p = t_n = 10$ µs and a repetition time of $T_s = 70$ µs, with combined zero load voltage durations, are presented. Asymmetric bipolar pulses are shown in Figs. 7*b* and *c*. In Fig. 7*b*, both pulse polarity voltages are 10 kV, while the pulse durations are $t_p = 10$ µs and $t_n = 20$ µs. Fig. 7*c* shows asymmetry voltage magnitudes, where the positive peak voltage is 6 kV and the negative voltage peak is 10 kV, with $t_p = t_n = 10$ µs.

Asymmetric bipolar pulses of 20 µs positive-pulse duration and 4 kV peak and 10 µs negative-pulse duration with 8 kV peak, are shown in Fig. 7*d*.

Finally, unipolar pulses of 10 µs pulse duration with 10 kV peak positive polarity, and 6 kV negative polarity are shown in Figs. 8*a* and *b*, respectively.

4 Experimental results

Scaled-down experimentation with three SMs is used to assess the proposed PG with the specifications in Table 1. Fig. 9*a* shows generated symmetrical bipolar pulses with a peak voltage of 300 V, pulse duration of 20, and 400 µs repetition time. Fig. 9*b* shows the three SM capacitor voltages, which fluctuate around 100 V, the input voltage. The input charging current is shown in Fig. 9*c*. Combined zero-load voltage duration pulses with asymmetric pulse voltage and pulse duration is shown in Fig. 10*a*, with a positive peak voltage of 100 V and duration of 20 µs, while the negative peak is 300 V with duration of 10 µs. Finally, unipolar pulses with a negative polarity of 300 V peak and 20 µs duration are shown in Fig. 10*b*.

5 Conclusion

This paper presented a new PG topology to generate HV pulses, hence, can be used in lethal electroporation applications such as water treatment. The PG is based on FB-MMC SMs, which provide modularity and scalability of the topology. Individual SM capacitors are charged sequentially through a reverse blocking semiconductor switch and an *rL* branch from an LVDC input supply. A bidirectional switch is required, such that both positive and negative pulse polarities can be generated across the load. The generated pulses are flexible, whereas appropriate insertion/bypass of the SM-capacitors allows symmetrical and asymmetrical bipolar pulse generation as well as unipolar pulse generation across the load. The proposed topology was assessed via simulation and scaled-down experimentation, which established the viability of the topology for lethal electroporation applications.

6 Acknowledgments

This work was supported by the Qatar National Research Fund (a member of the Qatar Foundation) under NPRP Grant (7-203-2-097). The statements made herein are solely the responsibility of the authors.

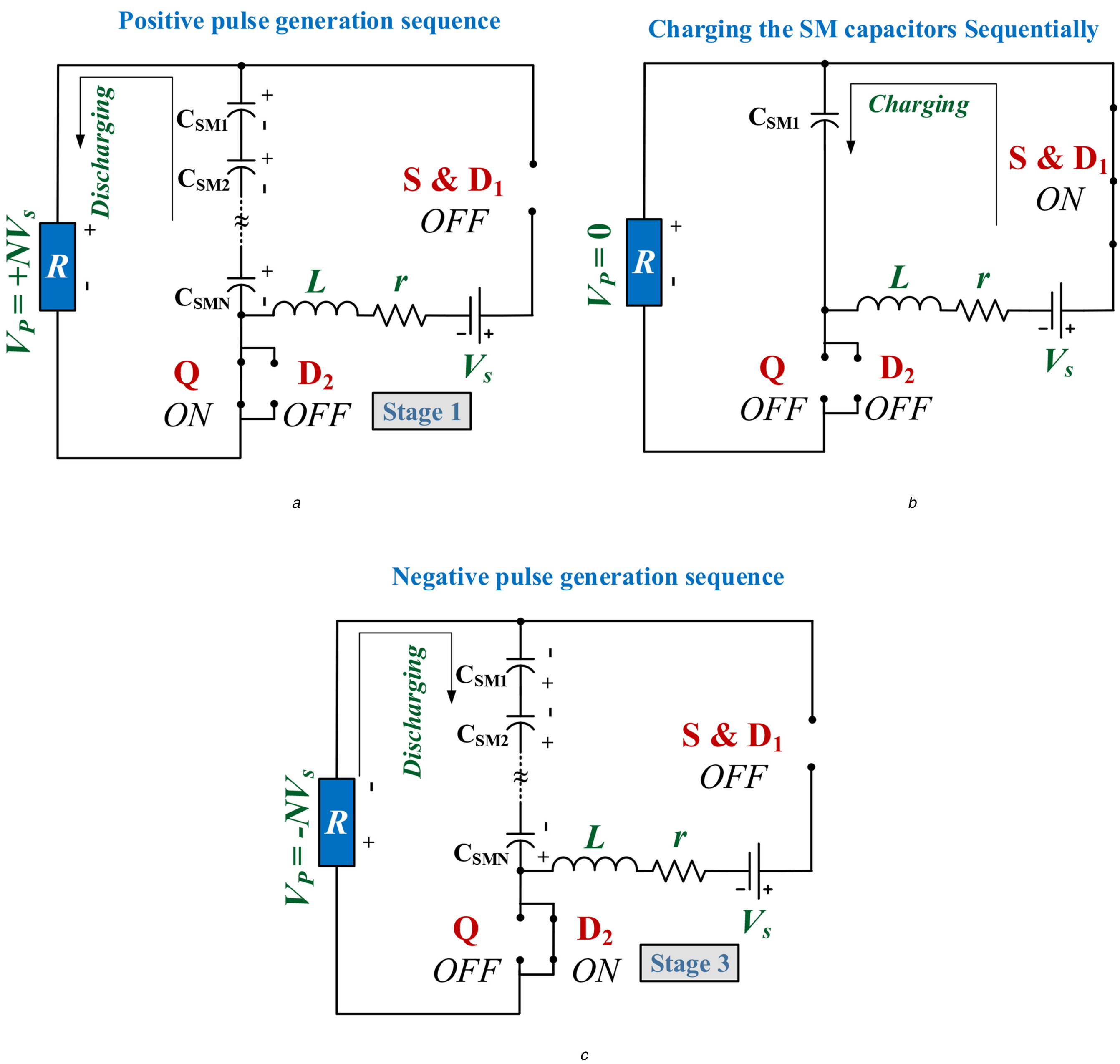


Fig. 5 *Circuit configuration during the generation of a bipolar pulse cycle*
(a) Stage 1, ***(b)*** Stages 2 and 4, ***(c)*** Stage 3

Table 1 Simulation and experimental specifications

Parameter		Simulation	Experimental
LVDC input voltage	V_s	2 kV	100 V
input inductance	r_L	0.1 Ω and 2 μH	0.5 Ω and 5 μH
number of SMs/arm	N	5	3
load resistance	R	1 kΩ	1 kΩ
SM capacitance	C_{SM}	5 μF	15 μF

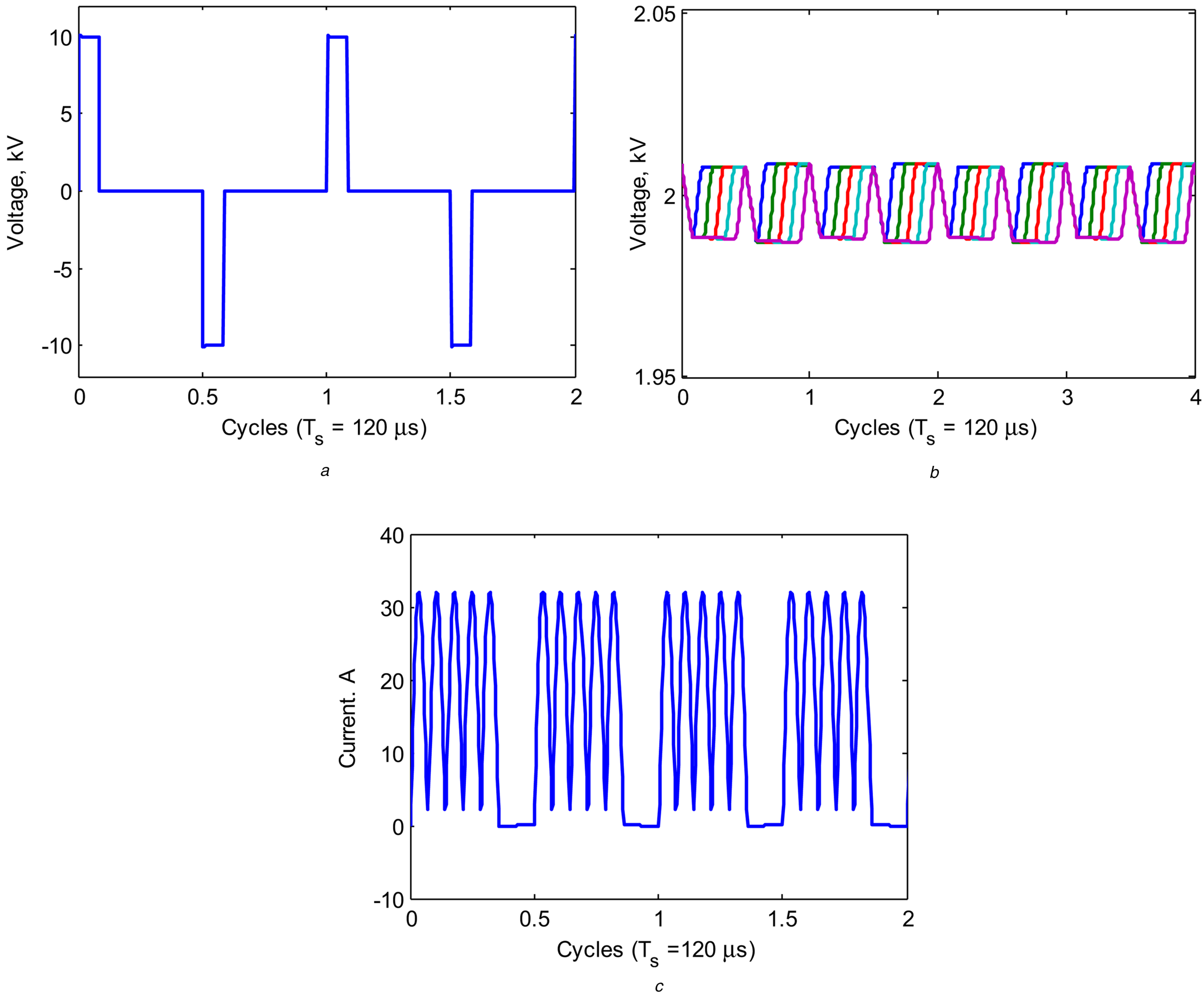


Fig. 6 *Generation of 10 kV symmetrical bipolar pulses*
(a) Voltage pulses across the load, ***(b)*** SM capacitor voltages, ***(c)*** Input charging current of SM capacitors

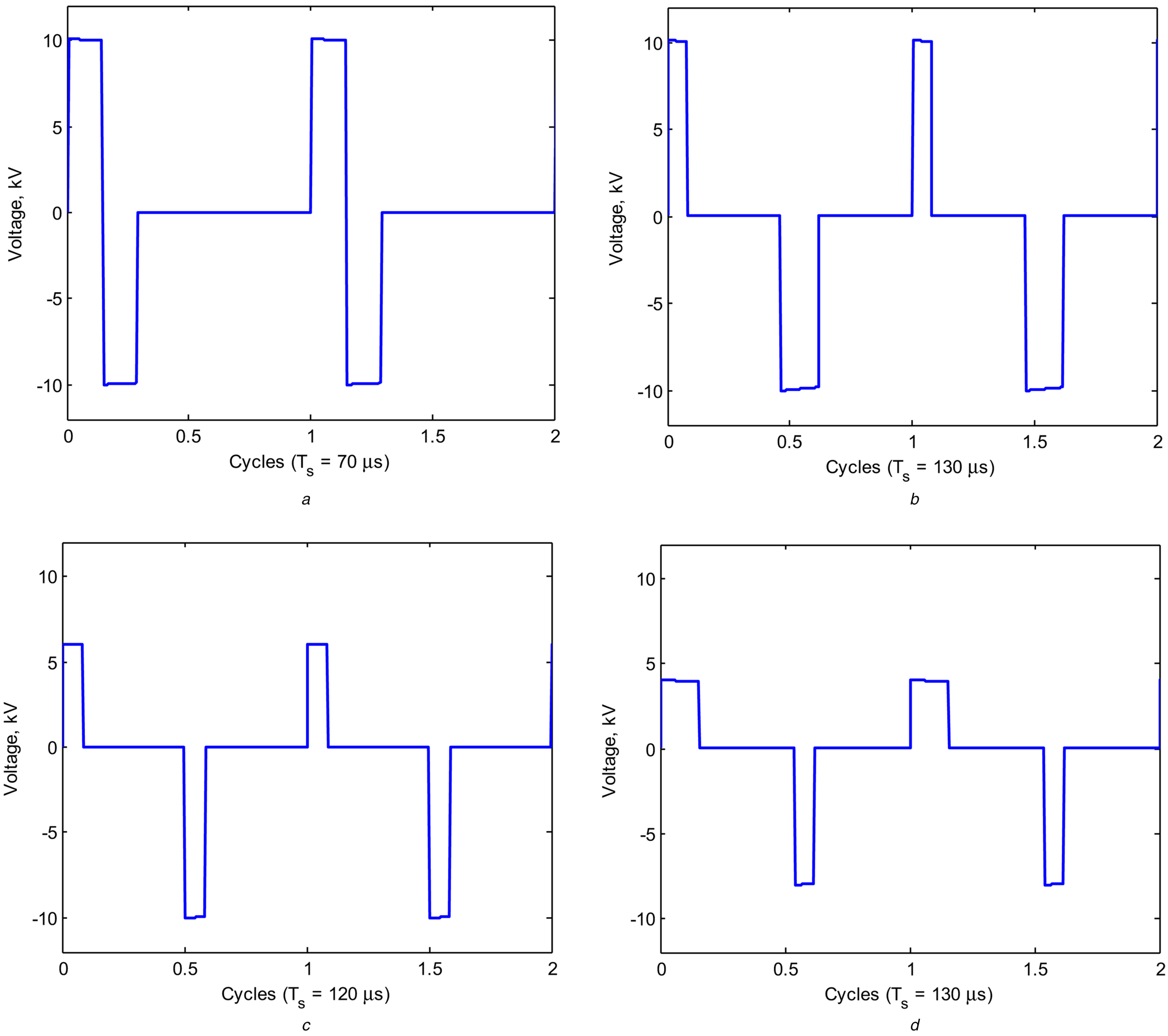


Fig. 7 *Bipolar HV pulses*
(a) Combined zero-load voltage duration, ***(b)*** Asymmetrical pulse durations, ***(c)*** Asymmetrical pulse magnitudes, ***(d)*** Asymmetrical pulse durations and magnitudes

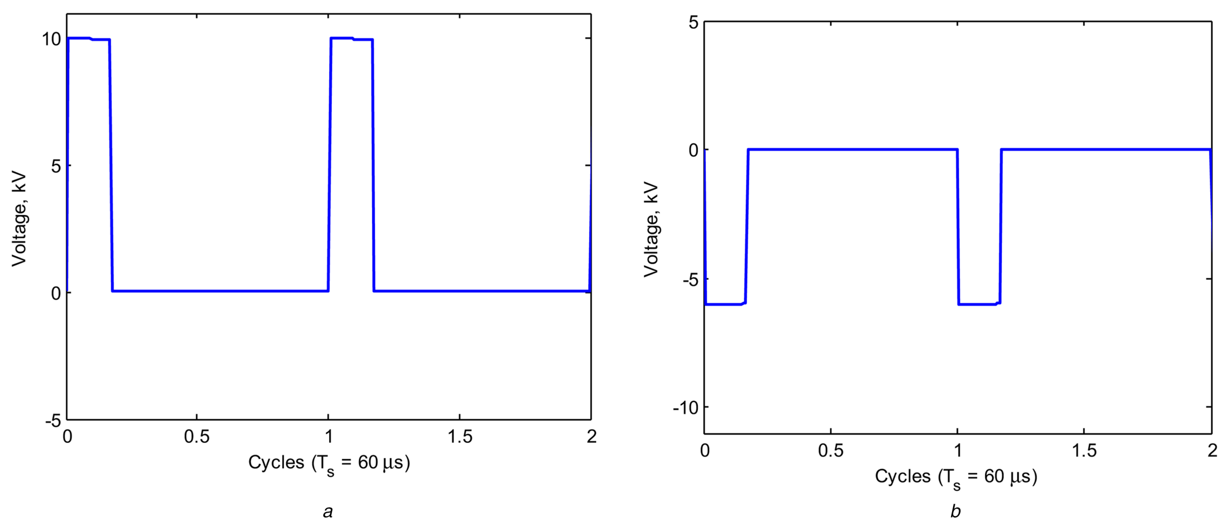


Fig. 8 *Unipolar HV pulses*
(a) Positive polarity, ***(b)*** Negative polarity

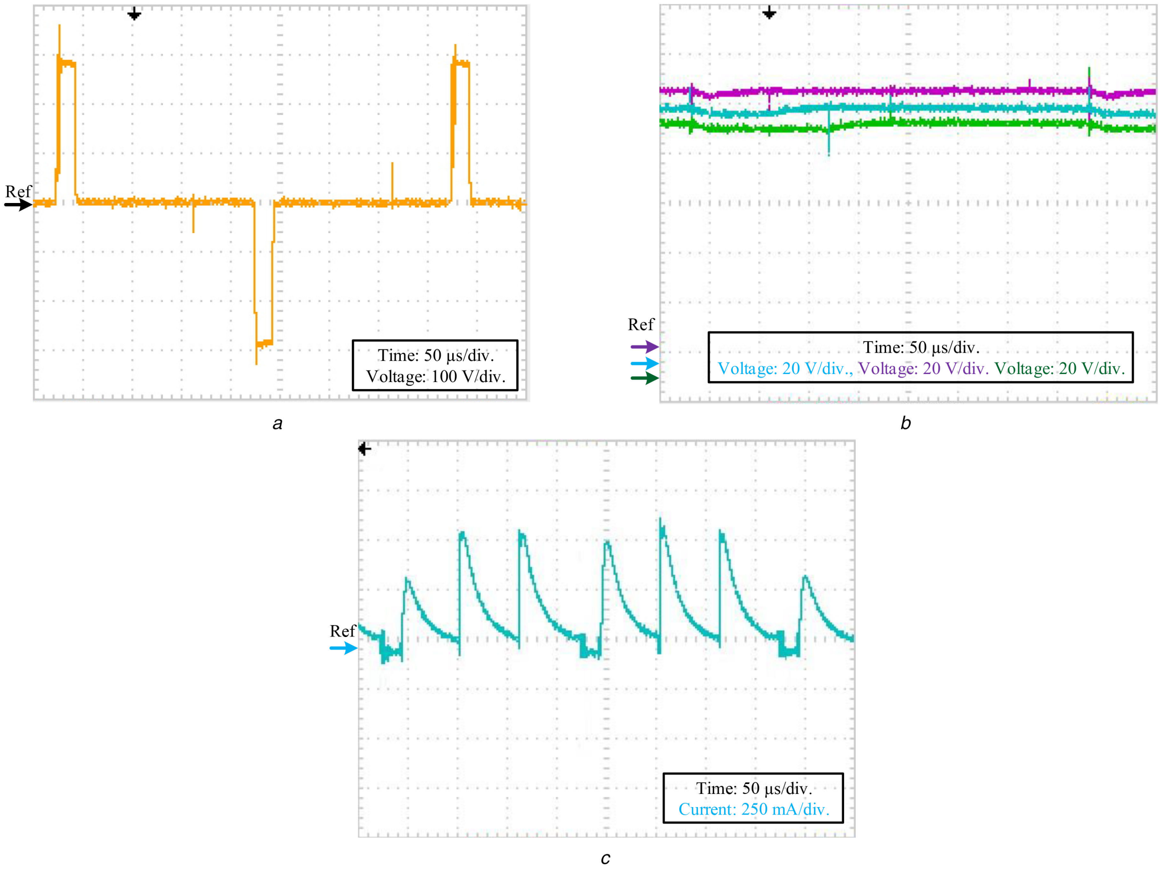


Fig. 9 *Scaled-down experimental results*
(a) Symmetrical bipolar pulses, ***(b)*** The three FB-SM capacitor voltages, ***(c)*** Input charging current

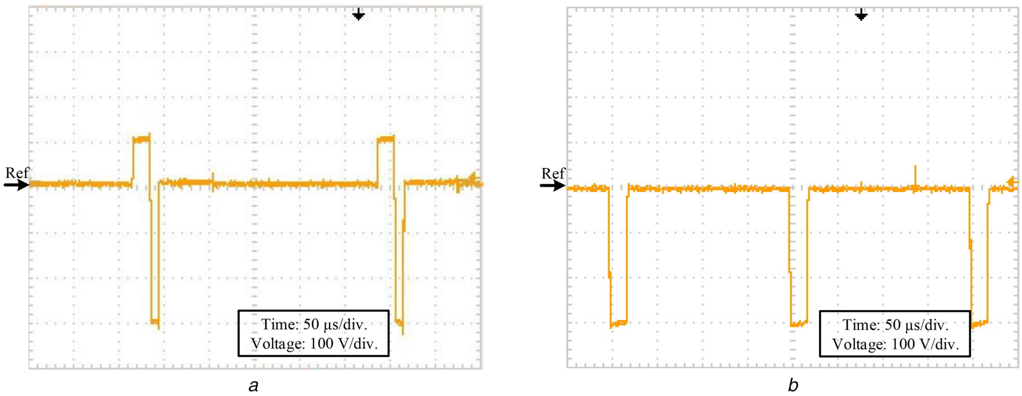


Fig. 10 *Scaled-down experimental results*
(a) Asymmetrical bipolar pulses with combined zero-load voltage durations, ***(b)*** Negative polarity unipolar pulses

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