Intelligent Fault Location in MTDC Networks by Recognising Patterns in Hybrid Circuit Breaker Currents During Fault Clearance Process

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***Abstract*—In this paper, a novel, learning-based method for accurate location of faults in MTDC networks is proposed. By assessing the DC circuit breaker currents during the fault clearance process, a pattern recognition approach is adopted from which the fault location is estimated. The implementation of the algorithm is allocated into three main stages, where similarity coefficients and weighted averaging functions (incorporating exponential kernels) are utilized. For the proposed algorithm, only a short-time window of data (equal to 6 ms) is required. The performance of the proposed method is assessed through detailed transient simulation using verified MATLAB/Simulink models. Training patterns have been retrieved by applying a series of different faults within an MTDC network. Simulation and experimental results revealed that the proposed scheme i) can reliably determine the type of fault ii) can accurately estimate the fault location (including the cases of highly resistive faults) and iii) is practically feasible.**

***Index Terms*—Fault Location, HVDC Transmission, DC Circuit Breakers, DC Faults, Pattern Recognition, Machine Learning.**

NOMENCLATURE

t_{LS}	*Time instant when load switch opens.*
t_{FMD}	*Time instant when fast mechanical disconnector opens.*
t_{rise}	*Time instant when fault current start rising.*
t_{LS}	*Time instant when load switch opens.*
I_{Lp}	*Current flowing at load path.*
I_{Cp}	*Current flowing at commutation path.*
I_{Ap}	*Current flowing at absorption path.*
A_{Lp}	*Integrated area of current flowing at load path.*
A_{Cp}	*Integrated area of current flowing at commutation path.*
A_{Ap}	*Integrated area of current flowing at absorption path.*
$\Psi(d)$	*Training data set with pre-simulated fault current cases (denoted by d).*
$\Lambda(d)$	*Sub-set of matching pre-simulated fault current cases (denoted by d).*
I_{CB+}	*Currents of positive pole.*
I_{CB-}	*Currents of negative pole.*
μ_d	*Mean of fault location case d.*
σ_d	*Standard deviation of fault location case d.*
μ_x	*Mean of fault location case x.*
σ_x	*Standard deviation of fault location case x.*
$\rho(d,x)$	*Pearson's correlation coefficient for fault location cases d and x.*
N	*Number of samples of fault current signal.*
S_{TH}	*Similarity threshold.*
$D_f(x)$	*Calculated distance to fault corresponding to case x.*
$D_f(d)$	*Known distance to fault of pre-simulated patterns d.*
D_f^*	*Known fault location.*
L_f	*Length of faulted line.*
x	*Fault case with unknown fault location.*
d	*Pre-simulated pattern with known-fault location.*
R_f	*Fault resistance.*
R_L, L_L	*Line resistance and inductance.*

I. INTRODUCTION

POWER transmission over long distances is expected to be based upon high voltage direct current (HVDC) grids, incorporating voltage-source converters (VSCs). VSC-based HVDC technology is promising due to their controllability, cost and operational losses, power quality support (e.g. reactive power, black start capability) [1], fault tolerance and ride though capabilities [2], [3] and interconnection of the existing AC networks. Apart from the existing point-to-point HVDC links, further economical and technical merits are expected to arise with the realization of multi terminal direct current systems (MTDC). Therefore, in order to enable widespread adoption of MTDC grids, there is a drive to analyze and mitigate any potential challenges related to their secure, reliable and efficient operation. After the occurrence of a permanent feeder fault on a transmission system, protection systems are expected to minimize its detrimental effects, by initiating clearing actions such as selective tripping of circuit breakers [4]. Following the successful fault clearance, the subsequent action is the accurate estimation of its location with regards to feeder's length. This will enable faster system restoration, diminish the power outage time, and therefore enhance the system overall reliability.

Fault location methods can be classified into three main categories such as travelling waves, reflectometry and learning-based. A thorough literature review of such categories, revealed that there are certain advantages and disadvantages, which are summarised in Table I. The literature review, revealed that most of the methods consider mainly point-to-point HVDC links in the study cases. As such, the captured voltages and currents have sufficient duration to allow accurate post-fault analysis (faults are usually interrupted on the AC side which can take several cycles). This raises a genuine question regarding their applicability in VSC-MTDC grids as dedicated DC circuit breakers are expected to clear the faulted line. The requirements of fast operation of HVDC protection (detection and interruption) could potentially make fault

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TABLE I
COMPARISON OF FAULT LOCATION SCHEMES AND CONTRIBUTIONS OF THE PROPOSED METHOD

Fault location category	Advantages	Disadvantages
Travelling waves [5]–[11]	-Very accurate -Suitable for hybrid feeders -Work well for different fault types -Immune to fault level and AC side parameters	-Difficulties in front wave detection -Sensitive to noise -Attenuation of waves for highly-resistive faults -High sampling frequency (range of MHz) -Requirement for time synchronization (for two-ended methods) -Computationally challenging -Detailed line parameters should be known
Reflectometry [12]–[14]	-Capability for repeated test-sets -Very accurate -Work well for different fault types -Immune to fault level and AC side parameters	-Additional equipment is required (i.e. pulse injectors) -Site visit and equipment assembly/disassembly are required -Feeders have to remain completely de-energized to allow testing -High sampling frequency (range of MHz)
Learning-based [15]–[19]	-Very accurate -Suitable for hybrid feeders -Ideal for multi-variable complex systems	-Training is required (this can be a storage/computational burden) -Large timeframes are required -Re-training is required for system changes -Moderate to high sampling frequencies (i.e. 100 kHz to 500 kHz) -Can be sensitive to noise
Contributions of the proposed scheme	-Re-training is not required for system changes -Immune to loading conditions -No need for synchronized measurements -Works efficiently for all fault types and highly-resistive faults -No need for additional equipment -Only fault current signatures during fault clearance are required (i.e. suitable for multi-terminal grids) -Compliant with IEC 61869-9 -Sampling frequency can be as low as 50 kHz -Robust to noise -Low storage requirements for the training database (range of 30 MB) -Experimentally validated	

localization more challenging as limited measurement data during the fault can be extracted. This fact has not been taken into account in the majority of the existing fault location studies.

To overcome this and other challenges summarised in Table I, this paper proposes a novel fault location method with many improvements over existing solutions. For example, compared to travelling waves, the proposed scheme requires very moderate sampling frequency, does not need time synchronization and is capable of dealing with highly-resistive faults. As opposed to methods based on reflectometry, there is no need for additional equipment and site visit for testing. The proposed scheme is based on the analysis of the DC circuit breaker (CB) internal currents during the DC-side fault clearance process, which makes it suitable for MTDC grids. Overall, the proposed method has been found to be immune to changes in loading conditions and AC parameters (e.g. fault level), robust to increased levels of noise. Additionally, compared to other learning-based methods, the proposed scheme does not require re-training for system changes and has a low requirement for data storage. Last but not least, the scheme has been experimentally validated, as opposed to other solutions which are mostly validated through simulations.

II. FAULT CURRENT INTERRUPTION IN MTDC GRIDS

A. HVDC Circuit Breaker Architectures

Following a successful and discriminative fault detection in MTDC grids, the CBs corresponding to the faulted line(s) attempt to break the current, and thus, clear the fault. DC CBs require a dedicated mechanism to drive the fault current to zero and dissipate the energy as there is an absence of natural zero crossing in the current.

Several DC circuit breaker concepts can be found in the literature such solid state, hybrid, super conducting, and resonant. Despite many design differences, all seem to have a common structure consisting of a commutation path, a switching component for voltage withstand, and an absorption path for dissipating energy [20]. Even though all the schemes have their own advantages and disadvantages, the hybrid circuit breaker (HbCB) has been found to possess the best overall performance including cost, losses and applicability [21]. For this reason the HbCB concept has been utilized in many power system studies for MTDC grids, including protection, fault analysis, DC switchgear and stability [22], [23].

B. The Hybrid Circuit Breaker

The circuit diagram of HbCB is presented schematically in Fig. 1, and the corresponding, typical fault current interruption process is shown in Fig. 2.

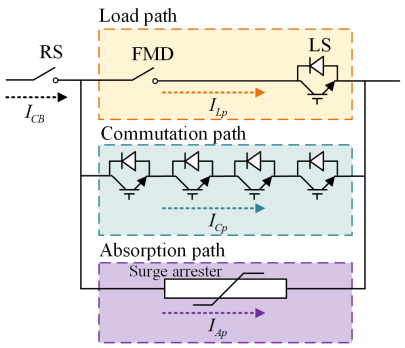

Fig. 1. Equivalent of hybrid circuit breaker.

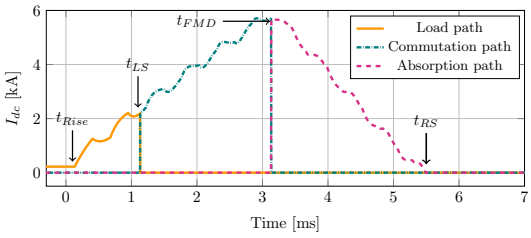

Fig. 2. Illustration of fault currents inside HbCB during interruption process.

During normal operation, the current (I_{Lp}) flows through the load path which includes the fast mechanical disconnector (FMD) and the load switch (LS). Following a fault occurrence the current in the load path starts rising at $t = t_{Rise}$. After a few milliseconds (fault detection delay) a tripping command is sent to the breaker, the LS opens at $t = t_{LS}$, forcing the current (I_{Cp}) to flow through

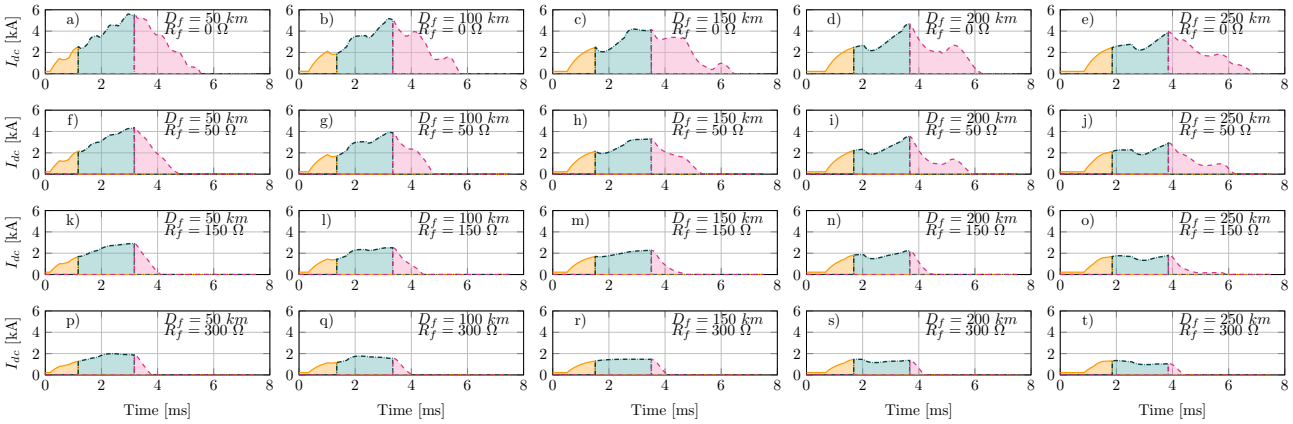

Fig. 3. Impact of fault distance and fault Resistance on fault current signatures of hybrid circuit breaker.

the commutation path. As no current flows through the FMD, it can now open at $t = t_{FMD}$. In the next stage, the power electronic valves in the commutation path turn off, which results in over-voltage. From this point, the surge arrester in the absorption path operates, and the current (I_{Ap}) gradually falls to zero while the energy is dissipated. When the current is in a near-zero region, the residual switch (RS) opens at $t = t_{RS}$ and the fault is finally cleared.

C. Fault Current Signatures

Prior to the presentation of the proposed fault location scheme, it is of utmost importance to demonstrate that the location of the fault and its resistance will create unique signatures in the HbCB currents. Assuming that a HbCB is connected in series with a transmission line, the transient periods can be analyzed in two distinctive periods, namely 'rising' and 'falling', as presented in equations (1) and (2) respectively.

$$I_{dc}(t) = \frac{V_{dc}}{R_f + R_L}\left(1 - e^{-\frac{R_f+R_L}{L_L}t}\right) + I_o e^{-\frac{R_f+R_L}{L_L}t} \quad (1)$$

$$I_{dc}(t) = \frac{V_{dc} - V_{arr}}{R_f + R_L}\left(1 - e^{-\frac{R_f+R_L}{L_L}t}\right) + I_p e^{-\frac{R_f+R_L}{L_L}t} \quad (2)$$

where R_L and L_L are the line resistance and inductance respectively, R_f is the fault resistance, I_o and I_p is the load current and the current determined in the previous interval respectively and V_{dc} and V_{arr} is the DC and arrested voltage respectively. Therefore, it is evident that different fault location and fault resistance values will create unique fault current signatures to the HbCB. It shall be highlighted that for transient-based analysis, transmission lines are represented by complex models (i.e. distributed parameter line), effectively, introducing high-order complicated equations which the system behaviour is based upon (i.e. non-homogeneous second-order differential equations and hyperbolic trigonometric functions [24]). The complexity of the system representation is significantly escalated when series-connected CB is highly non-linear as depicted in Fig. 4.

Consequently, the mathematical complexity of transmission lines and CB representations, in conjunction with the uncertainties of fault location and fault resistance, justify the need for utilizing a patter-recognition approach as proposed in this paper. It shall be also noted that the requirements for pattern recognition is

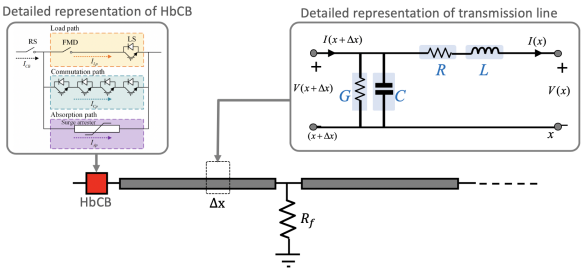

Fig. 4. Series-connected HbCB with faulted transmission line entailing detailed representation.

more pronounced when the non-linear characteristics of DC-side breakers are considered (historically DC-side faults on HVDC systems have been cleared by conventional AC-side breakers).

In order to assess the dependency of HbCB fault current signatures on distance to fault D_f, fault resistance R_f and fault type, a systematic study has been performed. The fault current signatures considering variations in fault distance D_f and fault resistance R_f are presented in Fig. 3. With increasing distance to fault D_f, the both resistance and inductance of the fault loop increase proportionally along the faulted line. The increasing inductance limits the rate of rise of current, and thus, increases the rise time, while the higher resistance reduces the current peak value. Fault distance has also a damping effect on the travelling wave-fronts in fault currents.

Fault resistance R_f also has a major influence on the fault current signatures. It is evident from Fig.3 that high value of fault resistance significantly reduces the fault current amplitude, which at the same time, weakens the impact of position D_f and makes it harder to determine where the fault occurred. Moreover, highly resistive faults severely attenuate the surges' wave-fronts. It is also interesting to point out that with increasing values of fault resistance, the fault clearing period is decreasing. This results directly from the fact that the lower values of fault current require less energy to be dissipated by the surge arrester, and therefore, the fault clearance time is reduced.

III. Proposed Fault Location Method

The proposed fault location technique utilizes the performance of the HbCB during the fault clearance, and takes into account that current measurements (individually for each conduction path of the HbCBs) can be assessed. This is due to the fact that current

measuring devices are installed inside the HbCB for self protection and control purposes [25]. Such measurements, together with a pattern recognition approach, are used for fault distance estimation. Specifically, by matching the HbCB currents (from a case with unknown fault location) individually for each conduction path, with existing patterns obtained by training data sets, the fault location is calculated. For the implementation of the algorithm, HbCB currents from one end of the line are utilized, both from the positive and negative poles. After careful analysis of the fault durations under all simulated conditions, the longest and the shortest fault clearance times were found to be 5.5 ms and 3.5 ms respectively. Accordingly, the proposed fault location scheme utilizes a short time window of 6 ms, which is sufficiently long to capture the entire DC fault clearance. As it will be explained in the following subsections, the fault location algorithm consists of three main stages which are illustrated in Fig. 5. For enhanced clarity of the algorithm description, a test case of a fault occurring at 100.5 km on a 300 km line is utilized. The sampling frequency for the proposed fault location algorithm is set to 96 kHz which is consistent with the industry standard IEC 61869-9 [26].

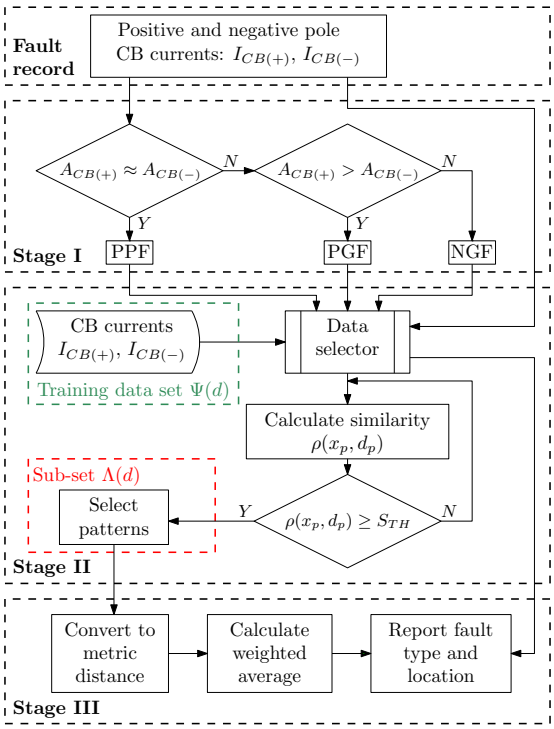

Fig. 5. Fault location algorithm flow chart.

A. Stage I: Fault Classification

In the first stage, the algorithm determines the type of fault, considering three possibilities: Pole-to-pole fault (PPF), positive pole-to-ground fault (PGF) and negative pole-to-ground fault (NGF). In Fig. 6 the currents of positive and negative pole HbCBs ($I_{CB(+)}$ & $I_{CB(-)}$ respectively) are illustrated for the three considered types of faults.

As demonstrated in Fig. 6 the characteristics of currents corresponding to those faults are very distinctive: in the case of PPF, both positive and negative pole currents are equal (or nearly equal), while for PGFs the faulted pole current is significantly higher than the healthy one. Therefore, a simple comparison of the two currents is generally sufficient to reliably determine the fault

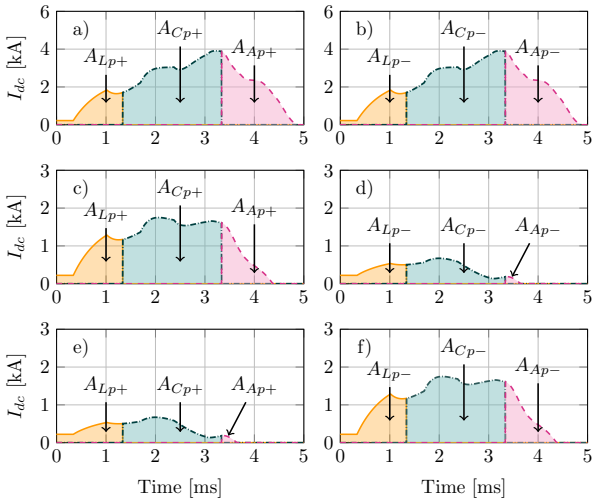

Fig. 6. Fault current signatures for different types of fault: a) PPF: positive pole HbCB, b) PPF: negative pole HbCB, c) PGF: positive pole HbCB, d) PGF: negative pole HbCB, e) NGF: positive pole HbCB, f) NGF: negative pole HbCB.

type. In order to obtain a single value which can be used in direct comparison between rapidly changing currents, the current time integral (i.e. area under the current waveform) is calculated over the whole duration of the fault. For positive and negative pole the current area is calculated using equations (3) and (4) respectively.

$$A_{I_{CB}(+)} = \underbrace{\int_{t_{Rise}}^{t_{LS}} I_{Lp(+)}dt}_{A_{Lp(+)}} + \underbrace{\int_{t_{LS}}^{t_{FMD}} I_{Cp(+)}dt}_{A_{Cp(+)}} + \underbrace{\int_{t_{FMD}}^{t_{RS}} I_{Ap(+)}dt}_{A_{Ap(+)}} \quad (3)$$

$$A_{I_{CB}(-)} = \underbrace{\int_{t_{Rise}}^{t_{LS}} I_{Lp(-)}dt}_{A_{Lp(-)}} + \underbrace{\int_{t_{LS}}^{t_{FMD}} I_{Cp(-)}dt}_{A_{Cp(-)}} + \underbrace{\int_{t_{FMD}}^{t_{RS}} I_{Ap(-)}dt}_{A_{Ap(-)}} \quad (4)$$

where I_{Lp}, I_{Cp}, I_{Ap} and A_{Lp}, A_{Cp}, A_{Ap} are the currents and their associated areas for load path, commutation path and absorption path respectively. Subscript signs $(+)$ and $(-)$ denote the positive and negative pole respectively.

Consequently, as illustrated on the algorithm flowchart in Fig. 5 (Stage I), a direct comparison of the current areas $A_{I_{CB}(+)}$ and $A_{I_{CB}(-)}$ is used to establish the fault type. If the two areas are almost equal (i.e within a margin of tolerance of $\pm$ 10% to account for measurement uncertainties, induced noise and other possible distortion factors) a decision is made that a PPF occurred. Otherwise, it is either PGF or NGF and the decision is made on the basis of the greater of the two current areas. This criterion can effectively classify faults with fault resistance of up to 1000 Ω. Other methods for fault classifiction could be also used like rate of change of current, over/under voltage or rate of change of voltage.

B. Stage II: Pattern Recognition

In this stage, a pattern recognition-based method is implemented which uses the fault classification output from Stage I and the training data set $\Psi(d)$ which contains pre-simulated fault current cases (denoted by d) on all MTDC lines and at various locations (the data set creation process is described in detail in section IV-B). Initially, the required data sub-set is selected corresponding to the known faulted line and the type of fault identified in Stage I. For

PPF and PGF, positive pole HbCB currents ($I_{CB(+)}$) are selected from the set, while for NGF negative pole HbCB currents ($I_{CB(-)}$) are used.

The pattern recognition mechanism is achieved by utilizing the Pearson's correlation coefficient $\rho(d, x)$ of the two variables d and x which is defined by generic equation (5):

$$\rho(d,x) = \frac{1}{N-1} \sum_{k=1}^{N} \left(\frac{d_{(k)} - \mu_d}{\sigma_d} \right) \left(\frac{x_{(k)} - \mu_x}{\sigma_x} \right) \qquad (5)$$

where d and x are the variables being compared using N scalar observations. The values μ_d, σ_d, μ_x and σ_x are the mean and standard deviation of d and x respectively. In this application, variable d corresponds to N samples of pre-simulated fault current (with known fault location), and x contains N samples of the observed fault current (with unknown fault location). The calculation of the correlation coefficient is performed separately for each of the three conduction paths, i.e. load, commutation and absorption.

The correlation coefficients $\rho(d_p, x_p)$ (with $p = 1, 2, 3$ representing the three conduction paths) are used as a measure of similarity and provide the ability to quantify the correlation of the observed behaviour x (with unknown fault location) with the individual training samples d (with $d \in \Psi(d)$). Correlation values approaching -1 and +1 imply high level of linear correlation (negative and positive respectively), while the values approaching zero indicate poor correlation. If two cases are similar, values of $\rho(d, x)$ close to 1 are expected. In this application a fixed similarity threshold S_{TH} has been introduced to select closely matching patterns. The patterns with a correlation coefficient of 0.985 and above are included in the sub-set $\Lambda(d)$ which is subsequently used in Stage III to calculate distance to fault according to formula (6).

It is also worth clarifying here that the similarity is calculated separately for each of the conduction paths, and if any of the three correlation coefficients $\rho(d_p, x_p)$ ($p = 1, 2, 3$) exceeds the threshold S_{TH}, the whole case is still selected and included in the matching sub-set $\Lambda(d)$. This essentially highlights that the extreme conditions for the pattern selection is determined by the level of similarity threshold S_{TH}.

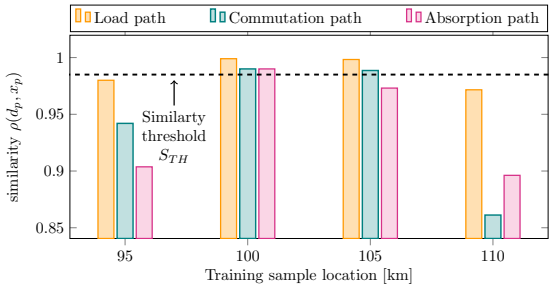

Fig. 7. Calculated similarity representation of a PPF (at 100.5 km on a 300 km line) and different training samples.

In Fig. 7 correlation coefficients of a PPF (located at 100.5 km on a 300 km long Line 1) calculated using four training cases at different fault locations are presented. In this small example, the pattern set $\Psi(d)$ contains four HbCB currents resulting from faults at 95, 100, 105 and 110 km from terminal T_3 (refer to Fig. 8). The similarity is calculated between these four samples (patterns) and the HbCB currents of the fault occurring at 100.5 km. As can be seen from Fig. 7, only two cases (i.e. 100 km and 105 km) exceed the similarity threshold S_{TH}. These two samples form the sub-set $\Lambda(d)$ which is used in the fault location calculation. Even though the similarity of the pattern at 105 km does not exceed the threshold S_{TH} for all the three paths (correlation coefficient for the absorption path is below S_{TH}), the whole case is still selected. Practically this indicates the two extreme conditions considering a fixed threshold S_{th} two are the cases corresponding to faults at 100 km and 105 km.

C. Stage III: Fault Location Calculation

This is the final stage of the algorithm where the fault type (as identified in Stage I) and its location are reported. After the sub-set of closely matching samples $\Lambda(d)$ have been identified in Stage II, the fault location is calculated using formula (6). The calculation utilizes a kernel-based weighted averaging principle [27]. For this application, exponential kernels have been put forward. In equation (6), the resulting value $D_f(x)$ is the calculated distance to fault corresponding to fault case x, $\Lambda(d)$ is a sub-set of $\Psi(d)$ with selected test patterns similar to case x, $D_f(d)$ is the known fault location of pre-simulated patterns d, and $\rho(d_p, x_p)$ ($p = 1, 2, 3$) is the Pearson correlation coefficient of the case x and pre-simulated patterns d (calculated separately for each conduction path). The purpose of the weighted function in (6) is to give more 'weight' (and thus have more influence on the result) to most closely matching patterns in the sub-set $\Lambda(d)$. For this reason the correlation coefficients $\rho(d_p, x_p)$ are converted to form a positive measure of distance between the ideal match (i.e. 1) and the value of $\rho(d_p, x_p)$. This can be seen in the exponent of e in (6), i.e. $(1 - \rho(d_p, x_p))^2$. Maximum values in the weighted function are achieved by the elements with the highest values of $\rho(d_p, x_p)$ (i.e. zero distance between actual and test case fault position), and the function should decay exponentially as the distance increases (according to the selected kernel).

IV. Simulation Studies

A. MTDC Study Grid

A five-terminal MTDC grid, developed in Matlab/Simulink®, has been utilized in all case studies as illustrated in Fig. 8. The network topology has been adopted from the Twenties Project test-bed, designed for studying feasibility and control of DC grids, with large penetration of wind and other renewable energy sources. In such network architecture, there are five MMCs operating at $\pm$400 kV (symmetric monopole), together with HbCBs, current limiting inductors and protection systems at each transmission line end [28]. Overhead lines have been included in the network adopting a distributed parameter modelling approach. The AC and DC network component parameters are provided in Table II.

B. Training Data

The training patterns (data set $\Psi(d)$) have been generated by simulating PPFs, PGFs and NGFs on all lines at varying distances and fault resistance values. The fault positions have been applied in 5 km increments, and fault resistances covered the range between 0 Ω to 500 Ω (in steps of 50 Ω). The size of the generated database has reached 29 MB, which enables its practical application as the need for extreme storage requirements is eliminated.

It should be highlighted that if the operating conditions would change in the system (e.g. load variations, voltage set-points, etc.), the training data bases would not have to be altered. Any change to the operating conditions would affect the steady state current flowing into the line and the circuit breaker. Practically, this

$$D_f(x) = \frac{\overbrace{\sum_{d\in\Lambda(d)} D_f(d)\ e^{-(1-\rho(d_1,x_1))^2}}^{Load\ path} + \overbrace{\sum_{d\in\Lambda(d)} D_f(d)\ e^{-(1-\rho(d_2,x_2))^2}}^{Commutation\ path} + \overbrace{\sum_{d\in\Lambda(d)} D_f(d)\ e^{-(1-\rho(d_3,x_3))^2}}^{Absorption\ path}}{\underbrace{\sum_{d\in\Lambda(d)} e^{-(1-\rho(d_1,x_1))^2}}_{Load\ path} + \underbrace{\sum_{d\in\Lambda(d)} e^{-(1-\rho(d_2,x_2))^2}}_{Commutation\ path} + \underbrace{\sum_{d\in\Lambda(d)} e^{-(1-\rho(d_3,x_3))^2}}_{Absorption\ path}} \tag{6}$$

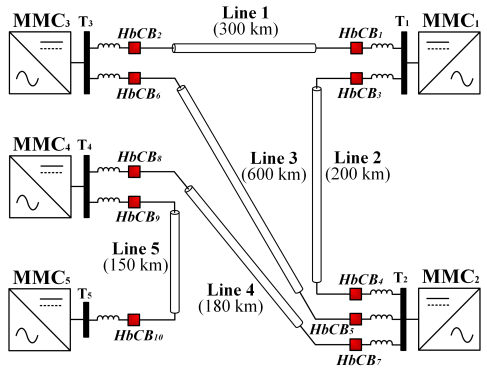

Fig. 8. Case study five terminal DC grid.

TABLE II
DC AND AC NETWORK PARAMETERS

Parameter	Value
AC voltage $[V_{AC,L-L}]$	400 kV
AC short-circuit level $[S_{s.c}]$	40 GVA
AC frequency $[f_n]$	50 Hz
DC voltage $[V_{DC}]$	$\pm$400 kV
DC line external inductance $[L_{DC}]$	150 mH
MMC number of sub-modules per arm	400
MMC arm inductance $[L_{DC}]$	0.1 p.u.

would introduce an additional offset (negative or positive) to the currents to be processed. These conditions will have no impact on the pattern-matching, as the deployed Pearson correlation of coefficients is naturally and mathematically immune to offsets and gains [29].

C. Fault Detection & Protection of Feeders

When it comes to post-fault analysis, it is a common practice for fault recorders to be triggered by protection operation as depicted in Fig. 9.

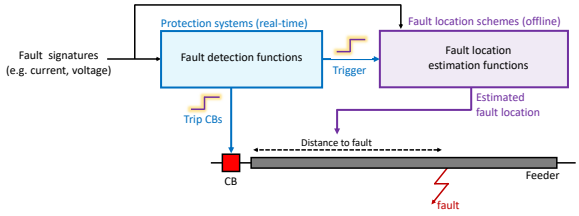

Fig. 9. Relationship between fault detection and fault location schemes.

After protection has operated, the fault signatures (i.e. current and/or voltage), which capture the whole duration of the incident, are available to other systems such as a fault location scheme. All fault locators which use the fault signatures measured during the fault, depend on the successful fault detection and clearance. In post-fault analysis, it makes no difference how the fault has been detected so long as it has been detected and cleared. Essentially, the tripping time of the protection systems shall not play a significant role to the effectiveness of the proposed algorithm. Even though the fault detection and protection strategies are out of scope of this paper, for each simulated case the HbCB sets on the faulted line have been tripped with the typical time associated with DC protection operation [28], [30], ensuring the MTDC grid is protected against all types of faults including pole-to-pole faults, positive pole-to-ground faults and negative pole-to-ground faults. Consequently, in all fault location studies reported in this paper, protection system has selectively disconnected the faulted line, taking also into account that the HbCB current never exceeds 9 kA (maximum breaking capacity).

D. Simulation Results

To achieve systematic accuracy assessment of the proposed scheme, DC faults have been simulated along all transmission lines within the MTDC grid, considering a wide range of fault positions, resistances and including all three types of faults. Specifically, for lines one to five, 290, 190, 590, 170 and 140 cases (for each type of fault) have been considered, representing different fault distances. It should be clarified that the faults have not been distributed equally along the lines. For each case, HbCB currents from the faulted line have been fed into the fault location algorithm. In order to better examine the robustness of the proposed fault location algorithm, artificial white noise has been added to the HbCB currents. In total the proposed scheme has been tested against 55,200 different cases. For every case, the fault location is estimated and the reported errors have been calculated according to (7).

$$error\ \% = \frac{D_f - D_f^*}{L_f}\ 100\% \tag{7}$$

where D_f is the calculated distance to fault, D_f^* is the actual distance to fault and L_f is the length of the faulted line.

The fault location results are presented graphically in Fig. 10. The statistical report of the fault location results are presented in Table III. The table considers PPFs, PGFs and NGFs with fault resistance of 1 Ω and includes maximum (Max.), and average (Avg.) error values evaluated for all considered fault positions.

As can be seen from Table III, the overall accuracy of the proposed fault location method is very high for a wide range of fault distances and for all the lines. In particular, the maximum estimation error considering all 4140 fault positions is 0.99998 %. Considering average values of errors for each line, the minimum value has been found to be 0.0676 % (PPF on Line 3), and maximum value was 0.1824 % (PGF on Line 4). It should be noted that the fault type (PPF, PGF or NGF) has been identified correctly in all cases by Stage I of the method.

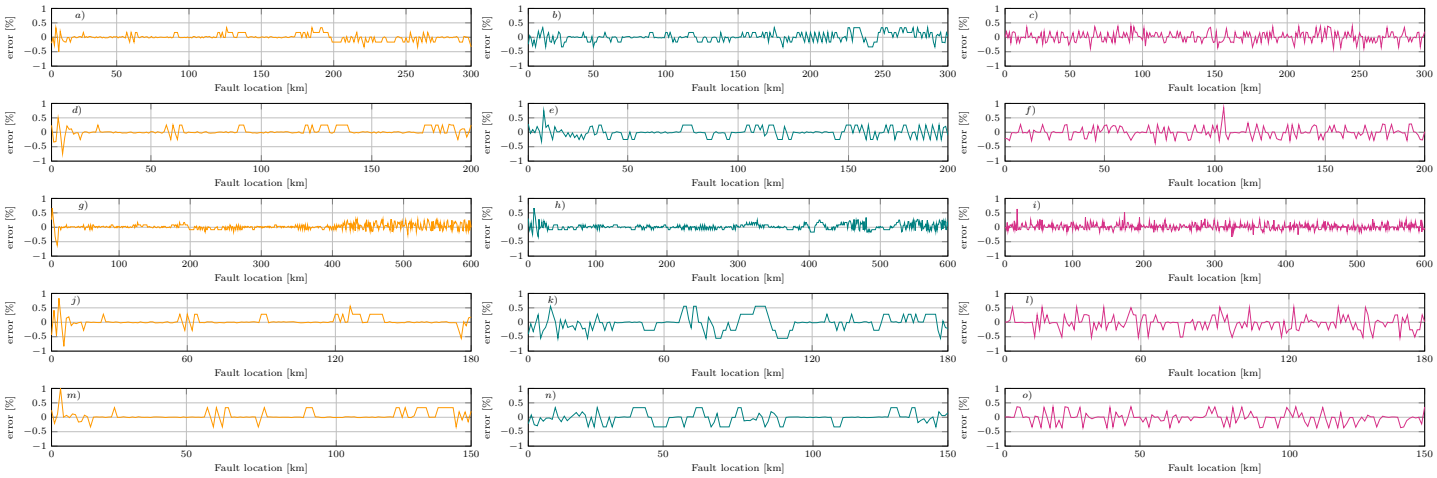

Fig. 10. Distribution of errors for different lines and fault types: a) PPF - Line 1, b) PGF - Line 1, c) NGF - Line 1, d) PPF - Line 2, e) PGF - Line 2, f) NGF - Line 2, g) PPF - Line 3, h) PGF - Line 3, i) NGF - Line 3, j) PPF - Line 4, k) PGF - Line 4, l) NGF - Line 4, m) PPF - Line 5, n) PGF - Line 5, o) NGF - Line 5.

TABLE III
FAULT LOCATION RESULTS FOR DIFFERENT LINES AND FAULT TYPES

Line	Fault type	Error [%] Max.	Error [%] Avg.
1	PPF	0.50000	0.07249
	PGF	0.33334	0.11303
	NGF	0.39190	0.11830
2	PPF	0.75000	0.07580
	PGF	0.74998	0.11640
	NGF	0.85160	0.11870
3	PPF	0.66566	0.06762
	PGF	0.66665	0.07340
	NGF	0.63520	0.07344
4	PPF	0.83334	0.07864
	PGF	0.55557	0.18235
	NGF	0.52750	0.16890
5	PPF	0.99998	0.09100
	PGF	0.33333	0.12979
	NGF	0.36670	0.13680

E. Performance with Highly Resistive Faults

The fault location algorithm has been additionally tested under the occurrence of highly resistive faults. The fault distance scenarios presented in Section IV-D have been repeated for a wide range of fault resistance values, including 50, 75, 100, 150, 200, 300, 400 and 500 Ω. The resulting average errors are presented in Fig. 11, Fig. 12 and Fig. 13, for PPFs, PGFs and NGFs respectively.

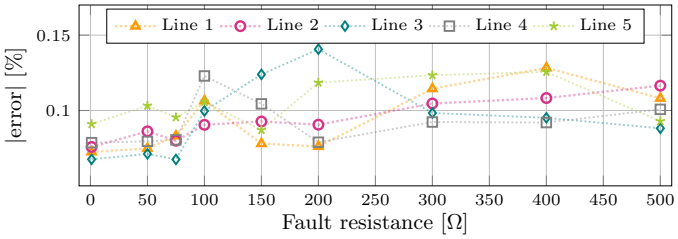

Fig. 11. Average error values for PPFs under different fault resistance values.

By observing Fig. 11, Fig. 12 and Fig. 13 the minimum and maximum averaged errors for PPFs are 0.06754 % and 0.14068 % respectively. For PGFs those errors correspond to 0.07340 % and 0.31836 %, and for NGF to 0.07258 % and 0.27524 %. It can be concluded that the proposed algorithm can maintain low estimation error even with highly resistive faults up to 500 Ω and the accuracy is not compromised.

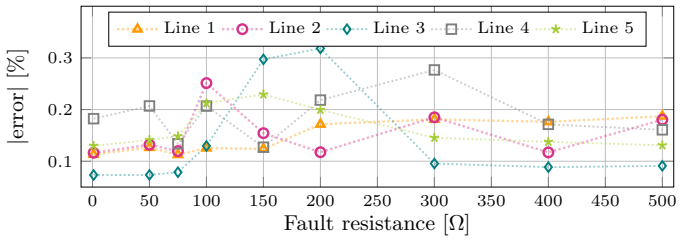

Fig. 12. Average error values for PGFs under different fault resistance values.

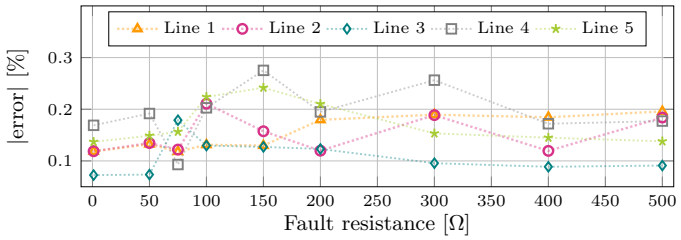

Fig. 13. Average error values for NGFs under different fault resistance values.

F. Impact of Sampling Frequency & Noise

In the interest of investigating the impact of sampling frequency on the proposed fault location technique, studies of PPFs have been repeated at different sampling frequencies. The resulting average errors are presented in Table IV and depicted graphically for convenience in Fig. 14.

TABLE IV
AVERAGE ERROR (%) VALUES FOR PPFS FOR DIFFERENT SAMPLING FREQUENCIES

f_s [kHz]	Line 1	Line 2	Line 3	Line 4	Line 5
5	0.7669	0.7351	0.6188	0.6912	0.9901
10	0.5042	0.4773	0.4686	0.4884	0.8891
20	0.3085	0.4008	0.4233	0.3688	0.5069
30	0.1678	0.2085	0.2488	0.2619	0.3141
40	0.1316	0.1479	0.1704	0.2304	0.2595
50	0.0953	0.0918	0.0784	0.1030	0.1131
96	0.0725	0.0758	0.0676	0.0786	0.0910
100	0.0724	0.0758	0.0676	0.0786	0.0909
200	0.0723	0.0756	0.0675	0.0785	0.0908
500	0.0708	0.0756	0.0654	0.0768	0.0888

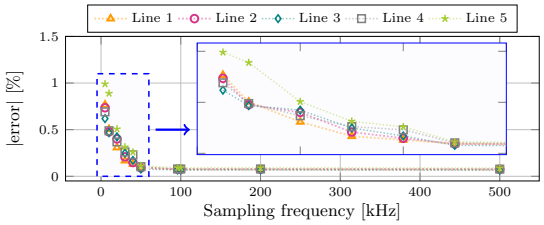

Fig. 14. Fault location estimation error with respect to sampling frequency

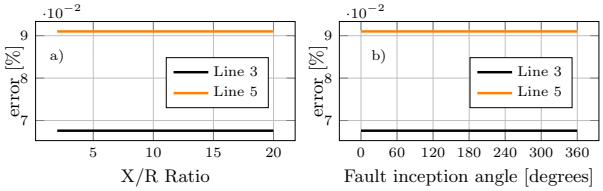

Fig. 15. Impact of AC parameters on the fault location accuracy: a) X/R ratio, b) fault inception angle.

By observing Table IV and Fig. 14, it can bee seen that the dependency of the accuracy on the sampling frequency is considerable for frequencies below 30 kHz. This is due to the fact that the entire current interruption process lasts about 6 ms and therefore with low sampling frequency only a few points can be extracted. Results indicate that in practical applications, the sampling frequency could be as low as 50 kHz without the accuracy being significantly compromised (practically this denoted the limitation and requirements of the method with respect to sampling frequency). Additionally, it is evident that exceeding sampling rate above 96 kHz results only in minor improvement in fault location accuracy.

In order to assess and further scrutinize the performance of the proposed fault location scheme, studies of PPFs have been repeated considering noisy inputs. In particular, the current measurements have been subjected to artificial noise with increasing amplitude up to 30 dB Signal to Noise Ratio (SNR). Increased level of noise can occur from transducers, modulators or power quality issues. The resulting values of fault location estimation are presented in Table V.

TABLE V
AVERAGE ERROR (%) VALUES FOR PPFS CONSIDERING NOISY INPUTS

SNR [dB]	Line				
	1	2	3	4	5
∞	0.0725	0.0758	0.0676	0.0786	0.0910
100	0.0768	0.0761	0.0666	0.0780	0.0933
80	0.0799	0.0820	0.0714	0.0786	0.0972
60	0.0804	0.0845	0.0877	0.0805	0.0910
30	0.0823	0.0967	0.0888	0.0833	0.1005

Compared to the noise-less signal (infinite SNR), the increase in noise level (lower dB values correspond to higher levels of noise) has a very small degrading effect on the fault location accuracy. It can be concluded that the proposed fault location scheme is robust to the additive noise. In terms of average error it has been found that the error rises by 0.0212 % (worst-case) for the SNR dropping to 30 dB.

G. Impact of AC side

In order to the investigate the impact of AC-side parameters, to the performance of the proposed fault location scheme, faults have been applied to the test network considering a wide range of values for fault inception angle and X/R ratio. Results are presented in Fig. 15 below, for PPFs occurring on Line 3 and Line 5 which are the longest and shortest line respectively.

The resulting values of estimation error, indicate that there is no correlation between the AC side parameters (i.e. fault inception angle and X/R ratio) and the performance of the proposed fault location scheme. This emanates from the fact that the first ms of the fault in VSC-HVDC based systems, are dictated by the discharge of DC capacitances in the system. Essentially these are transient periods where the AC-side variations (e.g. as inception angle, pre-fault load current, short circuit level etc) have no impact to the performance of the proposed fault location scheme.

V. EXPERIMENTAL STUDIES

A. Testing Methodology and Experimental Setup

In order to examine the practical feasibility of the proposed fault location scheme, a Hardware In the Loop (HIL) prototype has been developed using Real Time Digital Simulator (RTDS) and Opal-RT real-time simulation platforms.

A schematic of the experimental arrangement is depicted in Fig.16 while a photograph illustrating various elements of the experimental setup is shown in Fig. 17.

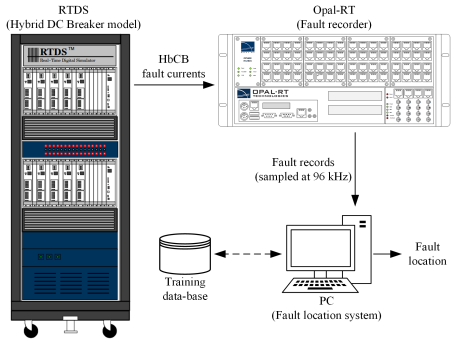

Fig. 16. Schematic of experimental arrangement.

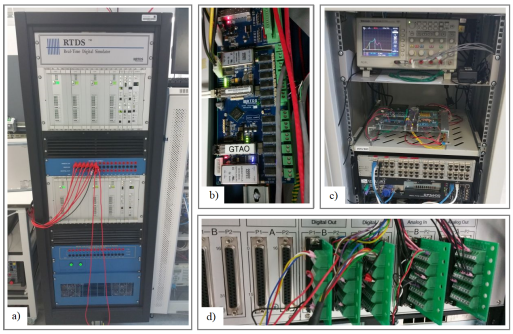

Fig. 17. Actual experimental arrangement: a) RTDS (front part), b) GTAO card (RTDS rear part), c) Opal-RT (front part), d) OP5340 analogue-in cards (Opal-RT rear part).

The testbed consists of the RTDS, where the actual network and HbCB are modelled. A Gigabit Transceiver Analogue Output Card (GTAO) has been used to interface analogue signals (i.e. HbCB fault current signatures) from the RTDS simulator to Opal-RT real time simulator. The GTAO signals have been sampled synchronously at a rate of 1 μs.

In this arrangement, the Opal-RT unit is utilized as a physical fault recorder to sample HbCB fault current signatures at 96 kHz

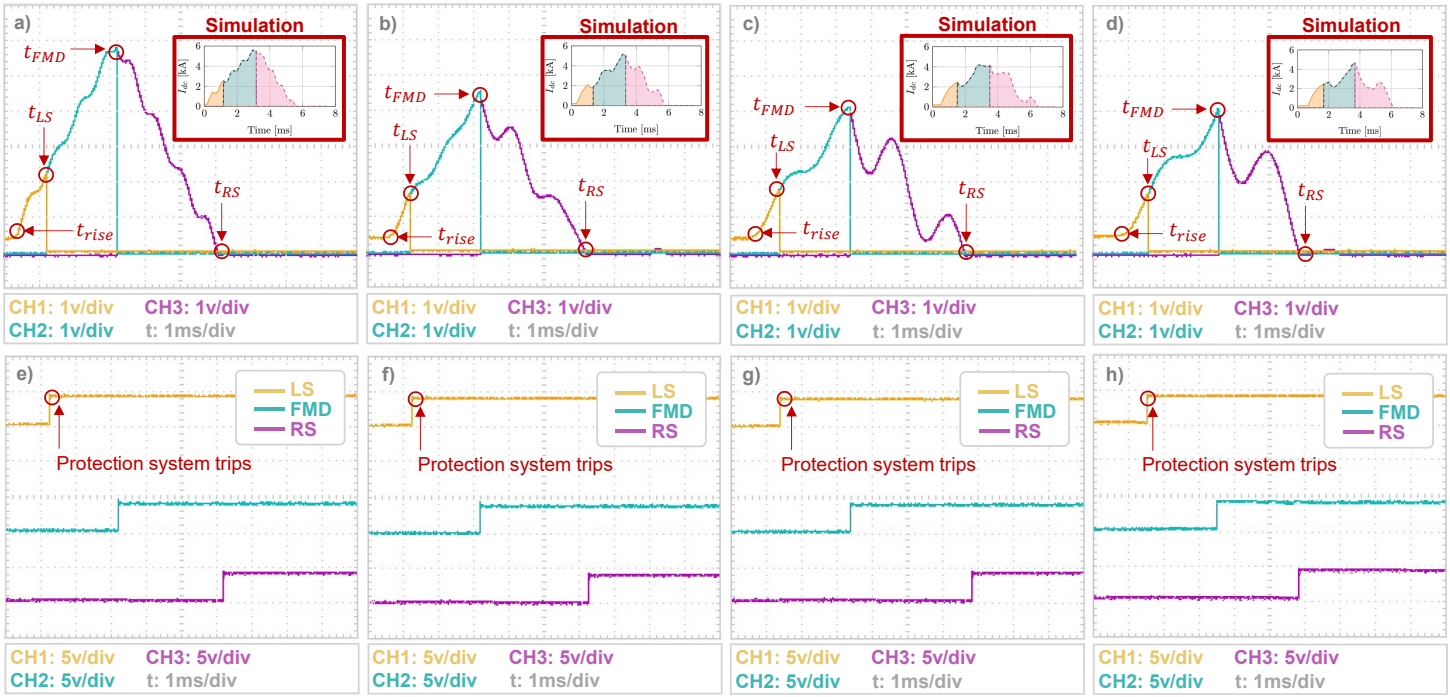

Fig. 18. Experimental results of HbCB fault current signatures and corresponding control signals: a-e) D_f= 50 km, b-f) D_f= 100 km, c-g) D_f= 150 km, d-h) D_f= 250 km.

(using OP340 analogue-in card). The actual electrical connections have been established using DB-37 slim breakout boards. The fault records obtained from Opal-RT have been stored locally on a PC for post-processing (i.e. fault location estimation).

B. Experimental Results

In order to examine the performance of the proposed fault location scheme, fourty cases of DC-side faults (PPFs) occurring on Line 1 have been considered for HIL testing. Due to space limitations four selected cases have been put forward for full pictorial representation as show in Fig. 18; these correspond to faults at locations: 50 km, 100 km, 150 km and 250 km.

The graphs at the top of Fig. 18, represent the currents inside the HbCB (the signals have been scaled accordingly to represent 1 kA/V) while the bottom graphs indicate all the control actions of HbCB.

By observing Fig. 18 it can be seen that following the fault occurrence, after a few milliseconds (fault detection delay) at $t = t_{LS}$, protection system initiate tripping signals (refer to the yellow line on bottom graphs) and the LS opens. At $t = t_{FMD}$ (after 2 ms which is associated with the mechanical delay of FMD) the FMD and power electronic valves in the commutation path turn off. The surge arrester will then drive the current to a near-zero region, where the RS opens at $t = t_{RS}$ and the fault is finally cleared. The experimental results demonstrate the anticipated behaviour of the system accounting for the evolvement of fault with respect to the physical system (i.e. fault current signatures) but also for the protection and control of the HbCB.

As it is difficult to recognize the difference between the experimental results and those obtained from simulation-based analysis (due to close resemblance of the current waveforms), the performance comparison is better appreciated by looking at the corresponding fault location estimate errors. The numerical experimental error values of fault location estimation obtained during HIL testing are presented in Fig. 19, together with those obtained from simulation-based analysis.

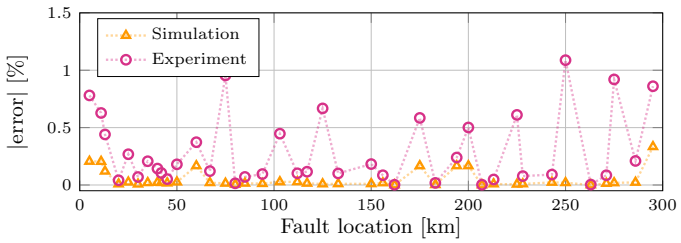

Fig. 19. Error values for simulation and experimental results for PPF on Line 1.

It can be observed from Fig. 19 that the high performance of the proposed fault location scheme is consistent when considering HIL testing. Even though some deterioration of accuracy is visible (maximum and average error in HIL testing is 1.08769 % and 0.28961 % respectively), the results confirm very high estimation accuracy of the scheme across hardware in the loop testing environments, which verifies its practical applicability. The deterioration in accuracy can be considered as one of the limitations of the method which is going to be addressed in the following subsection.

C. Enhancement of Training Database

The fault current signatures obtained from the HIL testing have been imported back to the training database as training patterns (i.e. set $\Psi(d)$) in order to investigate any improvement to fault location accuracy. The experimental cases have been fed again to the fault location system as test cases, considering two different variations of the training database: i) the initial database considering only simulated faults and ii) an enhanced training database where experimental cases are also included. The fault location results are presented graphically in Fig. 20.

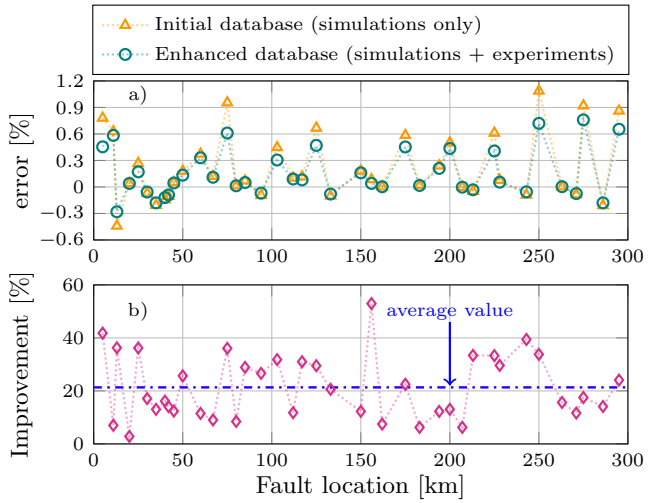

Fig. 20. Experimental-based fault location results considering different training databases: a) Comparison of percentage errors for simulation-only and enhanced training databases, b) Improvement of fault location accuracy when the enhanced training database is utilized.

It can be seen from Fig.20(a) that when the enhanced training database is utilized, the fault location error can be reduced for most of the fault cases. This practically signifies that any real-world data can further elevate the accuracy of the proposed fault location scheme.

The actual improvement (in percentage values) is depicted in Fig.20(b) and has been calculated according to the following expression:

$$\text{Improvement } [\%] = \frac{e_{idb} - e_{edb}}{e_{idb}} \, 100\% \tag{8}$$

where e_{idb} and e_{edb} is the error obtained by using the initial and enhanced database respectively.

Considering the average value of the results presented in Fig.20(b), the accuracy of the proposed fault location scheme can be improved by 21.33083 %. It shall be noted that even though this is a very effective way of improving the fault location accuracy, obtaining an actual record (or generating an experimental test-set) might not be always achievable.

VI. Conclusions

In this paper a novel fault location method is proposed for locating fault in MTDC networks. The method is based on the current measurements of HbCBs during the interruption process supported by pattern recognition-based approach. Training patterns and test cases have been generated, taking into account a wide range of fault distances, types and resistance values. The sampling frequency was set to 96 kHz to conform with the IEC 61869-9 standard, which enhances the standardization for HVDC automation and control applications. Additional artificial noise has been added to represent uncertainties and any other possible source of noise. The fault location method was found to be capable of classifying PPFs, PGFs and NGFs while the accuracy achieves values within an acceptable range even for highly resistive faults up to 500 Ω. Considering average values of errors, the minimum and maximum value has been found to be 0.06754 % and 0.31836 % respectively. The proposed scheme overcomes challenges related to travelling wave-based methods and those based on reflectometry (e.g. requirement for high sampling frequency and additional equipment such as GPS or signal generator). Further sensitivity analysis revealed that a minimum sampling frequency of 50 kHz would be sufficient in practical applications. Furthermore, due to the utilization of Pearson's correlation of coefficients, the scheme is characterized by immunity to offsets and gains arising from different operating conditions. The performance and practical effectiveness of the scheme has been also validated by utilizing real-time simulation with hardware in the loop testing. It has been also demonstrated that by enhancing the training database with experimental results, the fault location accuracy can be increased by 21.33083 %. The limitations of the method with respect to its practical implementation and the improvement of its accuracy have been also discussed in the paper.

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