A Mechanical DCCB with Re-Closure Capability and Its Performance in MMC based DC Grid

Binye Ni, Wang Xiang*, Meng Zhou, Xiaojun Lu, Wenping Zuo, Wei Yao, Jinyu Wen

State Key Laboratory of Advanced Electromagnetic Engineering and Technology, Huazhong University of Science and Technology, Wuhan 430074, China

***Abstract*-** For the modular multilevel converter (MMC) based DC grids using overhead line transmission, to restore the power transmission quickly, the DC circuit breakers (DCCB) are required to be able to re-close after DC line faults. To meet this requirement, an improved mechanical DCCB topology with re-closure capability is proposed in this paper. It consists of a pre-charged capacitor, an auxiliary capacitor, an oscillation inductor, and anti-parallel thyristors. Firstly, the topology and operating principle of the mechanical DCCB are presented in detail. Then, the general sizing methods associated with the impact of parameters on interruption capability are disclosed. The feasibility of the proposed mechanical DCCB is validated in a stiff DC system. Finally, the transient performance of the DC grid embedding the proposed mechanical DCCBs is investigated under various operating scenarios. The results verify the DC fault interruption and fast automatic re-closure capabilities of the proposed DCCB. It is shown that the mechanical DCCBs can be well applied to the overhead MMC based HVDC grids systems.

***Key Words* - DC grid, mechanical DC circuit breaker (DCCB), DC fault clearance, automatic re-closure, energy dissipation.**

I. INTRODUCTION

With the increasing demand for large scale renewable energy utilization, the modular multilevel converter (MMC) based DC grid technology is widely recognized as a promising approach for long distance power transmission [1]-[4].

To deal with the DC faults on overhead lines, the high power DC circuit breakers (DCCB) are adopted to isolate the faulty lines [5][6]. On detecting DC faults, DCCBs will be tripped to interrupt the fault current

Corresponding author: xiangwang1003@foxmail.com (W. Xiang)

within several milliseconds, which avoids the blocking of converters and realizes un-interrupted power transmission of the DC grid [7]. Among the various DCCB technologies, the hybrid DCCBs based on fast mechanical switch and full-controlled power electronic devices are conventionally considered as the most suitable solution [8]-[11]. Some prototypes of hybrid DCCB have been developed, such as the DCCBs with transfer branches consisting of full-bridge sub-modules and diode bridges [12][13]. These two prototypes will be applied in the ±500 kV *Zhangbei* DC grid project [14], which is the first MMC based DC grid in the world. However, according to the bidding results of this project, the cost of hybrid DCCBs accounts for about 20.1% of total investment, which is very close to the cost of valves (33.4%) [15]. The high cost of DCCBs hampers the further development of DC grid technology.

In order to reduce the cost of hybrid DCCB, some researches propose several improved topologies, such as the DCCBs disclosed in [16][17]. These topologies introduce an uncharged commutation capacitor in the main branch to make the cost economically competitive. However, these improved topologies still suffer from relatively large conduction power loss. An alternative scheme is to adopt mechanical DCCBs. Unlike hybrid DCCBs, the mechanical DCCBs utilize inductors and pre-charged capacitors to generate an oscillated current and create a zero crossing point in the fault current. Since no full-controlled power electronic devices are used, the capital cost and power loss can be significantly reduced. But the traditional mechanical DCCBs have the problem of long interruption time (more than 10 ms) [18]-[19], failing to meet the high-speed requirement of MMC-HVDC systems.

Recently, with the development of mechanical switch technology, the interruption time of mechanical DCCBs is much improved [20]-[22]. References [23]-[24] propose a coupling mechanical DCCB topology, which has the interruption capability and speed comparable to the hybrid DCCBs. The commutation branch of the mechanical DCCB is consisted of a low-voltage triggering circuit and a high-voltage oscillation circuit. When DC faults happen, the triggering circuit will generate a pulse current and an oscillation current will be induced at the high-voltage side through the coupling reactors. In 2017, this DCCB has been successfully put into operation in the ±160 kV *Nan'ao* three-terminal HVDC project.

Similar to AC grids, for the MMC based DC grids using overhead transmission lines, the transmission system operator (TSO) requires the DCCB to automatically re-close after fault isolation to ensure fast recovery of power transmission. For instance, in *Zhangbei* project, the DCCBs will automatically re-close within 300 ms [14]. If DCCBs re-close to permanent faults, they will trip again. However, since it is difficult to recharge the pre-charged capacitor within the reclosing time, the commissioned mechanical DCCBs are not able to re-close when instantaneous faults occur.

To overcome the technical defects of the existing mechanical DCCBs, this paper proposes a mechanical DCCB with re-closure capability. It consists of a pre-charged capacitor, an auxiliary capacitor, an oscillation inductor, and anti-parallel thyristors. Different from the coupling mechanical DCCBs proposed in [23]-[24], the pre-charged capacitor can be recharged by discharging the auxiliary capacitor to obtain the re-closure capability. Compared with the mechanical DCCB proposed in [25], this DCCB replaces the switches in commutation branch by thyristor valve to increase the operation speed. Besides, without the use of extra pre-charged capacitor, the proposed DCCB has advantages in both cost and volume. The detailed comparisons between the proposed DCCB with typical existing DCCB topologies are shown in Table I. As can be seen, the proposed DCCB is more appropriate for the DC grid using overhead lines.

Table I The comparisons the proposed DCCB with existing DCCB topologies

Categories	Hybrid DCCB				Mechanical DCCB				
Publications	[10]-[11]	[12]	[13]	[17]	[20]	[25]	[23] [24]	[26] [27]	The proposed topology
Topologies	Inverse IGBTs submodule	Full-bridge submodule	Diode-bridge submodule	Capacitor commutated	LC resonant	Extra switch and capacitor	Coupling topology	LC-Bridge topology	
Interruption theory	Use full-controlled power electronic devices to commutate and interrupt fault current			Use capacitor to commutate current	Use pre-charged capacitor to inject inverse current to interrupt fault current				
Operation time	2.4 ms	⩽3 ms	⩽3 ms	3.21 ms	3~4 ms	10 ms	⩽5 ms	About 3 ms	About 3 ms
Re-Closure Capability	√	√	√	√	×	√	×	×	√
	More arresters (MOVs) should be installed to facilitate re-closure capability								
Cost	High (due to expensive IGBTs)			Lower than [10]- [13]	Lower than hybrid DCCB		Lower than typical topology		Higher than [23]- [27]
Conduction loss	High (due to IGBTs in LCS)				Low				
Volume	Small				Larger than hybrid DCCB (due to pre-charged capacitor)				

The remainder of this paper is organized as follows. Firstly, the system layout of the MMC based DC grid

is introduced in section II. Then, the operating principle and dynamics during the operation of the proposed DCCB are analyzed in section III. The parameters design of the main circuit components of this DCCB is discussed in section IV. Then, the performance and effectiveness of the DCCB are verified by the simulations in section V. Finally, the performance of the four-terminal meshed DC grid embedding the proposed DCCB is studied in section VI. And the conclusion is drawn in section VII.

II. DC Fault Management of the MMC Based DC Grid

The topology of a bipolar four-terminal meshed DC grid is shown in Fig. 1. Each converter employs the half-bridge sub-modules based MMC topology. The DCCBs and current limiting inductors are installed on both terminals of the overhead lines.

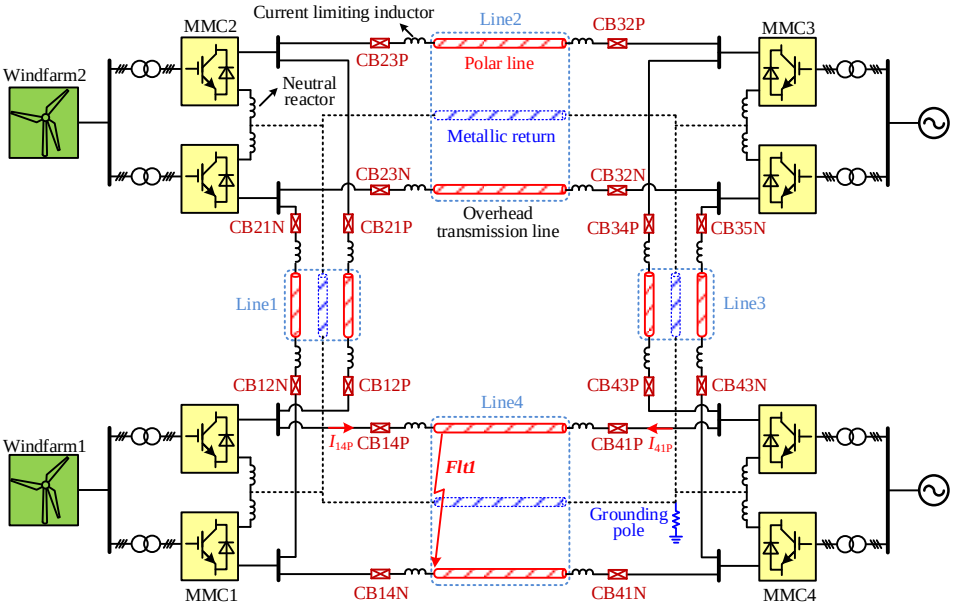


Fig. 1. The structure of a bipolar four-terminal MMC-based DC grid with mechanical DCCB.

The DC fault management sequence of the meshed overhead DC grid is shown in Fig. 2. When a DC fault occurs, the protection system sends the tripping orders to DCCBs on the faulty lines within 2-3 ms delay [28][29]. Then, the DCCBs trip and the fault current begins to decrease within 2-3 ms. After sufficient deionization of DC lines (200-300 ms) [14], the DCCBs automatically re-close. If the fault still exists, the line current will increase rapidly again. The DCCBs are considered to re-close to a permanent DC fault and immediately trip again.

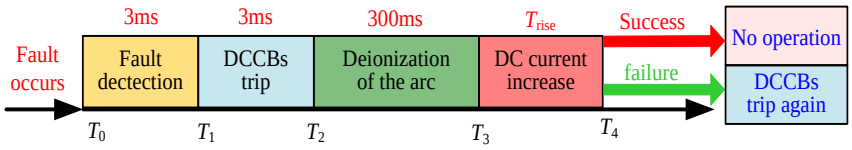


Fig. 2. The sequence of DC fault management for overhead DC grid.

III. Topology of Mechanical DCCB with Re-closure Capability

A. Re-closure Problem of the Existing Mechanical DCCB

The topology of a coupling mechanical DCCB is shown in Fig. 3. Similar to the conventional mechanical DCCB, this topology also consisted of the mechanical switch (MS), metal oxide varistors (MOVs), thyristors and a pre-charged capacitor. It adopts a triggering circuit at the low-voltage side, which reduces the withstanding voltages of the components and further reduces the cost of DCCB.

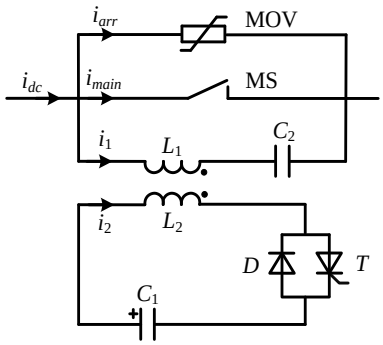


Fig. 3 Structure of the coupling mechanical DC circuit breaker.

However, the coupling mechanical DCCB also suffer from the problem of capacitor recharging during reclosing. After the DCCB interrupts the fault current, the voltage of the pre-charged capacitor may drop to 0 or even be opposite to the initial value. Due to the limited capacity of the charge circuit, it is impossible to charge the capacitor voltage to the initial value within the reclosing time (200-300ms). Therefore, the coupling mechanical DCCB lacks the re-closure capability and is not applicable to the DC grid using the overhead lines.

B. Mechanical DCCB with Re-closure Capability and its Operating Principle

To meet the requirement of post-fault re-closure, this paper proposes an improved topology of mechanical DCCB, as shown in Fig. 4. This topology takes advantage of discharging of the capacitor C_A to recharge the

pre-charged capacitor during reclosing operation.

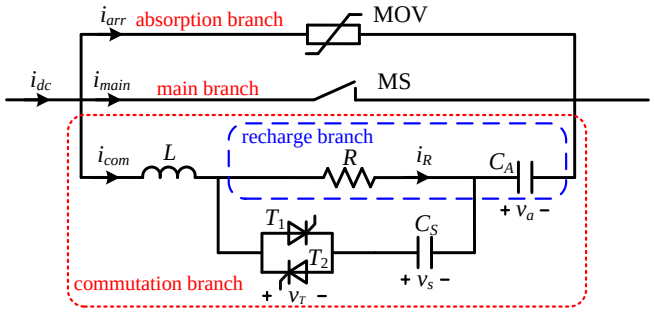
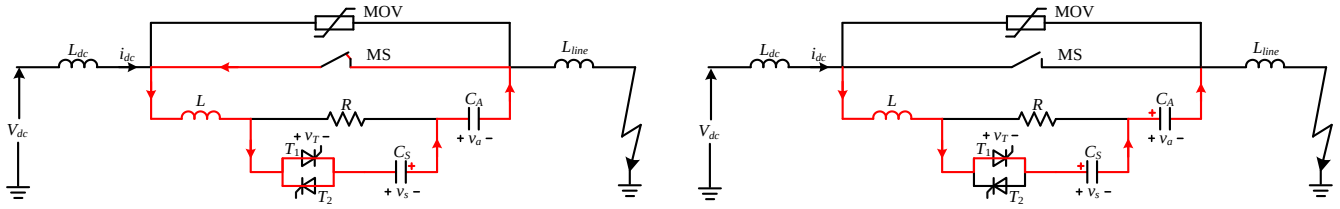


Fig. 4. Structure of the improved mechanical DC circuit breaker.

As can be seen, the improved DCCB also consists of three parallel branches, a main branch, a commutation branch, and an absorption branch. The main branch and absorption branch is similar to that of the coupling mechanical DCCB topology. The commutation branch adopts a recharge branch with a pre-charged capacitor C_S, an auxiliary capacitor C_A, an inductor L, and anti-parallel thyristors T_1 and T_2. The capacitor C_S is pre-charged by a DC power supply.

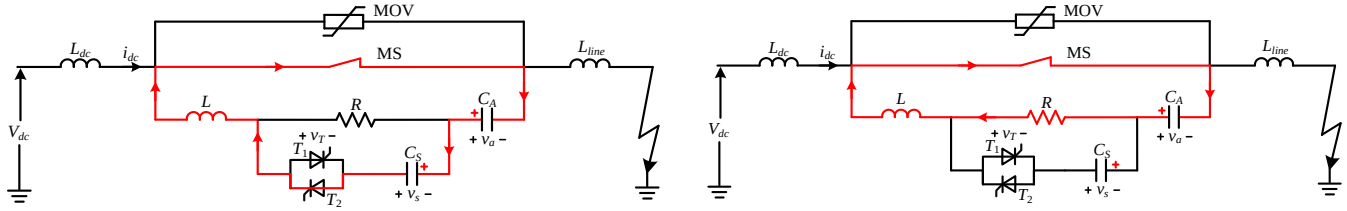
In normal operation, the DC current I_{dc} only flows through the main branch. The capacitor C_S is pre-charged. On receiving a tripping order, the mechanical switch opens firstly and the arc is established between the contacts. After the contacts reaching sufficient dielectric distance, thyristors T_1 and T_2 are turned on. Then, an oscillation current is imposed on i_{main} to extinguish the arc on the MS through the red line shown in Fig. 5(a). The arc is extinguished when i_{main} reaches zero. To ensure reliable arc-extinguish, the thyristors remain turning on for several oscillation periods to generate multiple zero-crossing points. Subsequent to the delay of arc-extinguish time Δt_{ae}, the DC current i_{dc} will be diverted to the commutation branch. Then, the DC current charges the capacitors C_S and C_A, as shown in Fig. 5(b). Once the sum of voltages of the capacitors reaches the threshold of MOVs, the DC current will be commutated to the absorption branch. Once i_{arr} is dissipated by the arresters, the DC fault current is completely cleared and the voltage across the breaker restores to V_{dc}. The first tripping operation finishes.



(a) process of arc-extinguish (b) process of commutation

Fig. 5. The first tripping operation of the proposed mechanical DCCB.

After deionization of faulty lines, the DCCB begins to automatically re-close. Since C_S is reversely charged by fault current during the first tripping, thyristor T_2 is turned on to discharge C_S prior to re-closure of MS. After sufficient discharge time, MS re-closes. Then, C_S will be recharged and C_A will be discharged within hundreds of microseconds. The current path is shown in the red line of Fig. 6(a). Due to the unidirectional conductivity of thyristor T_2, C_S is unable to discharge and its voltage will remain the pre-set value. As a result, it is able to generate an oscillation current again. Meanwhile, the residual voltage across C_A discharges through the red line shown in Fig. 6(b), and eventually decays to 0 kV. If the DCCB re-closes to a permanent fault, T_1 and T_2 will be turned on and DCCB is able to trip again.



(a) process of C_S recharge (b) process of C_A discharge

Fig. 6. The reclosing operation of the proposed mechanical DCCB.

C. Dynamic during First Tripping

In normal operation, the DC current i_{dc} only flows through the main branch. The voltage of the auxiliary capacitor C_A (v_a) equals to 0. The voltage of the capacitor C_S (v_s) is pre-charged to V_{s0}.

On receiving the tripping order, MS opens firstly and then thyristor T_1 is turned on to extinguish the arc. During the short arc-extinguish time Δt_{ae}, as the current rise rate is limited by the current limiting inductance, the i_{dc} is assumed to be constant. Therefore, we have

$$i_{main} + i_{com} = I_{dc(trip)} \tag{1}$$

$$\begin{aligned} L\frac{di_{com}}{dt} &= v_s + v_a = V_{s0} - \frac{1}{C_S}\int_{0^+}^{t}\left(i_{com} - i_R\right)dt - \frac{1}{C_A}\int_{0^+}^{t} i_{com}dt \\ &\approx V_{s0} - \frac{1}{C_S}\int_{0^+}^{t} i_{com}dt - \frac{1}{C_A}\int_{0^+}^{t} i_{com}dt \end{aligned} \tag{2}$$

where $I_{dc(trip)}$ is the DC current at the moment when the thyristor T_1 is switched on, i_R is the current flowing through the discharge resistor R. The integral of i_R is far smaller than that of i_{com} and therefore can be neglected. Assuming that T_1 receives a trigger signal at t=0, from equation (2), the analytical expressions of i_{main}, v_s, and v_a during arc-extinguished process are as follows

$$i_{main} = I_{dc(trip)} + V_{s0}\sin\left(\omega_0 t\right)/Z_c \tag{3}$$

$$v_s = V_{s0} - V_{s0}\left[1-\cos\left(\omega_0 t\right)\right]/\left(\omega_0 Z_c C_S\right) \tag{4}$$

$$v_a = -V_{s0}\left[1-\cos\left(\omega_0 t\right)\right]/\left(\omega_0 Z_c C_A\right) \tag{5}$$

where $Z_c = \sqrt{L(C_S + C_A)/(C_S C_A)}$, $\omega_0 = \sqrt{(C_S + C_A)/(LC_S C_A)}$.

After the delay of arc-extinguish time Δt_{ae}, the DC current is diverted to the commutation branch. Denote that at this instant the voltages of C_S and C_A are V_{s1} and V_{a1}, respectively. Therefore, we have

$$i_{dc} = i_{com} = C_S\frac{dv_s}{dt} + i_R \approx C_S\frac{dv_s}{dt} \tag{6}$$

$$\left(L_{dc} + L\right)\frac{di_{dc}}{dt} + \frac{1}{C_A}\int_{\Delta t_{ae}^+}^{t} i_{dc}dt + v_s = V_{dc} - V_{a1} \tag{7}$$

The i_R is far smaller than i_{dc} and thus can be ignored. From equations (6) and (7), the analytical expressions of i_{com}, v_s, and v_a during the commutating process are as follows:

$$i_{com} = I_{dc(trip)} + I_0\sin\left[\omega_1\left(t - \Delta t_{ae}\right)\right] \tag{8}$$

$$v_s = V_{s1} + I_0\left[1-\cos\omega_1\left(t - \Delta t_{AE}\right)\right]/\left(\omega_1 C_S\right) + I_{dctrip}\left(t - \Delta t_{ae}\right)/C_S \tag{9}$$

$$v_a = V_{a1} + I_0\left[1-\cos\omega_1\left(t - \Delta t_{AE}\right)\right]/\left(\omega_1 C_A\right) + I_{dctrip}\left(t - \Delta t_{ae}\right)/C_A \tag{10}$$

where $Z_{c1} = \sqrt{(L + L_{dc})(C_S + C_A)/(C_S C_A)}$, $I_0 = \left(V_{dc} - V_{s1} - V_{a1}\right)/Z_{c1}$, $\omega_1 = \sqrt{(C_S + C_A)/[(L + L_{dc})C_S C_A]}$. Once the sum of voltages across the capacitors reaches the action threshold of MOVs, the commutation process ends.

D. Dynamic during Reclosing

Thyristor T_2 is firstly turned on and then MS re-closes. The main branch and commutation branch form an

oscillating circuit. Therefore, we have

$$L\frac{di_{com}}{dt}+\frac{1}{C_S}\int_{0^+}^{t} i_{com}dt+\frac{1}{C_A}\int_{0^+}^{t} i_{com}dt=-V_{dc} \tag{11}$$

Assuming that MS re-closes at t=0, from equation (11), the analytical expressions of i_{com}, v_s, and v_a during the recharging process are as follows

$$i_{com}=-V_{dc}\sin(\omega_0 t)/Z_c \tag{12}$$

$$v_s=-V_{dc}\left[1-\cos(\omega_0 t)\right]/(\omega_0 Z_c C_S) \tag{13}$$

$$v_a=V_{dc}-V_{dc}\left[\cos(\omega_0 t)-1\right]/(\omega_0 Z_c C_A) \tag{14}$$

After recharge time of Δt_{rch}, the oscillation ends with the arrival of zero current, due to the unidirectional conductivity of the thyristor T_2. The voltages of C_S and C_A are as follows

$$V_{s2}=-2V_{dc}/(\omega_0 Z_c C_S) \tag{15}$$

$$V_{a2}=V_{dc}-2V_{dc}/(\omega_0 Z_c C_A) \tag{16}$$

C_S is unable to discharge and its voltage will remain V_{s2}, whereas the residual voltage across C_A discharges through the red line shown in Fig. 6(a). The discharge process of C_A is described by

$$L\frac{di_{com}}{dt}+\frac{1}{C_A}\int_{\Delta t_{rch}^{+}}^{t} i_{com}dt+Ri_{com}=-V_{a2} \tag{17}$$

Since the discharge resistor R is relatively large, the discharge process is an overdamped process. Therefore, the analytical expressions of v_a during the discharge process is as follows

$$v_a=\frac{V_{a2}}{2\beta}\left[(\alpha+\beta)e^{(-\alpha+\beta)t}-(\alpha-\beta)e^{-(\alpha+\beta)t}\right] \tag{18}$$

where $\alpha=R/(2L)$, $\beta=\sqrt{\alpha^2-1/(LC)}$. After the sufficient decay time, which equals $5/(\alpha-\beta)$, v_a almost decays to 0.

IV. Parameter Design of the Proposed Mechanical DCCB

A. *Dimensioning of the Pre-Charged Voltage V_{s0}*

During the tripping process, capacitor C_S will discharge to impose an inverse oscillation current on the main branch current to extinguish the arc. The amplitude of the oscillation current represents the maximum

current that the DCCB can interrupt successfully (maximum breaking current). From equation (3), it is evident that the maximum breaking current is related to the pre-charged capacitor voltage (V_{s0}). According to the positive direction of v_s shown in Fig. 4, the value V_{s0} is negative. Fig. 7 shows the absolute value of V_{s0} versus the maximum breaking current of DCCB. Parameters for the tested mechanical DCCB are listed in Table II, except that $|V_{s0}|$ is varied from 0 to 500 kV. The representative DC grid requires that the DCCB is able to interrupt the fault current of 25 kA. To achieve the maximum breaking current of 25 kA, $|V_{s0}|$ should not be less than 314 kV. As a conservative design, the pre-charged voltage V_{s0} is dimensioned as -320kV.

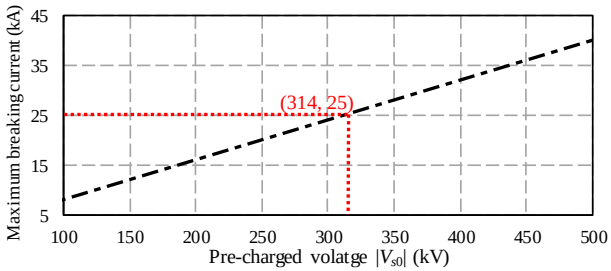


Fig. 7. Maximum breaking current versus pre-charged voltage $|V_{s0}|$.

B. Dimensioning of the Inductance L

From equation (3), the arc on the MS is commonly extinguished before the oscillation current reaches the first peak point. Thus, the arc-extinguished time Δt_{ae} is normally less than a quarter of the oscillation period. Conservatively, Δt_{ae} takes its theoretical maximum.

Fig. 8 shows the arc-extinguish time of DCCB versus inductance L. Decreasing inductance L results in reduced Δt_{ae}, which represents a higher interruption speed of DCCB. However, a low inductance means higher current change rate (dI/dt), which leads to lower reliability and higher cost of the thyristors and MS. There is a trade-off between the arc-extinguish time and the cost for the dimension of the inductance. In this paper, the inductance is designed as 0.8 mH to achieve the arc-extinguish time of 100 μs.

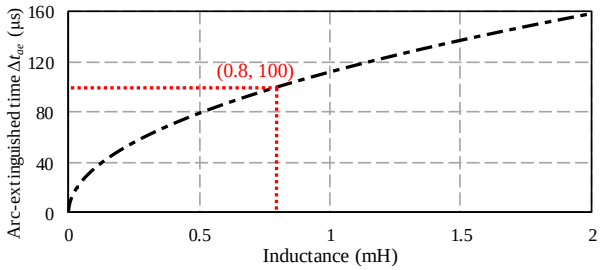


Fig. 8. Arc-extinguish time Δt_{ae} versus inductance L.

C. Dimensioning of the Capacitances

After the arc is extinguished, the residual current is continually flowing through the commutation branch and charges the capacitors until the sum of their voltages reaches the thresholds of the arrester. The duration of this commutation process (Δt_{com}) can be calculated from equations (9)-(10). To simplify the calculation, the DC current is assumed to be constant and equals to $I_{dc(trip)}$. Therefore, Δt_{com} is obtained

$$\Delta t_{com} = \frac{C_E}{I_{dc(trip)}}\left(V_{arr} + V_{s0}\cos\Delta t_{AE}\right) \tag{19}$$

where $C_E = C_S C_A / (C_S + C_A)$, V_{arr} represents the protection threshold of the arrester.

Fig. 9 shows the commutation time versus breaking current $I_{dc(trip)}$ and equivalent capacitance C_E. Increasing the breaking current $I_{dc(trip)}$ or decreasing the equivalent capacitance C_E results in reduced commutation time. There is a trade-off between the commutation time and the cost for the dimension of the capacitors. The equivalent capacitance is designed as 5.1 μF to achieve the commutation time of 0.5 ms in terms of $I_{dc(trip)}$ = 10 kA. The commutation time versus breaking current with C_E = 5.1 μF is shown in Fig. 10.

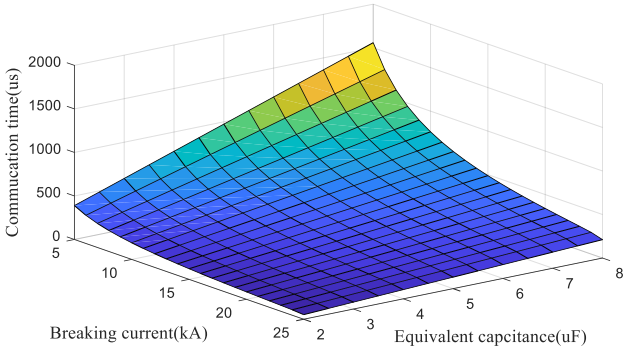


Fig. 9. Commutation time versus breaking current $I_{dc(trip)}$ and equivalent capacitance C_E.

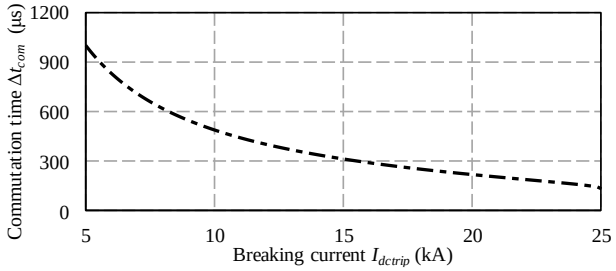


Fig. 10. Commutation time versus breaking current with C_E = 5.1 μF.

During reclosing, C_S is recharged while the auxiliary capacitor C_A is discharged. The relationship between the recharged voltage V_{s2} and the capacitance ratio C_S/C_A can be obtained from equation (15).

Fig. 11 shows the recharged voltage $|V_{s2}|$ versus capacitance ratio C_S/C_A. To achieve a recharged voltage of -320 kV, the capacitance ratio needs to be less than 2.125. As a conservative design, the capacitance ratio C_S/C_A is dimensioned as 2.04. Combined with C_E = 5.1 μF, the capacitance of the C_S and C_A are chosen as 15.5 μF and 7.6 μF, respectively.

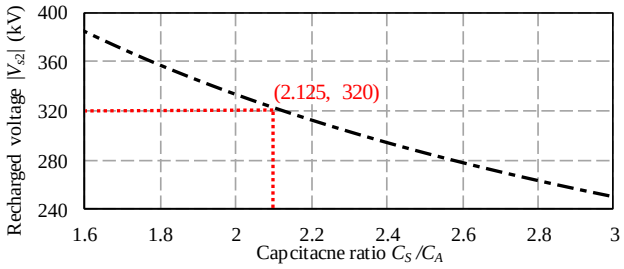


Fig. 11. Recharged voltage $|V_{s2}|$ versus capacitance ratio.

D. Dimensioning of the Discharge Resistance R

Following the recharge process, the voltage across C_A reaches a steady-state value. Then, through the circuit composed of discharge resistor, C_A discharges and its voltage eventually decays to 0, as shown in equation (18). The decay time of this voltage is related to the value of discharge resistance.

Fig. 12 shows the decay time versus the discharge resistance. The residual voltage of v_a may affect the arc-extinguish process of the second trip. To ensure the twice-tripping capability of the DCCB, the voltage across C_A must decrease to 0 prior to the second breaking. Considering the secondary interruption normally starts at 5ms subsequent to re-closure, the decay time should be no more than this duration. Therefore, the value of discharge resistance is dimensioned as 125 Ω.

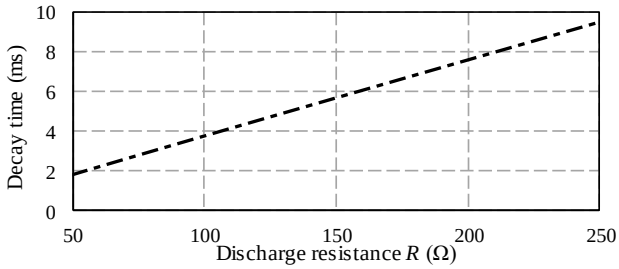


Fig. 12. Decay time versus discharge resistance.

E. Dimensioning of the Rating of Thyristors

To achieve the control of oscillation current, the inverse paralleled thyristors are implemented in the commutation branch, as shown in Fig. 4.

During normal operation, there is no current flowing through the commutation branch. The thyristors directly withstand the voltage stress across the capacitor C_S. Therefore, the voltage rating of the thyristors is V_{s0}.

During reclosing operation, the oscillation current, caused by the discharge of the C_A, flows through the thyristors to recharge the C_S. From equation (12), the maximum current through the thyristors is

$$I_T = V_{dc} / Z_c \tag{20}$$

Besides, the thyristor T_2 is turned off after the capacitor C_s has been recharged. The thyristors T_1 and T_2 need temporarily withstand the DC line voltage ($V_{s2} + V_{a2} = V_{dc}$).

Take ABB's Thyristor 5STP 08F6500 [30] as example to design T_1 and T_2. This type of thyristor has a rated voltage of 4.34 kV and can withstand the peak voltage of 6.5 kV for 10 ms. And it can tolerate the surge current of 15.1 kA. Therefore, it is required to combine 3 individual thyristors in parallel (withstand 45.3 kA) as a group and connect 80 groups in series (withstand 520 kV) to form T_1 or T_2.

V. SIMULATION OF THE PROPOSED MECHANICAL DCCB

To verify the performance of the mechanical DCCB, the test system shown in Fig. 13 is simulated. In Fig. 13, the DCCB is connected to a stiff 500kV DC voltage source. The nominal DC current is 3.0 kA. The switch S_{flt} is closed to initiate the fault. Such stiff DC voltage source imposes most stringent requirements on DCCB.

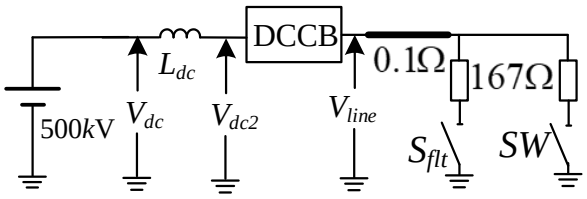


Fig. 13. Tested single-terminal system.

Table II Parameters of the Tested Mechanical DCCB

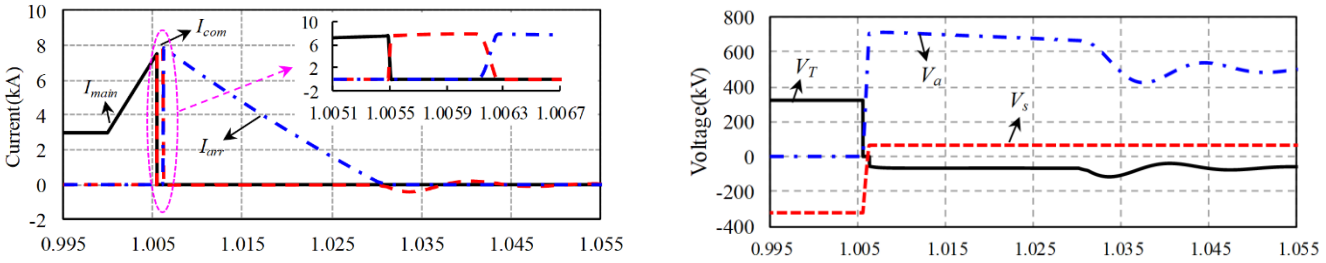
Parameter	*Value*
Rate DC voltage V_{dcn}/kV	500
Rate DC current I_{dcn}/kA	3
Maximum breaking current I_{max}/kA	25
Operation time of the MS T_{mec}/ms	2.5
Pre-charged voltage V_{s0} of capacitor C_S /kV	-320
Pre-charged capacitance C_S/μF	15.5
Auxiliary capacitance C_A/μF	7.6
Oscillation inductance L/mH	0.8
Discharge resistance R/Ω	125
Rated voltage of the thyristor valve V_{Tn}/kV	320
Rated voltage of the arrester V_{arr}/kV	660

Table II lists the parameters of the tested mechanical DCCB. S_{flt} is closed at 1s to simulate a permanent low-resistance fault. The tripping order of the DCCB is sent at 1.003 s to simulate the fault detection delay. Due to 2.5 ms of the operation delay of MS, the trigger signals of thyristors T_1 and T_2 are sent at 1.0055 s and last until 1.007 s. The deionization time is set as 300ms. Therefore, the trigger signal of thyristor T_2 is issued at 1.293 s, and MS is re-closed at 1.303 s. Then, the protection system determines whether the fault is still existing. Once the DC current exceeds 6.8 kA, tripping order of DCCB will be sent again. The simulation results are shown in Fig. 14 and Fig. 15.

Fig. 14 (a) shows the currents i_{main}, i_{com}, and i_{arr}. Once the thyristors receive the trigger signal, i_{main} begins to decrease and reaches zero after Δt_{ae} arc-extinguish time. Then, the DC current transfers to the commutation branch and charges C_S and C_A. During the commutation time of Δt_{com}, the current in the commutation branch i_{com} barely changes. The Δt_{com} is approximately 600 μs and the tripping current $I_{dc(trip)}$ is 8 kA, which is in line with the calculated value shown in Fig. 10. In the meantime, the voltages across capacitors C_A and C_S (v_a and v_s) increase with a fast slope, as shown in Fig. 14 (b). Once the sum of v_a and v_s reaches the threshold (typically $1.5V_{\mathrm{dcn}}$) of the arresters banks, the arresters conduct to suppress the current, and the DC current gradually decreases to zero. After i_{arr} decreasing to zero, C_A discharges through the commutation branch, and its voltage, which equals the voltage across the breaker, resumes to V_{dc}.

Fig. 14 (b) shows the voltage in the mechanical DCCB during fault clearance. Upon receiving the tripping

signal, the voltage across thyristors v_T decreases to almost zero immediately. Upon receiving the tripping signal, the voltage across thyristors v_T decreases to zero immediately. Then, v_a and v_s increase during the time of Δt_{ae} and Δt_{com}. Once arresters conduct, v_a and v_T remain constant since the thyristors are turned off. Before i_{arr} decreases to zero, v_a is maintained at the range from 720 kV to 660 kV.

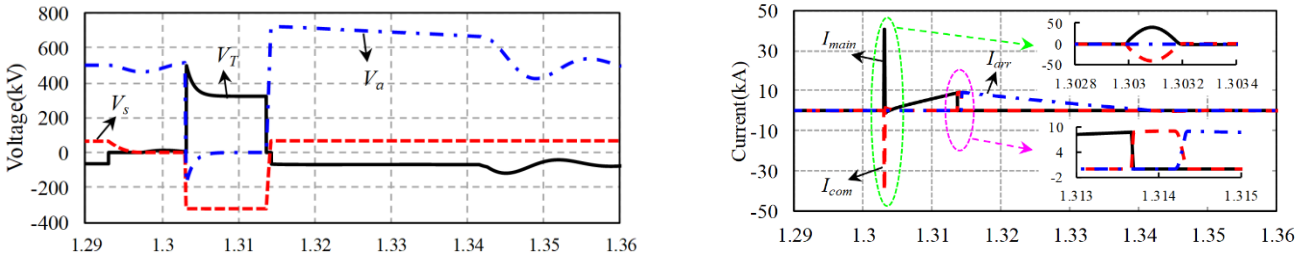


(a) Currents in the DCCB during fault clearance

(b) Voltages of the DCCB during fault clearance

Fig. 14. Simulation of the fault clearance of the mechanical DCCB.

Fig. 15 shows the voltages and currents of the mechanical DCCB during reclosing. Prior to re-closure of MS, v_s discharges to zero by turning on T_2. Once MS re-closes, v_s is recharged and v_a is discharged. The recharge process completes within 200 μs. Finally, v_s restores to -320 kV and v_a decreases to -176 kV, as shown in Fig. 15 (a). Therefore, the capacitor C_S is able to generate an oscillation current again. Then, C_A will discharge through the discharge resistor R and its voltage decreases to 0 within 5 ms. The mechanical DCCB recovers to the initial state before tripping operation and regains the interruption capability. As shown in Fig. 15(b), once the DCCB re-closes, the oscillation circuit generates an impulse current with 40.56 kA peak value. The second tripping operation is similar to that as shown in Fig. 14(a).



(a) Voltages of the DCCB during reclosing

(b) Currents in the DCCB during reclosing

Fig. 15. Simulation of reclosing of the mechanical DCCB.

VI. Performance of the DC Grid Embedding the Mechanical DCCB

To verify the applicability of the improved mechanical DCCB, a further simulation is performed in a four-

terminal HVDC grid embedding this DCCB, as shown in Fig. 1. The main circuit parameters of the converters in this system are given in Table III. The overhead lines are modeled with the frequency-dependent phase model provided by PSCAD/EMTDC. The parameters of transmission lines are shown in Table IV.

TABLE III PARAMETERS OF THE CONVERTER STATIONS

Parameters	MMC1	MMC2	MMC3	MMC4
DC voltage rating (kV)	±500	±500	±500	±500
Power rating (MVA)	3000	1500	1500	3000
AC voltage (kV)	230	230	525	525
Control mode	V_{ac}-f	V_{ac}-f	P-Q	V_{dc}-Q
Submodule capacitance (mF)	15	8	8	15
Arm inductance (mH)	50	100	100	50
Submodule number	244	244	244	244
Polar DC inductance (mH)	150	150	150	150
Neutral DC inductance (mH)	300	300	300	300
Grounding pole resistance (Ω)	None	None	None	15

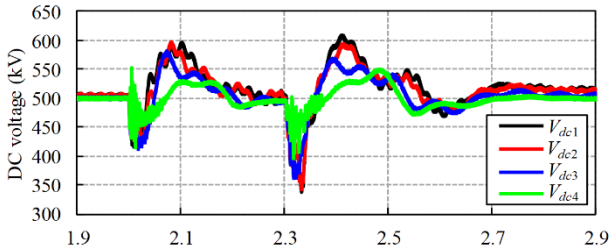
TABLE IV PARAMETERS OF THE OVERHEAD TRANSMISSION LINE

Parameters	Line1	Line2	Line3	Line4
Overhead line length (km)	49.6	205.1	187.1	206.4
Overhead line resistance (mΩ/km)	9.96	9.96	9.96	9.96
Metallic return resistance (mΩ/km)	18.8	18.8	18.8	18.8

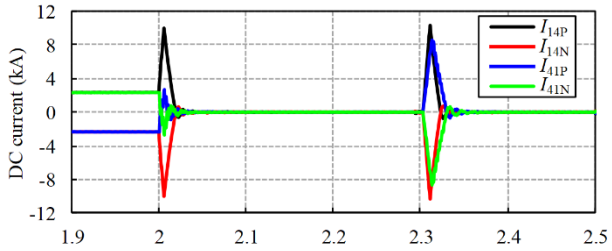
MMC1 and MMC2 operate as inverters in AC voltage and frequency control mode to maintain the stability of the wind farm. MMC3 operates as a rectifier in active and reactive power control mode. MMC4 operates as a rectifier in DC voltage control mode. Besides, the system also adopts a centralized protection scheme that the central controller detects the faults and delivers the trip orders to the specified DCCBs. The relay time of the DCCBs is assumed as 3 ms.

A. Response to Permanent DC Fault

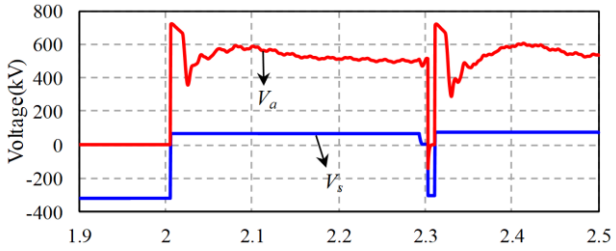
To verify the interruption capability of the mechanical DCCB in a four-terminal HVDC grid, a permanent pole-to-pole DC fault is applied at *Flt1* at 2.0 s. The fault location is at the DC terminal of MMC1, as shown in Fig. 1. The DCCBs receive the tripping order at 2.003 s. The reclosing time is set at 2.303 s due to 300 ms of the deionization time.



(a) DC voltage of positive pole at the DC terminal of each converter



(b) DC current in the faulty transmission line



(c) Capacitor voltages in CB14P

Fig. 16. DC grid response to a pole-to-pole DC fault.

Fig. 16 (a) shows the DC bus voltages of MMC1-MMC4. When the fault occurs, all DC voltages rapidly decrease. After fault clearance, all DC voltages restore to normal value after a certain transient. When the breakers re-close, the DC voltages V_{dc1}, V_{dc2}, and V_{dc3} decrease to 350 kV, while V_{dc1} decreases to 400 kV. Then, the DC voltages are similar to their performance during the first tripping.

Fig. 16 (b) shows the DC currents in the faulty transmission line during the operation of the DCCBs. When a fault occurs or DCCBs re-close, the DC current rises rapidly. During the first tripping, I_{14P} reaches the peak value of 10.01 kA at 2.0059 s, and I_{41P} reaches the peak value of 2.69 kV at 2.0064 s. During the second tripping, I_{14P} reaches the peak value of 10.34 kA at 2.3111 s, and I_{41P} reaches the peak value of 8.60 kA at 2.3132 s.

Fig. 16 (c) shows the voltages across capacitors in CB14P. Prior to reclosing operation, C_S is completely discharged and its voltage v_s decreases to 0 at 2.296 s. After the breakers re-close at 2.303 s, v_s is recharged to -304.67 kV immediately, while v_a reaches 142.24 kV and then is discharged to 0 at 2.308 s. That ensures the second interruption capability of the mechanical DCCB.

Table V shows the performance of the DCCBs on the faulty line. According to the values shown in Table V, the designed energy absorption of the arrester would not be less than 80.81 MJ (42.33+38.48 MJ). Besides,

during reclosing, the energy absorbed by CB41P and CB41N is larger than that of the CB14P and CB14N, though CB14P and CB14N have a larger peak fault current. It proves that the energy absorption of the arrester is mainly concerned with the energy stored in the transmission line, rather than the peak fault current.

TABLE V PERFORMANCE OF THE DCCBS ON THE FAULT LINE

Parameters	CB14P	CB14N	CB41P	CB41N
Peak fault current during first tripping (kA)	10.01	10.02	2.69	2.72
Energy absorption first tripping (MJ)	42.33	42.39	2.82	2.72
Peak fault current during second tripping (kA)	10.34	10.34	8.60	8.67
Energy absorption during second tripping (MJ)	38.48	38.42	48.13	48.19

B. Impact of the Dispersivity of the Breaking Time

Due to the time dispersivity of the mechanical movement of contacts during the tripping process of mechanical DCCBs, the breakers at positive and negative poles may not operate at the same time. Therefore, it is necessary to study the operational dispersivity of the two DCCBs and its influence on the performance of DCCBs.

A permanent pole-to-pole fault is applied at *Flt1* at 2.0 s. To simulate the time dispersivity of the breaking time, assume the breaking time of CB14P and CB14N are T_b and $T_b+\Delta t$, respectively. Δt is the dispersion time in the range from 0 to 0.5 ms. The simulation results are shown in Table VI.

Table VI shows the performance of the breakers under different dispersion time. The dispersion time mainly influences the peak fault current of CB14N and energy absorption of CB14P. These parameters increase with the rise of dispersion time. Therefore, the influence of the dispersivity of the breaking time should be considered in the design of the energy absorption of DCCB.

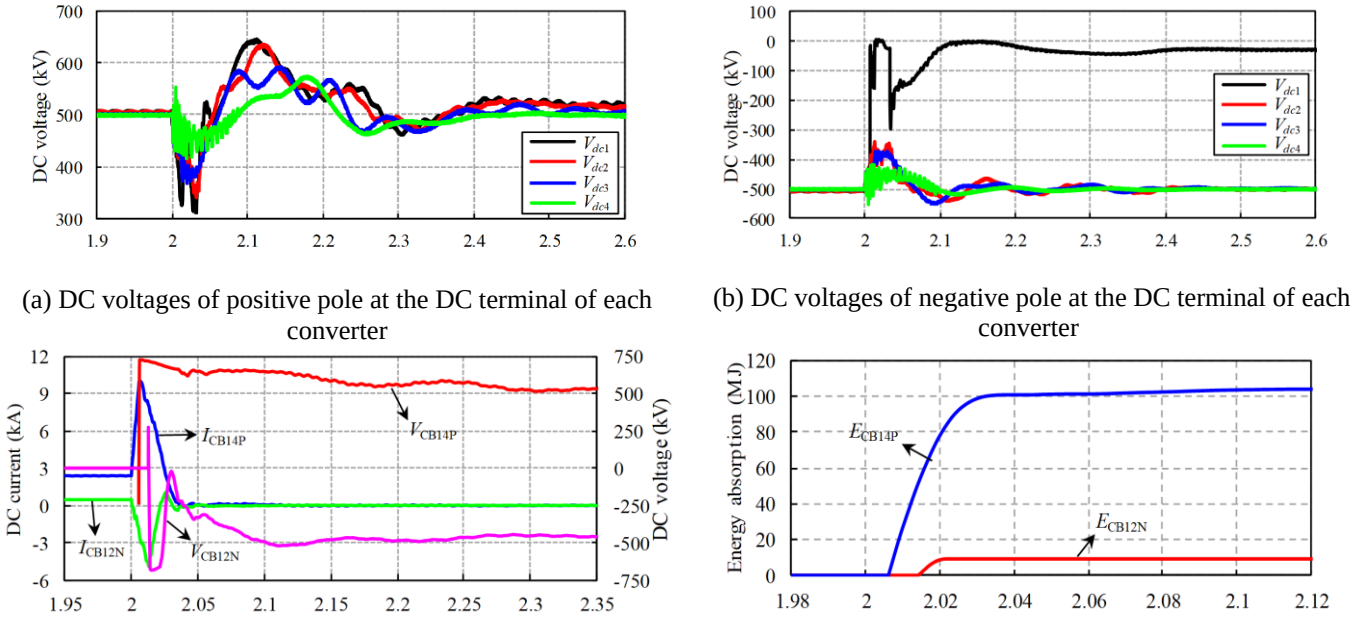
TABLE VI IMPACT OF THE INTERRUPTING TIME DISPERSION ON PERFORMANCE OF BREAKERS

Δt (ms)	0.1	0.2	0.3	0.4	0.5
Peak fault current of CB14P (kA)	10.02	10.02	10.01	10.01	10.01
Peak fault current of CB14N (kA)	10.17	10.31	10.44	10.56	10.67
Energy absorption of CB14P (MJ)	42.96	43.60	44.23	44.88	45.52
Energy absorption of CB14N (MJ)	42.61	42.81	42.99	43.14	43.29

C. Response to Malfunction of a DCCB

In the case of a DCCB malfunction, the normally operating DCCB will bear the fault current and pole-to-pole voltage until the backup protection reacts. It is an extremely severe situation for the normal operating DCCB. Therefore, this situation should also be considered in the design of DCCB.

A permanent pole-to-pole fault is applied at *Flt1* at 2.0 s to simulate this situation. Assume that CB14P can operate normally and CB14N fails to complete the tripping operation. After receiving the abnormally signal sent by CB14N, the backup protection commands CB12N to trip at 2.007 s. Then, the negative pole of MMC1 begins to block at 2.0071 s (considering the signal process delay), and the associated AC breakers completely trip at 2.009 s. The simulation results are shown in Fig. 17.



(a) DC voltages of positive pole at the DC terminal of each converter

(b) DC voltages of negative pole at the DC terminal of each converter

(c) Transient performance of CB14P and CB12N

(d) Energy absorption of CB14P and CB12N

Fig. 17. Response to a pole-to-pole DC fault with a negative DCCB failure.

Fig. 17 (a) and (b) show the DC bus voltages of the positive and negative poles, respectively. Similar to that in Fig. 16 (a), the bus voltages of positive pole recover to 500 kV after fault clearance, due to the normal operation of CB14P. As shown in Fig. 17 (b), the bus voltages of the negative pole of each converter can also restore to 500 kV except that of MMC1. The negative voltage of MMC1 increases to 0 rapidly after blocked. Then, it decreases to -300 kV after AC breakers tripping. Finally, the negative voltage of MMC1 becomes stable at the level of 30 kV.

Fig. 17 (c) shows the transient performance of the tripping breakers CB14P and CB12N. The fault current

of CB14P reaches the peak value of 10.03 kA at 2.006 s, and then the voltages across CB14P reached the peak voltage of 726.12 kV at 2.007 s. Afterward, the fault current of CB12N reaches the peak value of 4.89 kA at 2.013 s, and then voltages across CN12N reaches the peak voltage of 683.84 kV at 2.015 s. Besides, due to no operation of CB14N, the arrester in CP14P needs to bear the pole-to-pole voltage after CP14P trips. Thus, the arrester of CB14P conducts continuously until current on CB12N reached 0.

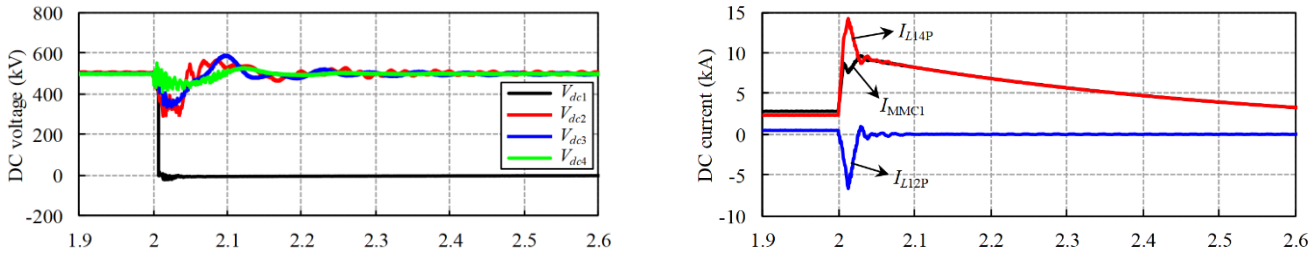
Fig. 17 (d) shows the energy absorption of CB14P and CB12N. Due to the earlier operating of CB14P, the energy absorption of CB14P rises earlier than that of CB12N. The eventual energy absorption of CB14P and CB12N are 103.91 MJ and 9.18 MJ, respectively. Therefore, the designed energy absorption of the arrester would not be less than 103.91 MJ.

D. Response to Malfunctions of Both DCCBs

A permanent pole-to-pole fault is applied at *Flt1* at 2.0 s. Assume that both CB14P and CB14N cannot operate normally. The backup protection commands CB12P and CB12N to trip at 2.007 s. Then, both positive and negative poles of MMC1 begin to block at 2.0071 s and the associated AC breakers completely trip at 2.009 s. The simulation results are shown in Fig. 18.

Fig. 18 (a) shows the DC bus voltages of the positive pole of MMC1-MMC4. The DC bus voltages of each converter can restore to 500 kV except that of MMC1. The voltage of MMC1 decreases to 0 rapidly after being blocked.

Fig. 18 (b) shows the current of MMC1 and adjacent lines. I_{L12P} is successfully interrupted by CB12P, and it reaches the peak fault current of 6.64 kA at 2.013 s. Due to the operation of CB12P, I_{L14P} begins to decrease after reaching the peak value of 14.20 kA at 2.013 s. Besides, because the energy stored in the current limiting inductor and neutral reactor of MMC1 cannot be dissipated through the arrester of CB12P, I_{L14P} and I_{MMC1} need relatively long time to dissipate to 0 through the stray circuit.



(a) DC voltages of positive pole at the DC terminal of each converter

(b) DC currents of positive pole of MMC1 and its connected lines

Fig. 18. Response to a pole-to-pole DC fault with both DCCBs failure.

VII. CONCLUSION

This paper proposes a novel mechanical DCCB with the twice-interruption capability to meet the requirement of overhead DC grid for automatic re-closure. This DCCB takes advantages of the discharging process of capacitor C_A to recharge capacitor C_S and thus achieve the second interruption capability. Taking the requirements of the representative four-terminal DC grid as an example, the parameter design methods of this DCCB are proposed. The DCCBs are designed as -320 kV pre-charged voltage of v_s, C_S of 15.5 μF, C_A of 7.6 μF, and L of 0.8 mH. It can interrupt the fault current of 25 kA within 3 ms. The breaking performance and re-closure capability of the proposed DCCB are verified in a stiff DC model.

A ±500kV four-terminal bipolar DC grid with the improved mechanical DCCB is tested. The simulation results for permanent pole-to-pole faults prove that the proposed DCCB can be well applied in the overhead DC grid. Two other simulations on the system in case of DCCBs malfunction show that the mechanical DCCB can work normally under extreme conditions and the energy absorption of the arrester would not be less than 103.91MJ. To further validate the effectiveness of the proposed DCCB, the experimental verification will be conducted in future work.

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