An Adaptive Fault Current Limiting Control for MMC and Its Application in DC Grid

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***Abstract*— This paper proposes an adaptive fault current limiting control (AFCLC) for modular multilevel converters (MMC). Without introducing extra current limiting devices, this control scheme enables fast fault current suppression during DC faults. The AFCLC will be triggered automatically once DC faults occur. By adaptively reducing the output DC voltages of MMCs, the fault current can be suppressed. Compared with the existing current limiting methods, the proposed AFCLC has a better performance on fault current limiting, since it only depends on the real-time operating condition and no fault detection delay is imposed. Firstly, the principle of the proposed AFCLC together with the mathematical analysis is disclosed. Then, the sensitivity analysis of the impact of key control parameters on the current limiting effect is investigated. Finally, the effectiveness of AFCLC is demonstrated in a four-terminal HVDC grid test model. The simulation results show that the proposed AFCLC can reduce the interrupted current and energy absorption of a DCCB from 10.39 kA and 38.24 MJ to 4.62 kA and 8.32 MJ, respectively. The simulation results also prove that the AFCLC will not affect the accuracy of the DC fault detection algorithms under DC faults.**

***Index Terms*—modular multilevel converters (MMC), DC grid, DC circuit breaker (DCCB), DC fault, HVDC transmission.**

I. Introduction

Due to the advantages of self-commutation and decoupling control of active and reactive power, the modular multilevel converter (MMC) based DC grid technology is widely recognized as a promising approach for large-scale renewable energy integration over long-distance [1]-[4]. To deal with the short-circuit faults on cables or overhead lines, the DC circuit breakers (DCCB) are adopted to isolate the faulty lines [5][6]. However, due to the low impedance of the DC grid, the fault currents rise rapidly and thus impose high interrupted current, energy absorption and breaking time requirements on the DCCBs, leading to the high cost of DCCBs. Taking the *Zhangbei* project as an example [7], it adopts 450mH current-limiting inductors to avoid blocking of MMCs during DC faults. However, the maximum fault current that needs to be interrupted is as high as 25 kA [8]. Moreover, the gross investment of DCCBs exceeds 60% of that of the converters [9], which hinders the development of the DC grid.

To reduce the cost of DCCB, a common method is to increase the inductance of DC inductors [10][11]. However, larger inductance may not only increase the total cost of the DC grid, but also result in the instability problem [12]. A feasible alternative is to use the fault current limiter to increase the impedance in the circuit [13][14].

Another option to limit the fault current is to use the controllability of converters. Many DC fault current limiting control schemes are proposed for the full-bridge MMC (FB-MMC) and the hybrid MMC based on mixed full-bridge sub-modules (FBSMs) and half-bridge sub-modules (HBSMs). Reference [15] proposed a DC fault ride-through strategy of the hybrid MMC based on the balancing control of arm capacitor energies. References [16] and [17] proposed the DC current control loop associated with the DC modulation index to decouple the AC and DC voltages. That enables the hybrid MMC to actively control the DC fault current. In [18], the feedforward DC line voltage control is used to optimize the DC current control loop and accelerate its response to DC faults. It is also validated in [19] that the full-bridge MMC can actively control the fault current, reducing the interruption energy of DCCB. Reference [20] proposed the methods of controlling the converter current or line current to zero to interrupt the fault current without implementing DCCBs for a four-terminal meshed DC grid.

The aforementioned fault current control schemes are all benefiting from the negative voltage output capabilities provided by the FBSMs. However, the utilization of FBSMs increase the cost of converters. Recalling the fault analysis in [21] and [22], the high fault current in the DC grid is mainly contributed by the SM capacitors. The fault current can be limited by altering the inserted number of SMs, thus, avoiding the discharge of SM capacitors. The fewer the number of inserted SMs during faults, the less fault current is contributed by the SM capacitors. Thus, some researches redirect to explore the potential control ability of HB-MMC for active fault current limitation. Since the HBSMs cannot output negative voltage, the fault current limiting control schemes for the full-bridge MMC cannot be directly applied to the half-bridge MMCs. A coordination scheme between HB MMCs and DCCBs was proposed in [23] to suppress the DC fault current. When DC faults happen, HB MMCs temporarily bypass all SMs to reduce the DC voltage of the converters during DCCB tripping. In [24], the DC voltage reference in the vector control is decreased to reduce the inserted number of SMs and the DC output voltage.

These approaches of reducing the DC voltages to a certain value are not applicable under all conditions. For example, in

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the case of different fault resistances, it requires different reductions in DC voltages rather than a constant given value. On the other hand, these methods need to be triggered following the command of the DC fault protection system. Due to the detection delay, the fault current rises freely during the detection period.

To overcome the defects of the existing HB MMC fault current limiting methods, this paper proposes an adaptive fault current limiting control (AFCLC) for HB MMC. By adaptively bypassing parts of SMs, this control scheme can reduce the MMC DC output voltages adjusting to different fault resistances. It can suppress the discharge of capacitors in MMC, thus reducing the fault current. Besides, the AFCLC operates immediately without waiting for the command from the protection system, thus achieving better performance on suppressing fault current.

The remainder of this paper is organized as follows. Firstly, the principle of the proposed AFCLC together with its coordination with DCCBs are introduced in Section II. Then, the mathematical analysis of the MMC with the proposed AFCLC is disclosed and the impact of the AFCLC parameters on fault current limitation performance is analyzed in Section III. The simulation of a four-terminal meshed DC grid applying the proposed AFCLC is performed in Section IV to verify its effectiveness. Besides, the performance of the system with the AFCLC is evaluated in Section V. Finally, the conclusion is drawn in Section VI.

II. The Adaptive Fault Current Limiting Control

A. Principle of the Proposed AFCLC

Referring to the existing methods of altering the number of the inserted SMs [23]-[25], the general fault current limiting concept based on DC voltage reducing is concluded in Fig. 1. It introduces a modulation factor K_M and makes the number of the inserted SMs of each arm unit become $K_M N_{p(n)}$. Therefore, the DC output voltage of the converter becomes $K_M V_{dcn}$, wherein V_{dcn} is the rated DC voltage of the DC grid. In normal operation, the modulation factor K_M equals 1.0. In fault conditions, the modulation factor K_M decreases within the range of $0 \le K_M < 1$ to reduce the inserted SM number and the DC voltage of the converter, thereby suppressing the fault current. In some existing publications [23]-[24], all the sub-modules are bypassed, indicating that K_M equals 0.

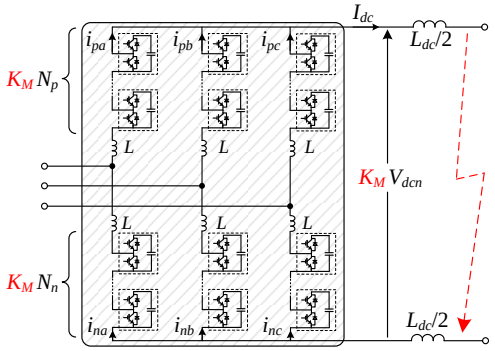


Fig. 1 Illustration of general fault current limiting methods.

In this paper, the value of modulation factor K_M is determined by the AFCLC. The diagram of the proposed AFCLC is depicted in Fig. 2, which can be divided into two parts, the adaptive current controller and the adaptive voltage limiter. K_M can be calculated as:

$$K_M = 1 - K_P\left(I_{dc} - I_{dc-set}\right) - K_D \frac{\mathrm{d}I_{dc}}{\mathrm{d}t} \quad (1)$$

where I_{dc} is the DC current; K_P and K_D are the scale and differential factors of the controller. $I_{dc\text{-}set}$ is the set point of the DC current of the converter. The schematic diagram to generate $I_{dc\text{-}set}$ is shown in Fig. 3 (a). For the converters controlling the active power, the set current $I_{dc\text{-}set}$ is calculated by the reference power. For the converters controlling the DC voltage, $I_{dc\text{-}set}$ is generated by sampling I_{dc} in a period of 100 ms. The derivative term is implemented by using a sampling element with sampling period of 200μs. Besides, a hysteresis comparator is used in the derivative term to avoid mal-operation in normal operation, as shown in the left bottom of Fig. 2. The activation threshold is normally set as half of the changing rate of the fault current ($V_{dc}/4L_{dc}$), and the return threshold is 0. The upper and lower limits of the adaptive current controller are 1.0 and K_{min}, respectively. The lower limit K_{min} is determined by the adaptive voltage limiter. The inputs of this limiter (V_{line1}, V_{line2}, …, V_{lineN}) are the DC voltages of the transmission lines that connect to the converter, as shown in Fig. 3 (b). The adaptive voltage limiter divides the minimum value of these line voltages by the rated DC voltage V_{dcn} to get K_{min}.

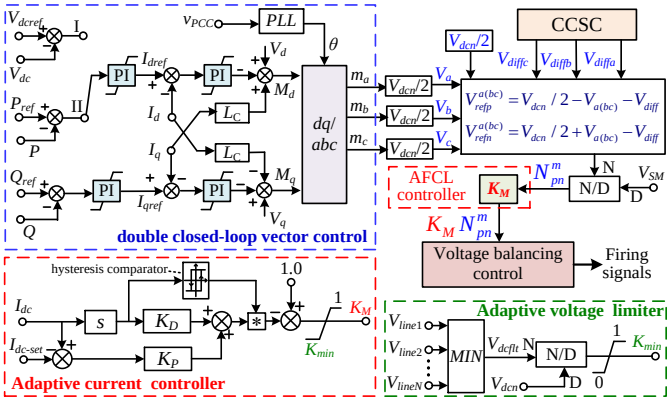
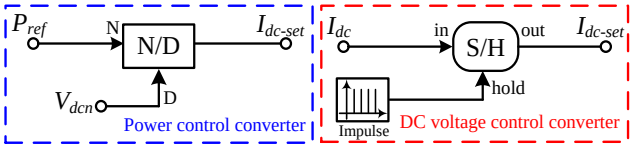
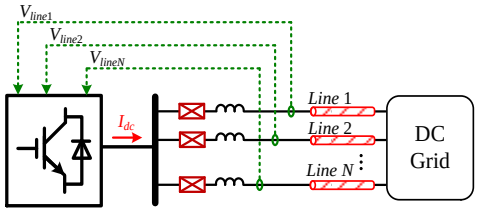


Fig. 2 The diagram of the adaptive fault current limit control.



(a) Generation of $I_{dc\text{-}set}$ for different converters



(b) Measurements of the DC current and line voltages

Fig. 3 Generation of $I_{dc\text{-}set}$ and measurement of DC line voltages

In normal operation, the DC current $I_{dc\text{-}set}$ maintains at the rated value and the DC line voltages approximately equal to V_{dcn}. Therefore, K_M remains 1.0 without interrupting the operation of the converter. Once a short-circuit fault occurs, the

DC current I_{dc} rises rapidly and the voltage of the fault line decreases immediately. Thus, K_M reduces, as shown in the equation (1), to suppress the fault current.

The sequence of DC fault protection and AFCLC triggering is shown in Fig. 4. After the fault occurs, the traveling wave induced from the fault point will propagate through the transmission lines. Once it arrives at the line terminals, the DC fault protection algorithm will be activated. Meanwhile, the line voltage V_{line12} decreases and the converter current I_{dc1} rises. Thus, the hysteresis comparator is triggered and the AFCLC is enabled. Then, the AFCLC operates to reduce the DC output voltage of MMC. Since the AFCLC starts later than the arrival of the traveling wave, it will not affect the detection of the traveling wave head. Besides, the reduction of MMC output voltage caused by the AFCLC is far slower than that resulting from the DC fault traveling wave. Therefore, the AFCLC has little effect on the traveling wave based DC fault detection algorithms.

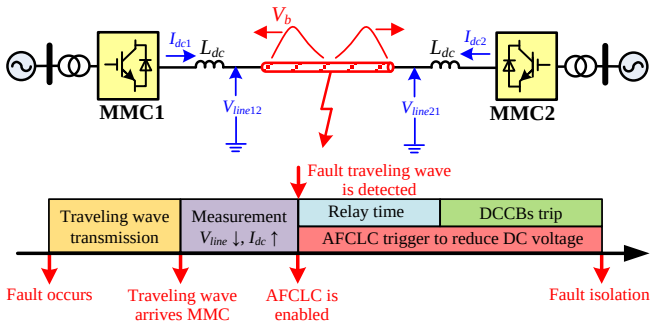


Fig. 4 The sequence of fault detection and AFCLC triggering.

B. Coordination of AFCLC and DCCBs

The flowchart of the coordination scheme between AFCLC and DCCB is shown in Fig. 5. The activation of AFCLC is independent of the fault protection system. Once a fault occurs, it is triggered automatically to limit the fault current. Due to the current limiting effect provided by the AFCLC, the fast fault protection and strict DCCB tripping requirement are mitigated. Subsequent to receiving the isolation information from DCCBs, the AFCLC exits operation, and the DC voltages will be recovered.

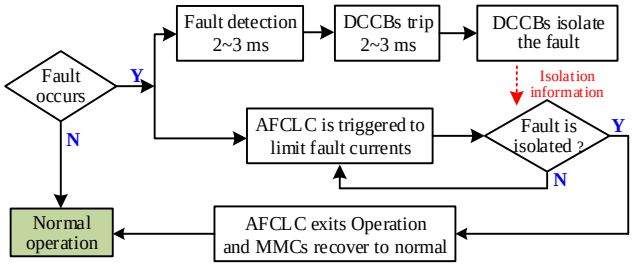


Fig. 5 Flowchart of coordination of AFCLC and DCCBs.

III. Current Limiting Principle of AFCLC

A. Fault Currents Analysis of MMC Employing AFCLC

A mathematical model is used to analyze the fault current of MMC employing the proposed AFCLC. To simplify the calculation, the equivalent arm capacitors are approximated by voltage sources. The equivalent circuit of the MMC with AFCLC is shown in Fig. 6, wherein L_{ac} and R_{ac} are the AC system inductance and resistance, respectively. L_{arm} is the arm inductance. R_{arm} is the equivalent arm resistance that equals to the sum of the switching-on resistance of the IGBTs in each arm. L_{dc} and R_{dc} are the inductance and resistance of the DC side, respectively. R_f is the fault resistance. $v_{p(n)j}$ and $i_{p(n)j}$ are voltage and current of the upper(lower) arm of phase j, and v_j is the AC grid voltage of phase j, where "j" represents phases a, b, c.

According to the superposition theorem, the equivalent circuit shown in Fig. 6 can be further divided into a DC equivalent circuit and an AC equivalent circuit. These equivalent circuits are shown in Fig. 7 and Fig. 8, where $v_{dc\text{-}j}$ and $v_{ac\text{-}j}$ are the DC and AC components of arm voltages, respectively. The expressions of $v_{dc\text{-}j}$ and $v_{ac\text{-}j}$ are as follows:

$$\begin{cases} v_{dc-j} = v_{pj} + v_{nj} = K_M V_{dcn} \\ v_{ac-j} = \dfrac{v_{pj} - v_{nj}}{2} = K_M V_{arm} \cos\left(\omega t + \alpha_j\right) \end{cases} \tag{2}$$

where V_{arm} and α_j are the amplitude and initial phase of $v_{ac\text{-}j}$, respectively.

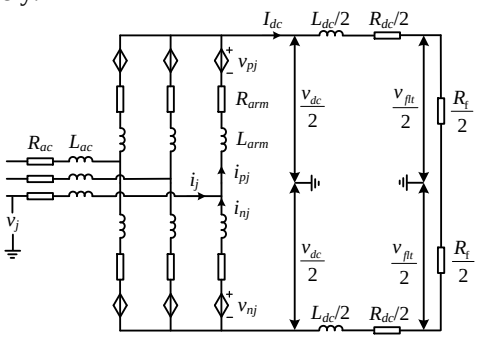


Fig. 6 Equivalent circuit of MMC employing the AFCLC.

1) DC current

According to the DC equivalent circuit shown in Fig. 7, the differential equation of I_{dc} is as follows:

$$\frac{\mathrm{d}I_{dc}}{\mathrm{d}t} + \frac{R_{eq1}}{L_{eq1}} I_{dc} = \frac{v_{dc-j}}{L_{eq1}} = \frac{K_M V_{dcn}}{L_{eq1}} \tag{3}$$

where L_{eq1} and R_{eq1} are the total inductance and resistance of the DC equivalent circuit and are given as:

$$L_{eq1} = L_{dc} + \frac{2}{3} L_{arm}, R_{eq1} = R_{dc} + R_f + \frac{2}{3} R_{arm} \tag{4}$$

Combining equation (1) and (3), we have

$$\frac{\mathrm{d}I_{dc}}{\mathrm{d}t} + \frac{R_{eq1} + K_P V_{dcn}}{L_{eq1} + K_D V_{dcn}} I_{dc} = \frac{\left(1 + K_P I_{dc-set}\right) V_{dcn}}{L_{eq1} + K_D V_{dcn}} \tag{5}$$

Assuming a fault occurs at t = 0. The solution of (5) is

$$I_{dc} = \left(I_{dc-set} - I_s\right) e^{-\frac{t}{\tau_{dc}}} + I_s \tag{6}$$

where I_s is the steady-state DC current of I_{dc}. τ_{dc} is the time constant of the DC equivalent circuit.

$$I_s = \frac{\left(1 + K_P I_{dc-set}\right) V_{dcn}}{R_{eq1} + K_P V_{dcn}} \tag{7}$$

$$\tau_{dc} = \frac{L_{eq1} + K_D V_{dcn}}{R_{eq1} + K_P V_{dcn}} \tag{8}$$

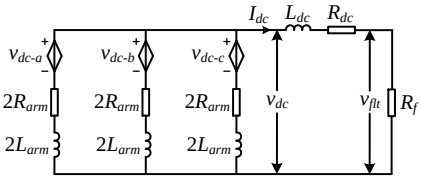


Fig. 7 DC equivalent circuit of MMC.

From equations (6)-(8), it is obvious that the proposed AFCLC can limit the DC fault current to a low steady-state value and decrease the current rising rate. The steady-state current is related to K_P. The current rising rate is associated with K_P and K_D. The DC fault current can be suppressed by configuring the reasonable parameters of the AFCLC.

2) AC side and arm currents

The equivalent resistance and inductance of the AC equivalent circuit shown in Fig. 8 are

$$R_{eq2} = R_{ac} + \frac{R_{arm}}{2},\ L_{eq2} = L_{ac} + \frac{L_{arm}}{2} \tag{9}$$

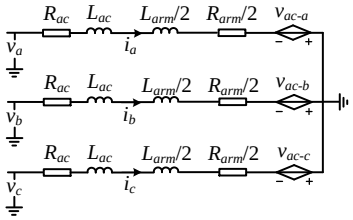


Fig. 8 AC equivalent circuit of MMC.

Assuming the amplitude and initial phase of v_j are respectively V_{ac} and β_j, which can be obtained by measuring the operation of the system, we have

$$v_j = V_{ac}\cos\left(\omega t + \beta_j\right) \tag{10}$$

According to the equivalent circuit shown in Fig. 8 and the expressions of $v_{ac\text{-}j}$ and v_j, the differential equation of the AC side current i_j is as follows

$$\frac{\mathrm{d}i_j}{\mathrm{d}t} + \frac{R_{eq2}}{L_{eq2}} i_j = \frac{K_M V_{arm}}{L_{eq2}}\cos\left(\omega t + \alpha_j\right) + \frac{V_{ac}}{L_{eq2}}\cos\left(\omega t + \beta_j\right) \tag{11}$$

According to equations (1) and (6), the modulation factor K_M is represented as:

$$K_M = 1 + K_P\left(I_{dc-set} - I_s\right) + \left(K_D/\tau_{dc} - K_P\right)\left(I_{dc-set} - I_s\right)e^{-\frac{t}{\tau_{dc}}} \tag{12}$$

Combining equations (11) and (12), the differential equation of i_j can be solved. Assuming a fault occurs at t=0, the AC current after fault occurrence can be expressed as:

$$i_j(t) = i_j^+(t) + \left[i_j^-(0) - i_j^+(0)\right]e^{-\frac{t}{\tau_{ac}}} \tag{13}$$

where "-" denotes the steady-state operating condition before fault occurrence and "+" denotes the operating condition after fault occurrence. $\tau_{ac} = L_{eq2}/R_{eq2}$, is the time constant of the AC equivalent circuit. The expressions of i_j^- and i_j^+ are

$$i_j^- = \frac{V_{ac}\cos\left(\omega t + \beta_j - \delta\right)}{\sqrt{R_{eq2}{}^2 + \left(\omega L_{eq2}\right)^2}} + \frac{V_{arm}\cos\left(\omega t + \alpha_j - \delta\right)}{\sqrt{R_{eq2}{}^2 + \left(\omega L_{eq2}\right)^2}} \tag{14}$$

$$\begin{aligned} i_j^+ = {} & I_1\cos\left(\omega t + \beta_j - \delta\right) + I_2\cos\left(\omega t + \alpha_j - \delta\right) \\ & + I_3\cos\left(\omega t + \alpha_j - \varphi\right) \end{aligned} \tag{15}$$

where

$$\begin{cases} \tan\delta = \dfrac{\omega L_{eq2}}{R_{eq2}} \\ \tan\varphi = \dfrac{\omega L_{eq2}}{R_{eq2} - L_{eq2}/\tau_{dc}} \end{cases} \tag{16}$$

$$I_1 = \frac{V_{ac}}{\sqrt{R_{eq2}^2 + \left(\omega L_{eq2}\right)^2}} \tag{17}$$

$$I_2 = \frac{\left[1 + K_P\left(I_{dc-set} - I_s\right)\right]V_{arm}}{\sqrt{R_{eq2}^2 + \left(\omega L_{eq2}\right)^2}} \tag{18}$$

$$I_3 = \frac{\left(K_D/\tau_{dc} - K_P\right)\left(I_{dc-set} - I_s\right)V_{arm}e^{-\frac{t}{\tau_{dc}}}}{\sqrt{\left(R_{eq2} - L_{eq2}/\tau_{dc}\right)^2 + \left(\omega L_{eq2}\right)^2}} \tag{19}$$

According to the relationship between DC current, AC currents and arm currents, the expressions of arm currents are:

$$\begin{cases} i_{pj} = \dfrac{I_{dc}}{3} + \dfrac{i_j}{2} \\ i_{nj} = \dfrac{I_{dc}}{3} - \dfrac{i_j}{2} \end{cases} \tag{20}$$

The detailed expressions can be obtained by substituting equations (6) and (13) into (20).

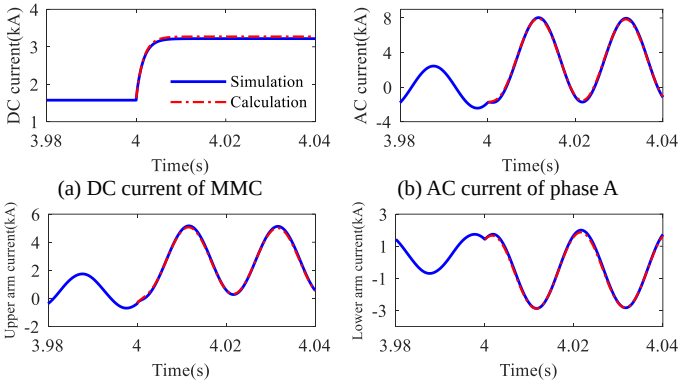
B. Verification of Effectiveness of the Proposed AFCLC

To illustrate the effectiveness of the proposed AFCLC and verify the mathematical analysis presented in the previous sub-section, a tested MMC converter is built in PSCAD. The parameters of the test circuit are shown in Table I. The parameters of the converter are the same as that of MMC1 in Table II. A permanent metallic short-circuit fault is applied at 4 s at the DC terminal of the converter. Besides, to verify the effect of the AFCLC in a longer time scale, it is assumed that the MMC does not block and the DCCB does not trip during the fault. The parameters of the AFCLC are set as: K_P = 0.6, K_D = 0.0003.

Table I Parameters of circuit of one-terminal MMC system

Parameter	Symbol	Value
Fault resistance	R_f	0.01 Ω
AC resistance	R_{ac}	0.1 Ω
AC inductance	L_{ac}	0.1 H
DC resistance	R_{dc}	2 Ω
DC inductance	L_{dc}	0.2H

Fig. 9 shows the fault current characteristics of the MMC employing the proposed AFCLC. The blue solid line shows the simulation results and the calculation results shown with a dash-dotted line are obtained by equations (6), (13) and(20). As can be seen, the results show a good agreement, which verifies the mathematical analysis presented in the previous sub-section. The DC current increases to the maximum value of 3.22 kA within 6ms and then stays steady, which illustrates the effectiveness of the proposed AFCLC.



(a) DC current of MMC (b) AC current of phase A

(c) Upper arm current of phase A (d) Lower arm current of phase A

Fig. 9 Fault currents of the MMC employing the proposed AFCLC.

C. *Analysis of the Arm Currents during Fault Limit Control*

The proposed AFCLC also has effect on reducing the arm current during fault limit control. The equations (6), (13) and (20) can be used to calculate the arm current with the AFCLC. As for the case of no current-limiting control, the expression of the DC current can be obtained by setting K_P and K_D to be zero:

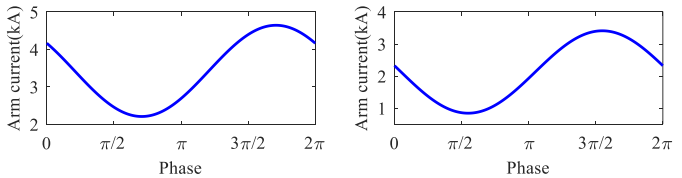
$$I_{dc-normal} = \left(I_{dc-set} - \frac{V_{dcn}}{R_{eq1}} \right) e^{-\frac{R_{eq1}}{L_{eq1}}t} + \frac{V_{dcn}}{R_{eq1}} \tag{21}$$

Due to the effect of the vector control of the MMC, the AC components in arm voltages ($v_{ac\text{-}j}$) has little change during fault limit control. Therefore, the AC current without current limiting control does not change after fault occurs. It can be expressed as:

$$i_{j-normal}(t) = i_j^-(t) \tag{22}$$

Similar to Section III.B, a single-terminal MMC is used to calculate the maximum arm current. The parameters of the converter are the same as that of MMC2 in Table II. The parameters of the AFCLC are set as the same as that of MMC2 in Table III. A short-circuit fault is applied at 4 s and the DCCBs tripped at 4.006 s.

The arm currents would reach the peak value when fault is interrupted by the DCCBs at 4.006 s. Since the arm currents are depending on the voltage phases, it is required to cover the range of (0, 2π) to obtain the largest arm current during fault isolation. The arm currents at 4.006 s versus varying phases are calculated, as shown in Fig. 10. It can be observed that the AFCLC reduce the maximum arm current from 4.64 kA to 3.41 kA. Although the AFCLC increase the amplitude of the AC component of the arm current, the DC component are significantly reduced. That results in the reduction in arm current. According to [8], the current of 3.41 kA is acceptable in HVDC applications.



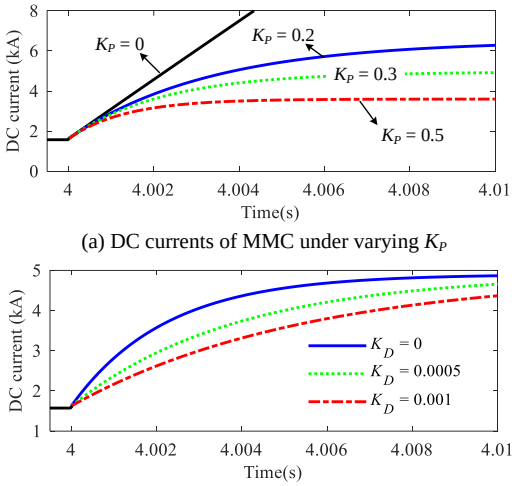
(a) No control (b) AFCLC

Fig. 10 Calculation results of the arm current at 4.006 s under different control schemes.

D. *Sensitivity Analysis of Controller Parameters*

According to equations (6)-(8), the characteristics of the DC current are associated with the controller parameters of the AFCLC. To study this relationship, the DC currents of MMC under varying parameters of the AFCLC are shown in Fig. 11.

Fig. 11(a) shows the DC currents of MMC under varying scale factor K_P. The differential factor K_D identically equal to 0. If K_P = 0, the DC current rises rapidly without limit. Increasing the scale factor K_P can significantly suppress the fault current. Fig. 11(b) shows the DC currents under varying differential factor K_D. The scale factor K_P identically equal to 0.3. It can be observed that increasing the differential factor K_D can reduce the rate of current rise. Increasing K_P and K_D is beneficial to fault current limitation, but may bring about a larger decrease of DC voltages of MMCs during the fault, which means a larger power interruption and a lower AC terminal voltage. There is a trade-off between limiting fault current and mitigating power interruption.

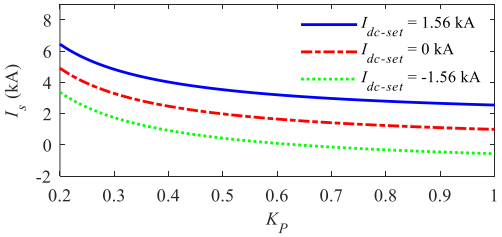


(a) DC currents of MMC under varying K_P

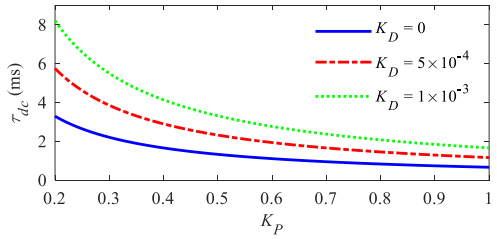
(b) DC currents of MMC under varying K_D

Fig. 11 DC currents versus varying parameters of AFCLC.

The sensitivity analysis of the AFCLC controller parameters is shown in Fig. 12. Fig. 12 (a) shows the steady-state current I_s versus scale factor K_P. It can be observed that increasing the scale factor K_P results in reduced steady-state current I_s. Besides, decreasing the DC current set-point $I_{dc\text{-}set}$, which represents the operation state of the converter, also causes a reduction in steady-state current I_s. Fig. 12 (b) shows the time constant τ_{dc} versus scale factor K_P. It can be observed that decreasing the scale factor K_P results in the increase of the time constant τ_{dc}. Besides, increasing the differential factor K_D also leads to an increase in the time constant τ_{dc}. Generally, K_P is designed to achieve the I_s of less than $2.5|I_{dc\text{-}set}|$, and K_D is designed to ensure the τ_{dc} of less than 3 ms (half of the time from fault occurrence to DCCB opening).



(a) Steady-state current I_s versus scale factor K_P



(b) Time constant τ_{dc} versus scale factor K_P

Fig. 12 Relationships between the characteristics of DC current and controller parameters.

IV. Verification of the AFCLC in DC Grid

To further verify the effectiveness of the proposed AFCLC, a simulation of a four-terminal HVDC grid employing the proposed AFCLC is performed in PSCAD. The structure of this DC grid is shown in Fig. 13. All converters adopt the half-bridge MMC topology. The detailed parameters of the converters are given in Table II. The overhead lines are modeled with the frequency-dependent phase model provided by PSCAD, and the resistance in per unit length of the overhead lines is 0.011Ω/km. The inductance of the current limiting reactor L_{dc} is 200mH. The DCCBs in this system adopts the hybrid DCCB topology proposed by ABB. The operating time of the ultra-fast disconnector in the DCCB is 3ms. The relay time of the fault detection algorithm is 3ms [26][27].

MMC1, MMC2 and MMC3 operate in active and reactive power control mode to regulate power at 500, 1000 and -500 MW, respectively. MMC4 operates in DC voltage control mode to maintain the DC voltage at 640kV. According to the normal operating state of the converters and equations (7)-(8), the parameters of the AFCLC are set as shown in Table III to achieve the desired steady-state DC current and time constant.

To investigate the effectiveness of the proposed AFCLC in the DC grid, a permanent short-circuit fault (F_{L23}) is applied at the head of overhead line 23, as shown in Fig. 13. The fault occurs at 4 s and the fault resistance is 0.01 Ω. There are three schemes being performed for comparison. Scheme 1 represents that the converters operate without current-limiting control (No control). Scheme 2 represents that all converters bypass all SMs once the fault has been detected (Bypass). Scheme 3 represents that the converters adopt the proposed AFCLC. The simulation results are given from Fig. 14 to Fig. 21.

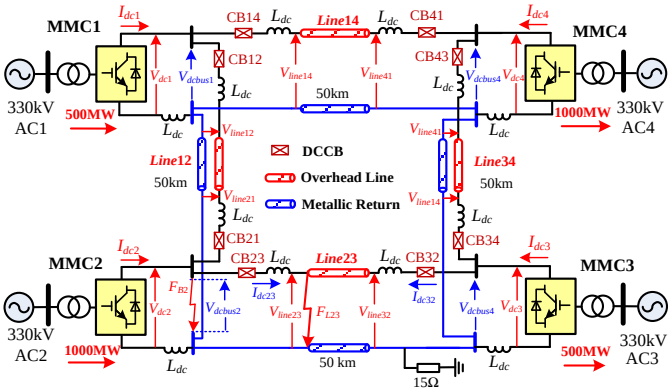


Fig. 13 The structure of the four-terminal DC grid.

Table II Parameters of the Converters in DC Grid

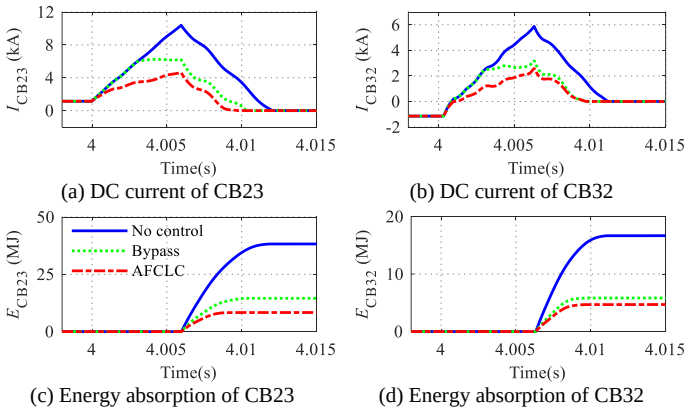
Parameters	MMC1	MMC2	MMC3	MMC4
Rated capacity (MVA)	500	1000	500	1000
Rated DC voltage (kV)	640	640	640	640
AC voltage (kV)	330	330	330	330
AC inductance (mH)	0.1	0.2	0.05	0.05
Transformer ratio	330/352	330/352	330/352	330/352
Transformer Reactance (p.u.)	0.15	0.15	0.15	0.15
Arm inductance (mH)	44	88	44	88
Submodule capacitance (mF)	6.5	12	6.5	12
Submodule number	200	200	200	200
DC inductance (mH)	200	200	200	200
Grounding pole resistance (Ω)	None	None	None	15

Table III Parameters of the AFCLC

Parameters	MMC1	MMC2	MMC3	MMC4
K_P	0.363	0.509	0.357	0.279
K_D	4.28×10^{-4}	8.66×10^{-4}	4.11×10^{-4}	1.76×10^{-4}
I_s (kA)	3.5	3.5	2	2
τ_{dc} (ms)	3	3	3	3

A. Comparisons of Interruption Capacity of DCCBs

Fig. 14 shows the interrupted currents and absorbed energy of CB23 and CB32. The blue solid line shows the simulation results of Scheme 1. The green dotted line shows the simulation results of Scheme 2. The red dash-dotted line shows the results of Scheme 3. It can be observed that the proposed AFCLC can immediately operate after fault occurrence to suppress the rising fault current, whereas the method of bypassing needs to wait for the delay time caused by the fault detection algorithm. Therefore, the AFCLC can further decrease the fault currents and reduce the interruption capacity than the method of bypassing. Taking CB23 as an example, the AFCLC can reduce the interrupted current from 10.39 kA (No control) and 6.21 kA (Bypass) to 4.62 kA, and decrease the absorbed energy from 38.24 MJ (No control) and 14.52 MJ (Bypass) to 8.32 MJ. For CB32, the AFCLC can reduce the interrupted current from 5.88 kA (No control) and 3.20 kA (Bypass) to 2.61 kA, and decrease the absorbed energy from 16.66 MJ (No control) and 5.83 MJ (Bypass) to 4.69 MJ. This reduction caused by the AFCLC would allow the technical requirements of the DCCBs to be designed at a lower rating, thus reducing the investment of the DCCB. These simulation results demonstrate one of the advantages of the proposed AFCLC.



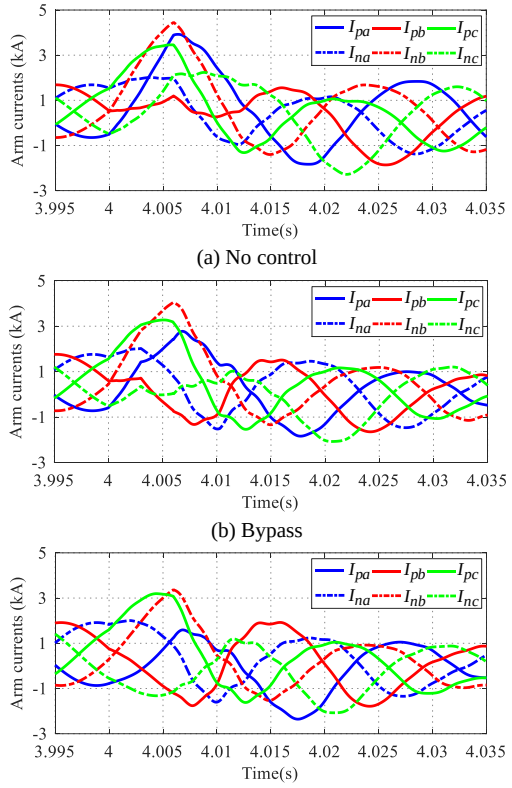
(a) DC current of CB23 (b) DC current of CB32

(c) Energy absorption of CB23 (d) Energy absorption of CB32

Fig. 14 Influence of AFCLC on the technical requirements of DCCBs.

B. *Comparison of Arm Currents*

Fig. 15 shows the three-phase arm currents of MMC2. The peak values of arm currents in Scheme 1 and Scheme 2 are 4.45 kA and 4.02 kA, respectively, whereas the maximum arm currents in Scheme 3 is decreased to 3.36kA. In Scheme 1, the increase of the arm currents mainly results from a rapidly rising DC current. In Scheme 2, since the converter bypasses all SMs, it is equivalent to a short-circuit fault for the AC system. Hence, the contribution of AC currents to the arm currents increases. While the proposed AFCLC can not only reduce the DC current, but can also maintain a certain AC voltage to avoid the excessive rise of AC currents as well as the arm currents. These simulation results illustrate another advantage of the proposed AFCLC.



(a) No control

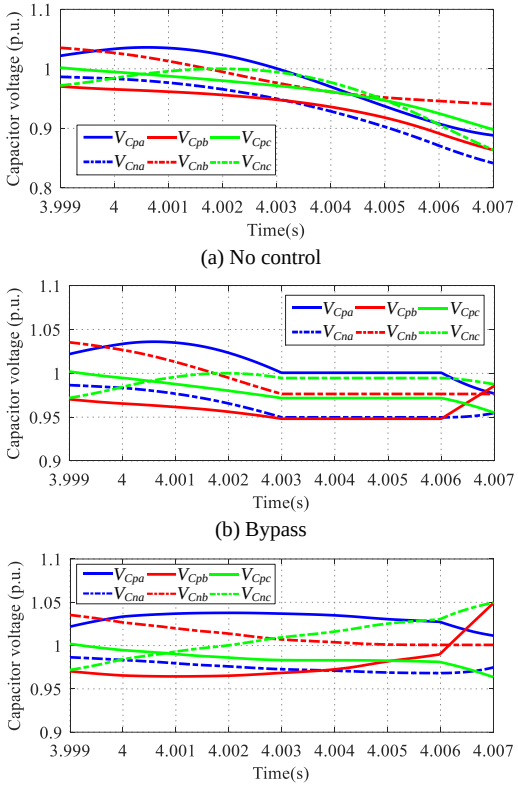
(b) Bypass

(c) AFCLC

Fig. 15 Comparison of three-phase arm currents in MMC2.

C. *Comparison of Capacitor Voltages*

Fig. 16 shows the average SM capacitor voltages of MMC2. The fault occurs at 4.000s, and the DCCBs trip at 4.006s. In Scheme 1, the SMs are inserted into the fault circuit. Therefore, the capacitor voltages drop significantly after 4.000s. In Scheme 2, all SMs are bypassed after 4.003s. Hence, the capacitor voltages maintain constant between 4.003s and 4.006s. In Scheme 3, since only part of SMs are inserted after the fault occurs, the capacitor voltages remain in the range of 0.95-1.05 p.u. The average SM capacitor voltages of each arm at 4 s and 4.006 s are shown in Table IV At 4.006s, the capacitor voltages in Scheme 3 are larger than that in Scheme 1 and 2. These simulation results prove the effect of the AFCLC on suppressing the discharge of the SM capacitors.



(a) No control

(b) Bypass

(c) AFCLC

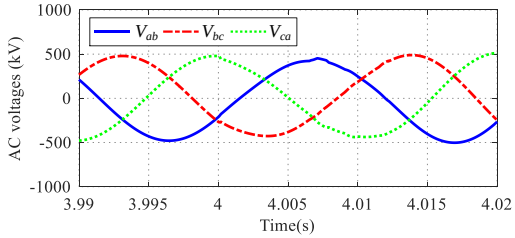
Fig. 16 Comparison of average SM capacitor voltages of each arm in MMC2.

Table IV Average SM capacitor voltages of each arm at 4 s and 4.006 s

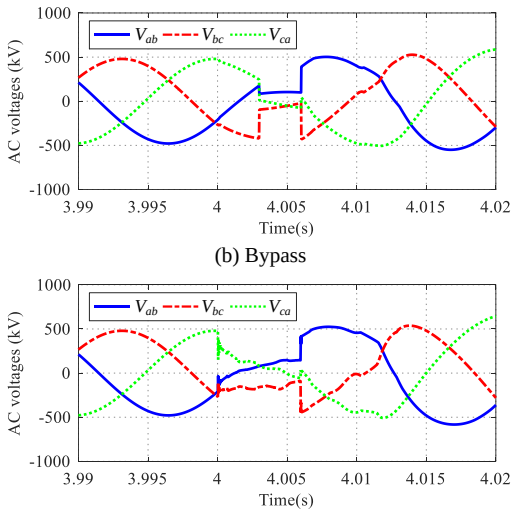
Time	4.000 s	4.006 s		
Scheme		No control	Bypass	AFCLC
V_{Cpa} (p.u.)	1.034	0.908	1.001	1.027
V_{Cna} (p.u.)	0.983	0.871	0.950	0.968
V_{Cpb} (p.u.)	0.966	0.891	0.948	0.991
V_{Cnb} (p.u.)	1.027	0.946	0.976	1.001
V_{Cpc} (p.u.)	0.995	0.925	0.971	0.981
V_{Cnc} (p.u.)	0.984	0.906	0.995	1.031

D. *Comparison of AC Side Voltages*

The AC side voltages of MMC2 under different control schemes are shown in Fig. 17. In Scheme 1, since the converter does not take any current limiting methods, the AC side voltages are hardly affected. In Scheme 2, all SMs in MMC2 are bypassed after fault is detected at 4.003s. Hence, the AC side voltages drop sharply and even approach 0 (still have some residual inductor voltage). In Scheme 3, the AC side voltages begin to drop after the fault occurs at 4.000s. Since not all SMs are bypassed, the AC side voltage can maintain a certain level. This AC side voltage that is not completely reduced to 0 can prevent excessive AC current from flowing into the converter.



(a) No control



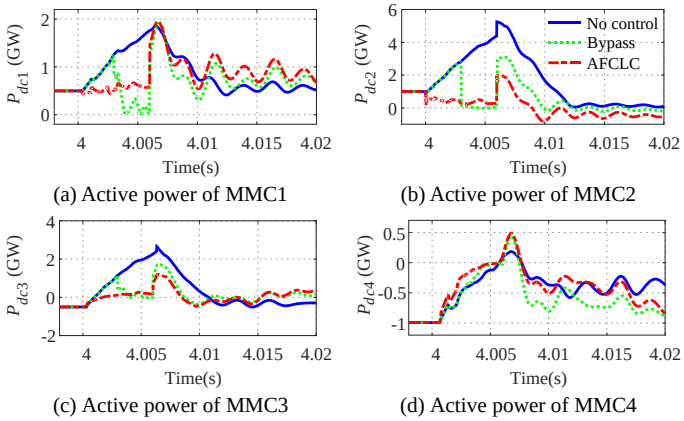
(b) Bypass

(c) AFCLC

Fig. 17 Comparison of AC side voltages in MMC2.

E. Comparison of Transient Performance

Fig. 18 shows the transmitted active power of all converters in the DC grid. In Scheme 1, the active power constantly increases until the fault current is interrupted at 4.006 s. In Scheme 2, the power rises at the same rate before 4.003 s and decreases to almost 0 between 4.003 and 4.006s. In Scheme 3, the active power fluctuation is less severe compared with Scheme 1. Moreover, different from Scheme 2, the active power does not decease to 0 during fault interruption. It can be concluded that the AFCLC can reduce the active power fluctuation compared with the other schemes.

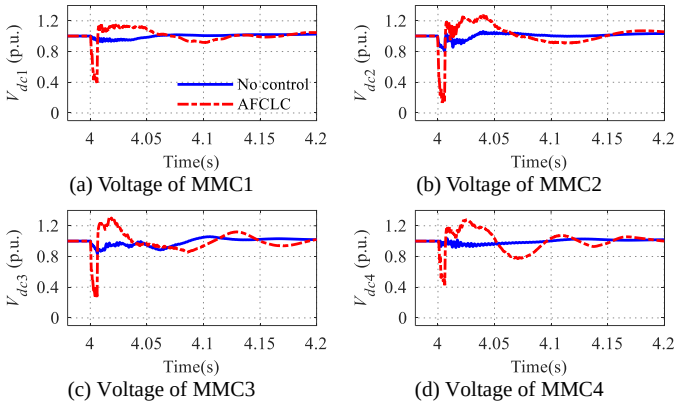


(a) Active power of MMC1 (b) Active power of MMC2

(c) Active power of MMC3 (d) Active power of MMC4

Fig. 18 Comparison of active power of all converters.

Fig. 19 shows the DC voltages of all converters in the DC grid. Since the three curves would overlap in this time scale and the comparison of Scheme 1 and 3 is more significant, the simulation results of Scheme 2 are not involved. It can be observed that the AFCLC increases the fluctuation range and prolongs the restoration of DC voltages. In Scheme 1, the DC voltage fluctuation is not severe. The restoration times of V_{dc1}, V_{dc2}, V_{dc4} are within 100 ms, while that of V_{dc3} is about 150 ms. In Scheme 3, the DC voltages are adaptively reduced by the AFCLC during fault to suppress the fault current. After the fault line is isolated at 4.006 s, the DC voltages begin to recover and the maximum voltage does not exceed 1.3 p.u. The restoration times of the DC voltages are increased to 200ms. However, the fluctuation range of 0.2-1.3 p.u. and the restoration time of 200 ms are still acceptable for the operation of the DC grid [23][24].

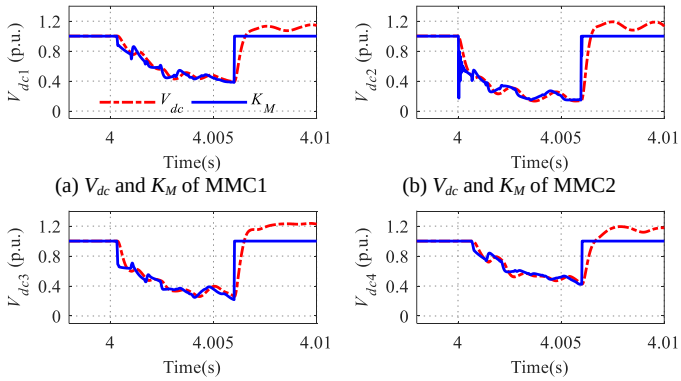


(a) Voltage of MMC1 (b) Voltage of MMC2

(c) Voltage of MMC3 (d) Voltage of MMC4

Fig. 19 Comparison of DC voltages of all converters.

Fig. 20 shows the DC voltages and modulation factors of all converters in Scheme 3. It can be observed that both curves are identical between 4.000s and 4.006s. The decrease of K_M can effectively reduce the DC voltages of converters. After 4.006s, the AFCLC is disabled for a period to avoid affecting the restoration of the system. According to the reclosing time of the DCCBs [8], the disable time is designed as 300ms.

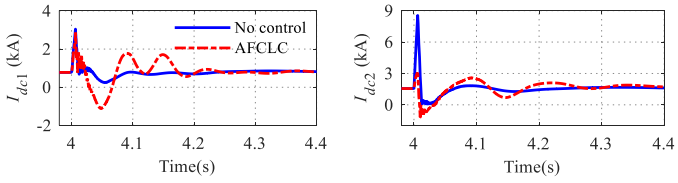


(a) V_{dc} and K_M of MMC1 (b) V_{dc} and K_M of MMC2

(c) V_{dc} and K_M of MMC3 (d) V_{dc} and K_M of MMC4

Fig. 20 Comparison of DC voltages and modulation factors in Scheme 3.

Fig. 21 shows the DC currents of all converters in the DC grid. Similarly, only the simulation results of Scheme 1 and Scheme 3 are displayed for comparison. It can be observed that before the fault is isolated, the currents of MMC1 and MMC4, which are remote from the fault point, are similar in both situations. The maximum currents of MMC2 and MMC3 in Scheme 3 is significantly reduced compared to that in Scheme 1, due to the effect of the AFCLC. Since MMC2 and MMC3 are the major contributors to fault currents, this reduction results in the decrease of currents in CB23 and CB32, as shown in Fig. 14. During the restoration process, the AFCLC also increases the fluctuation range and restoration time of DC currents. The fluctuation range of I_{dc4} is of 3.3-1.8 kA in Scheme 3. In Scheme 1, the restoration times of I_{dc1}, I_{dc2}, I_{dc3} are 200 ms, while that of I_{dc4} is 300ms. In Scheme 3, the restoration times of DC currents are increased to 300 ms.



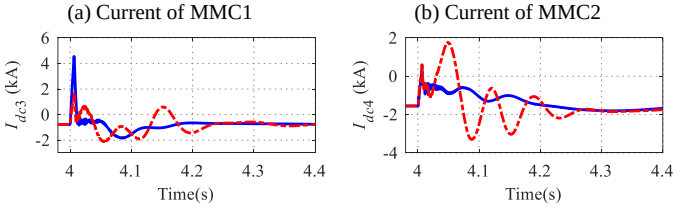


Fig. 21 Comparison of DC currents of all converters.

V. Performance Evaluation

A. Response to Change of Operating Conditions

To prove that the proposed AFCLC would not affect the operation of the DC grid in case of operating conditions changing, a certain step change of DC power is applied in MMC2. The reference value of the active power of the MMC2 increases from 1000 MW to 1100MW at 4 s, and then decreases to 900 MW at 5 s. The simulation results are shown from Fig. 22 to Fig. 23.

Fig. 22 shows the DC voltages and modulation factors of all converters in case of operating conditions change. It can be observed that the lower limits of the AFCLC of all converters are no less than 0.98 p.u. Since the current change rate is unable to trigger the hysteresis comparator, the modulation factors of all converters are maintained at 1.0. These simulation results illustrate that the AFCLC does not false trigger in this situation.

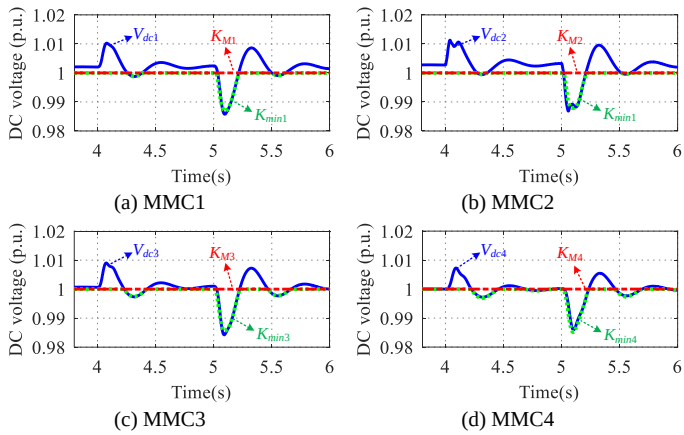
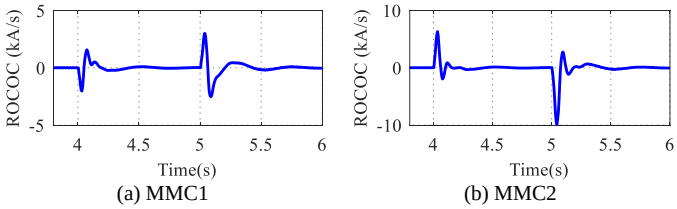


Fig. 22 DC voltages and modulation factors in case of operating conditions change.

Fig. 23 show the rate of change of current (ROCOC) of all converters. It can be observed that the ROCOC of all converters are less than 10 kA/s. The activation threshold of the hysteresis comparator is set as half of the changing rate of the fault current ($V_{dc}/4L_{dc}$ = 800 kA/s). Since the ROCOC of all converters are far smaller than this threshold, the AFCLC is not triggered in this situation.



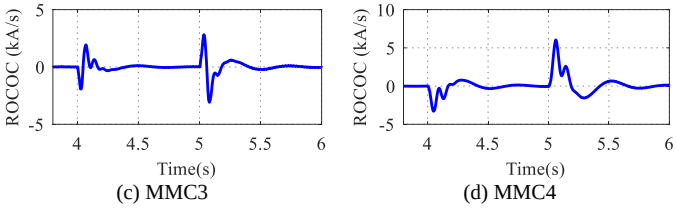


Fig. 23 ROCOC of all converters in case of operating conditions change.

B. Influence on Fault Detection

Since the proposed AFCLC operates immediately to reduce the DC voltages of converters after fault occurrence, it may interfere with the fault detection algorithms. Therefore, it is necessary to study the impact of the AFCLC on fault detection. In this paper, a fault detection method of measuring the rate of change of voltage (ROCOV), which is proposed in [11], is employed in the test system to analyze the influence of the AFCLC. The trigger threshold of fault detection is set as -2.0 kV/μs.

1) Faults at Overhead Line

A permanent short-circuit fault is applied at the head of overhead line 23 (F_{L23}) at 4s. Fig. 24 and Fig. 25 show the ROCOV of the DC bus and line voltages. The blue solid line shows the results of the case that converters operate without any current-limiting control, while the red dash-dotted line shows the simulation results of the proposed AFCLC. It can be observed that the results are almost identical. Due to the effect of the AFCLC on reducing the DC voltage of converter, the ROCOV of DC bus voltages has a slight reduction compared with that in case of *No control*. The measured ROCOV exceeds -2 kV/μs only for the internal faults, i.e., the ROCOV of V_{line23} and V_{line32}, as shown in Fig. 25 (c)-(d). These results indicate that the ROCOV can effectively identify internal and external faults. And the AFCLC has little effect on the ROCOV of the line and DC bus voltages.

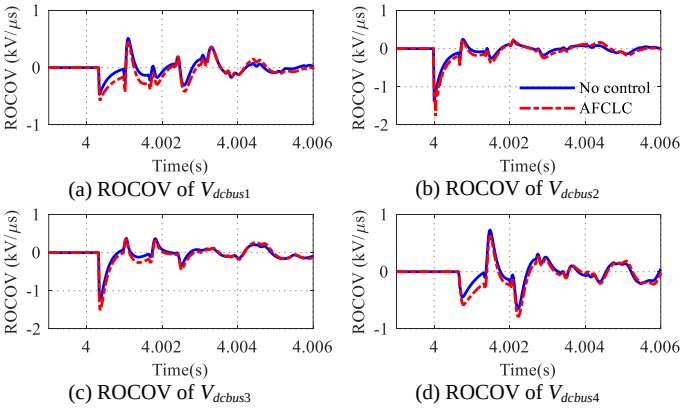
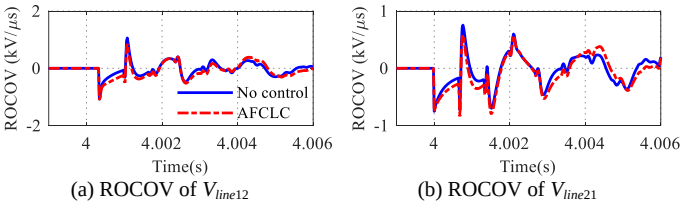
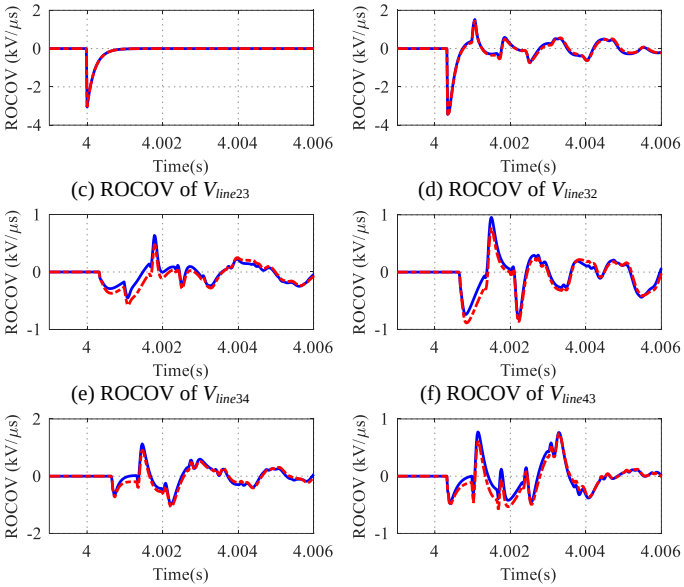


Fig. 24 ROCOV of the DC bus voltages in the case of F_{L23} fault.



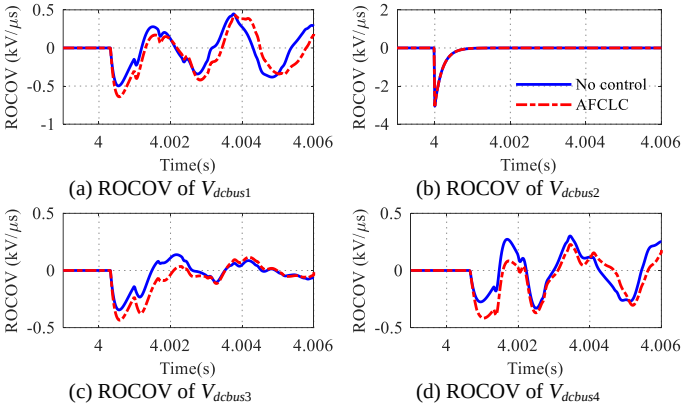


(c) ROCOV of V_{line23} (d) ROCOV of V_{line32}
(e) ROCOV of V_{line34} (f) ROCOV of V_{line43}
(g) ROCOV of V_{line41} (h) ROCOV of V_{line14}

Fig. 25 ROCOV of the line voltages in the case of F_{L23} fault.

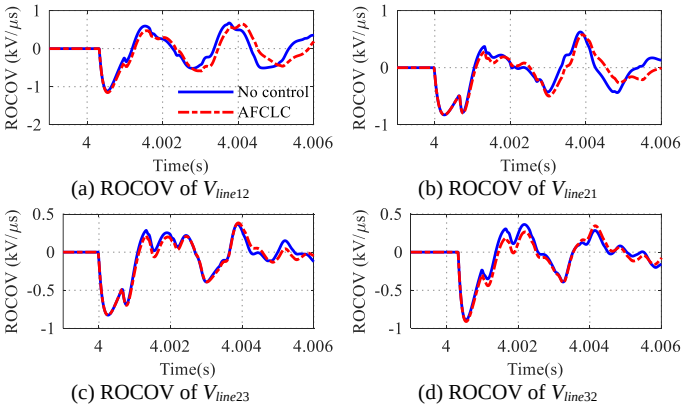
2) Faults at DC Bus

A permanent short-circuit fault is applied at the DC bus of MMC2 (F_{B2}) at 4s. Fig. 26 and Fig. 27 show the ROCOV of the DC bus and line voltages. It can be observed that results under AFCLC comply well with the other. Due to the effect of the AFCLC, the ROCOV of non-fault DC buses decrease a little compared with those in case of *No control*. As can be seen, only the measured ROCOV of V_{dc2} exceeds -2 kV/μs and all the other ROCOVs are larger than -2 kV/μs. These results indicate that the AFCLC will not cause false detection.

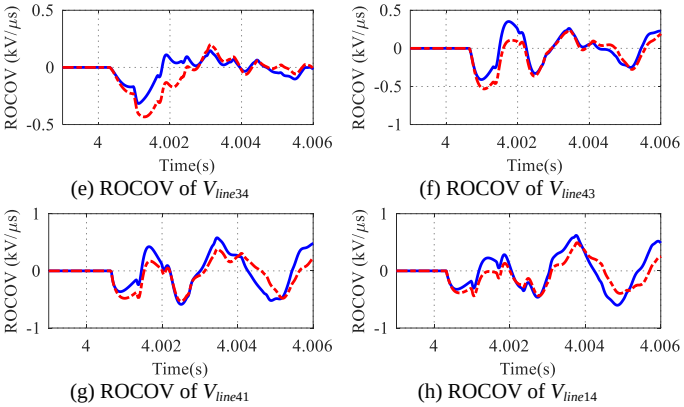


(a) ROCOV of V_{dcbus1} (b) ROCOV of V_{dcbus2}
(c) ROCOV of V_{dcbus3} (d) ROCOV of V_{dcbus4}

Fig. 26 ROCOV of the DC bus voltages in the case of F_{B2} fault.



(a) ROCOV of V_{line12} (b) ROCOV of V_{line21}
(c) ROCOV of V_{line23} (d) ROCOV of V_{line32}



(e) ROCOV of V_{line34} (f) ROCOV of V_{line43}
(g) ROCOV of V_{line41} (h) ROCOV of V_{line14}

Fig. 27 ROCOV of the line voltages in the case of F_{B2} fault.

VI. Conclusion

This paper proposes an adaptive fault current limiting control to limit the fault current of HB-MMC without adding supplementary devices. This control scheme can adaptively reduce the voltages of MMC to limit the fault current according to different fault conditions. The AFCLC is triggered immediately once a fault occurs and its activation is independent of the DC fault protection system. The theoretical analysis of the AFCLC verifies its effect on fault current limiting and reducing the current rise rate. It is also shown that increasing the parameters of the AFCLC means a better effect on suppressing fault current.

A four-terminal HB-MMC DC grid is simulated to further investigate the effectiveness of proposed AFCLC. The simulation results under DC short-circuit fault shows that compared with normal control, the AFCLC can reduce the interrupted current and energy absorption of a DCCB from 10.39 kA and 38.24 MJ to 4.62 kA and 8.32 MJ, respectively. Besides, the AFCLC also has the advantage of preventing overcurrent in arms during the fault. The simulation results of operating conditions changing validate that the AFCLC would not be falsely triggered under normal operation. The comparisons of ROCOVs between the normal control and the AFCLC shows that the AFCLC will not affect the fault detection accuracy under DC faults.

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