Enhanced Modular Multilevel Converter for HVdc Applications: Assessments of Dynamic and Transient Responses to ac and dc Faults

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***Abstract*—This paper describes the operating principles and theoretical relationships that underpin the modelling and control system of the enhanced modular multilevel converter (EMMC). A full-scale model of a point-to-point HVdc link that employs EMMCs is used to examine its performance during normal operation in all four quadrants, and resiliency to symmetrical and asymmetrical ac and dc faults. Results of exhaustive simulation studies reveal that the improved ac and dc power qualities, which are achieved by incorporation of a few full-bridge cells into the arms of conventional half-bridge modular multilevel converter (HB-MMC) with medium-voltage cells to create the EMMC do not affect its ac and dc fault ride-through capability nor its dynamics during normal operation as active and reactive power set-points being varied. In addition, a variant of the EMMC is proposed, in which the number of full-bridge cells to be added into the arms of HB-MMC could be increased to offer bespoke features beyond that explicitly defined in original vision of the EMMC, such as reduced dc voltage operation during pole-to-ground dc fault, and potential extension of fault clearance times in multi-terminal HVdc grids. Moreover, the validity of the new variant has been confirmed using results obtained from high-fidelity HVdc link models developed in EMPT-RV platform, in which the EMMCs are replaced by the proposed variant.**

***Index Terms*—Hybrid multilevel converter, HVdc, faults**

I. Introduction

Present generations of multilevel voltage source converter high-voltage direct current (VSC-HVdc) transmission systems have received a universal acceptance of the power industry due to the high efficiency and power quality at both ac and dc sides, and internal fault management during cell failure. The latter feature is becoming increasingly important with rapid growth in the power handling and dc operating voltage of VSC-HVdc transmission systems, and the prominent role they expect to play in smart and multi-terminal dc grids.

Generally, the modular multilevel converter (MMC) can be realized using unipolar cells (such as the half-bridge (HB) cell), symmetrical bipolar cells (such as the full-bridge (FB) cell) and asymmetrical bipolar cells (such as the hybrid cell, which is equivalent to series connection of HB and FB cells) [1]. In these categories of the MMC, the cell type determines the MMC characteristics such as control range, resiliency to dc faults and semiconductor losses [2], [3]. Between the two established implementations, the MMCs with large number of cells per arm, where the switching devices and capacitor of each cell block sized for relatively low voltage of 1.5kV-2.8kV [4] have been exhaustively researched and adopted in many projects offered from different manufacturers of HVdc systems. Even though such an approach leads to an increase in overall system complexity, it has numerous practical advantages such as superior ac and dc power quality and allowing continuous operation by bypassing faulted cells. While the alternative approach in which the MMC uses low number of medium-voltage cells [5] significantly simplifies the overall system implementation, it introduces a few disadvantages. Firstly, it requires large number of series-connected press-pack IGBTs (which is extremely challenging and not fully mastered by most of major manufacturers), and secondly, the use of medium-voltage cells leads to relatively large errors in the synthesis of the common-mode voltage, which appear as high-frequency ripples in dc side voltage and current, lead to the requirement of small dc side filters [6].

In the last two decades, numerous hybrid converter topologies have been proposed by industry and academia. Most of these hybrid converters were motivated by the performance optimization such as the trade-offs between resiliency to dc faults, efficiency and footprint.

The typical MMC arm is realized by series connection of identical cells. In recent years, many cell topologies are proposed, mostly aim to improve specific aspects of MMC performance, which include control range, efficiency, fault resiliency, redundancy and complexity [1]. These cells can be categorised as unipolar, symmetrical and asymmetrical bipolar cells. Unipolar cells can generate two-level or multilevel output voltages, e.g.HB and neutral-point-clamped (NPC) [1], [7] cells. Therefore, the MMCs that employ unipolar cells have mostly similar attributes and limitations to the HB-MMC. Cells that produce equal number of positive and negative voltage levels are referred as symmetrical bipolar cell, e.g. FB and five-level cross-connected cells [1]. Hence, the MMCs with symmetrical bipolar cells offer similar functionalities and operating range to the FB-MMC, and more likely to suffer from high semiconductor loss. A cell that generates unequal number of positive and negative voltage levels such as hybrid cell is referred as asymmetrical bipolar cell. Therefore, the MMCs with asymmetrical bipolar cells are mostly to inherent the features of the conventional mixed cells MMCs with 50% HB cells and 50% FB cells. In summary, unipolar cells have reduced number of semiconductors in the conduction path, hence, leads to efficient MMCs compared to bipolar cells [1]. In contrast, MMCs with asymmetrical bipolar cells offer controlled operation over wide range of unipolar dc voltage from rated to zero, including fault current control during dc

short circuit [1]. Whereas the MMCs with symmetrical cells inherent all the attributes of the MMCs with asymmetrical bipolar cells, and offer additional features such as bipolar dc voltage operation that facilitates power reversal by dc voltage or current [8]. Therefore, the MMCs with symmetrical bipolar cells are best fit to operate alongside line commutated converters (LCCs) in future transnational dc grids. [9], [10].

Broadly, the hybrid converters could be divided into two groups. The first group is often referred to as hybrid MMC. The majority of the hybrid converters which belong to this group retain most of the characteristics of the MMC, and they perform optimization primarily by mixing different types of cells to create arbitrary asymmetrical bipolar arms with custom capabilities. Amongst hybrid MMCs, the mixed cell modular multilevel converter (MC-MMC) is the most attractive topology because it retains many of the attributes of the conventional MMC, while it permitting delivery of customized features, i.e. trade-offs between control range, semiconductor losses and resiliency to dc faults [11]–[13]. The second group of hybrid converters mixes the basic building blocks of MMC such as the HB and FB chain-links or whole MMC power circuits with so called director switches (which are formed by series connected thyristors or IGBT) [14], [15]. Although the latter group compromises system modularity compared to the former, they offer a range of advantages, from nearly doubling the power extraction compared to that of the MMC, to bipolar dc voltage operation with semiconductor losses similar to that of the HB-MMC [16]–[19].

An enhanced modular multilevel converter (EMMC) proposed in [6] aims to improve the quality of ac and dc waveforms of cascaded two-level converter (CTL) which represents alternative implementation of the MMC that uses reduced number of medium-voltage cells [5]. In particular, dc side voltage, current ripples and ac output voltage harmonic content. The EMMC adds a small number of FB cells rated for 1.5 kV to 2.5 kV into the arms of the CTL or MMC that uses a reduced number of medium-voltage HB cells (each cell is typically rated for 16kV to 20kV). Detailed steady-state studies presented in [6] have shown that the EMMC dramatically improves ac and dc power quality through its unique multiplication feature, which is instituted by the nested multilevel concept.

However, detailed assessments of the EMMC dynamic operation over all four quadrant and, ac and dc fault responses are not yet investigated. Therefore, the first part of this paper presents brief review of the EMMC operating principle, modelling and control. A comprehensive assessment is included, demonstrating EMMC's performance during normal and abnormal conditions such as: dynamic operation of the P-Q envelope, responses to symmetrical and asymmetrical ac faults, reduced dc voltage operation, and response to pole-to-pole dc short circuit fault.

The second part of this paper presents a new topological extension of the EMMC, known as EMMC$_0$. In EMMC$_0$ both HB and FB chain-links contribute to fundamental voltage synthesis, while the FB chain-link blocking voltage directly determines the control range, resiliency to dc faults and efficiency. To date, FB-MMC and MC-MMC are not realized through CTL structure because it is practically challenging to use the negative polarity of the MV FB cells. Therefore, the proposed EMMC$_0$ could open the way for practical realization of special breeds of customized MC-MMC, in which the relatively simplicity of control, power circuit, protection, and high quality of ac and dc side waveforms can be retained. To support the above claims, an EMMC$_0$ simulation demonstrates the operation of 50% of the rated dc voltage, when the proportion of HB and FB chain-links blocking voltage is 75% and 25% respectively.

The paper is organized as follows: Section II describes the operation principles and modelling of the EMMC. Section III present illustrative simulation results of steady, transient and faulty state. Section IV presents an additional variant of an EMMC. Sections V and VI provide high-level summary and conclusion with highlights of the main findings of this work.

II. The Enhanced Modular Multilevel Converter

A. Operating principle

Each arm of the EMMC in Fig. 1 consists of high-voltage and low-voltage chain-links HVCL and LVCL respectively. Each HVCL could be constructed from unipolar cells (such as HB cells), symmetrical bipolar cells (such as FB cells) or a combination of unipolar and symmetrical bipolar cells, while the LVCL must be constructed from symmetrical bipolar cells so that their capacitor voltage balancing can be achieved. In the base case design of EMMC, each HVCL must be sized to block the full dc link voltage V_{dc} as in conventional MMC, while the LVCL must be sized to block half the rated voltage of a single cell of the HVCL [6]. The EMMC uses the HVCL rated at full pole-to-pole dc voltage to synthesize the fundamental voltage with major voltage steps $V_{C_{HVCL}}$ as described in (1).

$$V_{C_{HVCL}} = \frac{V_{dc}}{N_{HVCL}} \tag{1}$$

where N_{HVCL} is the number of cells in the HVCL. In contrast, the LVCL of each arm that consists of cascaded FB cells with combined blocking voltage of half of that of one cell of the

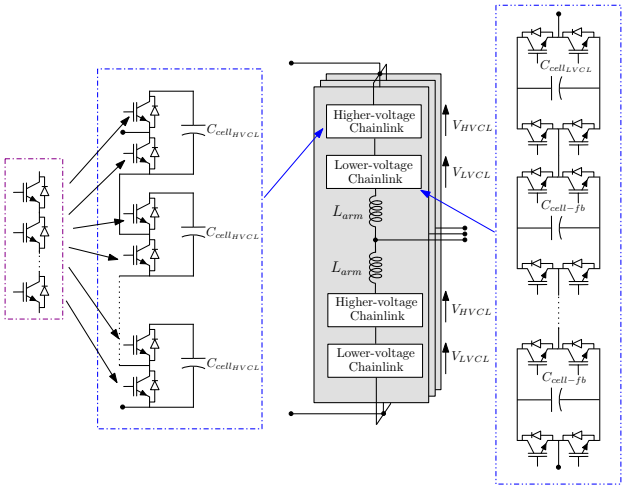

Fig. 1. EMMC circuit topology

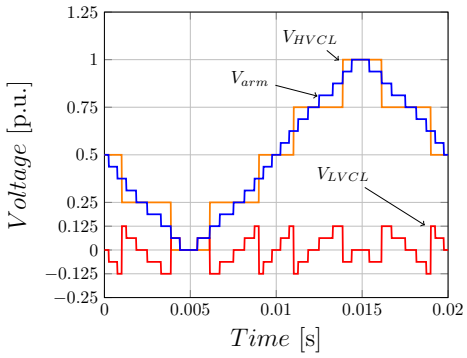

Fig. 2. EMMC internal synthesized voltage

HVCL, synthesises a multilevel waveform with minor voltage steps $V_{C_{LVCL}}$ as described in (2).

$$V_{C_{LVCL}} = \pm\frac{V_{C_{HVCL}}}{2N_{LVCL}} \tag{2}$$

Therefore, each arm voltage of the EMMC represents the algebraic sum of the approximate fundamental voltage that the HVCL generates and the harmonic voltage that the LVCL injects.

Notice that the HVCL facilitates stepped transition between the major voltage levels through intermediate voltage levels separated by minor voltage steps.

Fig. 2 illustrates the ideal synthesis of the total arm voltage and voltages of the HVCL and LVCL, with all voltages being normalized to dc voltage V_{dc}. Fig. 2 shows that the HVCL of each EMMC arm synthesizes a stepped approximation of the sinusoidal fundamental voltage V_{HVCL} with a major voltage step equal to 0.25 p.u. (1), whilst the LVCL of each arm synthesizes a bipolar voltage V_{HVCL} with positive and negative peaks of ± 0.125 p.u. (2), and a minor voltage step of $\frac{0.125}{2}$ p.u. as described in (3).

$$V_{cell_{LVCL}} = \pm\frac{V_{dc}}{2N_{LVCL}\cdot N_{HVCL}} = \pm\frac{V_{cell_{HVCL}}}{2N_{LVCL}} \tag{3}$$

where N_{LVCL} is the number of cells in the LVCL. The total arm voltage V_{arm} is the algebraic sum of the voltages V_{HVCL} and V_{LVCL}, synthesized by the HB and FB chain-links respectively. The minor voltage step seen in V_{arm} is derived directly from the voltage produced by a single LVCL cell $V_{cell_{LVCL}}$. The positive and negative peaks of V_{LVCL} in each arm are limited to $\pm\frac{1}{2}V_{cell_{HVCL}}$, which suggests that the minimum blocking voltage of the FB chain-link is $\frac{1}{2}V_{cell_{HVCL}}$.

The number of voltage levels each arm the of EMMC can generate can be expressed in general as in (4).

$$N_{EMMC} = 2\cdot N_{HVCL}\cdot N_{LVCL} + 1 \tag{4}$$

The HVCL and LVCL cell capacitance may be sized similar to a conventional MMC as described in (5).

$$C_{cell} = \frac{\cdot N\cdot S\cdot E}{3\cdot V_{dc}^2} \tag{5}$$

where N is the number of cells of HVCL or LVCL, S is the apparent power, E is the cell energy stored.

The relationship between the HVCL and LVCL cell capacitance is described in (6).

$$C_{cell_{LVCL}} = C_{cell_{HVCL}}\cdot\frac{N_{LVCL}}{2} \tag{6}$$

The total capacitance of the LVCL chain-link is equal to half the total HVCL cell capacitance. The widely accepted method for MMC cell capacitor sizing based on stored energy or inertia ranging from 30-40kJ/MW and +/-10% capacitor voltage ripple is adopted for HVCL [5], and (5) and (6) guarantee that the cell capacitor voltage ripple will not exceed $\pm 10\%$.

B. EMMC Modelling and Analysis

This section uses a generalized switching function to model the EMMC arms.Considering the EMMC arm depicted in Fig. 3. The cell capacitor currents $i_{cell_{HVCL,i}}(t)$ and $i_{cell_{LVCL,y}}(t)$ in the i^{th} and k^{th} HB and FB cells of the HVCL and LVCL can be expressed in terms of arm current $i_{arm}(t)$ and their respective switching functions as:

$$i_{cell_{HVCL,i}}(t) = S_{x_i}(t)\cdot i_{arm} \tag{7}$$

$$i_{cell_{LVCL,k}}(t) = (S_{1k}(t) - S_{3k}(t))\cdot i_{arm} \tag{8}$$

where $S_{xi}(t)$ is the HB cell switching function, and becomes 1 or 0 when the cell voltage is included or bypassed respectively. Similarly for the FB cell switching functions, $S_{1k}(t)$ and $S_{3k}(t)$ become 1 or 0 when the cell voltage is included or bypassed. From (7) and (8), the cell capacitor voltage dynamics of each HB and FB cell respectively can be described by:

$$\frac{dV_{C_{HVCL,i}}(t)}{dt} = \frac{i_{cell_{HVCL,i}}(t)}{C_{cell_{HVCL}}} \tag{9}$$

$$\frac{dV_{C_{LVCL,k}}(t)}{dt} = \frac{i_{cell_{LVCL,k}}(t)}{C_{cell_{LVCL}}} \tag{10}$$

The output voltages of the arbitrary HB and FB cells are:

$$V_{cell_{HVCL,i}}(t) = S_{xi}(t)\cdot V_{C_{HVCL,i}}(t) \tag{11}$$

$$V_{cell_{LVCL,i}}(t) = (S_{1k}(t) - S_{3k}(t))\cdot V_{C_{LVCL,i}}(t) \tag{12}$$

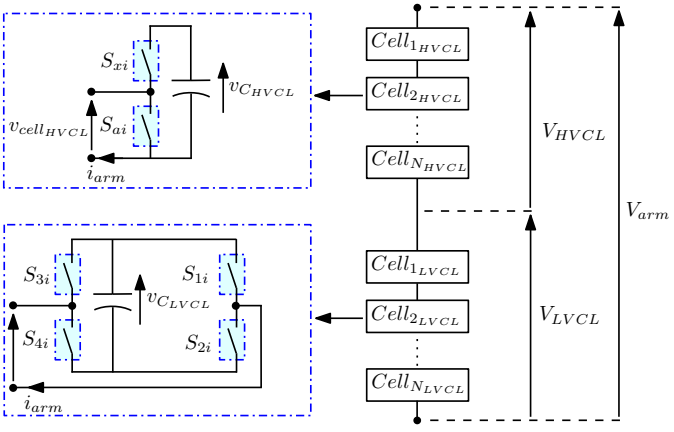

Fig. 3. Compact depiction of EMMC arm.

The total voltages that the HVCL and LVCL generate are:

$$V_{HVCL}(t) = \sum_{i=1}^{N_{HVCL}} V_{cell_{HVCL,i}}(t) \tag{13}$$

$$V_{LVCL}(t) = \sum_{k=1}^{N_{LVCL}} V_{cell_{LVCL,k}}(t) \tag{14}$$

The total arm voltage is:

$$V_{arm}(t) = V_{HVCL}(t) + V_{LVCL}(t) \tag{15}$$

Based on (7) to (15), the full switching function model of the EMMC is developed, in which the switching functions correspond to the gating signals of the switch S_{x_i} in each HB cell of the HVCLs, and to gating signals of the switches S_{1_k} and S_{3_k} in each FB cells of the LVCLs. Considering upper and lower arms of phase a as examples, the voltage of the HVCL of the arbitrary arm in (13) can be expressed as:

$$V_{HVCL,j}(t) = \\ = V_{HVCL} \cdot \text{round}\left[\frac{1}{2} N_{HVCL}\left(1 + (-1)^y \sin(\omega t + \delta)\right)\right] \tag{16}$$

where $j = u$ and $y = 1$ for the upper arm, and $j = l$ and $y = 2$ the lower arm. The expression (16) represents the stepped approximation of the arm voltage to be synthesized by the medium-voltage HB cells of the HVCLs, which is predominantly the dc component in addition with the fundamental voltage and harmonics. Despite the presence of dc and fundamental components in both arm current and voltage, the dc power produced in each arm due to dc components balances the average ac power from the fundamental current and voltage, hence the HVCL of the arms exchange zero average power between ac and dc side.

Similarly, the voltage of the LVCL of arbitrary arms in (14) can be rewritten as:

$$V_{LVCL,j}(t) = V_{LVCL}\Bigg[\frac{1}{2} N_{HVCL}\big(1 + (-1)^y sin(\omega t + \delta)\big) - \\ - \text{round}\big[\frac{1}{2} N_{HVCL}\big(1 + (-1)^y sin(\omega t + \delta)\big)\big]\Bigg] \tag{17}$$

whilst (17) represents the harmonic voltage to be injected into each arm by the FB cells of the LVCL in order to generate sinusoidal output voltage. Theoretically, since (17) comprises harmonic voltages only, its interaction with fundamental and dc components of the arm current will not produce average or active power, as described:

$$\overline{P}_j = \frac{1}{T}\int_0^T V_{LVCL_j}(t) \cdot i_{arm_j}(t) dt = 0 \tag{18}$$

To maintain the FB cell capacitor voltage fixed at set-point requires an additional mechanism to draw small active power to feed the power losses to be incurred as a result of current flow in semiconductor switches and passive elements. It is worth noting that the switching function is selected to model the EMMC it facilitates accurate simulation of full-scale systems, while retaining detailed inter-cell and inter-arm, inter-phase dynamics intact [6]. Each cell is simplified and described by two-state switching function that possesses 1 or 0 states as shown in (11) and (12). The synthesis of arm voltages V_{arm} reflects the cell capacitor voltage imbalance and dynamics as described in (15). Therefore, it is highly efficient for large HVdc networks where observation of cell-level transient phenomena is required. Fig. 4 illustrates an EMMC arm in which the HVCL and LVCL are modelled using switching functions.

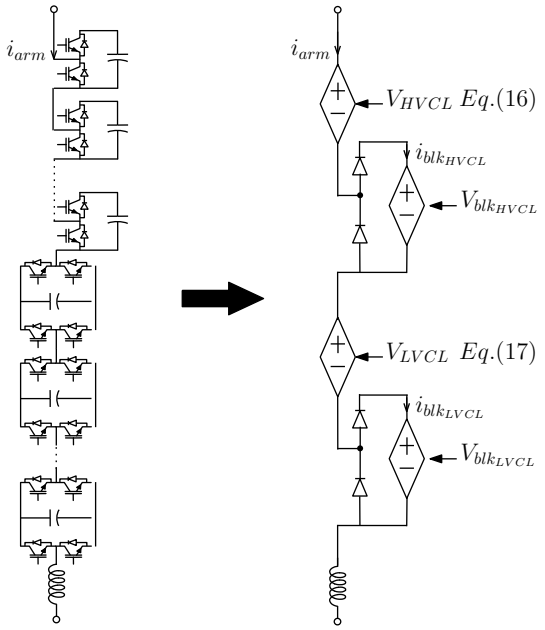

Fig. 4. Equivalent representations of arm components.

It is worth emphasizing that the LVCL in each EMMC arm must be bypassed during three-phase ac and dc faults to avoid exposure to high currents and excessive over-voltages across its capacitors and switching devices.

C. EMMC control

Synthesis of the output ac voltage, currents, common-mode and circulating currents in the EMMC are similar to that in the conventional MMC [20]. Fundamentally, maintaining balanced or constant cell capacitor voltages necessitates zero energy exchange with the ac or dc sides as described in (19) and (20).

$$E_{HVCL_{j,k}} = \int_0^T \Big(V_{HVCL} \cdot i_{arm_{j,k}}(t)\Big) dt = 0 \tag{19}$$

$$E_{LVCL_{j,k}} = \int_0^T \Big(V_{LVCL} \cdot i_{arm_{j,k}}(t)\Big) dt = 0 \tag{20}$$

Therefore, the dc bias of the LVCL voltage V_{HVCL} is manipulated in order to ensure that its FB cell capacitor voltages exchange zero net energy or active power with the HB cells of the HVCL and ac side. For ensuring zero energy exchange, the FB cell capacitor voltages of the LVCL are actively controlled according to the average cell energy that exist in HVCL. Notice that the active controllers that regulate the dc voltages of the LVCL inject small dc voltages to interact with the dc

component of the arm currents in order to produce small active power needed to sustain constant FB capacitor voltages of the LVCLs and feed their losses. Since the LVCLs only operate between major voltage steps of the cells of the HVCLs, the vertical and horizontal capacitor voltage controllers are incorporated to ensure the energy balance among the HVCLs to all phase legs. The vertical controller intends to mitigate the risk of dc offsets that may arise in the ac side voltages and currents as a result of unequal voltage distribution across upper and lower arms The horizontal controller aims to prevent the dc circulating currents between the phase legs. As in conventional MMC, both vertical and horizontal voltage controllers of the EMMC modify the common-mode components of the arm voltages, and therefore they have no negative influence in the ac side waveforms which are driven by the differential-mode components [21]. Fig. 5 shows the overall control system of the EMMC that includes the following:

- Outer controllers, active, reactive powers and dc voltage
- Inner positive and negative current controllers in the double synchronous reference frame that define ac components of modulating signals
- Horizontal and vertical capacitor voltage balancing controllers that modify common-mode components of the arm modulating signals

Fig. 6 shows the normalisation of the controllers which synthesising the reference voltages for the HVCL and LVCL.

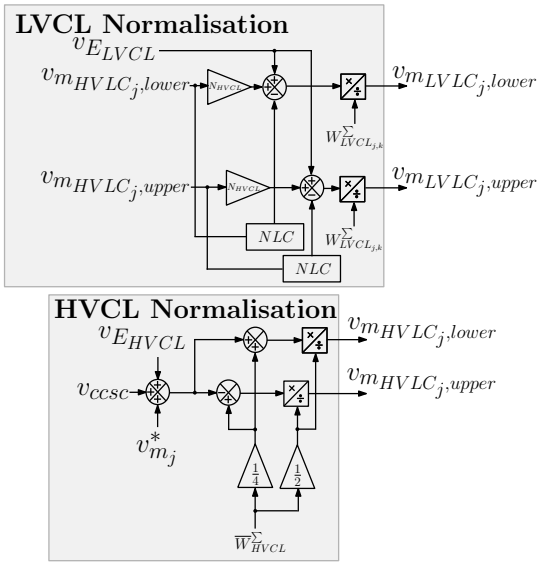

Fig. 6. Controller normalisation for HVCL and LVCL

The cell capacitor voltages of the HVCL and LVCL in each arm of the EMMC are balanced using two independent tolerance band capacitor voltage balancing methods [22].

III. Benchmark EMMC-HVdc system

This section presents a number of illustrative simulations that aim to demonstrate the operation of the EMMC and its control systems, during normal and abnormal operating conditions. These examples employ a two-terminal HVdc link simulated in EMTP-RV platform with time-step of $5\mu s$, and shown in Fig. 7. The HVdc link under investigation consists of two EMMCs which are configured as symmetrical monopoles

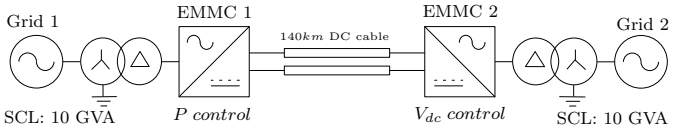

Fig. 7. HVdc test network

TABLE I
EMMC-HVdc specifications

Parameter	Value
Apparent power	1045 MVA
DC voltage	640 kV
Transformer reactance	12 %
Arm inductance	12 %
Cell capacitance inertia constant	35 $\frac{kJ}{MVA}$
Number of cells per HVCL	40
Number of cells per LVCL	5
HVCL voltage	640 kV
LVCL voltage	8 kV
Converter line-to-to-line ac voltage	320 kV
Grid line-to-line ac voltage	400 kV

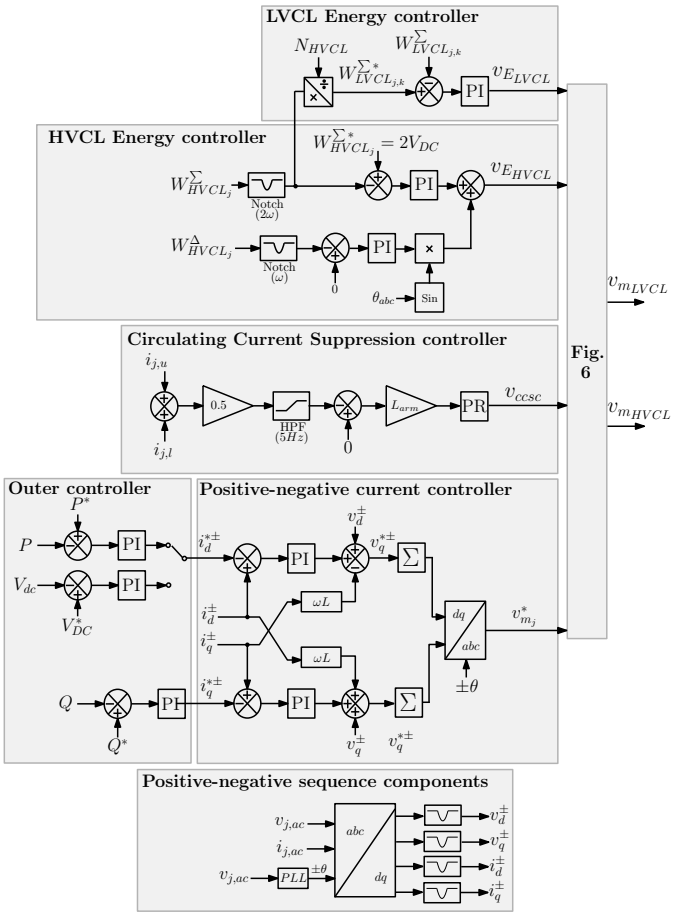

Fig. 5. EMMC control structure

and connected together via dc cables modelled as wideband frequency dependent cable model. EMMC1 controls active and reactive powers, while EMMC2 regulates dc voltage and reactive power. The ac grids are assumed to be a strong with with short circuit ratio SCR=10. Table I shows the rating and design specification of the HVdc converters.

A. Demonstration of improved ac and dc sides power quality

Fig. 8 displays examples of steady-state results for the EMMC1 that controls active power. These waveforms obtained when the EMMC was initially operating with both HVCLs and LVCLs active, and at t = 1 s, the LVCLs are bypassed, converting the EMMC to a conventional HB-MMC.

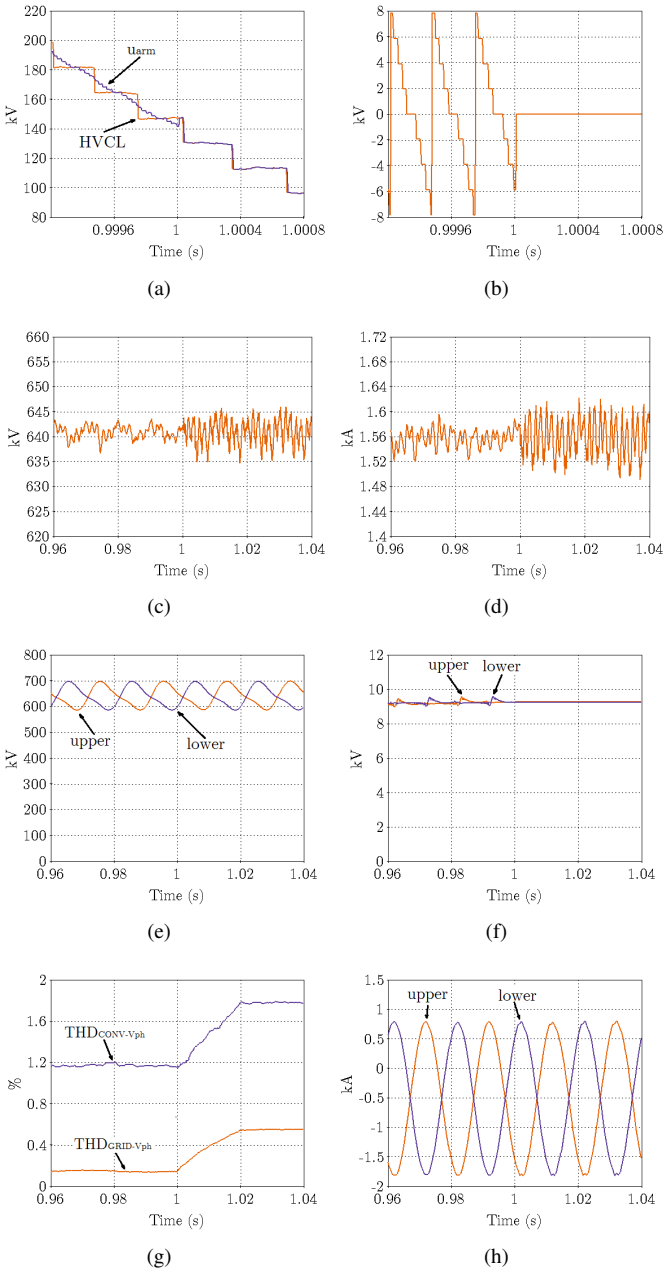

Fig. 8. LVCL bypass: (a) HVCL and total arm voltages, (b) LVCL voltage, (c) dc voltage, (d) dc current, (e) EMMC1 HVCL total capacitor voltages, (f) EMMC1 LVCL total capacitor voltages, (g) Grid and converter side phase voltage THD, (h) EMMC1 arm currents

Sample plots of the arm voltage, and sum of the upper and lower arm capacitor voltages in Fig. 8(a) and (b) indicate when the EMMC transits to HB-MMC mode. The power quality of the dc voltage and current, and arm and phase voltages clearly deteriorate after bypass of the LVCLs, as shown in Figs. 8(e) to (h). The deterioration in the harmonic content and dv/dt of the ac-side waveforms can be observed in the sudden change in the quality of the stepped approximation of the sinusoidal component of the arm voltage before and after bypass of the LVCLs, i.e. from fine steps to relatively larger steps. The larger step size of the arm voltages incline to increase the synthesis errors of the dc voltages (dc voltage ripple) which leads to increased dc current ripple. The sum of the LVCL capacitor voltages are well regulated and exhibit oscillatory behaviour during typical EMMC operation when both HVCLs and LVCLs are active, and become flat after bypass of the LVCLs when the EMMC operates in HB-MMC mode, as shown in Fig. 8(f).

B. Changes of active and reactive power set-points

To demonstrate that the dynamic performance of the EMMC is not compromised during normal operation and power reversal, at t=4.5s EMMC1 initiates a rapid active power reversal from -1p.u. to 1p.u. with a ramp rate of 20 pu/s, as shown in Fig. 9(a). Also, both EMMC1 and EMMC2 vary their reactive powers from 0.3p.u. to -0.3p.u. and vice versa for both rated positive and negative active powers, covering all four quadrants of the P-Q envelope as shown in Fig. 9(b). The plots for the dc voltages, the dc currents of EMMC1 and EMMC2 in Figs. 9(c) and 9(d) exhibit stable performance of the dc voltage and active power controlling converters. Observe that the cell capacitor voltages of the HVCLs of the EMMC1 and EMMC2 are well decoupled from the dc voltage due to the action of the horizontal capacitor voltage controllers, as shown in Figs. 9(e) and 9(f). Whilst the sum of the cell capacitor voltages of the LVCLs show noticeable adjustments, as they remain stable around 1/2V_{dc}/Nc during the whole active and reactive power exchange operation for both ac grids, shown in Figs. 9(f) and 9(g).

C. Reduced dc voltage operation

Since the original vision of the EMMC does not require the FB cells of the LVCLs to control any part of the dc link voltage, the EMMC control boundaries are largely defined by limitations of the unipolar HB cells of the HVCLs that block the full dc voltage. Therefore, this section demonstrates the capability of the EMMC to transfer power during reduced dc voltage. The EMMC minimum dc voltage V_{dc} must be selected to be equal to the magnitude of the rectified line-to-line ac voltage after excluding voltage drops in the arm and transformer reactors, and cell capacitor voltage ripple dV_{cell}. The minimum operating dc voltage for an EMMC can be approximated by (21).

$$V^*_{dc_{min}} > \hat{V}_{ac_{LL}} + 2\frac{V_{dc}}{N_{HVCL}}dV_{cell} \tag{21}$$

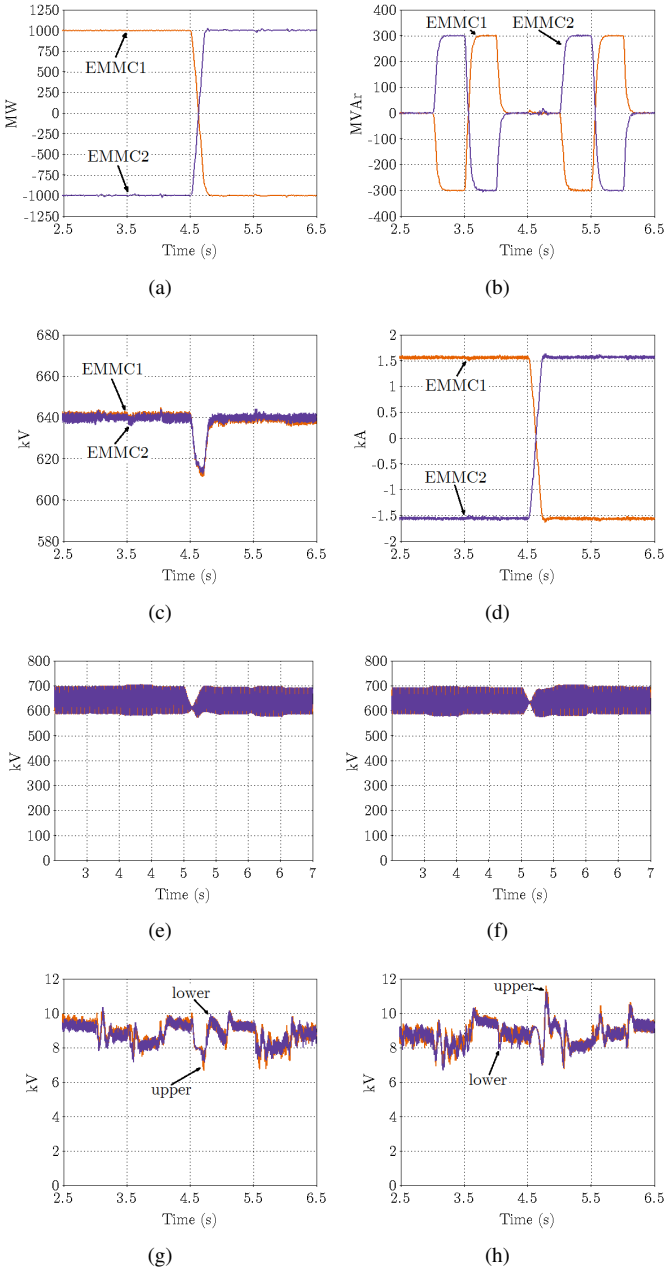

Fig. 9. EMMC PQ capabilities: (a) Active power, (b) Reactive power, (c) dc voltages, (d) dc currents, (e) EMMC1 HVCL total capacitor voltages, (f) EMMC2 HVCL total capacitor voltages, (g) EMMC1 LVCL total capacitor voltages, (h) EMMC2 LVCL total capacitor voltages

Fig. 10 shows the reduced voltage operation for a two-terminal HVdc link based on EMMC. The dc voltage initially regulated at the rated 640kV and at t=1.2s is quickly reduced to 80% of the rated dc voltage at 520kV. The active power transfer is reduced to 80% of the rated power at 800MW, as shown in Fig. 10(a). Observe that the dc voltage dynamics are largely decoupled from the HVCL HB cell capacitor voltages, as shown in Fig. 10(b), Figs. 10(c) and 10(d). Fig. 10(a) shows the dc currents of both stations quickly follow the active powers as anticipated. The EMMC is able to synthesize the high quality arm voltage during reduced and rated dc link voltages, exploiting both HVCL and LVCL

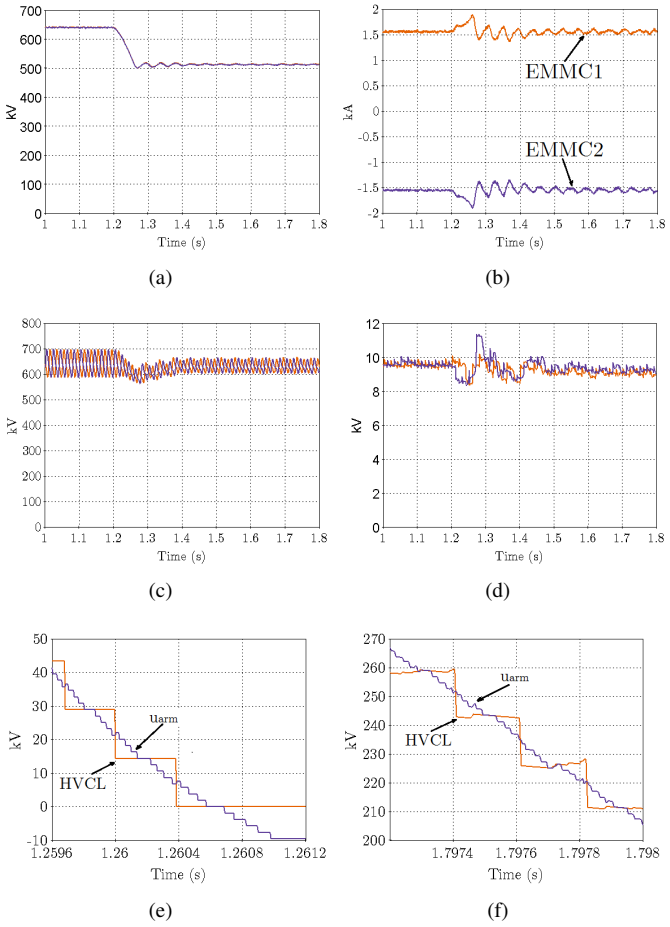

Fig. 10. Reduced dc voltage operation: (a) dc voltages, (b) dc currents, (c) HVCL total capacitor voltages, (d) LVCL total capacitor voltages, (e) HVCL and total arm voltages during over- modulation period, (f) HVCL and total arm voltages during reduced dc voltage operation.

voltage capabilities, as shown in the focused Figs. 10(e) and 10(f).

D. Three-phase symmetrical ac fault

To assess EMMC ac fault ride-through capability, the two-terminal HVdc system in Fig. 7 is subjected to a 200ms three-phase-to-ground ac fault at the PCC of EMMC 1. The waveforms for Grid 1 ac voltages and EMMC 1 currents measured at the converter side are shown in Figs. 11(a) and 11(b) respectively. Observe that the EMMC is able to ride through the ac fault with its current control fully functional as with other established VSCs. During the fault period, the EMMC1 output power is reduced to zero which results in zero dc current during the fault period as shown in Fig. 11(c). The sudden mismatch between the active powers of the ac and dc sides of EMMC1 and EMMC2 appears in the dc voltage as under and over-voltages as shown in Fig. 11(d). Despite the cell capacitor voltages being regulated independent of the dc link voltage, the temporary power imbalance between the ac and dc sides results in brief HVCL cell capacitor over-voltage at both terminals. Because of significantly smaller energy storage of the LVCLs compared to that of the HVCLs, bypass commands are sent to the LVCLs once ac the fault is

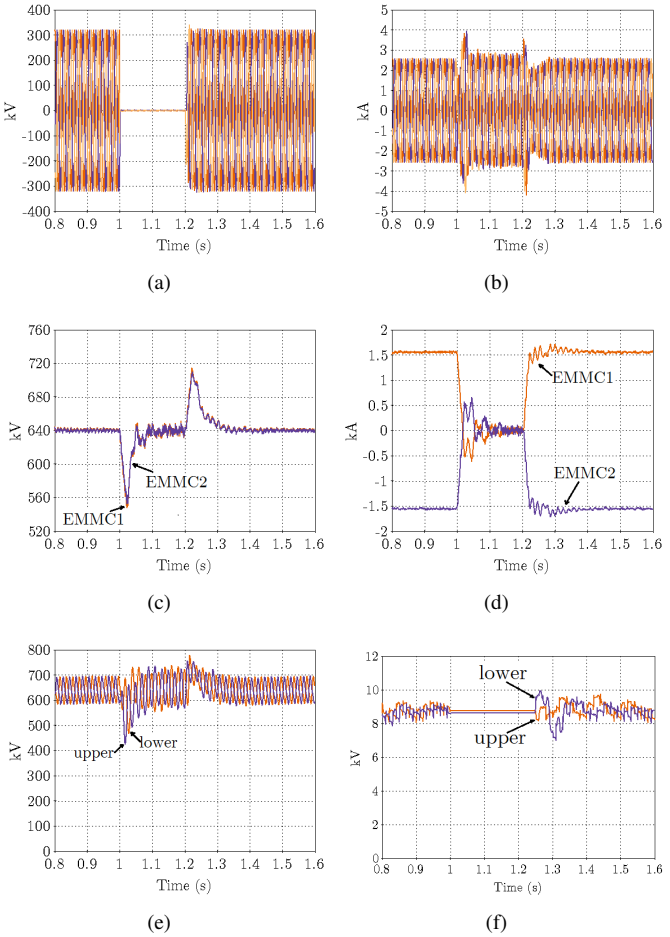

Fig. 11. EMMC ac symmetrical fault: (a) Grid 1 ac voltages, (b) EMMC 1 ac currents, (c) dc voltages, (d) dc currents, (e) HVCL total capacitor voltages, (f) LVCL total capacitor voltages.

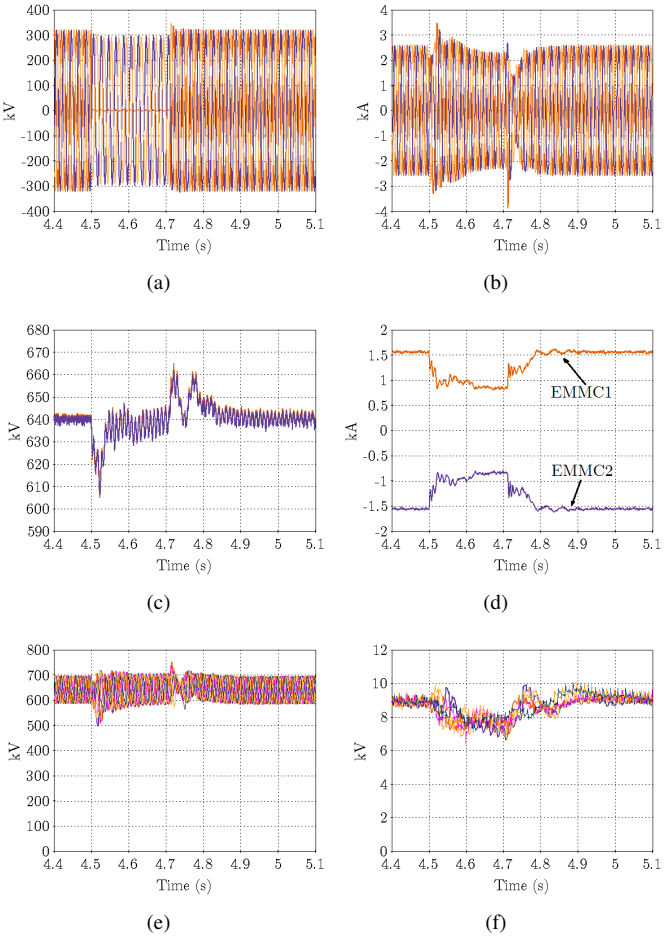

Fig. 12. EMMC ac unbalanced fault: (a) Grid 1 voltages, (b) EMMC 1 ac currents, (c) dc voltages, (d) dc currents, (e) HVCL total capacitor voltages, (f) LVCL total capacitor voltages.

detected in a effort to avoid any excessive voltage ripple in the FB cell capacitor voltages of the LVCLs, as shown in Figs. 11(e) and 11(f).

E. Asymmetric ac fault

Fig. 12 presents simulation waveforms that examine the response of the EMMC based HVdc link in Fig. 6 to a 200 ms single-line-to-ground ac fault at the PCC of EMMC1 in Grid 1, shown in Fig. 12(a). In this case, the double synchronous reference frame current controller is employed to suppress the negative sequence current at zero, maintaining balanced converter currents, as shown in Fig. 12(b). Although the dc voltages and currents of EMMC1 and MMC2 are affected by the power imbalance, the dc voltage exhibit a small increase in ripple magnitude, without the appearance of double frequency (100Hz) components in the dc currents, due to the use of PR based circulating current controller, as shown Figs. 12(c) and 12(d). Notice that the reduction in the active power transfer due to a single-phase ac fault has resulted in decreased dc current. In summary, the EMMC can control both positive and negative sequence ac currents during a asymmetrical ac fault with minimal dc current and voltage oscillations, and low capacitor voltage ripple in HVCL and LVCL, thus LVCLs is always connected, as shown in Figs. 12(e) and (f) respectively.

F. Pole-to-pole dc fault

Fig. 13 shows simulation results that examine the response of the EMMC-HVdc link to a permanent pole-to-pole dc fault at the middle of the dc line at t = 1 s. Figs. 13(a) and 13(b) show the response of dc voltages and currents of both stations EMMC1 and EMMC2. Observe that the dc voltages drop to zero after a short period of oscillation caused by the dc cable distributed inductance and capacitance, and the rise of dc currents shows the discharging of cable capacitances as expected. The plots for the ac output phase current and samples of the arm currents show rapid rise in the current magnitudes following by an uncontrolled converter stage similar to that of an HB-MMC, as shown in Figs. 13(c) and (d) respectively. Also, the cells are bypassed as soon as the EMMCs are blocked, hence the capacitor voltages of HVCL and LVCL remain flat, as shown in Figs 13(e) and (f).

IV. EMMC VARIANTS

In addition to the EMMC described in previous sections, this section proposes a variant of the EMMC in which both HVCL

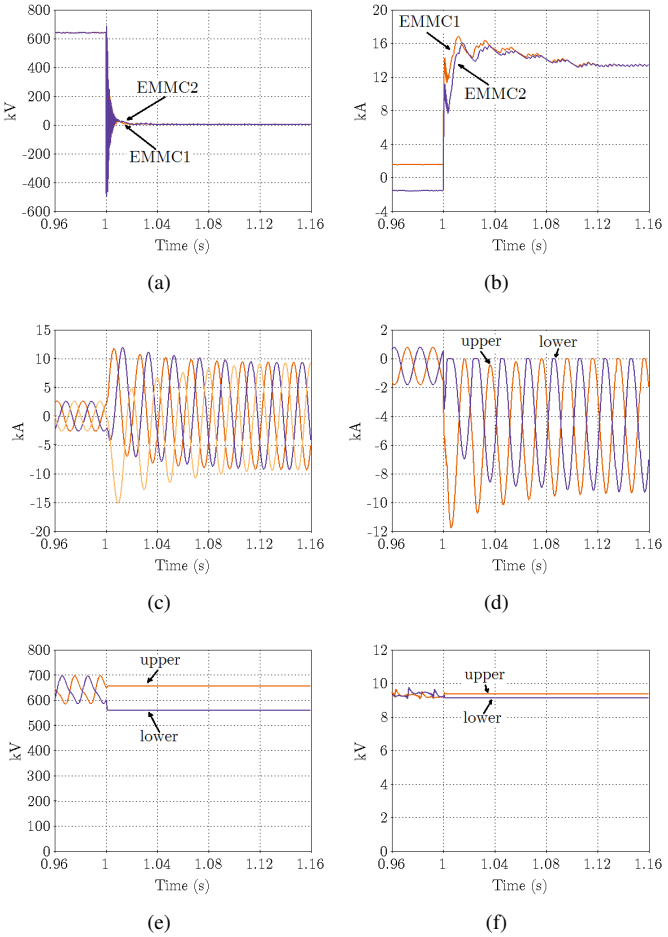

Fig. 13. EMMC dc pole-to-pole fault (a) dc voltages, (b) dc currents, (c) EMMC 1 ac currents, (d) EMMC 1 arm currents, (e) HVCL total capacitor voltages, (f) LVCL total capacitor voltages.

and LVCL contribute to the synthesis of fundamental voltage. In this variant, the total blocking voltage of the LVCL is traded for customised dc fault performance. For distinguishing between the two versions of the EMMC described in this paper, the latter will be referred to as EMMC_0. In principle, the EMMC_0 could be seen as a sub-category of the MC-MMC because the ratio of the blocking voltage between the LVCL and the HVCL defines its control range and dc fault performance. Recall that the ratio of the number of FB cells to HB cells determines the control range and dc fault performance of the MC-MMC.

Fig. 14 show the theoretical synthesis of the arm voltage in the EMMC_0 where the LVCL of each arm could be designed to block a part of the dc link voltage. However, in this illustration, the LVCL blocks only 25% of the total dc voltage (V_{dc}/4), with the HVCL synthesize the remaining 75% of the dc link voltage. For ease of understanding, the theoretical plots for the total arm voltage, and HVCL and LVCL voltages shown in Fig. 14, are normalized by the full dc voltage (V_{dc}). As in EMMC, the HVCL and LVCL of the EMMC_0 consist of cascaded HB and FB cells with major and minor voltage steps respectively. Fig. 14 shows that the EMMC_0 synthesizes the voltage levels between 0 and $0.75V_{dc}$ in each arm using a

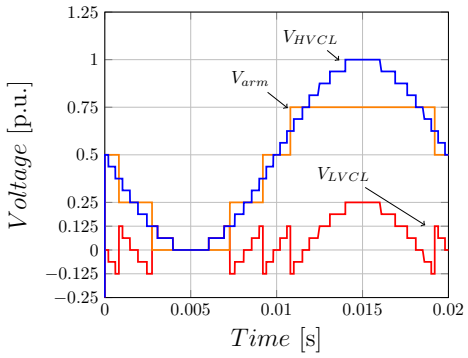

Fig. 14. $EMMC_0$ synthesis of internal voltages,i.e., HB and FB chain-link voltages, and total arm voltage.

similar philosophy which is employed in the EMMC. The LVCL only operates between successive major voltage steps in order to facilitate orderly stepped transitions through minor voltage steps. In contrast to EMMC, the LVCL in EMMC_0 are employed to synthesize the arm voltage levels between $0.75V_{dc}$ and V_{dc}. Considering that the blocking voltage of the LVCL in EMMC_0 is significantly larger than the LVCL in EMMC, the number of voltage levels generated per arm is

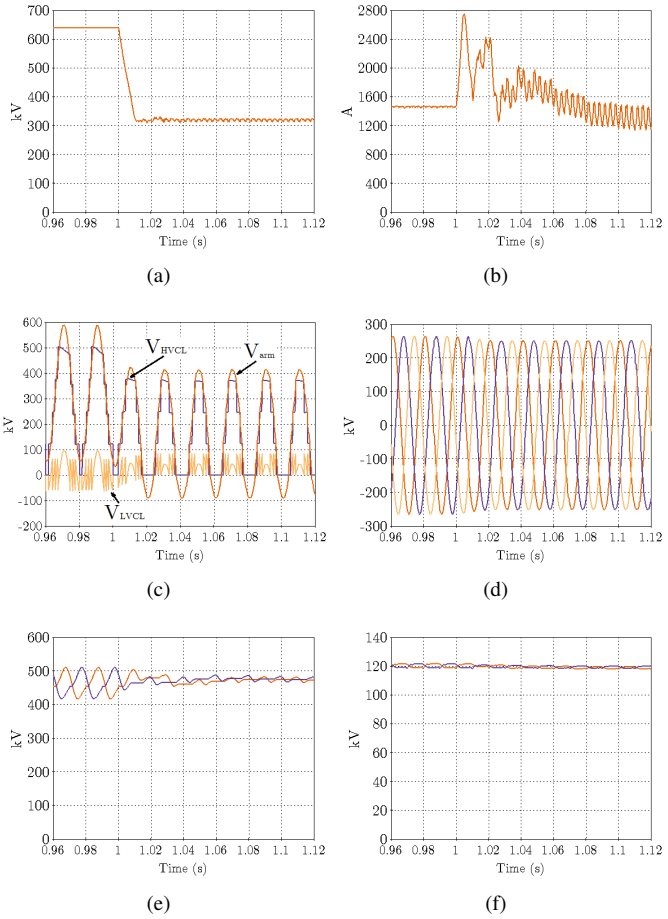

Fig. 15. $EMMC_0$ reduced dc voltage operation: (a) dc voltage, (b) dc current, (c) Chain-link voltages, (d) Converter ac phase voltages, (e) HVCL total capacitor voltages, (f) LVCL total capacitor voltages.

TABLE II
HIGH-LEVEL ATTRIBUTE SUMMARY.

	HB-MMC		EMMC	MC-MMC		$EMMC_0$
Number of cells	40	400	N_{HVCL}=40 N_{LVCL}=5	N_{HVCL}=30 N_{LVCL}=10	N_{HVCL}=300 N_{LVCL}=100	N_{HVCL}=30 N_{LVCL}=100
Input dc link voltage (kV)	640					
HB capacitor voltage (kV)	16	1.6	16	16	1.6	16
FB capacitor voltage (kV)	-	-	1.6	16	1.6	1.6
Number of voltage level per arm	41	401	401 Eq. (4)	41	401	401 Eq. (22)
Power circuit and control complexity	Low and proven [5], [23], [24]	High and proven [25], [26]	Moderate and promising	Medium, practical realization of MV FB cells is challenging and may cause excessive inrush currents	Medium and proven [27]	Moderate and promising
Total energy storage (kJ/MVA)	40	40	40	40	40	40
DC voltage and current ripples	High requires dc filters	Low	Low	High requires dc filters	Low	Low
AC fault ride-through	Yes					
DC fault ride-through	No			Yes, and bespoke		

calculated according to (22), which is different from that of the EMMC.

$$N^0_{EMMC} = \alpha N^0_{HVCL} + N^0_{LVCL} = \frac{\alpha}{\gamma} N^0_{HVCL} + 1 \quad (22)$$

where, $\alpha = V^0_{cell_{HVCL}}/V^0_{cell_{LVCL}}$ and $\gamma = V^0_{HVCL}/V_{dc}$ and number of FB cells $N^0_{LVCL} = \frac{\alpha(1-\gamma)}{\gamma}$.

For an example, $EMMC_0$ with FB chain-link rated to block 25% of the dc link voltage, $\gamma = 480/640 = 0.75$, N^0_{HVCL}=30 and each HB cell capacitor is rated for 16kV ($V^0_{cell_{HVCL}}$=16kV) and each FB cell is rated for 1.6kV ($V^0_{cell_{LVCL}}$=1.6kV), γ=16kV/1.6kV=10 and thus number of FB cells needed is $N^0_{LVCL} = \frac{\alpha}{\gamma} N^0_{HVCL} = \frac{10(1-0.75)}{0.75}30$=100. The number of voltage levels per arm is: $N^0_{EMMC} = \alpha N^0_{HVCL} + N^0_{LVCL} + 1 = \frac{\alpha}{\gamma} N^0_{HVCL} + 1 = \frac{10}{0.75}3 + 1 = 401$.

Furthermore, the proposed $EMMC_0$ could improve dc fault ride-through performance of multi-terminal dc grids by:

1) Extension of fault clearance time without loss of system controllability, opening the way for the use of relatively cheap and slow dc circuit breakers
2) Facilitation of continued operation and minimization of the voltage stresses during pole-to-ground ground.

The proposed $EMMC_0$ provides a way to offer extra desirable features without the full complexity of MC-MMC, where efficiency could be traded for the additional functionalities. The $EMMC_0$ uses fewer medium-voltage HB cells in its HVCLs and the increased number of low-voltage FB cells in the LVCLs. These could further contribute to overall reduction of switching losses in the $EMMC_0$. The conduction loss of the $EMMC_0$ is anticipated to remain practically the same as its equivalent MC-MMC. Apart from the modulation strategy, the control system of the $EMMC_0$ is similar to that of the EMMC described in Section II.C.

A. Simulation illustration of $EMMC_0$

This section illustrates the operation of the $EMMC_0$ during reduced dc voltage. The $EMMC_0$ can operate in lower dc voltage compare to EMMC and HB-MMC, which allows dc pole voltage control for continuous operation during permanent pole-to-ground dc faults. At t=1s the $EMMC_0$ has its dc voltage reduced from the rated to half of the rated dc voltage V_{dc}, as shown in 15(a). Observe that the voltage waveforms of the HVCL and LVCL, shown in 15(c) are similar to their theoretical equivalents, as shown in Fig. 14. The LVCLs exploit their negative voltage generation capabilities to synthesize the necessary negative arm voltages to enable controlled operation during reduced dc voltage operation. Fig. 15(d) shows that the converter ac voltages remain intact during reduced dc voltage operation as with rated dc voltage. Notice that the HVCL and LVCL cell capacitor voltages remain tightly controlled around the desired set-points with the aid of the decoupled vertical and horizontal capacitor voltage controllers shown in Figs. 15(e) and 15(f).

V. HIGH-LEVEL COMPARISON

Table II summarizes the key attributes and limitations between selected HVdc converter topologies. The EMMC and $EMMC_0$ can provide number of voltage levels, harmonic context and dv/dt similar to HB-MMC and MC-MMC. The EMMC inherent the resilience of the HB-MMC on symmetrical and asymmetrical ac faults and its vulnerability to dc faults. The $EMMC_0$ retains the advantages of the equivalent MC-MMC by achieving custom features with trade-off between the degree of dc fault resiliency and efficiency. While the practical realization of the MC-MMC using reduced number of MV HB and FB cells is uncertain, the $EMMC_0$ could provide the

realisation, in which the potential downsides of FB cells with cell voltages of 16 kV to 20 kV can be avoided.

VI. Conclusions

This paper has assessed the technical viability of the EMMC and $EMMC_0$ for HVdc applications. The first part has been devoted to the theoretical basis which supports the operation and control of the EMMC. The EMMC dynamic and transient performance is assessed, operating in all four quadrants of the PQ envelope, in symmetrical and asymmetrical ac faults and dc short circuit fault. Detailed evaluation of the EMMC based in a two-terminal HVdc link, shows that it exhibits similar behaviour to the HB-MMC with large number of low-voltage cells. Moreover, the $EMMC_0$ has been investigated as potential extension of the EMMC concept, in which a customized trade-off between efficiency and wider range of operation can be achieved. Preliminary simulation studies show that the $EMMC_0$ represents a viable alternative to the MC-MMC, in which the attributes associated with reduced number of medium-voltage HB cells are preferred over that of the large number of low-voltage HB cells.

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