Characterization of Time Delay in Power Hardware in the Loop Setups

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***Abstract*—The testing of complex power components by means of power hardware in the loop (PHIL) requires accurate and stable PHIL platforms. The total time delay typically present within these platforms is commonly acknowledged to be an important factor to be considered due to its impact on accuracy and stability. However, a thorough assessment of the total loop delay in PHIL platforms has not been performed in the literature. Therefore, time delay is typically accounted for as a constant parameter. However, with the detailed analysis of the total loop delay performed in this paper, variability in time delay has been detected as a result of the interaction between discrete components. Furthermore, a time delay characterization methodology (which includes variability in time delay) has been proposed. This will allow for performing stability analysis with higher precision as well as to perform accurate compensation of these delays. The implications on stability and accuracy that the time delay variability can introduce in PHIL simulations has also been studied. Finally, with an experimental validation procedure, the presence of the variability and the effectiveness of the proposed characterization approach have been demonstrated.**

***Index Terms*—Time delay, power hardware-in-the-loop, delay identification, real-time simulation, component testing.**

NOMENCLATURE

Abbreviations

AC	Alternating current.
ADC	Analog to digital converter.
DAC	Digital to analog converter.
DC	Direct current.
DRTS	Digital real time simulator.
FPGA	Field-Programmable Gate Array.
GPS	Global positioning system.
HUT	Hardware under test.
IA	Interface algorithm.
ITM	Ideal transformer method.
PCC	Point of common coupling.
PHIL	Power hardware in the loop.
PI	Power interface.
PWM	Pulsed width modulation.

Time Delay Terms

T	Grouped delays.
τ	Single component delay.
$\mathrm{T}_{\mathrm{Acom_{FB}}}$	Feedback analog communication delay.
$\mathrm{T}_{\mathrm{Acom_{FF}}}$	Feed forward analog communication delay.
$\mathrm{T}_{\mathrm{Acom}}$	Analog communication delay.
$\tau_{\mathrm{ADC_{DRTS}}}$	DRTS's ADC delay.
$\tau_{\mathrm{ADC_{filter}}}$	ADC filter delay.
$\tau_{\mathrm{ADC_{PI}}}$	PI's ADC delay.
τ_{ADC}	Delay of ADC.
$\tau_{\mathrm{algorithm}}$	Orchestrator algorithm delay.
$\mathrm{T}_{\mathrm{com\_FB}}$	Feedback communication delay.
$\mathrm{T}_{\mathrm{com\_FF}}$	Feed forward communication delay.
$\mathrm{T}_{\mathrm{com}}$	Communication delay.
$\tau_{\mathrm{control_{PI}}}$	PI control delay.
τ_{coupling}	Delay of coupling source.
$\mathrm{T}_{\mathrm{d_{max}}}$	Maximum delay.
$\mathrm{T}_{\mathrm{d_{min}}}$	Minimum delay.
$\tau_{\mathrm{DAC_{DRTS}}}$	DRTS's DAC delay.
τ_{DAC}	Delay of DAC.
$\mathrm{T}_{\mathrm{Dcom_{FB}}}$	Feedback digital communication delay.
$\mathrm{T}_{\mathrm{Dcom_{FF}}}$	Feedforward digital communication delay.
$\mathrm{T}_{\mathrm{Dcom}}$	Digital communication delay.
$\mathrm{T}_{\mathrm{DRTS}}$	DRTS delay.
T_{d}	Total delay.
τ_{fiber}	Fiber optic link delay.
$\tau_{\mathrm{filter_{ADC_{DRTS}}}}$	DRTS's ADC filter delay.
$\tau_{\mathrm{filter_{ADC_{PI}}}}$	PI's ADC filter delay.
$\mathrm{T}_{\mathrm{fixed}}$	Total fixed delay.
$\mathrm{T}_{\mathrm{loop_{DRTS}}}$	Loop delay external to DRTS.
$\mathrm{T}_{\mathrm{loop_{PI}}}$	Loop delay external to PI.
$\mathrm{T}_{\mathrm{loop}}$	External loop delay.
τ_{meas}	Measurement device delay.
$\mathrm{T}_{\mathrm{other}}$	Other delays.
$\mathrm{T}_{\mathrm{PI_{Sw}}}$	Switched-mode PI delay.
T_{PI}	PI delay.
$\tau_{\mathrm{s_{DRTS}}}$	Time step of DRTS.
$\tau_{\mathrm{s_{PI}}}$	PI sampling period.
$\mathrm{T}_{\mathrm{var_{DRTS}}}$	Variable delay introduced by the DRTS.
$\mathrm{T}_{\mathrm{var_{PI_{max}}}}$	Maximum variable delay introduced by PI.
$\mathrm{T}_{\mathrm{var_{PI_{min}}}}$	Minimum variable delay introduced by PI.
$\mathrm{T}_{\mathrm{var_{PI}}}$	Variable delay introduced by the PI.
$\mathrm{T}_{\mathrm{var}}$	Total variable delay.

Functions

$H_{\mathrm{delay}}(s)$	Time delay transfer function.
$H_{\mathrm{DRTS}}(s)$	DRTS transfer function.

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$H_{\text{HUT}}(s)$	HUT transfer function.
$H_{\text{OL}}(s)$	Open loop transfer function.
$H_{\text{PI}}(s)$	PI transfer function.
$Z_{\text{DRTS}}(s)$	DRTS impedance transfer function.
$Z_{\text{HUT}}(s)$	HUT impedance transfer function.

Other Symbols

ω_{n}	Resonant frequency.
ζ	Damping ratio.
n	Number of variability steps.

I. Introduction

ELECTRIC power systems are facing a major change of generation resources, loads and control methodologies. Renewable energy technologies are continuously growing and their efficiency and cost have been improving to a point where such technologies are being considered to be the largest source of electric energy generation in the future. At the same time, governments and energy authorities are modifying the regulations required for this major advancement to be consolidated.

Power systems operators need to ensure that the system will remain resilient through all major changes. For securing resilient power systems under great variability, novel testing procedures for developing and testing the integration of novel complex power systems components at all levels (generation, transmission, distribution, loads and controls) with reduced development time scales, risks and costs have to be considered.

This supports the case for power hardware-in-the-loop (PHIL), where complex hardware components can be tested by connecting them to a simulated power system in real-time, leading to an increased awareness of the effects that can occur in the future by evaluating a large number of scenarios with reduced costs and time [1], [2]. Real-time is referred to when the computation of the simulation is in synchronism with the wall clock, meaning that a one second elapsed simulation time is equivalent to a one second wall clock time. This is a fundamental requirement for PHIL simulations as real hardware components, that by nature respond in real-time, are connected to the simulation. However, successful PHIL implementations depend on the stability and accuracy of the PHIL setup itself. Stability and accuracy challenges are mainly due to the power interface present between the simulated system and the hardware under test (HUT) [3].

The interface is responsible for amplifying the reference signal received from the simulation and for electrically coupling the HUT. The HUT response is then measured and fed back into the simulation for closing the loop, as seen in Fig. 1. Within this process, time delay is present due to the interconnection between components and the amplification stage that would not exist on a hardware only scenario. The total loop delay of PHIL simulations affects the stability of the simulation, but is often overlooked due to the importance of the interface algorithm (IA) and the relationship between impedances at both sides of the interface for achieving a stable simulation [4]–[6]. Furthermore, the phase relationship between current and voltage at the point of common coupling (PCC) is also affected. As a consequence, the power factor and apparent power of the simulated system are also altered [7]–[10]. This is even more relevant when evaluation of harmonics components is to be performed as the lag for harmonic phases will be larger than for the fundamental component.

In [9], [11], the conventionally identified time delay is compensated by phase-shifting the amplified voltage setpoint and the feedback current respectively. In [12] the time delay is compensated by adding a phase angle in the Park transformation, however neither the amount of time delay compensated nor how it was calculated are explained. When a time delay compensation method is implemented, a decrease of the overall time delay will help to further improve the accuracy of the simulation results with faster dynamics.

Most of the contributions on PHIL in the literature acknowledge that time delay is important [13]–[23], however a detailed study of time delay has not been published yet. Appropriate understanding of the time delay and its effect will lead to a reduced risk of instabilities and inaccuracies when performing PHIL experiments, allowing more resilient and accurate evaluation of complex power components [24]. A thorough characterization of delays in PHIL can also help to reduce the total loop delay and increase its accuracy. Hence, identification of the components and processes that introduce the delay is the first step towards a better understanding of it. However, previous work on PHIL simulations only focus on the total loop delay without analysing in detail why the time delay is produced or how it can be reduced. With a detailed assessment of the loop delay in PHIL, a variability in time delay is demonstrated, characterized and thoroughly analysed within this paper. Therefore, with the aim of providing a detailed characterization of time delays for PHIL simulations, the contributions of this paper are as follows:

- A detailed analysis of time delays associated with PHIL setups is undertaken to characterize the identified delays. The developed equations are generic, allowing for accurate analytical assessment of the time delay in PHIL setups.
- Contrary to the common assumption of a constant time delay, it is demonstrated that time delay associated with a PHIL setup is typically variable.

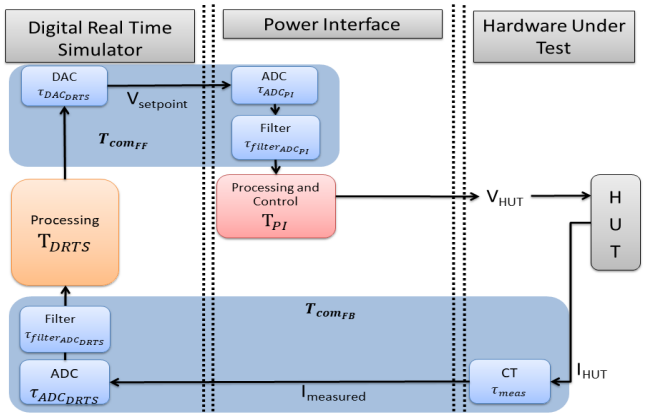

Fig. 1. PHIL delay diagram with contributing time delays.

- The impact of the identified variability in time delay on the stability and accuracy of PHIL setups is presented.
- Measures to mitigate the impact of the variability in time delay and ultimately eliminate it are proposed.
- The validity of the above is experimentally verified.

II. Conventional Time Delay Characterization

Typically, PHIL setups comprise three main components, (i) a Digital Real-Time Simulator (DRTS) for simulation of power system components in real-time, (ii) a HUT and (iii) a Power Interface (PI) for interfacing the DRTS with the HUT, as shown in Fig. 1. These components along with the approach used for interconnecting them are responsible for the majority of the introduced time delay. Conventionally, the total PHIL time delay is calculated as the sum of delays introduced by the components, their interactions and processes throughout the experimental loop. In the following sub-sections, the delay associated with each of the identified components and the processes associated with interfacing the components are analyzed in detail. Any delay associated with a single component or a process will be represented by τ followed by a subscript indicating the component or process itself, while T will be used for a group of delays.

A. Simulation platform delay

The DRTS used for PHIL applications is composed of processor cards, responsible for real-time processing, and an interface (analog or digital) for communicating with external components. The processor cards run the real-time simulation at a discrete time step while the interface communicates the set-points from the simulation PCC to the PI for amplification, and receives feedback from the HUT measurements. The time step of the simulation platform is typically determined by: (i) the complexity and number of nodes of the simulated power system, (ii) a specific requirement of a particular application or (iii) by platform limitations. Typical simulation platform utilizing powerful processors can achieve time steps in the range of 1μs to 200μs, however more advanced platforms utilizing FPGA technology can achieve sub-microsecond time steps. The time step of the DRTS, $\tau_{\mathrm{s_{DRTS}}}$, is always constant and constitutes the time delay introduced by the processing stage of the DRTS. Furthermore, the simulated component used for the electrical coupling with the simulated power system (usually a controlled current or voltage source) can introduce additional delays depending upon its implementation, τ_{coupling}. Hence, the total simulation platform delay can be expressed as:

$$T_{\mathrm{DRTS}} = \tau_{\mathrm{s_{DRTS}}} + \tau_{\mathrm{coupling}} \tag{1}$$

B. Communication delay

The time delay introduced due to the interfacing of the DRTS with external components, such as the PI and HUT, is defined as the communication delay, T_{com}. The flow of information from the DRTS will be referred to as the feed-forward path, to the DRTS as the feedback path and the communication delays associated with each path referred to as $T_{\mathrm{com_{FF}}}$, $T_{\mathrm{com_{FB}}}$ respectively. The two options available for interconnection of DRTS with external components are discussed in the following sub-sections.

1) Analog communication delay: If an analog interconnection is used, digital to analog converters (DAC) for sending the required signals on the feed-forward path and analog to digital converters (ADC) for receiving the HUT measurements on the feedback path are required at the DRTS. Similarly, the PI requires an ADC for receiving the signal at the feed-forward path. Both of these conversion processes have an inherent time delay, τ_{DAC} and τ_{ADC} respectively. The time required for information to pass from the processor card to the ADC or DAC is part of the total delay of each conversion component. Generally, an anti-aliasing filter is added at the ADC, the time delay of which (depending upon the cut-off frequency) can be larger than the actual time required for the ADC process and therefore should be considered, $\tau_{\mathrm{ADC_{filter}}}$. The measurement of the response of the HUT, τ_{meas} can also introduce additional delays into the feedback path and should also be considered. So, the feed-forward and feedback path delays when implemented with analog communication can be calculated as:

$$T_{\mathrm{Acom_{FF}}} = \tau_{\mathrm{DAC_{DRTS}}} + \tau_{\mathrm{ADC_{PI}}} + \tau_{\mathrm{filter_{ADC_{PI}}}} \tag{2}$$

$$T_{\mathrm{Acom_{FB}}} = \tau_{\mathrm{ADC_{DRTS}}} + \tau_{\mathrm{filter_{ADC_{DRTS}}}} + \tau_{\mathrm{meas}} \tag{3}$$

$$T_{\mathrm{Acom}} = T_{\mathrm{Acom_{FF}}} + T_{\mathrm{Acom_{FB}}} \tag{4}$$

2) Digital communication: High-speed serial protocols (such as PCIe and Aurora) can be used for digital interconnection of DRTS units with PI and HUT measurements [25]. Digital communication interfaces are much more efficient and faster than analog interfaces as DAC, ADC and corresponding anti-aliasing filters are not required, thereby reducing the time delay of the PHIL simulation loop. The digital communications interface delay depends on the latency of the optical fiber (τ_{fiber}), that for short cable runs (up to 300m) is less than 1μs and the processing delay of the algorithm ($\tau_{\mathrm{algorithm}}$) that orchestrates the communication between the components. The delay introduced by the device used for the measurement of the HUT response has to be also considered in the feedback path.

$$T_{\mathrm{Dcom_{FF}}} = \tau_{\mathrm{fiber}} + \tau_{\mathrm{algorithm}} \tag{5}$$

$$T_{\mathrm{Dcom_{FB}}} = \tau_{\mathrm{fiber}} + \tau_{\mathrm{algorithm}} + \tau_{\mathrm{meas}} \tag{6}$$

$$T_{\mathrm{Dcom}} = T_{\mathrm{Dcom_{FF}}} + T_{\mathrm{Dcom_{FB}}} \tag{7}$$

C. Power interface delay

Different types of power amplifiers can be used as the power interface for PHIL implementations [26]. For this study only switched-mode PI has been assessed in detail, which comprises an active rectifier for the interconnection with the grid supply point and a power converter amplifying the signals received from the DRTS unit. This AC/DC/AC converter operates across the four quadrants of the power plane, i.e., it can source and sink real and reactive power. This characteristic is required for PHIL applications as it allows for bi-directional power flows.

The time delay introduced by the switched-mode PI, $T_{\text{PI}_{\text{Sw}}}$, is the inherent delay of the digital control loop architecture of power converters. This delay is constituted by: (i) one sample period, $\tau_{\text{s}_{\text{PI}}}$, due to the discrete behavior of the controller that can only update the duty ratio at the beginning of the switching cycle and (ii) an additional half time step to compare the pulse width modulation (PWM) signal with the carrier waveform, considered equal to a zero order hold (ZOH) [27]. The total digital control loop delay, $\tau_{\text{control}_{\text{PI}}}$, can vary depending on the implementation but it is commonly between one and a half and two switching cycles. Therefore, the delay introduced by the PI can be represented as:

$$T_{\text{PI}_{\text{Sw}}} = \tau_{\text{control}_{\text{PI}}} \approx 2 \cdot \tau_{\text{s}_{\text{PI}}} \tag{8}$$

D. Other delays

The majority of the delay is introduced by the DRTS and PI units, however some other components or processes can introduce time delays of significant size and importance. Examples of such delays are: (i) digital filters added to the PHIL simulation loop to reduce the noise of measurement signals or to avoid resonances within the control of the PI [28], or (ii) the low pass filter used for improving the stability of PHIL implementations [16]. Such delays are referred to as T_{other}.

E. Total delay

Based on the delays identified in the earlier sub-sections, the total time delay using a conventional approach to the characterization is a function of cumulative delays, $T_{\text{d}} = f(T_{\text{DRTS}}, T_{\text{com}}, T_{\text{PI}}, T_{\text{other}})$ represented as:

$$T_{\text{d}} = T_{\text{DRTS}} + T_{\text{com}} + T_{\text{PI}} + T_{\text{other}} \tag{9}$$

III. Proposed Time Delay Characterization

Time delay associated with PHIL setups is typically treated as constant, obtained by the conventional approach presented. However, in a PHIL setup where more than one discrete time step components are utilized, such as the DRTS and switched-mode PI, a variability in delay presents itself. Within discrete time step simulators, a new value of input can only be updated at the beginning of the next time step, therefore, the variable delay introduced is the waiting time to the next time step of the simulator. This is an important aspect that has not been discussed in literature. This variability in delay can have implications on the stability and accuracy of PHIL simulations. Therefore, in this section, a novel characterization of time delay incorporating variability is proposed. In the remainder of this section, the proposed characterization considering two discrete time step components, i.e., a DRTS and a switched-mode PI, is presented.

The total external loop delay of the DRTS in a PHIL setup is illustrated in Fig. 2 and can be represented as:

$$T_{\text{loop}_{\text{DRTS}}} = T_{\text{com}_{\text{FF}}} + T_{\text{var}_{\text{PI}}} + T_{\text{PI}} + T_{\text{com}_{\text{FB}}} \tag{10}$$

where, $T_{\text{var}_{\text{PI}}}$ is the variable delay introduced as a result of the discrete time step of the PI. In a similar manner, the total external loop delay of the PI in a PHIL setup is shown in Fig. 2 and can be represented as:

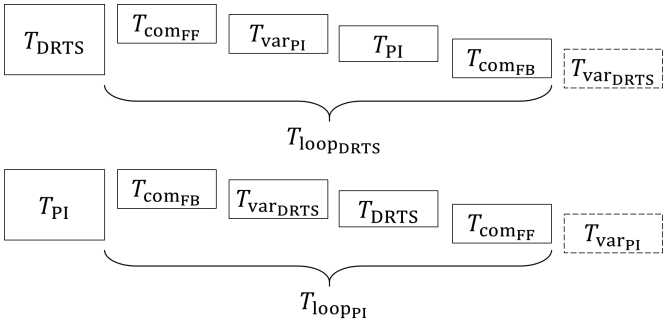

Fig. 2. Time delay loop for DRTS and PI.

$$T_{\text{loop}_{\text{PI}}} = T_{\text{com}_{\text{FB}}} + T_{\text{var}_{\text{DRTS}}} + T_{\text{DRTS}} + T_{\text{com}_{\text{FF}}} \tag{11}$$

where, $T_{\text{var}_{\text{DRTS}}}$ is the variable delay introduced due to the discrete time step of the DRTS. These two variable delays can be calculated as:

$$T_{\text{var}_{\text{DRTS}}} = T_{\text{DRTS}} \cdot \text{ceil}\left(\frac{T_{\text{loop}_{\text{DRTS}}}}{\tau_{\text{s}_{\text{DRTS}}}}\right) - T_{\text{loop}_{\text{DRTS}}} \tag{12}$$

$$T_{\text{var}_{\text{PI}}} = T_{\text{PI}} \cdot \text{ceil}\left(\frac{T_{\text{loop}_{\text{PI}}}}{\tau_{\text{s}_{\text{PI}}}}\right) - T_{\text{loop}_{\text{PI}}} \tag{13}$$

where $T_{\text{var}_{\text{DRTS}}} \in \mathbb{R} : T_{\text{var}_{\text{DRTS}}} \in [0, \tau_{\text{s}_{\text{DRTS}}}]$, $T_{\text{var}_{\text{PI}}} \in \mathbb{R} : T_{\text{var}_{\text{PI}}} \in [0, \tau_{\text{s}_{\text{PI}}}]$, and the ceil function represents scaling to the next integer number. Therefore, in contrast with the conventional delay estimation approach (Eq. 9), the proposed total time delay for PHIL implementations comprises a fixed delay, T_{fixed}, and a variable delay, T_{var}, as:

$$T_{\text{fixed}} = T_{\text{DRTS}} + T_{\text{com}_{\text{FF}}} + T_{\text{PI}} + T_{\text{com}_{\text{FB}}} \tag{14}$$

$$T_{\text{var}} = T_{\text{var}_{\text{PI}}} + T_{\text{var}_{\text{DRTS}}} \tag{15}$$

$$T_{\text{d}} = T_{\text{fixed}} + T_{\text{var}} \tag{16}$$

Calculating the delay with respect to the DRTS, the minimum and maximum delay of a specific PHIL implementation can be obtained as:

$$T_{\text{d}_{\text{min}}} = T_{\text{fixed}} + T_{\text{var}}\big]^{T_{\text{var}_{\text{PI}_{\text{min}}}}} \tag{17}$$

$$T_{\text{d}_{\text{max}}} = T_{\text{fixed}} + T_{\text{var}}\big]^{T_{\text{var}_{\text{PI}_{\text{max}}}}} \tag{18}$$

Defining n_1 and n_2 as:

$$\text{n}_1 = \text{ceil}\left(\frac{T_{\text{d}_{\text{min}}}}{T_{\text{DRTS}}}\right), \text{n}_2 = \text{ceil}\left(\frac{T_{\text{d}_{\text{max}}}}{T_{\text{DRTS}}}\right) \tag{19}$$

$$\text{n} = \text{n}_2 - \text{n}_1 \tag{20}$$

where n is the number of variability steps within the range of $T_{\text{d}} \in [T_{\text{d}_{\text{min}}}, T_{\text{d}_{\text{max}}}]$. Therefore, for a given PHIL setup, the time delay is characterized as

$$T_{\text{d}_{[T_{\text{DRTS}}, T_{\text{PI}}, T_{\text{com}}]}} = \left[T_{\text{d}_{\text{min}}}, T_{\text{d}_{\text{max}}}, \text{n}\right] \tag{21}$$

As such, variability in time delay can be defined as the continuous change in time delay for every PHIL simulation loop. The variability is produced as a result of the PHIL

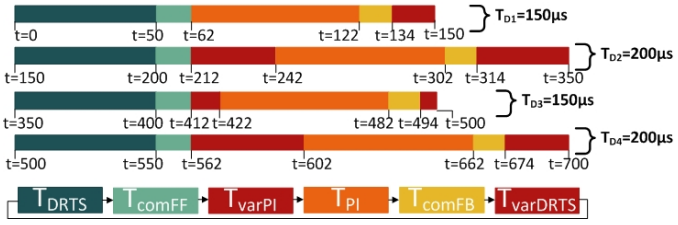

Fig. 3. Sequence of time delay variability.

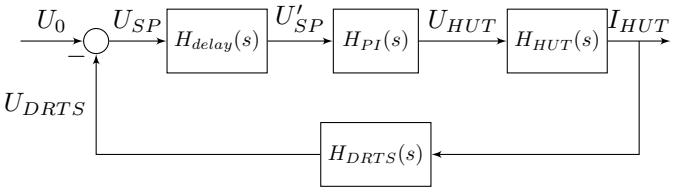

Fig. 4. PHIL control loop diagram.

setup including a DRTS and switched-mode PI in this case. A sample value can only be updated at the beginning of the next time step and so if an input is not received at the exact beginning of the time step, the input needs to wait for the next time step. This behaviour can be present at each of the discrete time step components. The waiting time is a result of the external loop delay, T_{loop}, of a discrete time step unit (the time from when a sample is output to when the response to that output is received) not being an exact multiple of its time step.

For further clarification, a theoretical example with only four components in a PHIL time delay structure is presented in Fig. 3, with $T_{\text{DRTS}} = 50\mu$s, $T_{\text{com}_{\text{FF}}} = 12\mu$s, $T_{\text{PI}} = 60\mu$s and $T_{\text{com}_{\text{FB}}} = 12\mu$s. Assuming there is no waiting time at the first time step of the PI, as can be observed from the first time delay loop of the setup under consideration, although the sample is ready for input at t=134μs, due to the time step of DRTS being 50μs the value will need to wait until the next time step that will be at t=150μs, consequently adding 16μs to the loop (this is essentially $T_{\text{var}_{\text{DRTS}}}$). Similarly, continuing with the next time delay loop, as a result from the PI running at a fixed step of 60μs the input at the PI will only be processed at t=242μs, and accordingly $T_{\text{var}_{\text{PI}}}$ will be 30μs. In the same loop the DRTS will have to wait again, in this case this waiting time varies with respect to the previous loop being $T_{\text{var}_{\text{DRTS}}} = 36\mu$s. This is continued for two more cycles in the figure, which clearly demonstrates that even when the time delay of all the individual components of the loop are always fixed the overall delay is not fixed. This shows that on a loop by loop basis, the time delay can vary referred to as variability in time delay. In this example case, the time delay can be characterized as:

$$T_{\text{d}_{[T_{\text{DRTS}}, T_{\text{PI}}, T_{\text{com}}]}} = [150\mu\text{s}, 200\mu\text{s}, 1]$$

IV. Impact of Variability in PHIL Simulations

In this section, an analysis of the implications of the variability in time delay on accuracy and stability of PHIL simulations as well as possible measures for their improvement are thoroughly discussed.

A. Impact of variability on stability

It is of utmost importance to assess the stability of a PHIL setup before its implementation, as unstable PHIL setups can cause severe damage to the HUT and PI. For this reason, the variability in delay should be given more attention as it can lead to erroneous stability assessments, placing costly laboratory equipment at risk. In this sub-section, the impact of variable delay on stability of PHIL setups is demonstrated.

The stability assessment is undertaken with a PHIL setup using switched-mode PI, ideal transformer method (ITM) IA [4] and a linear load. Nonetheless, the study can be extrapolated to other IA methods. The PHIL system under study can be represented at each side of the interface by a Thevenin equivalent system. Approximating the system to be linear at an operating point, linear control theory and frequency domain techniques (such as the Nyquist stability criterion) can be applied for analyzing the stability of the system [29]. The Nyquist criterion has been chosen as the frequency domain technique for stability analysis due to its clear graphical representation of the effect of time delay within a PHIL simulation. The aggregated total delay of the system is considered for stability analysis.

The equivalent control loop of the PHIL simulation is shown in Fig. 4, where H_{HUT}, H_{DRTS}, H_{PI}, H_{delay}, represent the transfer functions of the HUT, the DRTS, the PI, and the time delay of the PHIL implementation respectively, and are defined as:

$$H_{\text{HUT}}(s) = \frac{1}{Z_{\text{HUT}}(s)} \tag{22}$$

$$H_{\text{DRTS}}(s) = Z_{\text{DRTS}}(s) \tag{23}$$

$$H_{\text{delay}}(s) = e^{-sT_{\text{d}}} \tag{24}$$

where T_{d} is the identified total delay, Z_{HUT} and Z_{DRTS} are the impedances of the HUT and DRTS respectively. H_{PI} can be approximated by a time delay and a second-order low pass filter derived from the output filter of the PI as [30]:

$$H_{\text{PI}}(s) = e^{-sT_{\text{PI}}} \cdot \frac{\omega_{\text{n}}^2}{s^2 + 2\zeta\omega_{\text{n}}s + \omega_{\text{n}}^2} \tag{25}$$

where ω_{n} is the resonant frequency of the output filter and ζ is the damping ratio. The closed-loop negative feedback PHIL system is approximated in continuous time for stability analysis as in [29], with Nyquist plot of the open-loop system subject to stability criterion determined by the number of encirclements of the point at $(-1, 0)$. If discrete-time approximation is considered, the Nyquist criterion for discrete systems can be employed. The open loop transfer function $H_{\text{OL}}(s)$, of the control loop in Fig. 4 can be represented as:

$$H_{\text{OL}}(s) = H_{\text{delay}}(s) \cdot H_{\text{PI}}(s) \cdot H_{\text{HUT}}(s) \cdot H_{\text{DRTS}}(s) \tag{26}$$

The stability condition for PHIL setups using ITM IA has been well discussed in literature and is typically considered as $Z_{\text{HUT}} > Z_{\text{DRTS}}$ [31], [32] when the PI is assumed ideal and only resistive components are considered. As the aim of this study is to demonstrate the impact of the time delay and its variability, the parameters Z_{HUT} and Z_{DRTS} have been chosen

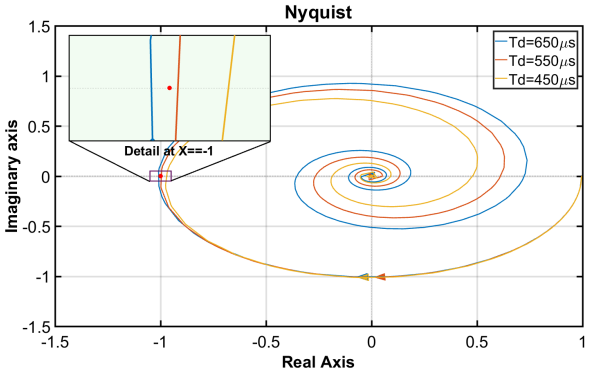

Fig. 5. Nyquist plot of time delay effect on PHIL.

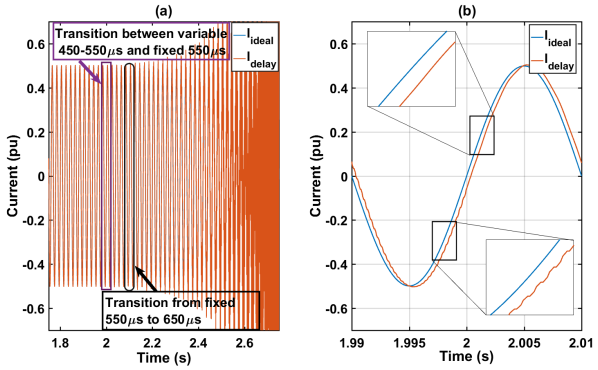

Fig. 6. Simulation assessment of stability and accuracy under variable time delay.

for a stable setup as resistive $1.005pu$ and $1pu$ respectively (i.e., $Z_{\text{HUT}} > Z_{\text{DRTS}}$). The damping ratio and the corresponding resonant frequency is ζ=0.63 and ω_{n}=6523.28rad/s. Assuming $T_{\text{d}} = [450,650,4]$, the stability is analyzed against the Nyquist criterion for the minimum, maximum and the average time delay.

In Fig. 5, the open loop Nyquist frequency response of the PHIL system has been plotted with positive frequencies. As can be observed, the system would be stable if a constant delay of T_{d}=450μs or 550μs is present. The stability margin decreases with increasing delay i.e., the contour moves closer to encircling the instability point (-1,0). The system would be unstable for a T_{d}=650μs, encircling the instability point even when the ratio between hardware and software impedance meets the requirements for a stable system. To summarize, the given system would lie between a stable and unstable region for a varying time in the total delay of 200μs, leading to instability. This illustrates the importance of considering the variability in time delay for PHIL simulations. Approximating time delay of PHIL setups or considering the delay to be constant can increase the risk and uncertainty of the experiments.

B. Impact of variability on accuracy

It has been established that the time delay affects the power factor of the HUT observed at the DRTS, leading to inaccurate active and reactive power exchanges compared to an ideal scenario. With a variable time delay, the response of the HUT will present a characteristic noise introduced by delay variations. Furthermore, the variations will introduce variability also in the injected power and could affect the voltage, the measurement of the signals and even to some controllers if no action is in place for its mitigation.

To demonstrate the impact of the variability in time delay, simulation based assessment of the described system in the previous sub-section has been conducted and is presented in Fig. 6. For the first 2s of the simulation, the delay, T_{d} is varied between 450 and 550μs every 300μs. As can be observed from Fig. 6 (a), the system is stable with this variable delay (from 0 to 2s) as expected from the stability assessment. However, the variability in delay presents itself as an oscillation as shown in Fig. 6 (b). At time t=2s, the simulation is switched to a fixed delay of 550μs, at which point the oscillations in the waveform cease. These oscillations will be observed as oscillations in power exchanged at the PCC, and can be significant if scaling of the currents is required. At time t=2.1s, the simulation is switched from a fixed delay of 550μs to 650μs, soon after which the system becomes unstable in accordance with the analysis presented earlier and as shown in Fig. 6 (a).

C. Reducing time delay

To improve the accuracy and stability of a PHIL setup, the time delay should be reduced to a minimum to achieve larger stability margins and the reproduction of faster transients. Once the time delay of the PHIL setup has been analyzed, different options for reducing the total time delay can be considered as below.

1) DRTS: The first improvement to consider towards decreasing the time delay is to reduce the simulation time step of the DRTS. The feasibility of decreasing the simulation time step will depend on the computational complexity of the simulated system and controls as well as on simulation platform hardware limitations. With the use of FPGA-based simulators the time step can be reduced to sub-microsecond levels. The level of improvement will depend on the initially chosen time step. If switched-mode amplifiers are used, decreasing the time step of the DRTS might not yield a significant reduction in total time delay due to the fixed step interactions (discussed earlier in Section III).

2) PI: For a switched-mode PI, similarly to the DRTS, if the control time step is reduced, the total delay can be reduced. This can be achieved in a number of ways, such as selecting a higher switching frequency of the converter to allow for faster control time steps (commercial converters have a range of 3-20kHz), or introducing a double update rate that will reduce the time step to half while maintaining the same switching frequency [27]. If a converter with a 20kHz switching frequency is selected instead of 3kHz device, a difference of 283.33μs in the time delay of the PI can be noticed without considering the variability. In terms of delay reduction, the ideal choice would be to use linear amplifiers, whose response can be in the order of nanoseconds, however limitations of cost and losses at high power ratings can restrict their use [26].

3) Communication: Replacing analog interfacing signals by fast digital communications protocols (such as Aurora or

PCIe) using fiber optic links avoids delays associated with ADC, DAC and signal filtering, establishing a fast connection with the external units while reducing the total time delay. Conversion times for different ADC and DACs can be in order of 10-100μs depending on the technology being used, this can be reduced to less than 1μs if fiber optic based communication is used instead (assuming less than 300m of cable).

4) Other delays: Using an external dedicated measurement for HUT response, the delay can be reduced in comparison with a setup where the measurement from the PI is used. The reduction in this case will at least be one PI control time step which can be up to 333.33μs when a 3kHz sampling rate is utilized. Furthermore, the use of filters, for different purposes such as anti-aliasing or low pass for improving stability, should be cautiously assessed, aiming at a maximum cut-off frequency with minimum delay.

D. Mitigating variability in time delay

The importance of including the variability of time delay in the assessment of stability and accuracy of PHIL setups has been demonstrated. In this sub-section, two options for improving PHIL simulations with variability in time delay are discussed.

1) Mitigating impact of time delay variability: To mitigate the impact of variability of time delay, a low pass filter can be employed to filter the oscillations due to the discrete time steps of the DRTS and PI. With low filter cutoff frequencies, the oscillations will be further reduced and abated. The filter will add its own delay, increasing the total time delay which could be compensated by time delay compensation methods. Depending on the characteristics of the filter used for abating the oscillations, harmonics of interest may be filtered out and the accuracy of the implementation reduced. It should also be noted that some filters have different phase lags at different frequencies and if time delay is to be compensated this has to be considered. At the same time, by adding a low pass filter the stability of the PHIL simulation can be improved [16].

2) Eliminating variability in time delay: The variability in time delay is introduced as a result of the interaction between two components with discrete time step computation. There are two ways to approach eliminating this variability:

(i) to ensure there is no waiting time for any input to be accepted by the receiving fixed discrete component upon its arrival, i.e., to ensure $T_{var} = 0$. Analytically, rearranging Eq. 10, 11, 12 and 13, the criteria is obtained as:

$$m_1 T_{\text{PI}} = T_{\text{DRTS}} + T_{\text{com}_{\text{FF}}} + T_{\text{com}_{\text{FB}}} \tag{27}$$

$$m_2 T_{\text{DRTS}} = T_{\text{PI}} + T_{\text{com}_{\text{FF}}} + T_{\text{com}_{\text{FB}}} \tag{28}$$

where m_1 and m_2 are integers defined as:

$$m_1 = \text{ceil}\left(\frac{T_{\text{loop}_{\text{PI}}}}{\tau_{\text{s}_{\text{PI}}}}\right) \tag{29}$$

$$m_2 = \text{ceil}\left(\frac{T_{\text{loop}_{\text{DRTS}}}}{\tau_{\text{s}_{\text{DRTS}}}}\right) \tag{30}$$

(ii) to find a suitable combination of time step of the discrete components such that the time delay at the PCC of the DRTS is constant. This can be achieved when for any possible value of $T_{\text{var}_{\text{PI}}}$, the variation of the external loop delay to the DRTS, $T_{\text{loop}_{\text{DRTS}}}$, remains within one time step of the DRTS. This condition for achieving constant time delay can be mathematically expressed as:

$$\text{ceil}\left(\frac{T_{\text{loop}_{\text{DRTS}}}}{\tau_{\text{s}_{\text{DRTS}}}}\right) = K \quad \forall T_{\text{var}_{\text{PI}}} \in [0, \tau_{\text{s}_{\text{PI}}}] \tag{31}$$

where K is a constant integer number. This condition is assessed, in a step by step procedure by which a single $\tau_{\text{s}_{\text{DRTS}}}$ is evaluated at a time for all possible values of $T_{\text{var}_{\text{PI}}}$, with $\tau_{\text{s}_{\text{PI}}}$ selected beforehand (as it can typically incur into hardware limitations). This process is repeated for any $\tau_{\text{s}_{\text{DRTS}}}$ of interest, identifying specific values of $\tau_{\text{s}_{\text{DRTS}}}$ that will satisfy the condition. If a large $\tau_{\text{s}_{\text{DRTS}}}$ is calculated, this might not always be an option as the increased time delay can lead the system to instability or an increased time step might not be appropriate for the type of study being undertaken. However, if the system is stable with the increased delay and the time step is suitable for the study to be undertaken, this larger time step will eliminate the variability.

V. Validation of Time Delay Characterization

For the validation of the variability in time delay and the proposed characterization methodology, two different case studies have been developed which will be analysed theoretically and experimentally. The case studies are:

- Case A: A time synchronized signal between DRTS and power interface.
- Case B: A PHIL platform with a digital communication interface.

For the two validation case studies, DRTS and PI with the same configuration and hardware components have been used as shown in Fig. 7. The specific characteristics of the hardware components used are:

- DRTS: A Real-Time Digital Simulator (RTDS), with capabilities similar to other DRTS in the market has been used. Different time steps have been utilized within each case study.
- PI: A switched-mode back-to-back converter is used as the PI, which can have different control frequencies (consequently different time steps), incorporating a control algorithm with a double update rate of the PWM signal, increasing the control frequency and thereby reducing the time delay.

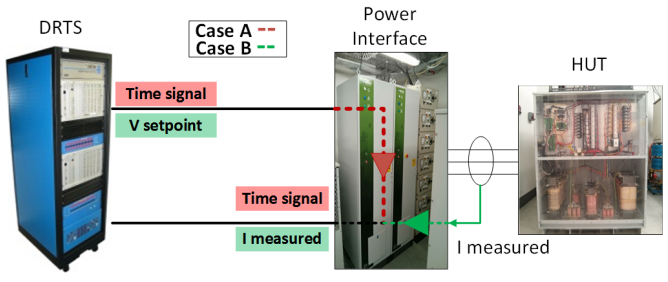

Fig. 7. PHIL experimental setup for Case A and B.

A. Case A: Validation with a time synchronized signal

For an accurate analysis of the time delay and its dynamic behaviour, a time synchronized signal (with GPS clock) is transferred from the DRTS to the power interface real-time control target with a fast digital communication link established between DRTS and PI. The signal is then sent straight back to the DRTS for closing the loop as shown in Fig. 7 (red). In this manner the loop delay of the setup can be analysed without uncertainties introduced by the measurement of the HUT response. This case study is presented for an initial analysis of the characteristics of the time delay in PHIL setups as identified in the previous sections, and hence it will provide the loop delay between the DRTS and the PI without taking into account the HUT, allowing for the verification of the behaviour of the DRTS, PI and the digital communication link.

In this case as the signal is directly routed to the output, T_{PI} is considered as only one time step rather than the two typically used when the HUT currents are measured by the PI. The time step of the PI is chosen as $\tau_{\text{s}_{\text{PI}}}$=66.667$\mu$s (15kHz). The communication delay of the feed-forward path in this case, due to a handshake process between the two ends of the serial link has been identified as:

$$\tau_{\text{algorithm}} = \begin{cases} \tau_{\text{s}_{\text{PI}}} - \tau_{\text{s}_{\text{DRTS}}}, & \tau_{\text{s}_{\text{PI}}} > \tau_{\text{s}_{\text{DRTS}}} \\ 0\mu\text{s}, & otherwise \end{cases} \tag{32}$$

by which, the PI needs to be the one establishing the communication and hence if $\tau_{\text{s}_{\text{PI}}}$ is larger than $\tau_{\text{s}_{\text{DRTS}}}$ the difference in time step is added to the communication delay, otherwise no extra delay is considered. The time delay of the fiber in this case is considered as τ_{fiber}=2μs. These types of considerations will need to be assessed on a case by case basis depending on the infrastructure and devices being used for the test.

1) Theoretical characterization: Multiple theoretical assessments have been performed with different $\tau_{\text{s}_{\text{DRTS}}}$ (from 10 to 60μs in steps of 10μs and 80, 100, 120, 150, 200μs). Time steps larger than 200μs have not been considered as variability saturates due to the time step of the DRTS being larger than its total outer loop delay (i.e., T_{DRTS}>$T_{\text{loop}_{\text{DRTS}}}$), and therefore always receives the response value before the start of the next time step. In this case T_{DRTS}=$\tau_{\text{s}_{\text{DRTS}}}$ as no coupling delay exists. For each different T_{DRTS} assessed the values of the characterized time delay for this particular PHIL implementation have been calculated with the conventional characterization method as well as with the proposed characterization presented in Section III. The characterized time delays for each implementation are presented in Table I.

2) Experimental assessment: For the validation in the experimental setup, the time synchronized signal is sent to the PI and when the time stamped signal is received at the DRTS the actual time is compared with the signal received, in this manner an accurate calculation of the total loop delay can be determined. In Fig. 8, four examples of the measured total delay per time step are shown. Each of the plots presenting different variations, from n=5 when $\tau_{\text{s}_{\text{DRTS}}}$=20$\mu$s, to a fixed delay, n=0, when $\tau_{\text{s}_{\text{DRTS}}}$=150$\mu$s.

The experimentally identified delay steps in these cases are equal to the ones identified theoretically by the proposed characterization method and presented in Table I. This process has been also carried out experimentally for all the other $\tau_{\text{s}_{\text{DRTS}}}$ theoretically assessed, with each of the experimental results generating the same delay variability characteristics as theoretically identified in Table I, thereby validating the time delay characterization approach presented in this paper. The suitability of time delay characterization is confirmed, also proving the existence of time delay variability in PHIL simulations which can adversely impact its stability and accuracy. However, a full PHIL implementation is also required to complete the analysis. In contrast, it can be observed that the conventionally identified time delay greatly differs from the delay experimentally measured. The total time delay identified conventionally appears to be always smaller than the measured one and at the same time the conventional method does not provide any measure of the variability of the time delay.

TABLE I
THEORETICAL TIME DELAY CHARACTERIZATION

PHIL Setup			Conventional Time Delay Characterization	Proposed Time Delay Characterization
T_{DRTS} [μs]	T_{PI} [μs]	T_{Dcom} [μs]	$Eq.9$ [μs]	$Eq.21$ [μs, μs, -]
10	66.667	58.667	135.334	[140, 210, 7]
20	66.667	48.667	135.334	[140, 240, 4]
30	66.667	38.667	135.334	[150, 210, 2]
40	66.667	28.667	135.334	[160, 240, 2]
50	66.667	18.667	135.334	[160, 240, 2]
60	66.667	8.667	135.334	[180, 240, 1]
80	66.667	4	150.667	[160, 240, 1]
100	66.667	4	170.667	[200, 300, 1]
120	66.667	4	190.667	[240, 360, 1]
150	66.667	4	210.667	[300, 300, 0]
200	66.667	4	260.667	[400, 400, 0]

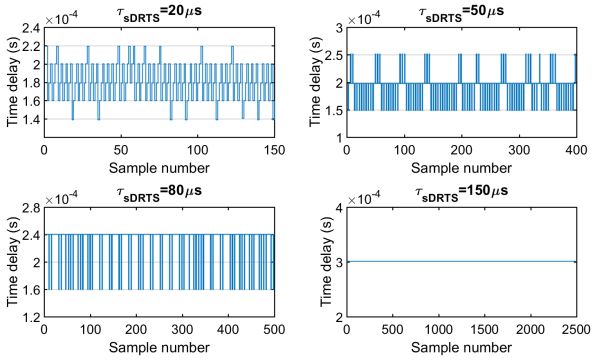

Fig. 8. Experimentally measured time delay variations.

B. Case B: A PHIL platform with a digital communication interface.

In this case, a resistive load bank has been added as the HUT with its measurement processed by the PI and sent back with the digital communication link as shown in Fig. 7 (green). Voltage ITM is chosen as the IA for the setup i.e., communicating a voltage setpoint to the power amplifier, and the consequent current response from the HUT to a controlled current source at the simulation end. The simulated part of the system comprises a voltage source and a small impedance Z_{DRTS}=$0.066\Omega/phase$ for a stable PHIL implementation, as the HUT impedance is much larger, Z_{HUT}=$15.87\Omega/phase$,

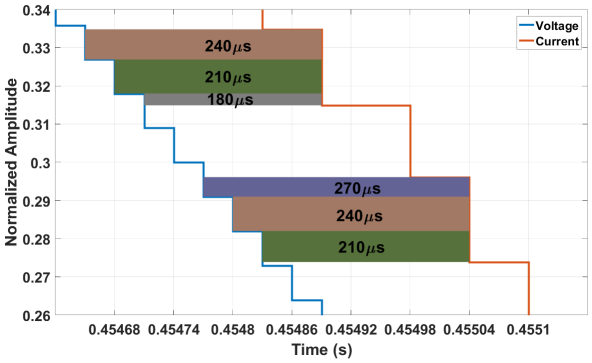

Fig. 9. Experimental delay assessment for T_{DRTS}=30μs.

and therefore the condition of stability will be met. This simple setup allows for an effective study of the time delay of the setup, as using a pure resistive component as the HUT, ensures voltage and current are in phase when no time delay is present. Therefore, by comparing the voltage and current waveforms at the simulation PCC the total time delay can be readily identified. The aim in this case is to identify the total loop delay of the PHIL setup, and by doing so validate the time delay characterization formulation along with the dynamic behaviours identified theoretically and experimentally in Case A. In contrast with case A, for the theoretical assessment of the total delay, T_{PI} is considered as $2\tau_{\text{s}_{\text{PI}}}$. T_{Dcom} remains the same as in Case A (the digital communication link remains same). The experiments considered for the assessment of the time delay in this case are for:

$$\tau_{\text{s}_{\text{DRTS}}} = [30, 40, 60, 80, 100, 120, 150, 200]$$

With the HUT connected, its response is fed back to the DRTS, leading to a complex measurement procedure of the loop delay. This is due to the fact that the time delay can vary in very short time periods (up to every time step). Therefore, solutions such as Fourier transforms (for the measurement of the phase difference of the fundamental) or the calculation of the phase difference at zero crossing of the voltage and current signals for evaluating the time delay are not accurate enough. The main reason being that the response will only be calculated every fundamental cycle as opposed to the per time step solution required in this case. Accordingly, as a resistive HUT is used, by using normalized voltage and current waveforms, the time delay has been considered as the time distance between the voltage and current waveforms when both of them present the same normalized amplitude (as in an ideal situation that would be the case at zero crossing). Hence, a step by step procedure for identifying the time delay has been developed with the help of a Matlab script using the data recorded from experiments as shown in Fig. 9 for an example with $\tau_{s_{DRTS}}$=30μs.

Experimental results have been obtained by calculating the delay between voltage and current waveforms as presented in Fig. 9 for half cycle of the fundamental waveform and values between 0.9pu and -0.9pu of the normalized amplitude. The experimental results are presented in Fig. 10 by means of a box plot for each of the experiments performed.

TABLE II
TIME DELAY OF PHIL WITH DIGITAL COMMUNICATION LINK AND $\tau_{\text{s}_{\text{PI}}}$ =66.667μS

$\tau_{\text{s}_{\text{DRTS}}}$ [μs]	Theoretical Delay [μs] [μs, μs, -]	Experimental Delay [μs] [μs, μs, -]
30	[210, 270, 2]	[180, 270, 3]
40	[240, 280, 1]	[200, 280, 2]
60	[240, 300, 1]	[240, 300, 1]
80	[240, 320, 1]	[240, 320, 1]
100	[300, 400, 1]	[300, 400, 1]
120	[360, 360, 0]	[360, 480, 1]
150	[300, 450, 1]	[450, 600, 1]
200	[400, 600, 1]	[400, 600, 1]

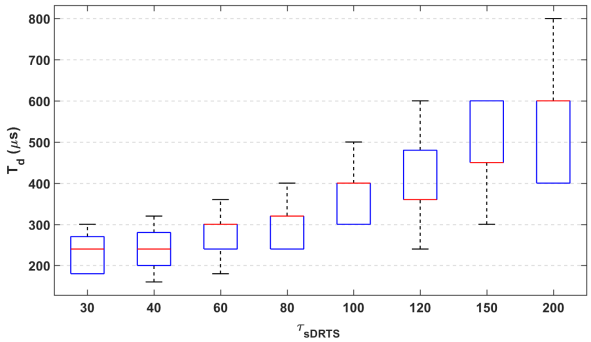

Fig. 10. Experimentally measured time delay for Case B

The components that form the whiskers of the box plot are considered to be produced by the noise introduced by the hardware and its measurements and by the actual calculation procedure of the total time delay. Consequently, in Table II theoretical and experimental time delays with $\tau_{\text{s}_{\text{PI}}}$=66.667$\mu$s are presented, considering the experimental delays as the box section of each experiment (as it represents the likely range of variation). Experimentally measured time delays can present a one time step variation from the theoretically calculated delay as can be observed in Table II. For the small time steps, the reduction in experimentally measured delay can occur due to the slack time (time between the finalization of the control calculation and the end of the time step) of the PI, as this can trigger the signal to be fed back prior to the theoretically assumed end of the time step. The knowledge acquired from the characterization can help reduce the total loop delay of the PHIL implementation while enabling more effective time delay compensation mechanisms to be employed when the exact delay is known. In addition, by using the condition presented in Eq. 19, DRTS time steps that would meet the condition for a fixed delay have been identified as 68μs and from 102 up to 121μs. This is in perfect alignment with the theoretical results from Table II, validating the theoretical condition for constant delay. However, the exact figure of 68μs is very limited as variations on the identified delays of the individual components by more than 1μs can make it fail. Similarly this can be observed with the range from 102 up to 121μs, as only 120μs has been experimentally assessed an error larger than 2μs would cause a variable delay, and in this case variable delay has been identified for 120μs as presented in Table II.

VI. Conclusions

This paper has proposed and validated a time delay characterization method for accurately calculating and identifying time delays and their variability for PHIL experiments. Novel formulations for measuring the total time delay in a PHIL simulation have been developed and validated through an experimental PHIL implementation. The presented detailed analysis has led to the identification of a variable time delay present in PHIL implementations with switched-mode PI, that has not been identified before, and its impact on PHIL simulations has been analysed. The identified variable time delay produces oscillatory behaviours that can be mistaken with communication or measurement noise. With the knowledge acquired through application of this delay characterization, it is now possible to reduce the risk of PHIL simulations performing meticulous stability and accuracy assessments. Moreover, measures for the reduction of the total time delay in PHIL have been discussed. Mitigation techniques along with a formulation for the calculation of parameters that can lead to the elimination of delay variability have been presented, which will improve the stability and accuracy of PHIL simulations and also the accuracy of time delay compensation techniques. Accordingly, future work will be focused on the development of an online time delay identification technique in the absence of time synchronization signal and time step optimization for a reduction in time delay variability. Furthermore, studies will pursue the probabilistic identification of delay with the objective of achieving an optimal time delay compensation for PHIL simulations.

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