An Improved Voltage-based Protection Scheme for an LVDC Distribution Network Interfaced by a Solid State Smart Transformer

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Abstract: The increasing electrification of transport and heat will place increasing demand on low voltage (LV) networks with the potential to overload MV/LV transformers and LV cables. Deployment of a solid state transformer (SST) at MV/LV substations and using LV Direct Current (LVDC) distribution systems offer great potential to address such challenges. However, the SST deployment in addition to the introduction of LVDC will fundamentally change LV fault behaviour and protection requirements due to the limited short-circuit capabilities of such technologies. The SST will deliver limited fault currents, making current-based protection (widely used in LV networks) less reliable. Therefore, this paper presents an advanced communication-less protection scheme which can effectively detect and locate DC faults even with reduced fault levels. The developed protection scheme overcomes the selectivity limitations in LVDC voltage-based protection solutions by using a combination of DC voltage magnitude, voltage concavity (sign of d^2v/dt^2) and the sign of the rate of change of current (di/dt) regardless of the current magnitudes. The credibility of the developed protection algorithm is tested against different fault scenarios applied on an active LVDC network model built in PSCAD/EMTDC. Noise signals have been included in the simulation to appraise the resilience of the developed scheme.

1. Introduction

Existing low voltage (LV) distribution networks are already under pressure to host growing numbers of low carbon technologies such as electric vehicles, heat pumps, electrical storage, micro winds and solar generation. For example, the sale of petrol and diesel vehicles will be banned and replaced by electrical vehicles (EVs) in many countries such as in Norway by 2025, Germany by 2030 and the UK by 2040 [1]. Such a radical change in the transport sector in addition to the electrification of heat (e.g. heat pumps) will add a significant demand to existing LV networks. Considering the UK as an example under a future low carbon scenario, the high penetration of electrical vehicles is expected by 2050 to result in an annual demand of up to 90TWh [2]. This represents an increase in demand by 30% from 2017. Also, heat pumps are expected to dominate in the UK by 2050 with the expectation that the use of gas boilers will fall by 70% of present volume [2]. These will require a large investment, estimated to be £30-45 billion for the UK grid and as such, radical solutions in LV networks will be needed for meeting these expect demand increases [3]. LV Direct Current (LVDC) distribution systems have recently been recognised by a number of industrial and research groups as one of the preferable solutions to alleviate the strain and increase the capacity of existing LV networks in order to meet this anticipated growth in transport and heat demand [4, 5].

The LVDC implementations at present are still at the stage of research and trial. However, the total annual implementation spending for DC distribution is expected to exceed $48.4 billion by 2027 as reported in [6]. Benefits such as energy saving and enhanced controllability have already been demonstrated by few trials available across the world [7, 8]. To pave the way for wider LVDC uptake, this effort has been recently supported by technical guidance and standards development by the International Electrotechnical Commission (IEC) [9]. One of the key challenging areas identified by different research and by the recent IEC LVDC technology report is the need for reliable DC protection solutions that can provide adequate protection with a good level of safety, selectivity and resilient operation [10, 11].

In general, the design and performance of LVDC protection schemes are highly influenced by the interface between the main grid and the LVDC last mile. Two-level voltage source converters (VSCs) have been widely used for connecting LVDC to AC grids due to their simplicity and low cost. However, they do not provide any fault control capabilities and hence require higher equipment ratings and fast protection due to high di/dt and high fault current infeed from the AC grid. There are already a number of DC protection solutions available in the literature to meet such requirements [12-15]. Very recently, new innovative interface technologies such as solid state transformers (SSTs) have been proposed to replace conventional transformers at medium to low voltage (MV/LV) secondary substations with the additional capability to provide both LVAC and LVDC supply [16]. A 250kVA SST has already been implemented in an LVDC pilot project presented in [17] to convert 10kV AC to 560V DC. The SST deployment has also been considered for a real utility-owned MV/LV (DC and AC) distribution systems to provide more effective voltage control, independent real and reactive power control, and bidirectional real power control [18]. From a protection perspective, the SST will provide reduced prospective fault currents and potentially enable the use of equipment with lower current ratings. However, its deployment at distribution substations will fundamentally change fault profiles on the associated LVDC distribution networks. With suitable controls and configuration, the SST can limit and completely block fault current contributions from the AC grid for the purpose of self-protection against faults. Consequently, reducing the magnitude of prospective fault currents by the SST will make the widely used LV overcurrent-based protection solutions less reliable [19]. There are a few

methods that have been proposed in the literature which use the changes in voltage profiles as an alternative to detect DC short circuit faults with limited fault current. However, due to the relatively small values of DC cable impedances, the DC voltage disturbance will propagate very rapidly, leading to protection coordination and selectivity challenges.

Therefore, this paper presents an enhanced DC voltage-based protection scheme to rapidly detect and precisely locate DC faults in a faulted SST-interfaced LVDC distribution network. The developed scheme does not require communication links while the protection actions of the relays are all driven by local measurements of a combination of parameters including DC voltage magnitude, DC voltage concavity (sign of d^2v/dt^2, extracted from the increasing and decreasing trends of rate of changes of DC voltages (dv/dt)), and the sign of rate of change of fault currents (di/dt) regardless of the current magnitudes. To achieve this objective, the paper is structured as follows. Section II outlines the key protection challenges, state of the art and solutions associated to an LVDC network interfaced by an SST. Section III explains in detail the principles of the developed protection scheme. Section IV presents simulation studies for testing the performance of the proposed scheme against different DC faults. Finally, the conclusions of the paper are given in section V.

2. Protection challenges of a SST-interfaced LVDC distribution network

The deployment of SSTs as an innovative technology to improve the controllability and flexibility of secondary substations has recently attracted the interest of a number of utilities and researchers [20]. With regards to LVDC, the SST can either be configured as a two-stage conversion (shown in Fig. 1 (a)) to provide dedicated LVDC outputs, or as a three-stage (shown in Fig. 1 (b)) to provide both DC and AC outputs. The introduction of the SST at secondary substations and its associated LVDC network will introduce new forms of faults. Especially for the steady state DC fault current, as shown in Fig. 2, it is quite limited with two-stage SST compared to the typical fault current with a two-level VSC that can potentially impact existing protection performance. For example, the research in [21] and [22] have concluded that the constraints on the SST's contribution to the fault current can have a significant impact on the operation and coordination of overcurrent relays. In response to this, a number of DC voltage-based protection methods have been proposed and developed by different researchers for protecting DC systems against limited prospective fault currents. The research developed in [23] has proposed the usage of under-voltage to detect DC faults and dv/dt for fault discrimination. Another method proposed in [24] involves estimating the impedance within the DC fault path using the ratio between the DC steady state voltages and fault currents in order to identify the fault location in a DC ring microgrid. In addition to these, a new protection method called "Prony's method" is developed in [25] to estimate DC fault locations using attenuation factors and angular frequencies extracted from the voltage resonance when the fault is initiated.

The aforementioned voltage-based protection methods may be sufficient for protecting against faults on LVDC downstream feeders, but cannot guarantee adequate protection with a good level of selectivity for upstream faults. The upstream faults are referred to as DC pole-to-pole SST internal faults, faults on the main DC bus and faults at the beginning of the outgoing DC feeders and are shown in Fig. 1 as faults at location 1, 2, and 3 respectively. In this case, the SST will experience the same changes in the current and voltage for the internal fault at location 1, the faults at the main bus at location 2 and at the beginning of the LVDC feeders at location 3. This could potentially lead to unnecessary trip of the SST for faults at the main bus or at the main feeders, leading to unnecessary power outages of healthy parts. The relays of outgoing healthy LVDC feeders will also see the same under-voltage and dv/dt as seen by the relay of the adjacent faulted feeder. With voltage-based protection, the healthy feeders will be tripped in this case.

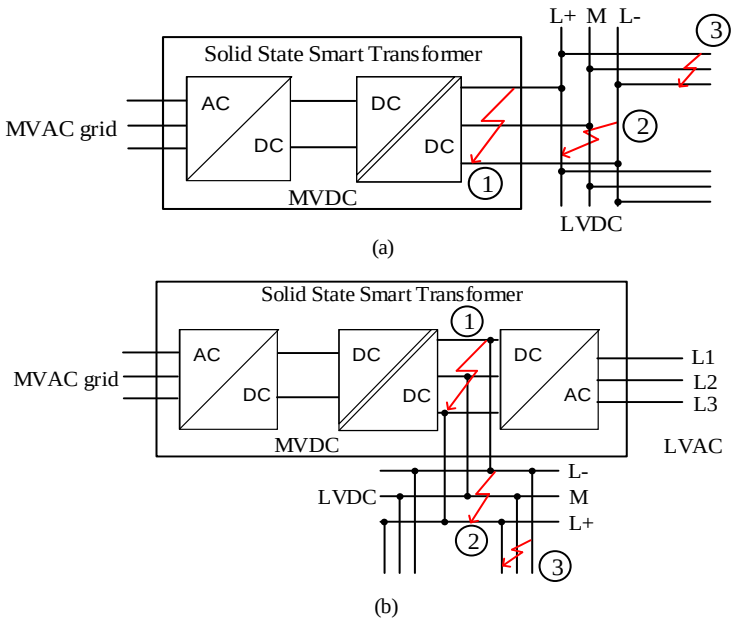

Fig. 1. *A solid state transformer (SST) layout: (a) two-stage SST with DC outputs, and (b) three-stage SST with DC and AC outputs*

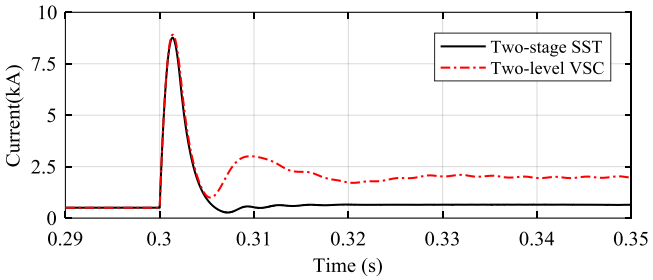

Fig. 2 *Fault current comparison between two-stage SST and two-level VSC*

For other applications such as HVDC systems, the research in [23] has proposed the addition of an inductance at the start of the DC line to create a voltage drop (Δv) which can be used to distinguish between faults on the main DC bus and faults at the beginning of the line by using different dv/dt thresholds. The issue with this method is that any resistive fault on the main bus with relatively high Δv will be seen as a remote fault on the DC lines. In this case, the error in the fault location estimation will be increased as the resistance of the fault increases and dominates the fault path impedance [24].

Therefore, this paper presents a new DC protection scheme which improves the performance of a voltage-based protection method to provide a good level of selectivity and discrimination between upstream and downstream faults in an LVDC distribution network. The new developed protection scheme implements the direction of the slope of the rate of fault current change (di/dt) (i.e. whether the direction is moving towards uphill or downhill) in combination with voltage magnitudes and voltage concavity (sign of d^2v/dt^2, extracted from rate of change of voltages during the fault). Compared to existing under-voltage and dv/dt based protection methods with fixed thresholds, the concavity of the voltage enables upstream and resistive DC faults to be accurately detected and located. The proposed protection scheme is discussed in more detail in the following sections.

3. An Improved Voltage-based Protection Scheme for Fast Detection and Location of LVDC Faults

This section presents the protection algorithm of the developed scheme, depicted in Fig. 3, and its principles are explained as follows.

3.1. Measured parameters for the protection scheme

The key parameters measured by the local relays within the protection algorithm as shown in Fig. 3 are the DC voltages and their rates of change (dv/dt) along with the DC currents and their rates of change (di/dt) (direction of the slope). An assistive inductance is also used at the beginning of each DC feeder to create additional boundaries to enhance the discrimination of the voltage responses under different short circuit faults. In general, the measurements of these parameters are exposed to different levels of noise which can be caused by measurement devices. Thus, a moving-average low pass filter is used to eliminate the noise of all measured di/dt and dv/dt profiles.

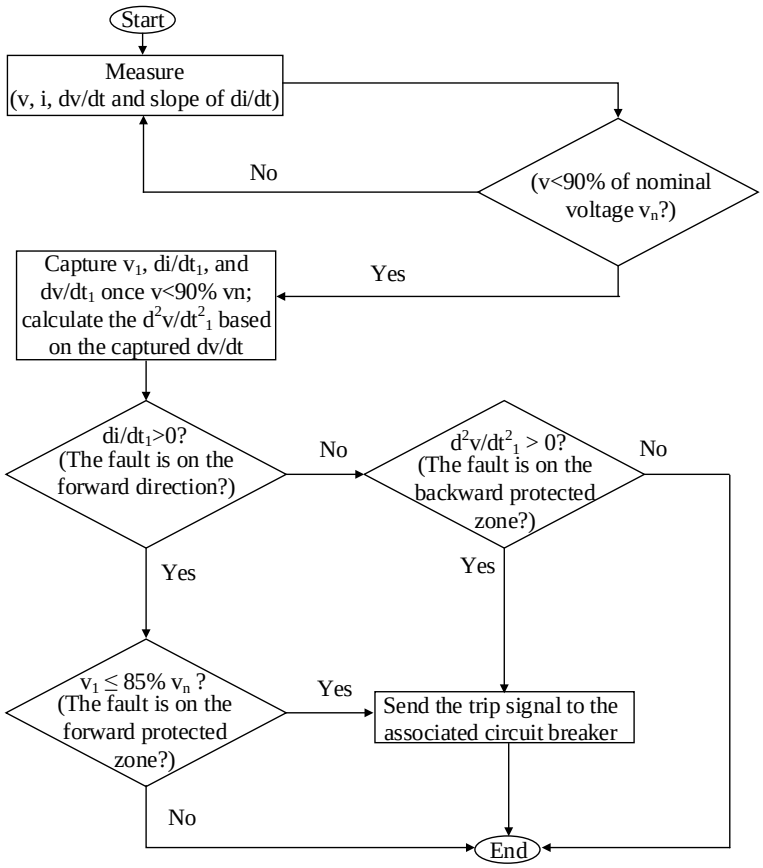

Fig. 3. *The developed protection algorithm*

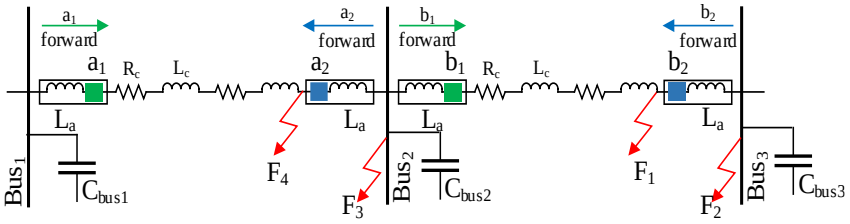

Fig. 4. *A simplified single line diagram of LVDC feeders*

3.2. LVDC fault detection

The LVDC distribution network is considered to be under faulted conditions if the DC voltage decreases to < 90% of the nominal operating voltage (v_n) (defined as δ_1). No standard exists governing DC voltage variations of LVDC public distribution networks and thus this value is chosen based on the recommendations from the IEC60092-101 for marine-based DC distribution systems. During fault conditions, voltage, dv/dt and di/dt will continue to change until they reach their steady state. Therefore, the captured transient di/dt and dv/dt values (immediately after the fault is detected) are recorded and used for fault location and selective tripping.

3.3. LVDC fault location and protection selectivity

A simplified single line diagram of LVDC feeders is presented in Fig. 4 and is used to explain how the developed protection scheme can distinguish between different DC faults at different locations. A capacitor is added to each bus to emulate the smoothing capacitors present in converters. The relays at the beginning of the feeders 'a_1' and 'b_1' are defined to consider the current flow from upstream to downstream (i.e. left to right) as the forward direction in respect to their locations. The relays at the end of the feeders 'a_2' and 'b_2' are defined to consider the current flow from downstream to upstream (i.e. right to left) as their forward direction. If the measured di/dt is positive, the fault lies in the forward direction, otherwise, the fault is located in the backward direction with respect to the relay location. Each protection device has its own protected region and it will operate as soon as any fault is located within this region. For example, looking at the protection relay 'b_1', it should operate when faults are located within the cable region between relays 'b_1' and 'b_2' and at the backward bus (Bus_2). Whatever the fault condition (i.e. forward or backward), its location can be defined as follows.

3.3.1. Forward fault location

A DC pole-to-pole fault located at F1 (see Fig. 4) is selected as an example to illustrate the voltage responses of the relay 'b_1' under a forward fault condition. Before the fault happens, the voltage of relay 'b_1' is equal to the DC nominal voltage (v_n). After the fault is initiated, the transient voltage change at relay 'b_1' can be defined as follows.

$$v_{bus2}(0^-) = v_{bus2}(0^+) = v_n \tag{1}$$

The voltage measured at bus_2 can be written as in (2). Where, v_{bus2} is the voltage at bus_2, v_{fault} is the voltage at the fault point (F1), L and R are the inductance and resistance from the bus_2 to the fault point (F1) and i is the current that flows in the cable section from the bus_2 to the fault point (F1). At the start of the fault (i.e. at time (0^+)), the transient voltage, v_{fault}, at the fault point (i.e. between positive pole and the negative pole) is almost zero due to the relatively small impact of the cable capacitor. Therefore, at time (0^+) immediately after the fault initiates, the initial current magnitude is relatively small. As a result, the term ($i \cdot R$) is relatively small and can be neglected, allowing the formula presented in (2) to be simplified as in (3). The voltage difference between the voltage at the relay measured point and the voltage at the fault point is directly influenced by the equivalent inductance between these two points. For example, as shown in Fig. 4 and at time (0^+) immediately after the fault F1 happens, the transient voltage at the bus_2 (where the relay 'b_1' is connected to through assistive inductance (La)) can be expressed in (4).

$$v_{bus2} - v_{fault} = L \cdot \frac{di}{dt} + i \cdot R \tag{2}$$

$$v_{bus2} = v_n \approx L \cdot \frac{di}{dt} \tag{3}$$

$$v_{b1-F1}(0^+) \approx \frac{v_{bus2}(0^+)}{L} \cdot L' = \frac{v_n}{L_{cable} + L_a} \cdot L_{cable} \tag{4}$$

The size of the assistive inductance (L_a) can easily be calculated from (4) in accordance with the transient voltage drop settings. In this paper, 85% of v_n (defined as δ_2) is selected as a transient voltage drop setting to restrict the maximum size of the assistive inductance (La) to 10% of the total cable inductance. After the fault is detected, if the captured transient voltage (i.e. immediately after the fault is initiated) is below 85% of the nominal voltage (v_n), and the di/dt slope is positive, then the fault is located within the forward protected region of the associated relay.

3.3.2. Backward fault location

As for backward faults (e.g. fault F3 in Fig. 4 in respect to relays b_1 and a_2 locations) and as discussed in section II, it is very important to ensure that resistive faults do not impact the accuracy of detecting and locating DC faults. Taking relay b_1 in Fig. 4 as an example, the resistive fault at location F3 can potentially lead to ≤ dv/dt for a fault at F4. To explain this further, Fig. 5 shows the trace of the resultant dv/dt of a pole-to-pole fault at the location F3 for varying resistance. It can be clearly seen from Fig. 5 that for any fault with a resistance

$\geq 0.05\Omega$, the dv/dt will overlap with solid faults at location F4. This means the relays b_1 and a_2 will both see any faults at Bus2 with a resistance $\geq 0.05\Omega$ as out of their protected backward regions and hence none of them will operate if the protection relies solely on dv/dt thresholds as proposed in the literature [23]. To overcome this issue, the developed algorithm in this paper utilises multiple points of dv/dt to identify the concavity of the voltage behaviour. The voltage concavity under faulted conditions is derived as follows.

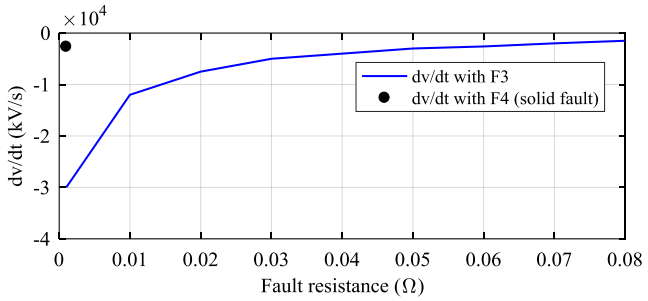

Fig. 5. *dv/dt measured at bus_2 under fault F3 with different fault resistance*

When a resistive fault occurs at location F4 (see Fig. 4), an RLC circuit consists of the fault resistance (R_f), the assistive inductance (L_a) and the bus_2 smoothing capacitor (C_{bus2}) within the fault path. The current leaving bus_2 (i_{bus2}) can be expressed as in (5), and the derivative of (5) yields equation (6). Since the di/dt of the bus_2 smoothing capacitor is positive, the secondary rate of change of voltage has to be negative. This means during the transient period of the fault at location F4, the magnitude of the dv/dt is increasing with a negative slope and the voltage drops with a convex trend.

$$i_{bus2} = -C_{bus2} \cdot \frac{dv_{bus2}}{dt} \tag{5}$$

$$\frac{di_{bus2}}{dt} = -C_{bus2} \cdot \frac{d^2 v_{bus2}}{dt^2} \tag{6}$$

On the other hand, when a backward fault occurs at location F3 (see Fig. 4), a resistor-capacitor (R-C) circuit is formed. In this case, the di/dt is negative and the sign of the second derivative of voltage (d^2v/dt^2) is positive. This means that during the transient period of the fault F3, the magnitude of the dv/dt is decreasing with a negative slope and the voltage drops with a concave trend. The voltage concavities calculated at bus_2 and relay b_1 are similar.

Consequently, the protection selectivity of the developed protection algorithm is defined as follows.

- If $(di/dt>0) \cap (v_1 \leq 85\% v_n)$, the fault is located within the relay forward protected region.
- If $(di/dt<0) \cap (d^2v/dt^2>0)$, the fault is located within the relay backward protected zone.

3.3.3. Converters fault discrimination and coordination with downstream protection

Voltage concavity-based fault detection is also integrated within the SST interface to distinguish between faults on the main SST terminals (i.e. PCC) and the fault at the beginning of outgoing feeders. If the sign of d^2v/dt^2 as seen by the SST is positive, then the fault is located at the PCC. Whilst, if the sign of d^2v/dt^2 is negative, the fault is located at the beginning of the feeder (i.e. after the assistive inductance of the faulted feeder). Based on the fault location, the SST is considered to provide two key protection functionalities. For faults at the PCC, the SST will act as a circuit breaker and interrupt the fault infeed from the grid side. When faults happen at the beginning of the LV feeders, the SST limits the fault current first to facilitate safe interruption of the fault currents by the circuit breakers.

4. Testing of the protection scheme performance through transient simulation studies

The performance of the developed protection scheme is evaluated through transient simulation studies. A representative LVDC distribution network is built in detail using PSCAD/EMTDC. The test network model is described next, followed by simulation studies of different DC fault scenarios.

4.1. Test network modelling

4.1.1. An LVDC distribution network model

An LVDC test network as depicted in Fig. 6 is developed and used for the studies. The LVDC network is interfaced to an AC grid through a two-stage SST. The SST provides ±750V DC at the point of common coupling (PCC). The MVAC grid is modelled as a voltage source with an equivalent impedance to provide a practical fault level representative of an urban MV/LV network [26]. The LVDC feeders are modelled as an equivalent resistance in series with an inductance with each feeder assumed to be 250m long. A summary of the parameters of the developed test network are given in Table 1. The LVDC network supplies four loads, each modelled as a lumped (200kW) load and interfaced to the LVDC network through dual active bridge (DAB) DC-DC converters with galvanic isolation transformers. The local sources are modelled as ideal DC voltage sources.

Table 1 *Parameters of the modelled LVDC distribution network*

Parameter	Value
AC supply	11kV
Fault level	156MVA
SST capacity	1MVA
SST DAB parameter	20kV DC/±750V DC, switching frequency 20kHz, LV smoothing capacitor 10mF, choke inductor 0.5mH [27]
MVDC voltage	20kV (pole-to-pole)
LVDC voltage	±750V (pole-to-pole)
LVDC cables	0.164 Ω/km, 0.00024 H/km, 250m each section
DC customers	200 kW each
Local DC source	200V
Assistive inductors	0.011mH for each pole

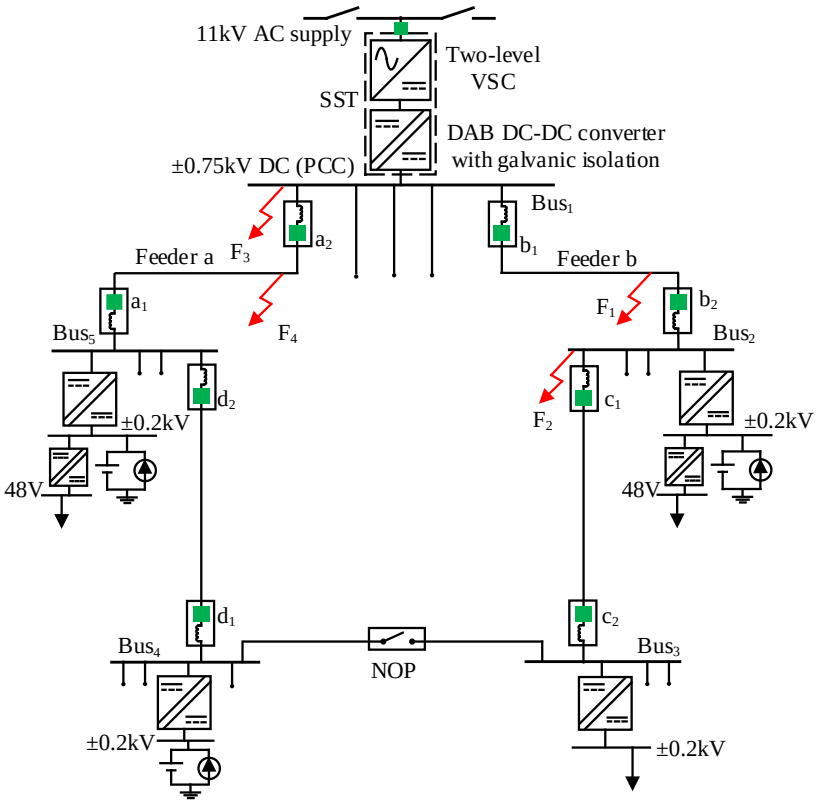

Fig. 6. *A test model of an LVDC distribution network*

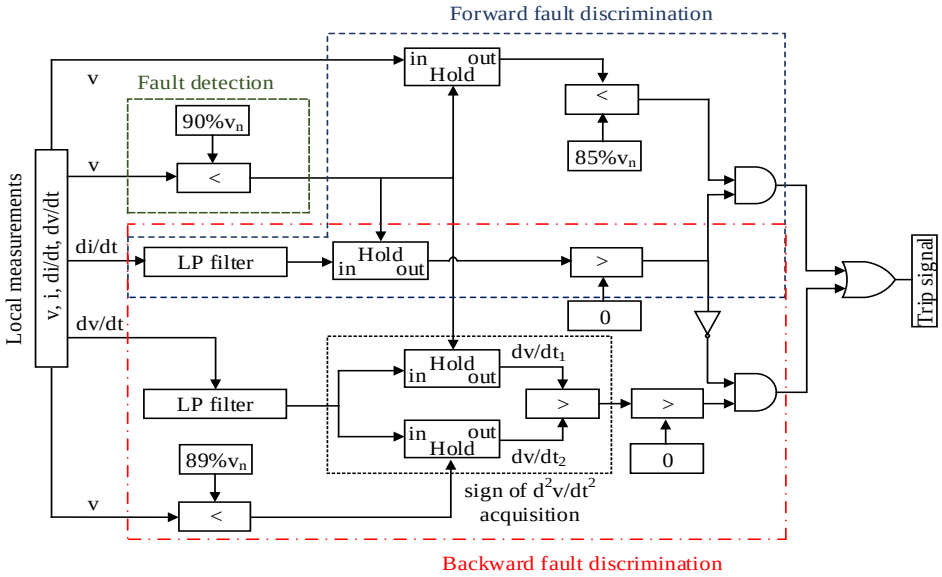

Fig. 7. *Model of the developed protection scheme*

4.1.2.Modelling of a two-stage solid state transformer

The SST is modelled as a non-modular two-stage SST as previously shown in Fig. 1 (a). The stage one AC-DC rectifier is modelled as a typical two-level VSC to convert 11kV AC to 20kV DC. The stage two DC-DC converter is modelled as a DC-DC DAB converter with an isolation transformer to convert 20kV DC to ±750V DC. Each converter is modelled as a detailed switching model. The VSC is fully controlled using an oriented vector control in a synchronous rotating d-q reference frame with the sinusoidal pulse width modulation (SPWM) technique and is operated as a regulator of the DC voltage on the MVDC link and reactive power on the MVAC side. The stage two DC-DC DAB converter is modelled to regulate the DC voltage on the LVDC link of the SST. A simplified proportional integral (PI)-based DC voltage controller is used for controlling the DC-DC DAB converter in normal operation. Under short circuit fault conditions, the DAB converter limits the fault current during the steady state fault period by activating a current-based phase shift controller added to the converter. The key SST model parameters are listed in Table 1.

4.1.3. Modelling of the developed protection scheme

A model of protection relay representing the protection algorithm as shown in Fig. 7 is developed and implemented to each protection device model of the test network. The relay measures locally the key parameters (e.g. voltage, current, di/dt, and dv/dt) and processes them by fault detection and fault location circuits (see Fig. 7) for providing the required tripping signals to the associated breakers if a fault is detected. A simplified DC solid state circuit breaker (SSCB) with 0.5ms operation time is modelled and used for fault interruption [28]. A 0.011mH assistive inductor is added to each breaker. The size of the inductor is calculated using the developed formula in (4), and it is designed as 10% of the total cable inductance.

To improve the accuracy and the reliability of the developed protection scheme, the impact of noise on the simulation of di/dt and dv/dt is considered within the protection model. Since the protection algorithm depends on the direction of di/dt as one input parameter to locate the fault, the measurement of noise can potentially increase the error in the di/dt direction. Therefore, an actual noise signal captured from a DC current transducer in a laboratory is added to the measured currents in the simulation studies [12]. Fig. 8 shows an example of a di/dt profile of a DC current with added practical noise. A moving average low pass filter with 100µs window size is selected to eliminate such noise from the measured di/dt and dv/dt signals. In addition, 1MHz sampling frequency is applied for the simulation studies to ensure that the protection scheme can obtain the derivative signals within high resolution windows [29].

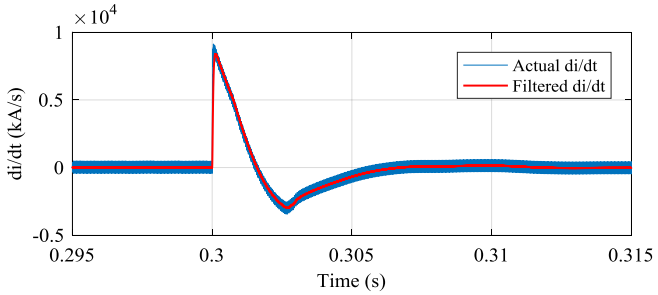

Fig. 8. *A di/dt signal profile with and without filtering*

4.2. Simulations Studies

4.2.1 Test case 1: downstream fault discrimination

Under this fault scenario, two downstream pole-to-pole solid faults labelled as F1 and F2 in Fig. 6 are applied at the end of feeder 'b' and on bus$_2$ respectively. When fault, F1, is applied on feeder 'b', the voltage responses captured by relay 'b_1' and relay 'b_2' are shown in Fig. 9. For the detection of the fault, it can be clearly seen from Fig. 9 that the DC voltages measured by relays 'b_1' and 'b_2' exceed the fault detection threshold (δ_1=90% of the v_n). For the fault location, the signs of the di/dt slopes as seen and captured by relays 'b_1' and 'b_2' (shown in Fig. 10) are positive. These indicate that the fault is located in the forward direction of relays 'b_1' and 'b_2'.

Following the detection of the fault using the detection threshold δ_1 and the indication of the fault location in the forward direction using the sign of di/dt, relays 'b_1' and 'b_2' then identify whether the fault is located within their forward protected regions or not via a fault discrimination threshold δ_2=85% of the v_n. From Fig. 9, it can be clearly seen that for the both relays ('b_1' and 'b_2') the transient voltages following the fault exceed δ_2=85% of the v_n. Therefore, the fault is located within the protected forward regions and the relays 'b_1' and 'b_2' will send trip signals to their associated breakers to trip the feeder 'b' and clear the fault.

For the downstream fault applied at location F2 on bus$_2$ (see Fig. 6) and as demonstrated in Fig. 9, the relay 'b_1' still detects this fault and sees it as a forward fault. Since the transient voltage measured by the relay 'b_1' following the initiation of the fault F2 does not exceed the discrimination threshold δ_2 (85% v_n), the fault then is located outside of its forward protected region.

The developed protection scheme requires only 100µs to detect and locate the faults within the relay's forward protected regions and 500µs to interrupt the fault current using SSCBs (see the grid fault current profile in Fig. 11). This has demonstrated quick recovery of the main DC bus voltage as shown in Fig. 9.

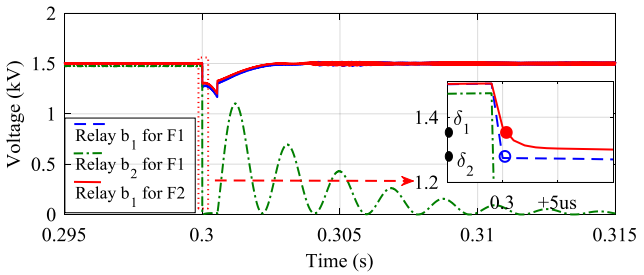

Fig. 9. *Voltages measured by relay b_1 and b_2 for a solid fault at location F1*

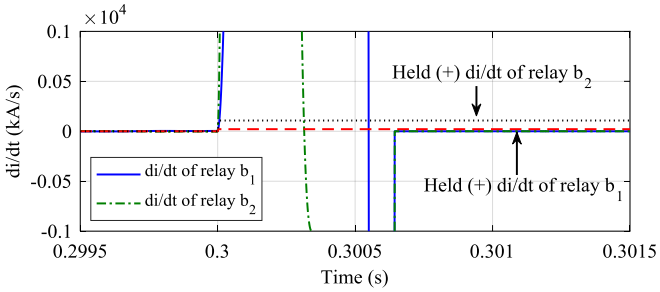

Fig. 10. *Filtered di/dt of relay b_1 and relay b_2 for a solid fault at location F1*

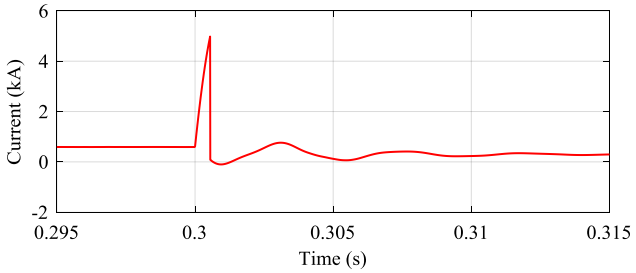

Fig. 11. *Grid current for a solid fault at location F1*

4.2.2 Test case 2: upstream fault discrimination

Under this fault test scenario, two upstream pole-to-pole solid faults, F3 and F4 in Fig. 6, are applied at the main DC bus

(PCC) and at the beginning of feeder 'a' respectively. The protection responses of both relays 'b_1' and 'a_2' when protecting outgoing feeders 'a' and 'b' in addition to the SST protection functionality are studied.

When fault F3 is applied, the DC voltages sensed by relays 'b_1' and 'a_2' exceed the fault detection threshold (δ_1=90%v_n) (see Fig. 12). In this case, the signs of the di/dt slopes as shown in Fig. 13 are negative. Consequently, the fault is located in the backward direction of relays 'b_1' and 'a_2'.

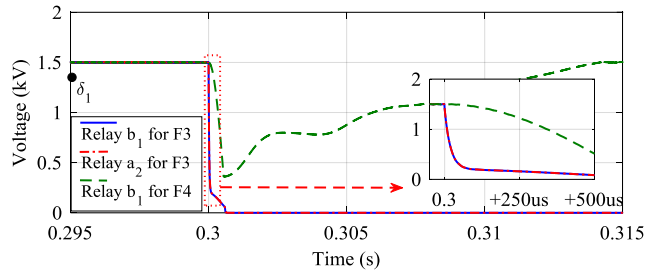

Fig. 12. *Voltage of relay b_1 and relay a_1 for a solid fault at location F3*

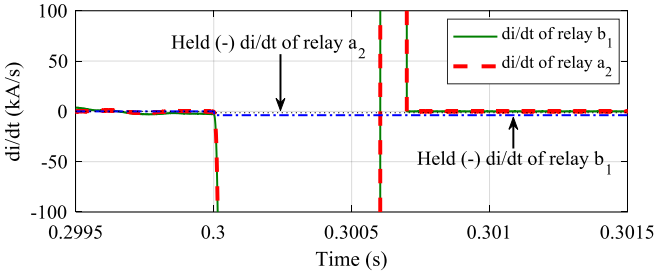

Fig. 13. *Filtered di/dt of relay b_1 and relay a_2 for a solid fault at location F3*

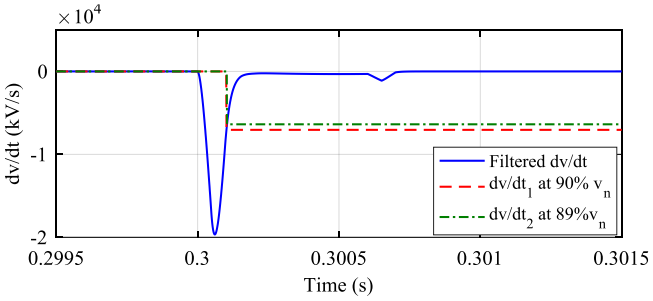

Fig. 14. *dv/dt of relay b_1 captured at 90%v_n and 89%v_n for a solid fault at location F3*

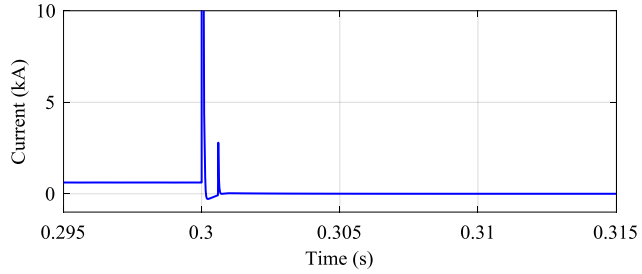

Fig. 15. *Grid current measured at PCC for a solid fault at location F3*

By capturing two dv/dt values shown as dv/dt_1 and dv/dt_2 in Fig. 14, it can be clearly noticed that the dv/dt of relay 'b_1' and 'a_2' have a decreasing trend with a negative slope after the fault is detected. This indicates a positive sign of d^2v/dt^2 and thus implies the fault is located within the protected backward regions of relays 'b_1' and 'a_2'. Accordingly, trip signals will be sent by these relays to interrupt any reverse fault currents supplied by local sources (e.g. battery sources). The fault is also cleared from the AC grid side by blocking the SST as shown in Fig. 15. The SST, through the voltage concavity-based fault discrimination functionality (implemented in its control), easily detects and locates the fault at the main bus (PCC).

For the upstream fault applied at location F4 on feeder 'a' (see Fig. 5) and as illustrated in Fig. 12 and Fig. 16, the fault detection threshold of relay 'b_1' protecting the healthy feeder is passed and therefore, relay 'b_1' detects this fault. However, the measured transient dv/dt following the fault shows an increasing trend with a negative slope, implying a d^2v/dt^2 with a negative sign and thus the fault seen by the relay is located outside of its backward protected region. Thus, no protection action will be taken by relay 'b_1' and the fault will be cleared by relays 'a_2' and 'a_1' by tripping feeder a.

Fig. 17 shows the timing diagram of the proposed protection scheme to detect and locate extreme DC faults. As the proposed protection relies on the initial fault voltage and current responses, fault detection is very fast. The main time consuming part of the protection algorithm is fault location because of the delay of using filters to process the current and voltage derivative signals. For the entire protection scheme, fault isolation consumes most of the time due to the difficulties of DC fault current breaking that is modelled with a fixed time delay.

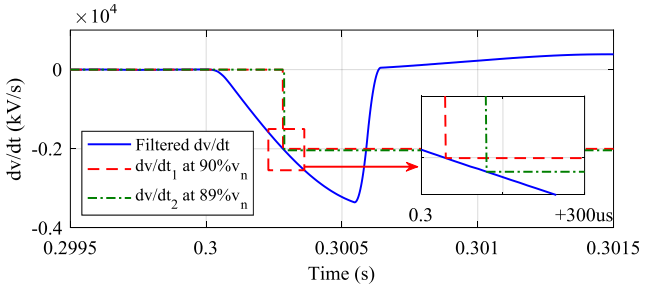

Fig. 16. *dv/dt of relay b_1 captured at 90%vn and 89%v_n for a solid fault at location F4*

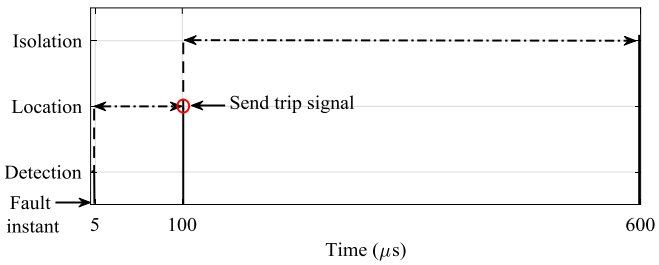

Fig. 17. *Timing diagram of the proposed protection scheme*

4.2.3 Test case 3: protection against resistive faults

As discussed and explained in Section 3, voltage-base protection schemes are in general vulnerable to resistive faults. Therefore, this test fault scenario investigates the resilience level of the developed protection algorithm as an improved voltage-based protection to DC resistive faults. An upstream DC pole-to-pole resistive fault (selected as an

example) is applied at location F4 as shown in Fig. 6. The fault is applied with different resistance and in each case, the increasing and decreasing trends of dv/dt (which are used to identify the sign of the d^2v/dt^2 concavity for accurate fault location) are tested.

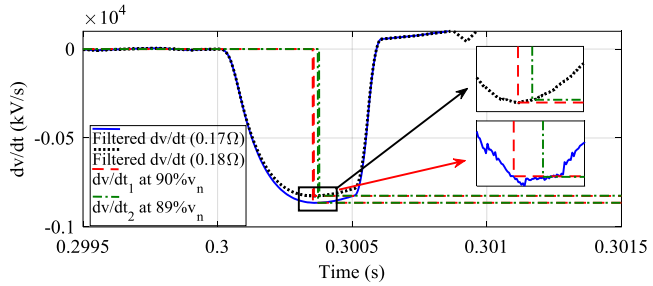

Fig. 18. *dv/dt of relay b_1 captured at 90%v_n and 89%v_n for a resistive fault (0.17Ω) and (0.18 Ω) at location F4*

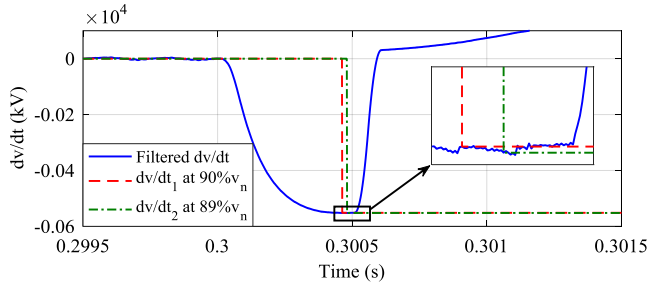

Fig. 19. *dv/dt of relay b_1 captured at 90%v_n and 89%v_n for a resistive fault (0.25 Ω) at location F4 with 15% of total cable inductance*

The simulation results presented in Fig. 18, combined with trial and error, have found that the developed voltage concavity-based fault discrimination method becomes less effective when the fault resistance reaches 0.17Ω. When the fault resistance exceeds this value, the dv/dt as presented in Fig. 18 crosses the maximum point of |dv/dt| in the negative slope. This will cause relay 'b_1' for example (see Fig. 6) of the healthy feeder to see a positive d^2v/dt^2 concavity and hence trip for the fault F4 on the adjacent feeder. This limitation can potentially be addressed by relatively increasing the size of the assistive inductor (La) per DC pole to widen the range of d^2v/dt^2 concavity fault location. Fig. 19 shows that by increasing the La from 0.011mH (equivalent to 10% of the total cable inductance) to 0.018mH (equivalent to 15% of the total cable inductance), the capability of the developed protection algorithm to accurately locate resistive DC faults is improved from faults with fault resistance equal to 0.17Ω, to faults with fault resistance up to 0.25Ω.

From the above simulation studies, the key findings can be summarised as follows:

- Existing DC protection methods based on under voltages and rate of change of voltages have clear limitations for distinguishing between faults at the main DC bus (i.e. PCC) and faults at the beginning of outgoing DC feeders. The advanced protection algorithm presented in this paper using DC voltage concavity (d^2v/dt^2 by sensing the increasing and decreasing trends of dv/dt) has demonstrated its credibility to overcome such limitations.
- The developed protection solution has proven, through detailed simulation, its fidelity to detect and locate extreme DC faults and send trip signals within 100µs. With the use of fast breakers such as electronic DC breakers, the faults can be detected, located and completely interrupted within <0.6ms. Such fast-acting protection can significantly reduce the stress on the LVDC system during the fault and improve the post-fault system response. Examples include improved SST fault ride through capability and power quality by reducing the impact of voltage swells, sags and resonances which can be caused by faults with relatively slow protection.
- The developed protection scheme utilises only local measurements and no communications are required. This can potentially play an important factor for reducing the cost and avoiding any delays or reliability issues that may arise when utilising communication links.
- In comparison to existing dv/dt protection methods, the developed protection algorithm has demonstrated a considerable improvement in detecting and locating DC resistive faults. As proven by the results, faults with a resistance of up to 0.25Ω can be accurately located compared to 0.05Ω if conventional dv/dt is used. The limitation in using DC voltage concavity for locating relatively high resistive faults can be improved by increasing the size of the assistive inductors (La) (added in series with the DC breakers). However, the increase in La needs to consider its impact on the control of any converters connected to the DC supply network.

5. Conclusions

The paper has presented an advanced communication-less fast acting and fully discriminative protection scheme that incorporates a combination of DC voltage magnitudes, DC voltage concavity (sign of d^2v/dt^2), and the sign of rate of change of DC currents. The simulation results have proven the credibility of the developed protection scheme for reliably detecting and locating DC faults within a faulted LVDC network interfaced by a two-stage solid state transformer (SST) with effective coordination between the SST and LVDC system protection within 100µs. Such fast DC protection performance allows DC faults to be interrupted at an early stage, leading to reduced short circuit stress on the system and improved post-fault power quality and LVDC resiliency. Moreover, using voltage concavity has enabled the detection and location of resistive DC faults. It is demonstrated that DC faults with a resistance of up to 0.25Ω can be precisely located and with the increase of the size of the assistive inductor, higher resistive faults are able to be detected and located. Such a feat is not achievable through existing voltage-based protection solutions that rely on under-voltage or dv/dt alone.

6. References

1. M. Schneider, "The road ahead for electric vehicles," 2017.
2. "Future Energy Scenarios 2017," 2017. [Online]. Available: http://fes.nationalgrid.com/fes-document/fes-2017/.
3. C. Cluzel and A. Morley, "Transport Energy Infrastructure Roadmap to 2050," 2015. [Online]. Available: www.lowcvp.org.uk.
4. W. Pei, and *et al.*, "Potential of using multiterminal LVDC to improve plug-In electric vehicle integration in an existing distribution network," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3101–3111, 2015.
5. V. Vossos, and *et al.*, "Lawrence Berkeley National Laboratory Review of DC Power Distribution in Buildings : A Technology and Market Assessment," 2017 .[Online]. Available: https://eta.lbl.gov.
6. "Direct Current Distribution Networks," 2018. [Online]. Available: https://www.navigantresearch.com.

7. A. Elsayed, and *et al.*, "DC microgrids and distribution systems: An overview," *Electr. Power Syst. Res.*, vol. 119, pp. 407–417, 2015.
8. P. Nuutinen, and *et al.*, "Research site for low-voltage direct current distribution in a utility - structure, functions, and operation," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2574–2582, 2014.
9. K. Smith, D. Wang, A. Emhemed, S. Galloway, and G. Burt, "Overview Paper on: Low Voltage Direct Current Distribution System Standards," *Int. J. Power Electron.*, vol. 9, no. 3, pp. 287–310, 2017.
10. IEC, "LVDC: electricity for the 21st century," 2017. [Online]. Available: https://www.iec.ch/technologyreport.
11. K. Dinesh, F. Zare, and G. Arindam, "DC microgrid technology : system architectures, AC grid interfaces, grounding schemes, power quality, communication networks, applications, and standardizations aspects," *IEEE Access*, vol. 5, pp. 12230–12256, 2017.
12. A. Emhemed, K. Fong, S. Fletcher, and G. Burt, "Validation of fast and selective protection scheme for an LVDC distribution network," *IEEE Trans. Power Deliv.*, vol. 32, no. 3, pp. 1432 - 1440 , 2017.
13. S. Som and S. R. Samantaray, "Efficient protection scheme for low-voltage DC micro-grid," *IET Gener. Transm. Distrib.*, vol. 12, no. 13, pp. 3322–3329, 2018.
14. A. Abdali, and *et al*, "Simultaneous control and protection schemes for DC multi microgrids systems," *Int. J. Electr. Power Energy Syst.*, vol. 104, no. July 2018, pp. 230–245, 2019.
15. E. Tironi, and *et al*, "Selectivity and security of DC microgrid under line-to-ground fault," *Electr. Power Syst. Res.*, vol. 165, no. October, pp. 238–249, 2018.
16. A. Huang, "Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid," *IEEE Ind. Electron. Mag.*, vol. 10, no. 3, pp. 29–42, 2016.
17. X. Yuan, "System Control and Power Quality in LVDC," 2018. [Online]. Available: http://meeting.aeps.cc.
18. SP Energy Networks, "LV Engine-A Smarter Electricity Network," 2018. [Online]. Available: https://www.spenergynetworks.co.uk.
19. D. Wang, A. Emhemed, P. Norman, and G. Burt, "Evaluation of Existing DC Protection Solutions on an Active LVDC Distribution Network under Different Fault Conditions," in *CIRED 2017*, 2017.
20. J. Huber and J. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts," *Ind. Electron. Mag.*, vol. 10, no. 3, pp. 19–28, 2016.
21. T. Guillod, F. Krismer, and J. Kolar, "Protection of MV Converters in the Grid : The Case of MV/LV Solid-State Transformers," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 393–408, 2017.
22. H. Hooshyar, and *et al.*, "PMU-assisted overcurrent protection for distribution feeders employing Solid State Transformers," *Sustain. Energy, Grids Networks*, vol. 10, pp. 26–34, 2017.
23. W. Leterme, J. Beerten, and D. Van Hertem, "Nonunit protection of HVDC grids with inductive DC cable termination," *IEEE Trans. Power Deliv.*, vol. 31, no. 2, pp. 820–828, 2016.
24. P. Cairoli and R. Dougal, "Fault detection and isolation in medium voltage DC microgrids : coordination between supply power converters and bus contactors," *IEEE Trans. Power Electron.*, vol. 33, no. 5, 2018.
25. K. Jia, M. Li, T. Bi, and Q. Yang, "A voltage resonance-based single-ended online fault location algorithm for DC distribution networks," *Sci. China Technol. Sci.*, vol. 59, no. 5, pp. 721–729, 2016.
26. A. Emhemed and G. Burt, "An advanced protection scheme for enabling an LVDC last mile distribution network," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2602–2609, 2014.
27. F. Wang and Z. Zhang, "Overview of Silicon Carbide Technology: Device, Converter, System, and Application," *CPSS Trans. Power Electron. Appl.*, vol. 1, no. 1, pp. 13–32, 2016.
28. L. Qi, and *et al*, "Design of Solid-State Circuit Breaker-Based Protection for DC Shipboard Power Systems," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 260–268, 2017.
29. C. Li, and *et al.*, "Practical Computation of di/dt for High-Speed Protection of DC Microgrids," in *ICDCM*, 2017.