Control-based Fault Current Limiter for Modular Multilevel Voltage-Source Converters

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Abstract

The sharp rise in short-circuit currents of voltage-source converters is still a challenge for DC grid reliability, which imposes stringent requirements on DC breakers. Therefore, fault current limiters are used for slowing down the rise in short-circuit currents. This paper proposes a control-based fault current limiter (CbFCL) for modular multilevel converters (MMCs). The proposed method reduces the fault current purely by control action, thus not incurring costs and not leading to reduced stability, energy storage, conduction losses or the need for maintenance as impedance-based fault current limiters do. The CbFCL does not affect the system in normal operation, acting only in the presence of a fault. The CbFCL performance was evaluated performing simulations of a four terminal DC grid. The results confirmed that the CbFCL was able to limit the fault current of the MMC while keeping the AC currents within their nominal limits, and thus producing a minor impact on the grid operation.

Keywords: DC fault, fault current limiter (FCL), modular multilevel converter (MMC), multi-terminal HVDC, VSC-HVDC.

1. Introduction

Modular Multilevel Converters (MMCs) have drawn much attention in recent years due to their suitability for voltage-source converters (VSCs) used in High Voltage Direct Current (HVDC) transmission systems [1, 2].

MMCs can improve waveform quality, reduce losses due to lower switching frequencies and reduce filtering equipment compared to two- and three-level topologies [3]. Their modular construction makes them adaptable to various voltage levels. Moreover, as the converter capacitors are closed in submodules, even during a DC fault the number of inserted capacitors can be altered [4, 5].

However, the high short-circuit currents of VSC converters still pose a challenge for DC grid reliability [6]. In case of a fault in half-bridge MMC (HB-MMC), blocking the submodules Insulated-gate Bipolar Transistors (IGBTs) does not interrupt the fault current, as it flows through the freewheeling diodes [7]. Thus, DC circuit breakers can be used for providing current interruption capability for HB-MMC connected to DC grid cables/lines. These breakers consist of disconnectors for opening the circuit and also surge arresters for absorbing the DC fault dissipated energy [8].

The high magnitude short-circuit currents, which rise sharply, can damage the DC grid components and impose high current supportability, energy dissipation and breaking time requirements on the DC circuit breakers [9, 10]. The longer the time to interrupt the fault, the more energy the surge arresters have to dissipate, which increases the cost of the breakers [6].

Therefore, considering the DC circuit breakers, efforts are made to reduce the breaking time and increase the current withstanding capability [11]. Considering the converters, efforts are made to limit the short-circuit current and slow down the fault current rise [1, 12]. These fault current limiting (FCL) methods rely on in-

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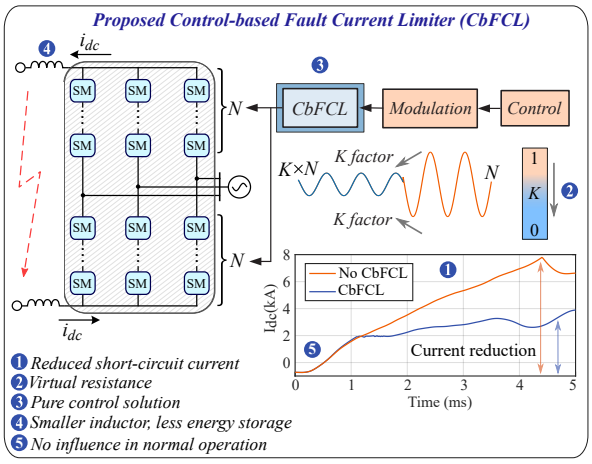

Figure 1: Conceptual representation of the proposed fault current limiter.

creasing the impedance between the converter and the fault.

A widely used method for fault current limiting is the insertion of a DC reactor between the converter and the line/cable [13]. Increasing the inductance raises the discharging time constant, providing extra time for the DC breaker opening [9, 14]. However, the size of the DC reactor may be limited by its cost and by the stability requirements of the DC grid [6].

Short-circuit currents can also be limited by solid-state FCL (SSFCL), which actively detects the overcurrent and quickly inserts an impedance in the circuit, limiting the fault [15]. Some applications in AC transmission systems can be found in [16, 17]. In HVDC systems, some DC circuit breakers perform this function by inserting impedances and creating a zero-crossing current through resonance [10]. Some investments in this technology were made to reduce the conduction losses [18].

There are also applications involving superconductor FCL (SCFCL), which show a rapid increase in the impedance in fault conditions [19, 20]. Recent developments aim to reduce the material cost and increase the SCFCL recovery time [18].

Recently, hybrid FCLs that combine control and semiconductors with passive elements have been proposed [21, 22]. In these propositions, the semiconductors provide the capacity to control the amount of impedance to be inserted into the system or the moment the impedance will be inserted, achieving more flexibility for the FCL scheme.

Whereas these technologies work by inserting impedances into the system, the proposed method reduces the fault current solely by control action. The method exploits the modular feature of MMCs and the influence of the modulation reference signal on the DC voltage [23, 24]. Thus, this pure control solution does not incur in costs and does not lead to reduced stability, increased energy storage, conduction losses or the need for maintenance. Another advantage of the proposed technique is that it does not affect the system in normal operation, acting only in the presence of a fault. These advantages are summarized in the conceptual representation of the technique in Fig. 1.

Other FCL techniques based on control have been proposed. An approach using PID controllers to reduce the fault current is presented in [25] and an approach using a duty cycle index is presented in [24]. Although the technique in [25] successfully reduced the fault current, it relies on using dead-band and closed-loop control, which can introduce additional delays in the operation. On the other hand, the technique proposed in this paper reduces the fault current by directly changing the insertion index of the submodules, thus not requiring closed loops. Additionally, both [25] and [24] lack of a design procedure and the impacts of the proposed technique in the AC grid. In this work, on the other hand, a complete design procedure following analytical derivations is presented, as well as the impacts of the proposed technique on the connected AC grid.

In this paper, our main goal is to propose a Control-based FCL (CbFCL) technique to reduce the DC fault current in MMC-HVDC systems. The paper is organized as follows. Section 2 introduces the HB-MMC operating principle and fault analysis. Section 3 describes the proposed CbFCL, presents the design procedure and shows analytical expressions of the influence of the CbFCL in DC fault currents and AC grid transients. Section 4 presents comparative simulations of a four-terminal DC grid with and without the proposed CbFCL. Finally, the conclusions are presented in Section 5.

2. MMC Operating Principle and Fault Analysis

The basic structure of a three-phase MMC is shown in Fig.2. The three-phase MMC comprises six arms and each arm consists of N series-connected submodules and one arm inductor. The submodules can be configured as half-bridge or full-bridge. This work analyses the half-bridge configuration.

When $S_1 = 1$ and $S_2 = 0$, the submodule is switched on and $v_{SM} = v_c$; when $S_1 = 0$ and $S_2 = 1$, the submodule is switched off and $v_{SM} = 0$, where v_{SM} is the submodule voltage and v_c is the capacitor voltage. The

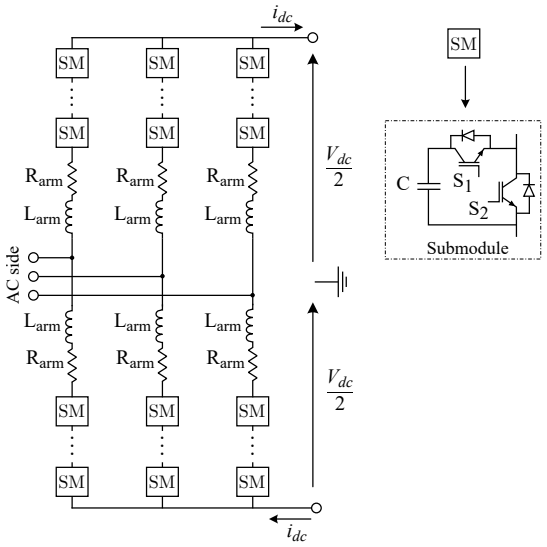

Figure 2: Three-phase MMC circuit diagram.

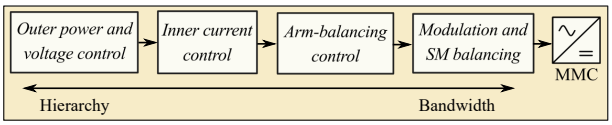

Figure 3: MMC cascaded control structure.

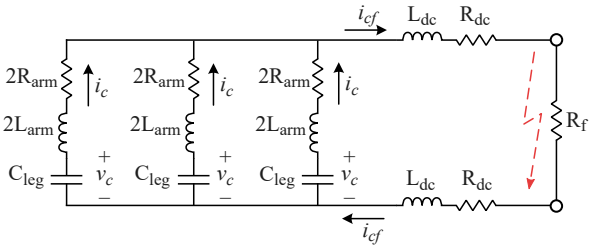

Figure 4: MMC circuit at the capacitive discharge stage.

proper operation of the switches is achieved by control structures.

2.1. MMC Control System

The MMC control system is structured in cascaded configuration [26]. The outer loop keeps the converter active and reactive power or AC and DC voltages at the specified set-point, providing references for the inner current control, which controls the converter output current. The arm-balancing control compensates the internal second harmonic current of each arm and maintains the circulating current close to $i_{dc}/3$. The modulation compares the output-voltage reference generated by the inner current loop and by the arm-balancing ($n_{p,n}$) against a carrier, thus defining the number of inserted submodules in each arm ($N_{p,n}$) (some modulation techniques such as the Nearest Level Modulation do not utilize a carrier-comparison technique) [7]. Given the number of inserted submodules and the sign of the arm current, the submodule balancing loop specifies which submodule will be inserted in order to balance the submodules voltages [1, 7]. The lower the hierarchy, the faster the loop is and the shorter the time range, i.e., 20-500 ms for the outer loop and some μs for IGBT switching [27]. The control structure is depicted in Fig. 3.

2.2. MMC Fault Analysis

The MMC fault analysis can be divided into three different stages: the capacitive discharge stage, the AC transient infeed stage and the AC steady-state infeed stage [5]. The capacitive discharge state includes the period between the occurrence of the fault and the converter block. In this stage, the energy stored in the SM capacitors is discharged in the short-circuit until the arm currents reach the limit value of the converter's internal protection. The AC transient infeed stage starts by blocking the converter and is characterized by the sum of the currents flowing through the freewheeling diodes and the currents resulting from the release of the stored energy in the arm inductors and DC inductors. After the inductors have been discharged, the fault is fed solely by the AC grid in the AC steady-state infeed stage. DC or AC circuit breakers have to open the circuit in order to isolate the sustained fault. At any stage, DC breakers can open the circuit, isolating the fault, or after the converter blocking AC breakers can also isolate the sustained fault [4].

Regarding the capacitive discharge stage, Fig. 4 shows the equivalent circuit of the MMC during this stage, where L_{arm} and R_{arm} are the arm inductance and resistance, respectively, L_{dc} and R_{dc} are the inductance and resistance of the fault path, respectively, R_f is the fault resistance and C_{leg} is the leg capacitance in this fault stage. L_{dc} is the sum of the DC fault current limiting inductor and the cable inductance. $C_{leg} = 2C_{SM}/N$ [28]. Applying Kirchhoff's voltage law in the equivalent circuit of Fig. 4 and assuming $i_c = i_{cf}/3$, results in

$$v_c = \left(\frac{2L_{arm}}{3} + 2L_{dc}\right)\frac{\mathrm{d}i_{cf}}{\mathrm{d}t} + \left(\frac{2R_{arm}}{3} + 2R_{dc} + R_f\right)i_{cf} \tag{1}$$

Moreover,

$$i_c = \frac{i_{cf}}{3} = -C_{leg}\frac{\mathrm{d}v_c}{\mathrm{d}t} \tag{2}$$

Considering $L_{eq} = 2L_{arm}/3 + 2L_{dc}$, $R_{eq} = 2R_{arm}/3 + 2R_{dc} + R_f$, $C_{eq} = 3C_{leg}$, the system of differential first order equations can be written as

$$\frac{\mathrm{d}i_{cf}}{\mathrm{d}t} = \frac{v_c}{L_{eq}} - \frac{R_{eq}}{L_{eq}} i_{cf} \tag{3a}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = -\frac{1}{C_{eq}} i_{cf} \tag{3b}$$

Let V_0 and I_0 be the voltage and current values at $t = 0$. The solution for (3) is

$$\begin{aligned} v_c(t) &= V_0 e^{\frac{-t}{\tau}} \left(\cos \omega t + \frac{1}{\omega\tau} \sin \omega t \right) - \frac{I_0}{\omega C_{eq}} e^{\frac{-t}{\tau}} \sin \omega t \\ i_{cf}(t) &= I_0 e^{\frac{-t}{\tau}} \left(\cos \omega t - \frac{1}{\omega\tau} \sin \omega t \right) + \frac{V_0}{\omega\tau R_{eq}/2} e^{\frac{-t}{\tau}} \sin \omega t \end{aligned} \tag{4}$$

where

$$\omega = \frac{\sqrt{\frac{4L_{eq}}{C_{leg}} - R_{eq}^2}}{2L_{eq}} \tag{5}$$

is the natural frequency of the circuit and $\tau = 2L_{eq}/R_{eq}$ is the circuit time constant.

Considering normal operation, $V_0 = V_{dc}$ and I_0 is the DC current, which depends on the operation set-point. If $I_0 = 0$, the expression for $i_{cf}(t)$ reduces for the one presented in [29].

The first order Taylor approximation of $i_{cf}(t)$ in (4) in $t = 0$ is

$$i_{cf}(t) \approx I_0 + \frac{t}{\tau/2} \left(\frac{V_0}{R_{eq}} \right) \tag{6}$$

On the other hand, if the discharge time is short and the capacitor voltage is kept almost constant, the capacitor is considered a DC source with $v_c(t) = V_0$. Thereby, the solution of (3) is

$$i_{cf}(t) = \frac{V_0 - e^{\frac{-t}{\tau/2}} \left(V_0 - I_0 R_{eq} \right)}{R_{eq}} \tag{7}$$

The first order Taylor approximation of (7) leads to

$$i_{cf}(t) \approx I_0 + \frac{t}{\tau/2} \left(\frac{V_0}{R_{eq}} \right) \tag{8}$$

which is the same expression as (6). As a result, in the short period of time of the capacitive discharge stage, the leg equivalent capacitor of Fig. 4 can be approximated by a DC source. The approximation is valid for large C_{eq} values. This will be particularly useful for simplifying the equivalent circuit of the MMC with the CbFCL in Section 3.1.

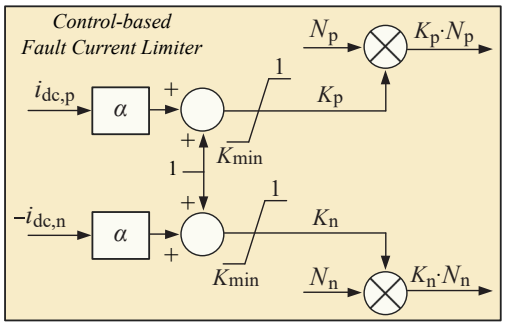

Figure 5: The Control-based Fault Current Limiter scheme.

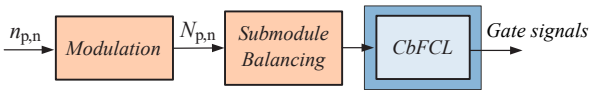

Figure 6: Location of the CbFCL in the modulation loop.

3. The Control-based Fault Current Limiter

The proposed CbFCL consists of a K factor that reduces the number of inserted submodules in the first stage of a DC fault, before the converter is blocked. Since the short-circuit current is directly related to the voltage of the converter feeding the fault, reducing the number of inserted submodules during the fault would reduce the converter contribution to the fault current [23]. The proposed CbFCL is depicted in Fig. 5 and it is inserted after the last modulation stage (Fig. 6).

The CbFCL K factor remains equal to 1 in normal operation. In a fault condition, when the current increases beyond 1 p.u., the CbFCL is triggered and the K factor assumes a value in the range $0 < K < 1$, reducing the number of inserted submodules in the capacitive discharge state of the fault, before the converter is blocked. Thus, the CbFCL does not interfere in the normal operation of the control system or in the modulation of the MMC, acting only during the short-circuit.

This scheme has some advantages when compared to impedance-based fault current limiters: it does not incur in additional costs, it does not slow down the system's dynamic response and it does not increase the inductive energy storage at the fault instant. Hence, the CbFCL can be used in conjunction with a smaller DC inductor, reducing its size, cost, and energy storage.

The K factor can be calculated as a linear function of the DC current, $K = 1 + \alpha\, i_{dc}$, however, other functions can also be utilized.

3.1. MMC with CbFCL Fault Analysis

The proposed CbFCL alters the number of inserted submodules in each arm of the converter. The reduction in the number of submodules reduces the total voltage of the arm and increases the total capacitance of the arm as the submodules are series-connected. Thus, the capacitor voltage equation is modified from

$$v_c(t) = V_0 - \frac{1}{C_{eq}} \int_0^t i_{cf}(t)\,\mathrm{d}t \tag{9}$$

to

$$v_c(t) = K \cdot V_0 - \frac{K}{C_{eq}} \int_0^t i_{cf}(t)\,\mathrm{d}t \tag{10}$$

Differentiating (10) with respect to time leads to

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \frac{\mathrm{d}K}{\mathrm{d}t} V_0 - \frac{K}{C_{eq}} i_{cf} - \frac{\mathrm{d}K}{\mathrm{d}t} \frac{1}{C_{eq}} \int_0^t i_{cf}\,\mathrm{d}t \tag{11}$$

As $\frac{\mathrm{d}K}{\mathrm{d}t} = \frac{\mathrm{d}K}{\mathrm{d}i_{cf}} \frac{\mathrm{d}i_{cf}}{\mathrm{d}t} = \alpha \frac{\mathrm{d}i_{cf}}{\mathrm{d}t}$, a system of differential equations can be written as in (3) as:

$$\frac{\mathrm{d}i_{cf}}{\mathrm{d}t} = \frac{v_c}{L_{eq}} - \frac{R_{eq}}{L_{eq}} i_{cf} \tag{12a}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \alpha \frac{\mathrm{d}i_{cf}}{\mathrm{d}t} V_0 - \frac{K}{C_{eq}} i_{cf} - \alpha \frac{\mathrm{d}i_{cf}}{\mathrm{d}t} \frac{1}{C_{eq}} \int_0^t i_{cf}\,\mathrm{d}t \tag{12b}$$

Although (12) can be numerically evaluated, its analytical solution is complex. Therefore, to find an analytical solution for i_{cf}, the assumption of Section 2.2 that the capacitor can be considered as a voltage source in the short capacitive discharge interval will be utilized. In this case, the approximation is better than the one in Section 2.2 because the effect of K in the converter DC voltage is greater than the voltage reduction due to the capacitive discharge. Considering this approximation, a new system of differential equations can be written as:

$$\frac{\mathrm{d}i_{cf}}{\mathrm{d}t} = \frac{v_c}{L_{eq}} - \frac{R_{eq}}{L_{eq}} i_{cf} \tag{13a}$$

$$\frac{\mathrm{d}v_c}{\mathrm{d}t} = \alpha \frac{\mathrm{d}i_{cf}}{\mathrm{d}t} V_0 \tag{13b}$$

The solution for (13) is

$$v_c(t) = KV_0 = (\alpha i_{cf}(t) + 1)V_0 \tag{14a}$$

$$i_{cf}(t) = \frac{V_0 - e^{-t/\tau_{FCL}}(V_0 - I_0 R_{FCL})}{R_{FCL}} \tag{14b}$$

Where $R_{FCL} = R_{eq} - \alpha V_0$ is the system equivalent resistance considering the influence of the CbFCL and $\tau_{FCL} = L_{eq}/R_{FCL}$ is the circuit time constant.

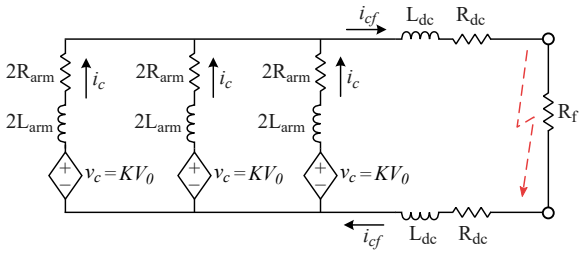

Figure 7: Approximate model of the MMC with CbFCL at the capacitive discharge stage.

The electrical circuit representation of (13) is presented in Fig. 7.

By comparing (7) with (14), it can be observed that the CbFCL virtually increases the equivalent resistance of the converter, from R_{eq} (converter physical resistance) to $R_{eq} - \alpha V_0$ (added virtual resistance), as α is always a negative value. The greater $-\alpha$ is, the bigger the equivalent internal resistance of the converter will be. It is worth noting that the added virtual resistance does not increase the converter's physical resistance, thus not elevating the converter losses during a fault or in normal operation.

As the internal resistance increases, the DC fault current limiting reactor (L_{sm}) size can be reduced. This reduces the cost and the energy stored in the inductor during the fault, which in turn relieves the energy dissipation constraints of the DC breakers.

It should be pointed out that this fault analysis considers just one converter feeding the fault. When more converters feed the fault, the voltage at the fault point will be higher and the current contribution of the analysed converter will be lower. Nevertheless, the analysis with just one converter is conservative as it is the worst case.

It should be mentioned that the K factor has to be chosen appropriately. If K is chosen close to 1, the fault current will be as large as the case without CbFCL. If K is chosen close to 0, the voltage seen by the AC grid will be too low leading to a great increase in the power flow to the converter. Moreover, as the faults in the DC grid affect all connected converters, even the ones that are not directly connected to the faulted link will trigger the CbFCL. This will impose transients in all connected AC grids, not only the AC grids feeding the converters close to the fault. Therefore, there is a trade-off between the DC fault current reduction and the transient in the AC grids. Thus, it is relevant to establish the upper and lower boundaries for the K factor given this trade-off.

3.2. Defining the K factor upper limit

The K factor upper limit is defined by the maximum allowable converter contribution to the DC fault current. If the maximum current in the converter is I_{max} at $t = t_{cr}$, where t_{cr} is the critical time, following (14b):

$$i_{cf}(t{=}t_{cr}) = \frac{V_0 - e^{-t_{cr}/\tau_{FCL}}(V_0 - I_0 R_{FCL})}{R_{FCL}} < I_{max} \quad (15)$$

Hence,

$$R_{FCL} > \frac{V_0 - V_0 e^{-t_{cr}/\tau_{FCL}}}{I_{max} - I_0 e^{-t_{cr}/\tau_{FCL}}} \quad (16)$$

As $\tau_{FCL} = L_{eq}/R_{FCL}$, R_{FCL} is not completely isolated in (16), its value can be calculated using an iterative process. Once R_{FCL} is defined, α is calculated as

$$\alpha = -\frac{R_{FCL} - R_{eq}}{V_0} \quad (17)$$

Following this procedure, it will be ensured that at the critical time, the current contribution of the converter is equal or less than the maximum one defined. The critical time can be defined by the current ratings of the grid elements, by the DC circuit breaker or by any other criteria.

3.3. Defining the K factor lower limit

When the CbFCL actuates, the converter's internal AC voltage amplitude decreases according to the K factor. Hence, the voltage difference between the AC grid and the converter becomes large, leading to a greater power flow from the AC grid to the converter. Thus, the lower limit for the K factor is defined by the maximum allowable power transient in the converter AC side. Therefore, the equation that relates the K factor to the power transient is derived in this section.

Following the convention of Fig. 8, the voltages are defined as:

$$\begin{cases} v_g(t) = \mathrm{Re}\left[A_g e^{j(\omega t+\phi_0)}\right] \\ v_i(t) = \mathrm{Re}\left[K(t) A_i e^{j(\omega t+\phi+\phi_0)}\right] \end{cases} \quad (18)$$

where v_i is the converter's internal voltage, A_g and A_i are the AC grid and converter internal voltage amplitudes, respectively, ϕ is the phase angle between the voltages and ϕ_0 is an initial phase angle. The reference was considered aligned with phase A. Re[.] stands for the real part. The same development applies for the other phases.

The full analytic solution considering $K(t)$ as a function of $i_{cf}(t)$ would increase the complexity of the equations. Therefore, it is assumed that the converter internal voltage falls instantly to its lower limit ($K(t) = K_{min}$). A balance condition and stiff AC grid is also assumed.

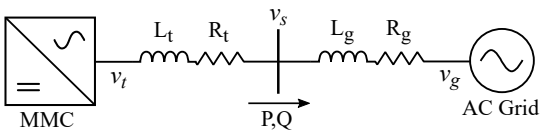

Figure 8: MMC AC connection single line diagram.

The AC current is calculated in the Laplace domain as:

$$I_s = \frac{V_i - V_g + L_{ac} I_{s0}}{sL_{ac} + R_{ac}} \quad (19)$$

and the converter AC side voltage is:

$$V_s = V_i - I_s(sL_{at} + R_{at}) + L_{at} I_{s0} \quad (20)$$

where $L_{ac} = L_{arm}/2 + L_t + L_g$ and $R_{ac} = R_{arm}/2 + R_t + R_g$ and $I_{s0} = i_s(t = 0)$, prior to the CbFCL action. The uppercase variables V_s, I_s, V_g and V_i represent the Laplace transform of the variables shown in Fig. 8 and defined in (18).

Inverting back to time yields:

$$i_s(t) = \mathrm{Re}\left[\underline{I_{s1}}(e^{j\omega t} - e^{\frac{-t}{\tau_{ac}}}) + \underline{I_{s0}} e^{\frac{-t}{\tau_{ac}}}\right] \quad (21)$$

where

$$\underline{I_{s1}} = \frac{A_i K_{min} e^{j(\phi+\phi_0)} - A_g e^{j\phi_0}}{R_{ac} + j\omega L_{ac}} \quad (22)$$

and for the voltage:

$$v_s(t) = \mathrm{Re}\left[\underline{V_{s1}} e^{j\omega t} + (\underline{I_{s0}} - \underline{I_{s1}})\left(\frac{L_{at}R_g - L_g R_{at}}{L_{ac}}\right) e^{\frac{-t}{\tau_{ac}}}\right] \quad (23)$$

where

$$\underline{V_{s1}} = \frac{A_i K_{min} e^{j(\phi+\phi_0)}(R_g + j\omega L_g) + A_g e^{j\phi_0}(R_{at} + j\omega L_{at})}{R_{ac} + j\omega L_{ac}} \quad (24)$$

where $\tau_{ac} = L_{ac}/R_{ac}$, $L_{at} = L_{arm}/2 + L_t$ and $R_{at} = R_{arm}/2 + R_t$. I_{s1} is the complex current magnitude after the CbFCL action.

From (21), it can be observed that there is a gradual shift from I_{s0} to I_{s1} determined by the time constant τ_{ac}. The same time constant applies to the voltage in (23) but the dominance of the inductive part over the resistive part in the second term of (23) allows the approximation $v_s(t) \approx \mathrm{Re}\left[\underline{V_{s1}} e^{j\omega t}\right]$.

Using i_s and v_s, the apparent power delivered to the AC grid is:

$$S_s = \underbrace{\frac{3}{2}\underline{V_{s1}}\underline{I_{s1}}^*}_{steady\ state} + \underbrace{\frac{3}{2}\underline{V_{s1}} e^{j\omega t} e^{\frac{-t}{\tau_{ac}}}(\underline{I_{s0}}^* - \underline{I_{s1}}^*)}_{transient} \quad (25)$$

Equation (25) shows that the power flow transient has an oscillatory characteristic given by $e^{j\omega t}$ which is further suppressed by $e^{\frac{-t}{\tau_{ac}}}$. The transient magnitude depends on the difference between I^*_{s0} and I^*_{s1}, which in turn is determined by K_{min}. Thus, the lower K_{min} is, the greater the transient will be.

It is also useful to calculate the maximum value of S_s between $0 < t < t_{cr}$ in order to define a maximum transient. To this end, the complex quantities are rewritten as $\underline{V_{s1}} = V_{s1}e^{j\theta_v}$, $\underline{I_{s1}} = I_{s1}e^{j\theta_i}$ and $\underline{I_{s0}} = I_{s0}e^{j\theta_{i0}}$. Therefore, separating (25) in real and imaginary parts and summing the currents in the transient part leads to:

$$P_s = \frac{3}{2}V_{s1}I_{s1}\cos(\theta_v - \theta_i) + \frac{3}{2}V_{s1}I_{seq}\cos(\omega t + \theta_v + \theta_{eq})e^{\frac{-t}{\tau_{ac}}} \tag{26}$$

$$Q_s = \frac{3}{2}V_{s1}I_{s1}\sin(\theta_v - \theta_i) + \frac{3}{2}V_{s1}I_{seq}\sin(\omega t + \theta_v + \theta_{eq})e^{\frac{-t}{\tau_{ac}}} \tag{27}$$

where

$$\begin{cases} I_{seq} = \sqrt{I_{s1}^2 + I_{s0}^2 - 2I_{s1}I_{s0}\cos(\theta_{i0} - \theta_i)} \\ \theta_{eq} = \theta_{i0} + \arctan\left(\dfrac{I_{s1}\sin(\theta_{i0} - \theta_i)}{I_{s0} - I_{s1}\cos(\theta_{i0} - \theta_i)}\right) \end{cases} \tag{28}$$

Therefore, the maximum values for P_s and Q_s can be calculated considering $\cos(\omega t + \theta_v + \theta_{eq})$ and $\sin(\omega t + \theta_v + \theta_{eq})$ equal to unity and calculating P_s and Q_s at $t = t_{cr}$.

Following both procedures to define the maximum and minimum values for the K factor will ensure the CbFCL provides the desired DC current limitation within the allowable transient in the AC grid.

4. The CbFCL Performance

The proposed CbFCL performance was analysed by simulating a symmetric monopole MMC-based multi-terminal HVDC (MMC-MTDC) system with four terminals [30], presented in Fig. 9. The system was modeled in PSCAD/EMTDC software and its parameters are summarized in Table A.1 in the Appendix. The converters were modeled with the detailed Thévenin equivalent model.

All DC lines were modeled using the frequency-dependent model. Line parameters were based on [31]. The converter arms' overcurrent protection was set to 2 p.u. = 3.87 kA for MMCs 1, 2 and 3, and 5.16 kA for MMC 4. The pick-up time was 0.1 ms. All faults were simulated at t = 1 s. MMCs 1, 2 and 3 performed active power control, with P_{MMC1} = 600 MW, P_{MMC2} = 600 MW and P_{MMC3} = −700 MW. MMC 4 performed DC grid voltage control with V_{dc} = 640 kV. All

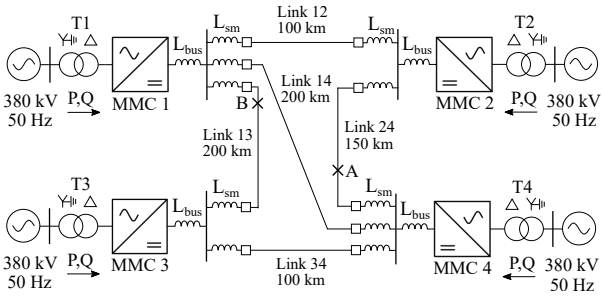

Figure 9: MTDC system single line diagram [30].

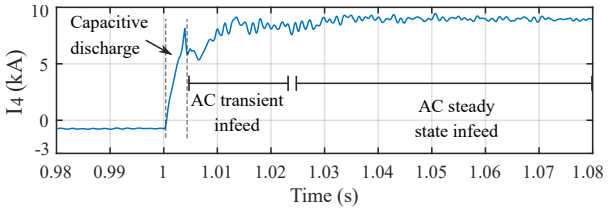

Figure 10: MMC 4 positive pole short-circuit current without CbFCL.

MMCs' reactive power set-points were −100 Mvar. The circulating current control was implemented using PR controllers.

4.1. System without CbFCL

Assuming MMC 4 as a reference, the system without CbFCL was submitted to a solid pole-to-pole short-circuit at Link 24, 30 km from MMC 4 (point A in Fig. 9). Figure 10 presents the MMC 4 positive pole short-circuit current.

High magnitude fault currents can be observed in Fig. 10, which would have to be limited by an increase in the value of the DC line reactor (L_{sm}). Instead of increasing L_{sm}, the CbFCL was installed in all four MMCs.

4.2. System with CbFCL

In order to analyse the proposed CbFCL, two different K factors were defined: K_1 was chosen to be less limiting, with I_{max1} = 6 kA. K_2 was chosen to be more limiting, with I_{max2} = 4 kA. Both critical times were 4 ms. V_0 = 640 kV. I_0 was considered equal to 1 p.u. as this is the value where the CbFCL triggers. R_{FCL} and α were calculated using (16) and (17). K_{min} was calculated for a maximum AC transient on the healthy converters (MMCs 1 and 3) of 1410 MVA for K_1 and 1940 MVA for K_2. This yielded to the following param-

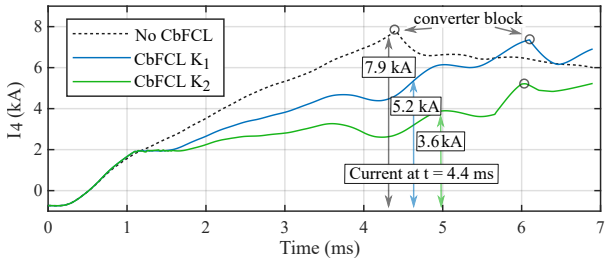

Figure 11: MMC 4 positive pole short-circuit currents. Comparison between the cases with and without CbFCL.

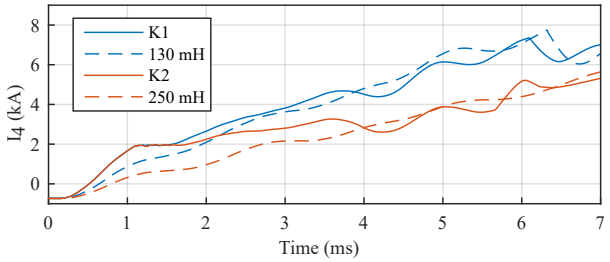

Figure 12: Size of DC reactor required to obtain same current reduction as obtained with the CbFCL.

eters:

$$K_1: \begin{cases} I_{max1} = 6\ \text{kA} \\ R_{FCL} = 102.1\,\Omega \\ \alpha = -0.1578 \\ K_{min} = 0.6 \end{cases} \qquad K_2: \begin{cases} I_{max2} = 4\ \text{kA} \\ R_{FCL} = 158.9\,\Omega \\ \alpha = -0.2465 \\ K_{min} = 0.3 \end{cases}$$

The same pole-to-pole fault was simulated in A. The results are presented in Fig. 11.

It can be observed in Fig. 11 that both the CbFCL with K_1 and the CbFCL with K_2 resulted in a reduction of the short-circuit current in the capacitive discharge interval, comparing the values at the same time instant (t = 4.4 ms, the converter block instant without CbFCL). With CbFCL K_1, the current contribution was reduced from 7.9 kA to 5.2 kA. With CbFCL K_2, the current contribution was reduced from 7.9 kA to 3.6 kA. To achieve the same degree of fault current reduction using only DC reactors, L_{sm} would have to be raised from 60 mH to 130 mH, to equal the limitation given by CbFCL K_1, and to 250 mH, to equal the limitation given by CbFCL K_2 (Figure 12). However, an increase in L_{sm} raises the inductor cost and the energy stored that slows down the system dynamics. The greater the energy stored in the inductors is, the higher the energy the DC breakers arresters will have to dissipate. On the other hand, the CbFCL only affects the fault current. Thus, if the CbFCL is used, the size of the limiting reactor can be reduced.

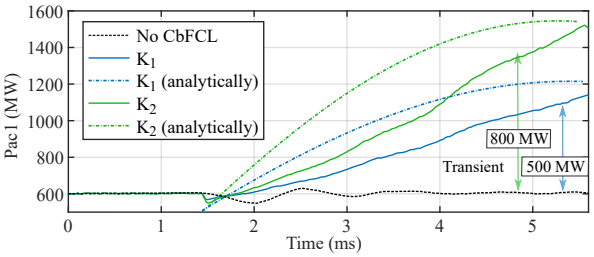

Figure 13: MMC 1 AC active power. Comparison between the cases with and without CbFCL.

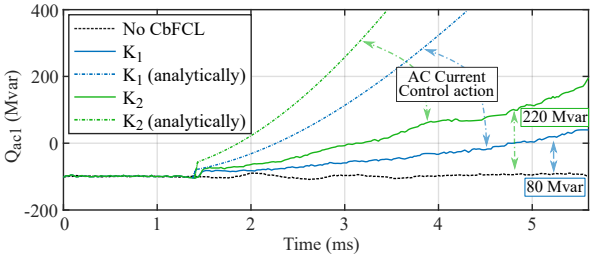

Figure 14: T4 AC reactive power. Comparison between the cases with and without CbFCL.

The maximum current for K_1 and K_2 was not equal to the defined I_{max} because as the other converters also fed the fault, the contribution of MMC 4 was reduced.

The circle in Fig. 11 represents the converter blocking time. With the CbFCL, the converter was blocked only after 6 ms. This demonstrates another advantage of using the CbFCL, which avoids blocking the converter if a DC breaker isolates the fault before the critical time. It should be pointed out that in Fig. 11 the current in the case without CbFCL drops, after the converter blocking. This is the expected behaviour of the converter during the AC transient infeed stage. Hence, between 4.4 ms and 6 ms, the MMC 4 is in the AC transient infeed stage in the case without CbFCL while it is in the capacitive discharge stage in the cases with CbFCL. However, after the AC transient infeed stage, the current will rise starting the AC steady state infeed stage, as discussed in Section 2.2 and depicted in Fig. 10.

Regarding the AC transients in the other converters, Fig. 13 and Fig. 14 present the active and reactive power injected by the MMC 1 in the AC grid during the DC fault. The simulated and calculated reactive power differed in Fig. 14 because as the AC current control sees the CbFCL as a disturbance, it acts to mitigate the CbFCL action by changing the modulation reference. Nevertheless, the AC transient equation can still be used as a worst-case scenario. Although the active power in Fig. 13 exceeds the converter nominal power (900 MVA), the converter internal power flow is

smaller because part of the power injected by the grid is absorbed by the system inductance during the transient period. Nevertheless, as the converter overcurrent protection was adjusted for 2 p.u., the power transient exceeded the threshold only after 6 ms. Fig. 15, Fig. 16 and Fig. 17 show the MMC 4 internal AC voltages. It can be observed that as the CbFCL acts, the internal voltage reduces, increasing the AC transient. The other converter internal variables: sum of capacitor voltages, arm currents and K factors, are shown from Fig. 18 to Fig. 24. By comparing Fig. 18 with Fig. 19 and with Fig. 20, it can be seen that the proposed technique resulted in higher submodule capacitor voltages, which means that less energy was discharged in the fault.

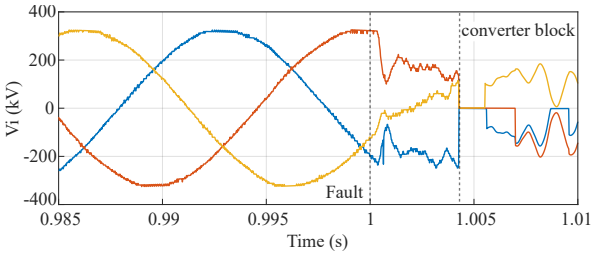

Figure 15: MMC 4 AC internal voltage (V_i). Case without CbFCL.

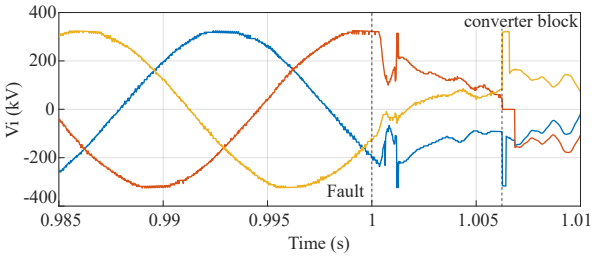

Figure 16: MMC 4 AC internal voltage (V_i). Case with CbFCL K1.

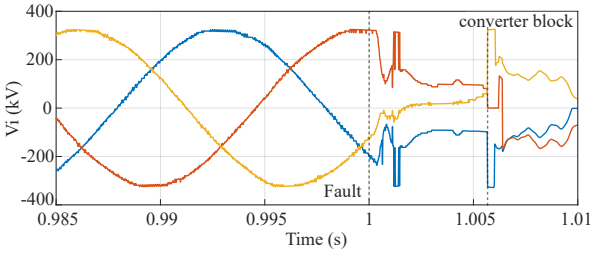

Figure 17: MMC 4 AC internal voltage (V_i). Case with CbFCL K2.

Despite the potential of the CbFCL in fault current reduction, it needs to be designed respecting the DC grid limits. The more limiting the CbFCL is, the lower the

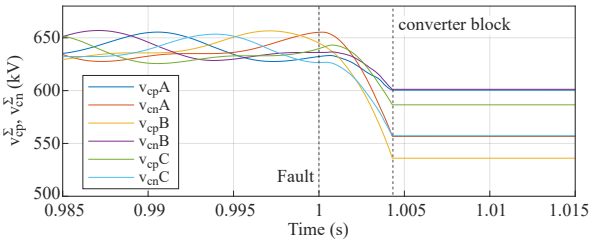

Figure 18: MMC 4 sum of capacitor voltages, top arms and bottom arms (v^{Σ}_{cp} and v^{Σ}_{cn}). Case without CbFCL.

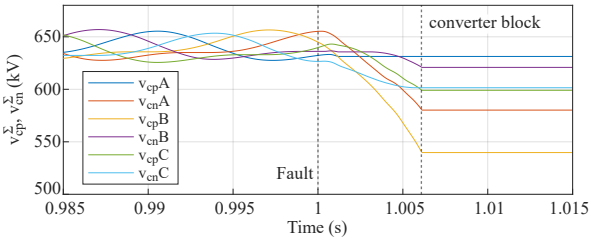

Figure 19: MMC 4 sum of capacitor voltages, top arms and bottom arms (v^{Σ}_{cp} and v^{Σ}_{cn}). Case with CbFCL K1.

DC voltage during the fault will be, which can be observed in Fig. 25 comparing the DC voltage in the same terminal and in Fig. 26 to Fig. 28 comparing the DC voltage at all four terminals. Therefore, in the extreme case where $R_{FCL} \rightarrow \infty$ ($K = 0$), the whole DC grid would be inoperable for any DC fault, which is undesir-

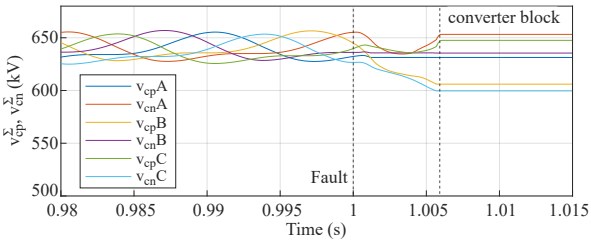

Figure 20: MMC 4 sum of capacitor voltages, top arms and bottom arms (v^{Σ}_{cp} and v^{Σ}_{cn}). Case with CbFCL K2.

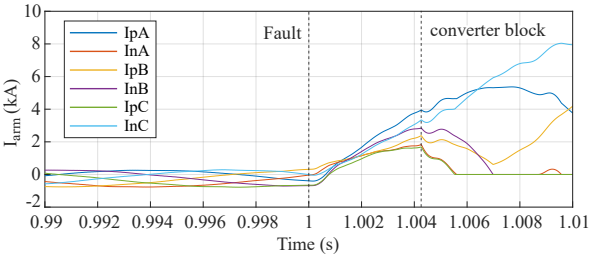

Figure 21: MMC 4 arm currents (I_{arm}). Case without CbFCL.

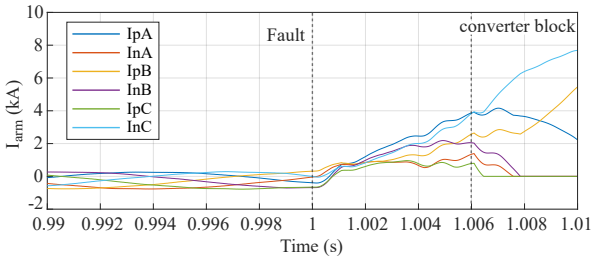

Figure 22: MMC 4 arm currents (I_{arm}). Case with CbFCL K1.

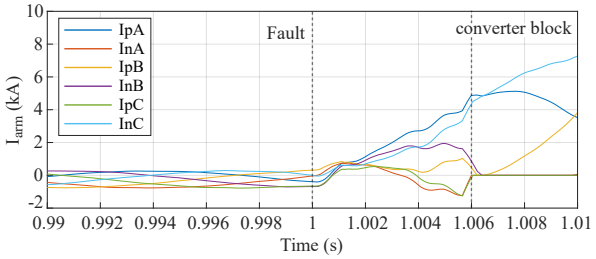

Figure 23: MMC 4 arm currents (I_{arm}). Case with CbFCL K2.

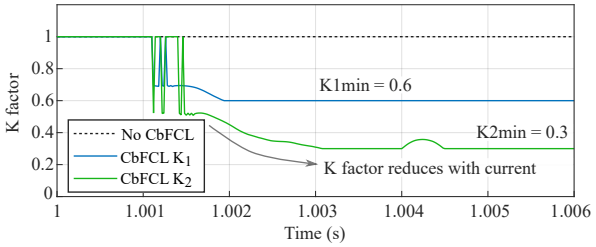

Figure 24: MMC 4 CbFCL K factors during the fault.

able from the availability point of view. For this reason and because of the AC transient, the K factor must be appropriately chosen.

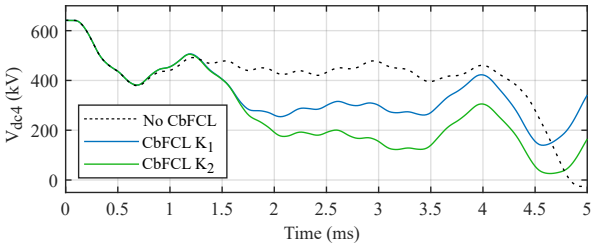

Figure 25: T4 DC voltage. Comparison between the cases with and without CbFCL.

It is worth mentioning that although the results in Fig. 11 to Fig. 28 are related to pole-to-pole faults, the proposed CbFCL is also effective in terms of reducing the fault current in pole-to-ground faults, as the CbFCL is inserted in each of the upper and lower converter

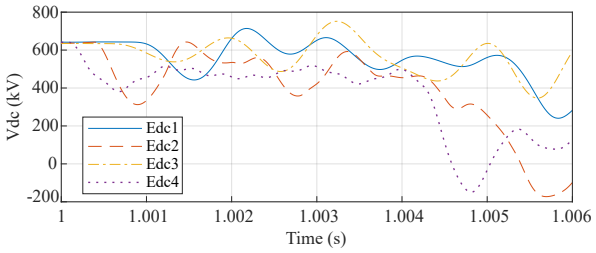

Figure 26: System DC voltages. Case without CbFCL.

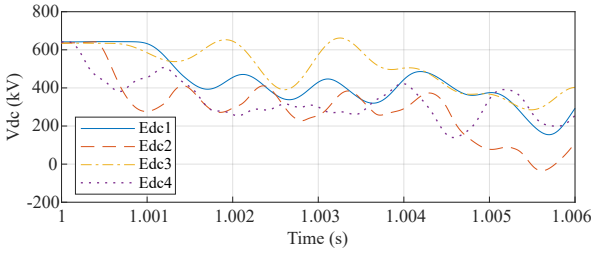

Figure 27: System DC voltages. Case with CbFCL K1.

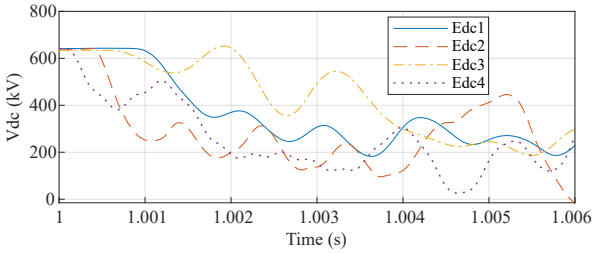

Figure 28: System DC voltages. Case with CbFCL K2.

arms. Accordingly, Fig. 29 presents the positive converter fault current for a solid pole-to-earth fault at Point B, at the beginning of Link 13.

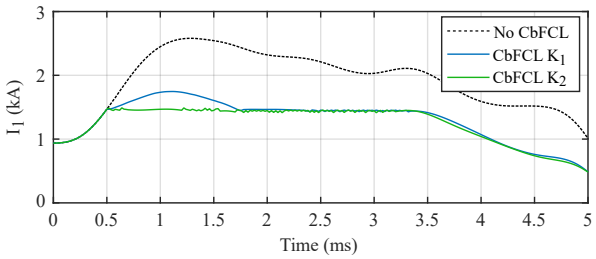

Figure 29: MMC 1 positive pole short-circuit currents for pole-to-earth fault. Comparison between the cases with and without CbFCL.

An advantage of the proposed technique is that it does not depend on the control system or modulation technique and it does not affect the system in normal operation, acting only in the capacitive discharge interval. It should be noted that the CbFCL reduces the MMC con-

tribution to the fault current, but it does not affect the contribution of other capacitive elements connected to the grid, e.g., DC bus capacitors and cables.

In this work, we considered that all equipment delay from current sensing to the actual submodule reduction are in the μs order, hence sufficiently fast to provide fault current reduction, and thus, able to operate faster than DC circuit breakers.

5. Conclusion

The present paper proposed an FCL for HB-MMC based on control action. Both theoretical and simulation analysis were presented, leading to a simple yet comprehensive and efficient FCL technique. By using equations and simulations, the reduction of short-circuit currents caused by the CbFCL could be observed.

Whereas the widely used FCL technologies work by inserting an impedance into the system, the proposed method reduces the fault current just by control action, exploring the modular feature of MMCs, thus not incurring costs and not leading to reduced stability, increased energy storage, conduction losses or the need for maintenance. Another advantage of the proposed technique is that it does not affect the system in normal operation, acting only in the presence of a fault.

Although the CbFCL is capable of reducing the fault current, it should be noted that the more limiting the CbFCL is, the greater will be the impact on the AC power and on the DC grid voltage during the fault. However, during the short-circuit, the DC current is the most prominent parameter to be mitigated.

The proposed technique reduces the DC currents while maintaining the AC currents within the nominal limits. The proposed solution is a pure control method, which allows reducing the inductor used for limiting the fault current.

Appendix A. System Parameters

System parameters are summarized in Table A.1.

Table A.1: MTDC system parameters.

	MMC 1,2,3	**MMC 4**	
AC Grid			
AC reactance	17.75	13.34	[Ω]
AC resistance	1.77	1.34	[Ω]
Transformer			
Power	900	1200	[MVA]
Leakage reactance	0.15	0.15	[p.u.]
Winding voltages	400/400	400/400	[kV/kV]
Converter			
Voltage	380	380	[kV]
Power	900	1200	[MVA]
SM per arm (N)	50	50	
SM capacitance	1465	1950	[μF]
Arm inductance (L_{arm})	84.8	63.6	[mH]
SM ON-state resistance	0.0177	0.0134	[Ω]
SM OFF-state resistance	100	100	[MΩ]
DC Bus			
DC bus reactor (L_{bus})	10	10	[mH]
DC capacitor (C_{bus})	2.5	2.5	[μF]
DC line reactor (L_{sm})	40	60	[mH]

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